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Analysis of the gate-to-channel capacitance variation for the tri-gate nanowire junctionless transistors

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Abstract In this paper, the gate-to-channel capacitance variation for the tri-gate nanowire junctionless transistor (JLT) has been analyzed. It is based on the 2-D electrostatic numerical simulation realized using Silvaco-TCAD Software. The flat-band voltage and the threshold voltage are extracted trough the plotting of the derivative for the gate-to-channel capacitance versus the gate voltage. This plotting is performed for different values of the channel width and the channel height of the tri-gate JLT. Moreover, the physical effect of the back-gate biasing has been investigated.

Keywords: *tri-gate junctionless nanowire, gate-to-channel capacitance, flat-band voltage, threshold voltage*

I. INTRODUCTION

The multiple-gates (MG) field-effect transistors (FETs) have become an industrial choice for semiconductor companies to realize complementary metal-oxide-semiconductor (CMOS) circuits with a recent technology nodes [1, 2]. The good electrical performances and the simple manufacturing process make the MG FET as one of the best candidate for the scaling of CMOS circuits [3-5]. Also, the MG FETs are MOSFET transistor with different gates configuration built on the SOI (silicon-on-insulator) technology. In addition, these types of device offer excellent control of the channel electrostatic potential, which minimize the impact of short-channel effects (SCEs) [6-9].

In order to continue the Scaling of CMOS circuits, the channel lengths of the MG FETs are moving beyond 15nm [6]. However, manufacturing the nano-scale MG FETs with sub 15nm has become a technological challenge for the semiconductor companies [2]. In this context, the realization of a gradual doping and the formation of ultrafine junctions become more and more complex [2, 10]. To overcome this challenge, the junctionless transistors (JLT) are proposed. These types of transistors are defined as MOSFETs transistors without junctions [11]. Moreover, the gradual doping is not required in the JLTs. In the case of JNTs, only one type of doping is realized in the all the device. For this reason the JLTs offer a simple and compatible manufacturing process [12]. In the other hand, comparing the JLTs with the classical MOSFETs, the JLTs transistors are accumulation mode devices with better electrical performances, excellent control of short-channel effects (SCEs) and a simpler fabrication process [13, 14].

In this work, we present the study and the analysis of the variation of the gate-to-channel capacitance for the tri-gate junctionless nanowire transistor (JLT). In this context, the threshold voltage and the flat-band voltage of the tri-gate JLT are extracted using the parameter extraction method through the numerical simulation results of the device performed with Silvaco-TCAD [15]. This type of study for the tri-gate JLTs offers helpful information for their practical applications as well as for a better understanding of the tri-gate JLTs behaviour, especially for the accurate description of the key parameters for the tri-gate JLTs device. Moreover, it is very useful for compact modeling of tri-gate JLTs devices.

II. ARCHITECTURE OF THE DEVICE

Let's consider the schematic view for the tri-gate junctionless transistor (JLT) shown in Fig.1 (a).

In this context, the structure of the gate-to-channel capacitance for the tri-gate JLT can be presented as shown in Fig.1 (b), it represents the cross section of a symmetrical tri-gate JLT device.

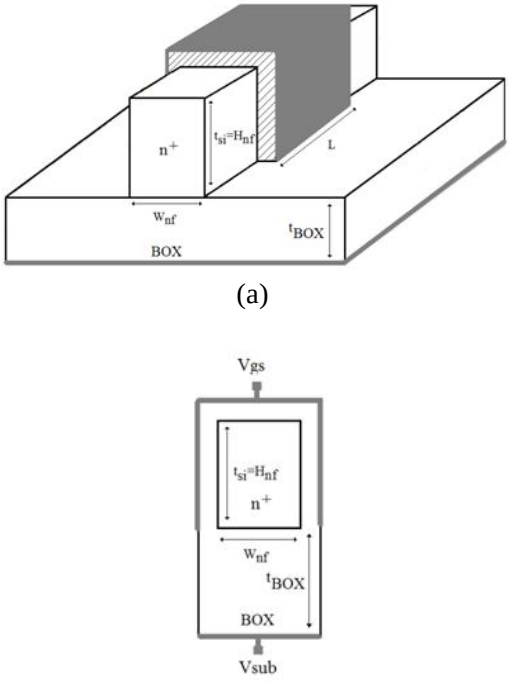


Fig. 1. (a) Schematic view of the tri-gate JLT. (b) Cross section of the tri-gate JLT.

In this case of study, we consider the gate-channel capacitance (Fig.1 (b)) for a heavily doped tri-gate JLT with a long channel. The technological parameters of this device are indicated in Table.1. V_{gs} and V_{sub} are the gate bias and back-gate bias, respectively.

TABLE 1
PARAMETERS OF THE CONSIDERED STRUCTURE

Parameters	Symbol	Value
Channel width	W_{nf}	12, 20, 40, 60, 80, 100 and 150nm
Channel length	L_{nf}	100nm
Channel height	H_{nf}	8, 16, 24 and 32nm
Oxide thickness	t_{ox}	1.3nm
Doping concentration	N_D	5.10^{18} cm^{-3}
Buried oxide thickness	t_{BOX}	145nm

III. DESCRIPTION OF THE PARAMETERS EXTRACTION METHOD

Several methods have been developed and revised for the extraction of electrical parameters of JLNs transistors, such as the flat-band voltage, the doping concentration, and the threshold voltage. Most of the proposed methods are based on the current-voltage characteristics or the capacitances-voltage measurement [16, 17].

To extract the flat-band voltage V_{fb} and the threshold voltage V_{th} of the gate-channel capacitance for tri-gate JLT, we use the gate-to-channel capacitance measurements based on the numerical simulations of the structure performed with Silvaco-TCAD.

Moreover, the considered method is based on the plotting of the average carrier concentration versus the gate voltage, for the extraction and the determination of important parameters such as the flat-band voltage, the threshold voltage, and also the doping concentration. Moreover, we use the GUMMEL method for the numerical solution calculation of the Poisson equation and the continuity equations for both electrons and holes.

IV. RESULTS AND DISCUSSIONS

Fig.2 shows the variation of the gate-to-channel capacitance C_{gc} versus the gate bias V_{gs} for the tri-gate JLT with a channel width of 20nm, and a channel height of 8nm. Indeed, the gate-to-channel capacity starts to increase, as a function of V_{gs}, it is related to the formation of bulk neutral channel in the initially fully-depleted channel.

The derivative of the gate-to-channel capacitance dC_{gc}/dV_{gs} versus the gate bias V_{gs} is presented in Fig. 3. We can see that the curves include two peaks, the first peak corresponds to

the threshold voltage V_{th}, and the second peak indicates the flat-band voltage V_{fb}. In this case, the flat-band voltage is equal to 0.35V but the threshold voltage varies with the channel height H_{nf} and the channel width W_{nf} of the device.

Fig.3 (a) shows the derivative of the gate-to-channel capacitance versus the gate bias with varying of channel width W_{nf}, from 12 nm to 150nm. We can conclude that reducing the channel width increase the position of the first peak which denotes the conduction threshold voltage. The reason for the important variation of the threshold voltage is that for narrow widths, the sidewall gate effect through the depletion region strongly affects the formation of the bulk neutral channel. Fig.3 (b) illustrates the derivative of the gate-to-channel capacitance versus the gate bias with varying of channel height H_{nf}, from 16nm to 32nm. In this case, the reduction of the channel height increase the threshold voltage described by the first peak. Also, the variation of the threshold voltage in this case is less important compared to the case of Fig.3 (a). This because the effect of the top-gate is very important compared to the sidewall gate effect. It can also be noted that the position of the second peak is still fixed, which means that the flat-band voltage does not change.

The increase of the carrier concentration is strongly related to the reduction of the channel height H_{nf} as shown on Fig.4. However, the significant reduction in the channel height creates a physical behavior equivalent to the planar JLTs devices.

In order to extract the doping concentration, we plot the average carrier concentration versus the gate voltage with varying the channel width as shown on Fig.5. The doping concentration and the flat-band voltage can be easily defined trough the curves intersection point. In this case, the doping concentration is equal to 5.10^{18} cm^{-3}, which is the adequate value of the considered doping concentration. However, it is worth noticing that the flat band voltage is equal to 0.45V. A voltage difference of 0.1V is noted between the value of the flat-band voltage obtained with this method and the one obtained through the second peak shown in Fig.3. Moreover, the reason for the offset of the second peak of the derivative of the capacitance is the variation of the increment of the electronic charge density in the depletion zone. Although the electronic charge density is lower than the doping charge (and so one is not in accumulation), then it cannot be neglected near the flat-band voltage.

Fig.6 shows the effect of the back-gate biasing V_{sub} on the derivative of the gate-to-channel capacitance versus the gate bias. The first peck which indicates the threshold voltage conduction is decreasing when increasing the substrate bias V_{sub}. The reason is the reducing of the bulk neutral channel which squeezing the depleted region. But in the case of a strong negative value of V_{sub}, the fully-depletion regime becomes important compared to the partial depletion. In addition, there will be a strong formation of a neutral channel.

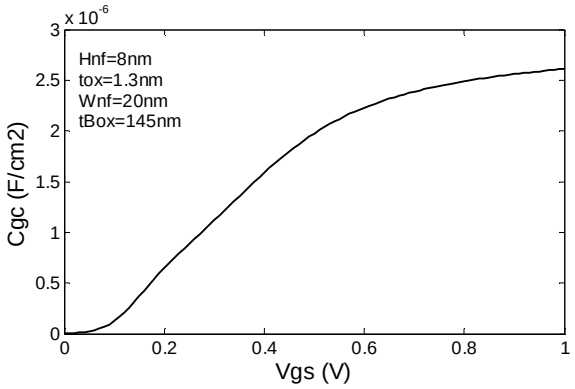
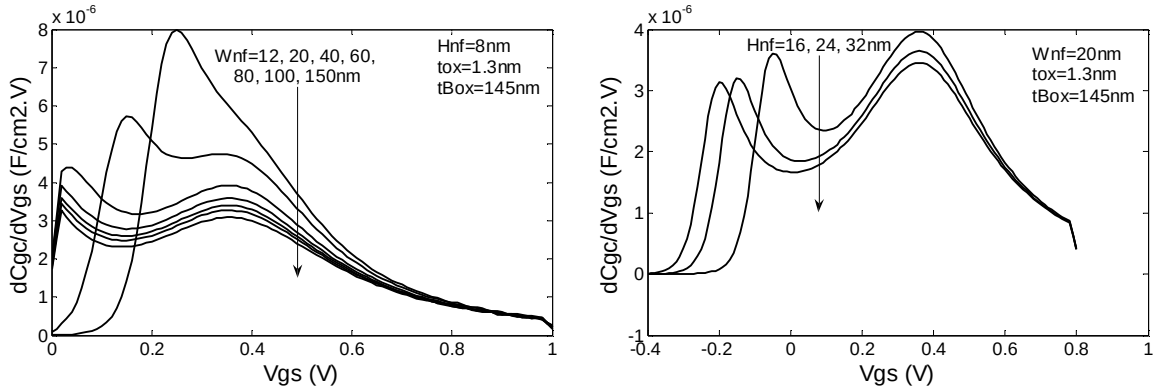


Fig. 2. The gate-to-channel capacitance C_{gc} versus the gate bias V_{gs}.



(a) (b)

Fig. 3. (a) The derivative of the gate-to-channel capacitance C_{gc} versus the gate bias V_{gs} with varying the channel width W_{nf}. (b) The derivative of the gate-to-channel capacitance C_{gc} versus the gate bias V_{gs} with varying the channel height H_{nf}.

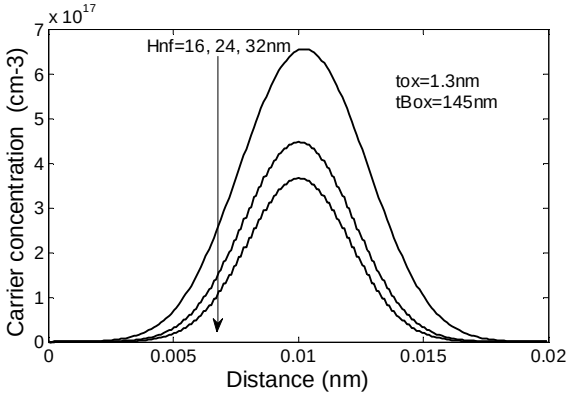


Fig. 4. The carrier concentration variation in the channel of the gate-to-channel capacitance.

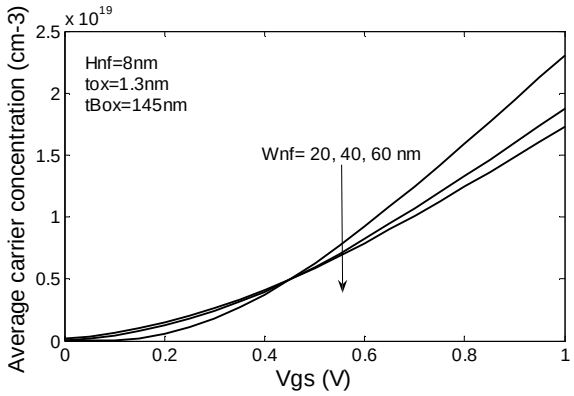


Fig. 5. The average carrier concentration as a function of the gate bias.

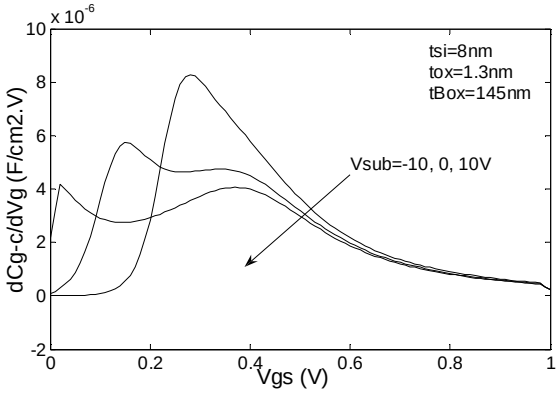


Fig. 6. The derivative of gate-to-channel capacitance C_{gc} versus the gate voltage V_{gs} with varying the substrate bias V_{sub}.

V. CONCLUSION

In this paper, we have extracted the parameters of the gate-to-channel capacitance in the tri-gate JLT, such as the flat-band voltage, the threshold voltage and the doping concentration. Moreover, we have analyzed the derivative of the gate-to-channel capacitance dC_{gc}/dV_{gs} versus the gate bias V_{gs} with varying the channel width, and also the channel height. The variation of dC_{gc}/dV_{gs} and the carrier concentration are strongly related to the channel height and especially the channel width. Indeed, the first peak in dC_{gc}/dV_{gs} variation, which denotes the threshold voltage, is influenced by the channel width variation through the sidewall gate effect of the structure. Moreover, the second peak in dC_{gc}/dV_{gs} variation, which describes the flat-ban voltage, is shifted because of the increment of electronic charge density in the depletion zone. The presented study is very useful for developing analytical compact solutions for accurate description of the second peak in dC_{gc}/dV_{gs} variation of tri-gate JLTs.

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