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Department of Power and Control

Final Year Project Report Presented in Partial Fulfilment of the Requirements for the Degree of

MASTER

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Option: **Power Engineering**

Title:

FPGA based control of single phase SVC

Presented by:

- **KAMEL Tayeb Djamel Eddine**
- **BOUDJOURAF Walid**

Supervisors:

Dr. KHELDOUN Aissa

Dr. METIDJI Brahim

Registration Number:……/2016

Dedication

I would like to dedicate my work to all those who helped me to succeed in my studies specially my parents, my sisters, my grandmother, my family, my friends, my teachers and all who love me and care about me, without forgetting all dears who left this life.

KAMEL Tayeb Djamel Eddine

I dedicate this modest work to:

My Mother and Father.

My brothers.

All my family.

All my dear friends and university mates.

All department's teachers, students and administrative staff and

Whoever helped to achieve this work.

BOUJOURAF Walid

Acknowledgement

We would like to express our deepest appreciation to all those who provided us the possibility to complete this project. A special gratitude we give to our final year project supervisors, Mr. KHELDOUN Aissa & Mr METIDJI Brahim, whose contribution in stimulating suggestions and encouragement, helped us to coordinate our project especially in implementation.

Furthermore we would also like to acknowledge with much appreciation the crucial role of the staff of our institute laboratory responsible, who gave the permission to use all required equipment and the necessary materials to complete the task.

Abstract

Power quality is one of the most important indicator in electrical engineering. Variations in the impedance should be noticed for any external disturbance or change in the parameters of the electrical systems. These variation affect the reactive power hence the power factor. The use of capacitors and inductors is the classical method to compensate the reactive power but still slow to operate and decreases the power quality.

Flexible AC transmission systems (FACTS) are compensators that uses a control unit and power electronic switches to vary the impedance of the systems. The idea of this work is to change the switching and the control method of the static VAr compensator (SVC).

Classical SVCs are based on thyristors for switching and using a simple control unit. Our method is to change the control unit by using an FPGA and a bidirectional switch to enhance the power quality and increase the speed of switching.

Contents

List of tables

List of figures

General introduction

One of the great engineering achievements of the last century has been, the evolution of large alternative current (AC) power grids, in which all the interconnected systems maintain the same precise electrical frequency. Today, the conventional electric power system is composed of three main level which are: generation, consummation, transmission and distribution.

In each electric power grid, some parameters must be maintained to insure a good service to the consumer. This parameters are frequency “50 Hz”, voltage, and the sinusoidal shape of the voltage.

When the load is inductive or capacitive, it may causes a reactive power perturbation that affect the power factor and the voltage which are the major problems in network especially in distribution level. Compensation is a method to control the reactive power in the network where the voltage or the power factor is out of range.

There exists modern and classical methods to compensate the reactive power which are, reactors and bank of capacitors that represent classical methods and static advanced method as a current voltage injection or variable impendences that requires a control of switching modules.

Static var compensator is a variable impedance compensator based on control signal that Triger the switches to move from inductive state to capacitive or reverse way, thyristors power electronic devices are mostly used on switching because of their ability to resist to high current, but still have slow switch off that may cause short circuit when more than one thyristor are used and steal slow to operate.

Thinking of an idea to have more safe and fast switching is not impossible due to the existence of fast switching semiconductors such us MOSFETs. The solution proposed in the project is to keep the same principle but, change the switching and control method using FPGA as a control device and IGBTs as switches.

The project starts with a simulation of the SVC using MATLAB Simulink and in order to induce FPGA-real time control, modelsim must be employed together with MATLAB Simulink.

An exchange of data should be done between Matlab and model sim in such away Matlab brings FPGA block from model sim, then generates a clock that should be sent to model sim with inputs data set on Matlab. Both software should simulate the data which is called co-simulation.

The idea was implemented following the simulation steps, signals are generated from DE0 board using hardware method, then buffered toward a combination of four switches called AC chopper placed between an inductor and a capacitor.

Our implementation of SVC should compensate the reactive power in the test is made from source in parallel with an inductive load. The change of current sign is important so that PWM at the input should provide a switching method arranged by the FPGA to make the absorption and injection of reactive power very fast and makes the switching more safe.

Chapter I

1.Compensation concepts

During the past few years, the demand of electrical energy has highly increased. More power plants, substations, and transmission lines need to be constructed. However, the Inductive load or step up transformer that increases the voltage hence more power transfer capability especially in transmission line creates a reactive power disturbance, which results an under/over voltage disturbance.

Reactive power Compensation was the solution to solve the problems of reactive power and helping generators to improve the power quality. Reactors, capacitors, and other classical method are used as first level reactive power compensation to absorb/ inject reactive power. However, long switching periods, discrete operation and harmonics injection Ferro-resonance and coast are the major problems found in classical compensation. These drawbacks have motivated the development of static compensators based on power electronics methods. Figure (1-1) shows the different compensation methods.

Static compensation still have some problems of the classical one, to minimize these drawbacks, large operational margins and redundancies are maintained to protect the system from dynamic variation and recover reactive power.

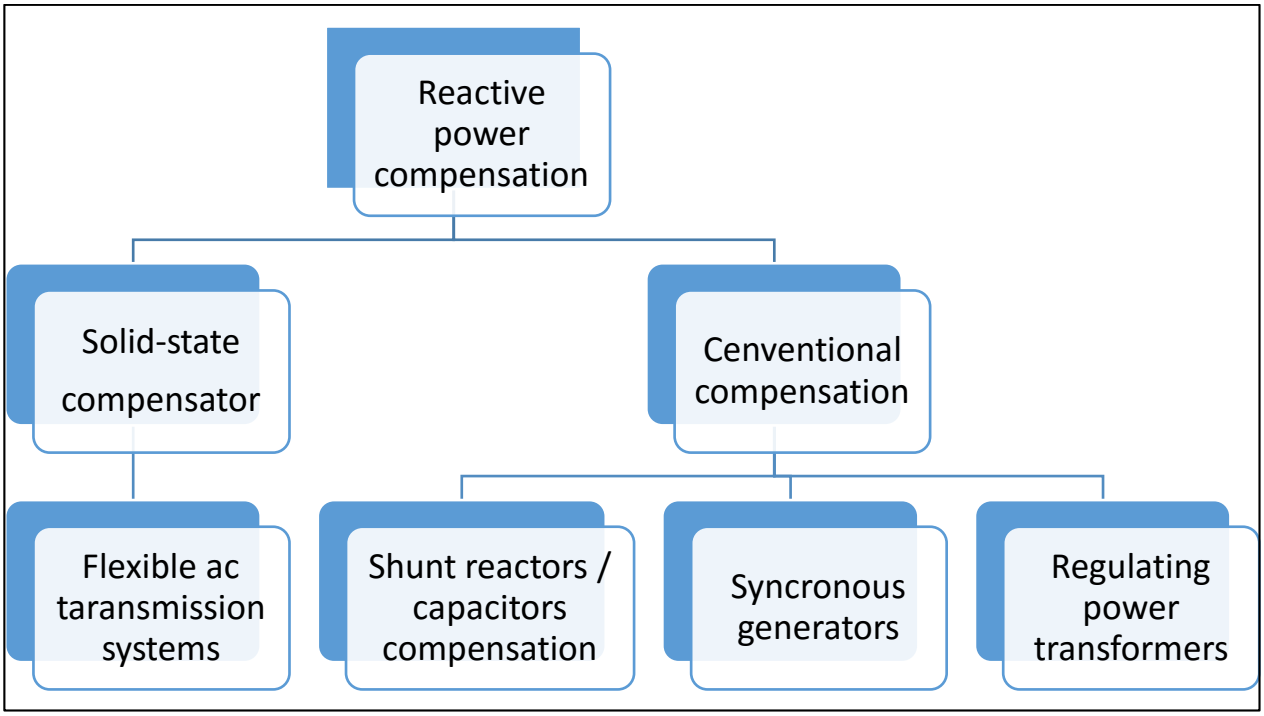


Figure 1-1: Type of compensation methods

Figure (1-2) shows the simplified model of a power transmission system. Two power grids are connected by a transmission line which is assumed lossless and represented by the reactance X_L. V $\angle\delta_1$ and V $\angle\delta_2$ represent the voltage phasors of the two power grid buses with angle $\delta = \delta_1 - \delta_2$ between the two [1].

The corresponding phasor diagrams shown in figure (1-2)(b)

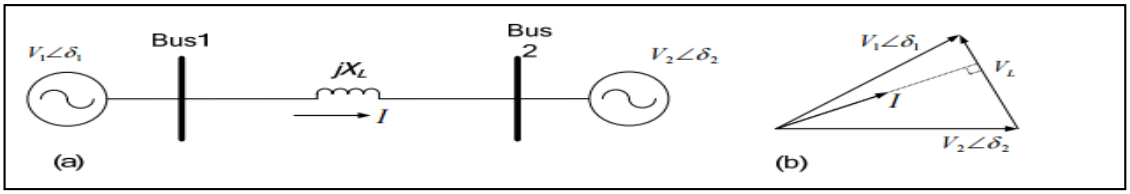


Figure 1-2: Simplified model of a power transmission system.

The magnitude of the current in the transmission line is given by

$$I = \frac{V_L}{X_L} = \frac{|V_1\angle\delta_1 - V_2\angle\delta_2|}{X_L} \tag{1}$$

Reactive components of the current flow at bus 1 are given by

$$\mathrm{I_{p1}} = \frac{\mathrm{V_2}\sin\delta}{\mathrm{X_L}} \tag{2}$$

$$\mathrm{I_{q1}} = \frac{\mathrm{V_1} - \mathrm{V_2}\cos\delta}{\mathrm{X_L}} \tag{3}$$

The active and reactive power at bus 1:

$$\mathrm{Q_1} = \mathrm{V_1}.\frac{(\mathrm{V_1} - \mathrm{V_2}\cos\delta)}{\mathrm{X_L}} \tag{4}$$

$$\mathrm{P_1} = \mathrm{V_1}.\frac{\mathrm{V_2}\sin\delta}{\mathrm{X_L}} \tag{5}$$

Similarly for the second bus we may have the same equations:

$$\mathrm{I_{p2}} = \frac{V1\ \sin\delta}{XL} \tag{6}$$

$$\mathrm{I_{q2}} = \frac{V_2 - V_1\cos\delta}{X_L} \tag{7}$$

$$Q_2 = V_2 . \frac{V_2 - V_1 \cos\delta}{X_L} \quad (8)$$

$$P_2 = V_1 . \frac{V_2 \sin\delta}{X_L} \quad (9)$$

These equations indicate that the active and reactive power/current flow can be regulated by controlling the voltages, phase angles and line impedance of the transmission system.

From the power angle curve shown in figure (1-3), the active power flow will reach the maximum when the phase angle $\boldsymbol{\delta}$ is 90º. In practice, a small angle is used to keep the system stable from the transient and dynamic oscillations. Two main groups in compensation are distinguished, which are series and shunt.

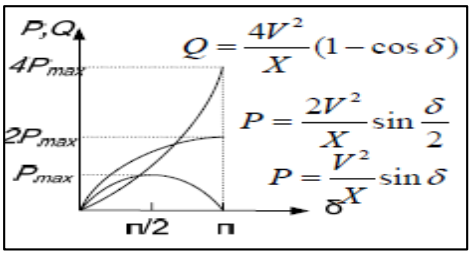


Figure 1-3: Power versus

1.1 Series compensation

Series capacitors are used to cancel a portion of the inductive reactance of the transmission line. This compensation, can improve the power transmission capability of the line. It has been applied to long transmission lines and other locations where the transmission distances are great and where large power transfers over long distances are required. Modern HV transmission lines are series compensated to improve power system performance.

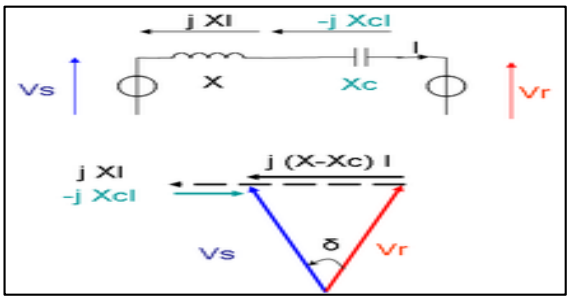


Figure 1-4: Series compensated transmission line and phasor diagram

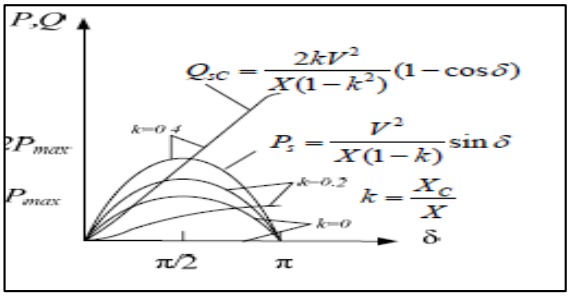


Figure 1-5: Power angle curve.

Let the capacitance of ***C*** to be a portion of the line reactance then

$$Xc = k.X_l \tag{10}$$

$$X = X_l - Xc \tag{11}$$

$$X = (1-k).X_l \tag{12}$$

The active power should be

$$\mathrm{P} = V^2.\frac{\sin\delta}{(1-k).X_l} \tag{13}$$

And the reactive power supplied by the capacitor is

$$\mathrm{Q_c} = 2.V^2.\frac{k.(1-\cos\delta)}{(1-k)^2.X_l} \tag{14}$$

Under short circuit condition, the produced high voltage may damage the capacitor and so series capacitor has to be protected using a spark gap with a high speed contactor. The use of series compensation introduces few problems like: Sub-synchronous resonance, Ferro-resonance and high recovery voltage.

1.1.1 Advantages of Series Compensation

1.1.1.1 Increase in transmission capacity

The power transfer capacity of a line is given by

$$P = \frac{E.V}{X}\sin\delta \tag{15}$$

To see the difference between the compensated and uncompensated we have to calculate the ratio:

$$P_1 = \frac{E.V}{X_L}\sin\delta \tag{16}$$

$$P_2 = \frac{E.V}{(X_L - X_C)}\sin\delta \tag{17}$$

$$\frac{P_2}{P_1} = \frac{X_L}{(X_L - X_C)} = \frac{1}{(1 - X_C / X_L)} = \frac{1}{1-K} \tag{18}$$

The economic degree of compensation K lies in the range of 0.4-0.7

1.1.2 Disadvantages of series compensation

1. Increase in fault current.
2. Bad operation of distance relay if the degree of compensation and location is not proper.
3. High recovery voltage of lines- across the circuit breaker contacts and is harmful.
4. Problems of Ferro-resonance: When an unloaded or lightly loaded transformer is energized through a series compensated line, Ferro-resonance may occur. It is produced due to resonance occurred in between the iron-created and in the reactance of the compensated line. This will cause a flow of high current.
5. Problems due to sub-synchronous resonance: The series capacitors introduces a sub-synchronous frequency (proportional to the square-root of the compensation) in the system.

1.2 Shunt compensation

Shunt reactive compensation has been widely used in transmission system to regulate the voltage magnitude, it improves the voltage quality, and enhance the system stability. Shunt-connected reactors are used to reduce the line over-voltages by consuming the reactive power, while shunt-connected capacitors are used to maintain the voltage levels by compensating the reactive power to transmission line.

Figure (1-6 a) shows the voltage magnitudes of the two buses assumed to be equal **V**, and the phase angle between them is **δ**. The transmission line is assumed lossless and represented by the reactance $\boldsymbol{X_L}$. At the midpoint of the transmission line, a controlled shunt capacitor C connected. The voltage magnitude at the connection point is maintained constant and equal.

From the power angle curve shown in figure (1-6)(c), the transmitted power can be significantly increased, and the peak point shifts from δ=90º to δ=180º. The operation margin and the system stability are increased by the shunt compensation.

The active power at bus one & two is given by:

$$\mathrm{P2} = \mathrm{P1} = 2\frac{V^2}{XL}\sin\frac{\delta}{2} \tag{19}$$

The reactive power injected by the capacitor

$$\mathrm{Qc} = 4.V^2.\frac{(1-\cos\delta/2)}{Xl} \tag{20}$$

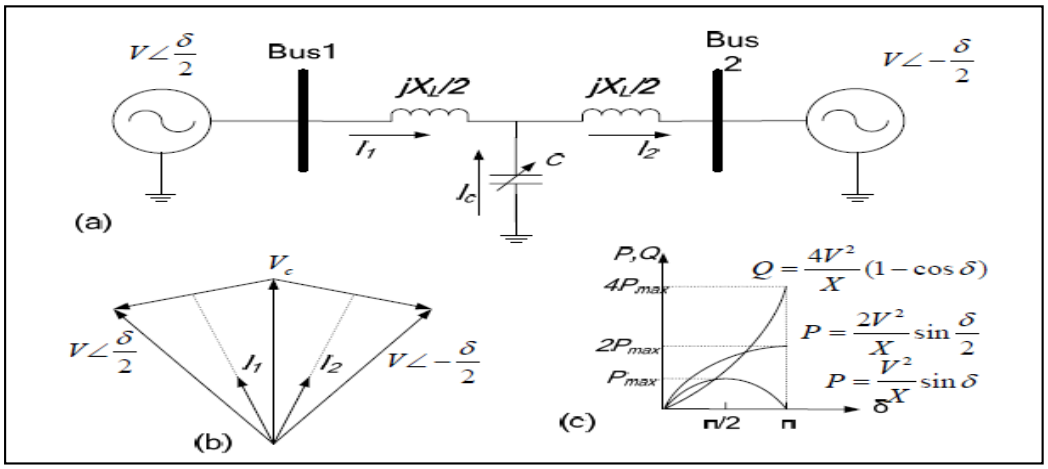


Figure 1-6: Voltage magnitudes of the two buses and power angle curve

1.3 Selection of Shunt or series compensation

- To maintain constant load voltage, performs better the series capacitor arrangement.
- Shunt capacitive arrangement reduces the total active power loss while series capacitive one does not.
- Series capacitive arrangement reduces the total reactive power loss by far as compared to Shunt-capacitive arrangement.

- Shunt capacitive arrangement improves the system power factor by far compared to Series capacitive one.
- Load power factor remains always constant with and without any compensation.
- When a system is to be extended by the addition of a new line or when one of the existing circuits is to be adjusted for parallel operation, series compensation is preferable to achieve maximum power transfer or minimize losses.

1.4 Conventional compensation

Reactive power demand changes, and consequently the voltage fluctuates on the line. In order to control and correct the voltage fluctuations, there are several voltage regulating devices that are used in the power system; which are briefly described as follows:

1.4.1 Synchronous generators

Can be used for both generation and consumption of reactive power. When they are in over-excitation mode, they deliver reactive power to the power system; while they absorb reactive power from the grid when working in under excitation mode.

1.4.2 Regulating power transformers

It is possible to change a power transformer's voltage ratio by using tap-changer which consequently affects the voltage level. But this method is limited particularly when the transformer is connected with many lines which have different load, it can cause a violation in certain lines.

1.4.3 Shunt capacitors

Capacitors generate reactive power to power system to which are connected, they do increase the voltage level. Typically they are used during heavy load conditions.

1.4.4 Shunt reactors

There are two main applications for Shunt Reactors. First, Shunt Reactors can be used for stability reasons especially on long transmission lines (EHV and HV lines/cables); For the purpose of voltage control, they can only switched in during light loaded conditions.

1.5 Flexible AC transmission systems

The electricity supply industry is undergoing a profound transformation worldwide. Market forces, depleting natural resources, and an ever-increasing demand for electricity are some of the drivers responsible for such unprecedented change.

The ability of the transmission system to transmit power becomes impaired by one or more of the following steady state and dynamic limitations:

-Angular stability;

- Voltage magnitude;

- Thermal limits;

- Transient stability;

- Dynamic stability.

These limits define the maximum electrical power to be transmitted without causing damage to transmission lines and electrical equipment. In principle, limitations on power transfer can always be relieved by the addition of new transmission lines and generation facilities.

Alternatively, Flexible Alternating Current Transmission System (FACTS) controllers can enable the same objectives to be met with no major alterations to power system layout. FACTS are alternating current transmission systems incorporating power electronic-based and other static controllers to enhance controllability and increase power transfer capability.

1.5.1 FACTS composition & properties

The FACTS concept is based on the substantial incorporation of power electronic devices and methods into the high-voltage side of the network, to make it electronically controllable. FACTS controllers aim at increasing the control of power flows in the high-voltage side of the network during both steady state and transient conditions.

This interest has led to significant technological developments of FACTS controllers. Several kinds of FACTS controllers have been commissioned in various parts of the world.

Popular FACTs are: load tap changers, phase-angle regulators, static VAR compensators, thyristors controlled series compensators, interphase power controllers, static compensators, and unified power flow controllers.

The main objectives of FACTS controllers are the following:

- Regulation of power flows in prescribed transmission routes.

- Secure loading of transmission lines nearer to their thermal limits.

- Prevention of cascading outages by contributing to emergency control.

- Damping of oscillations that can threaten security or limit the usable line capacity.

1.5.2 Types of FACTs based on controllers

FACTS technology consists of number of devices. Some of the FACTS devices are:

- Static Synchronous Compensator (STATCOM).
- Static Var Compensator (SVC).
- Unified Power Flow Controller (UPFC).
- Inter-phase Power Flow Controller (IPFC).
- Static Synchronous Series Controller (SSSC).
- Thyristor Controlled Series Compensator (TCSC).
- Super Conducting Magnetic Energy Storage (SMES). [2]

1.5.2.1 Shunt Mechanically-Switched Capacitors (SMSC):

An SMSC typically consist of a set of capacitor banks that control the voltage magnitude at a remote bus or at the bus at which they are connected.

The capacitor banks, which are defined in terms of their nominal reactive power, are switched on one at a time when the controlled-bus voltage magnitude reaches a minimum value, and they are switched off when the voltage reaches a maximum value.

Hence, these controllers can be readily modelled in steady state as depicted in figure (1-7).

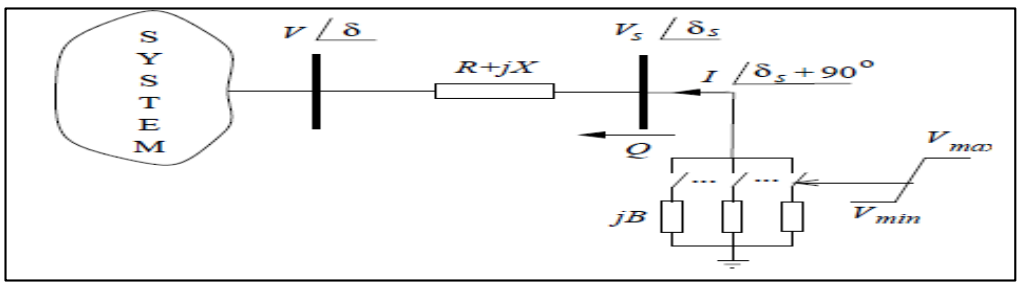


Figure 1-7: SMSC steady state model

1.5.2.2 **Static var compensator (SVC)**

The model shown in figure (1-8) is model where the controller is modelled as a variable susceptance controlled by the firing angle of the thyristor-controlled reactor of the SVC. Hence, control limits in this case are directly represented in the firing angle; however, given the one-to one correspondence between this firing angle and the corresponding equivalent susceptance value, one could assume that these limits directly correspond to limits on this susceptance, as it is typically done in most power system analysis tools. [2]

$$V = V_{ref} - X_d I \tag{21}$$

$$B_e(\alpha) V_s = I \tag{22}$$

$$B_e(\alpha) = \frac{1}{\pi X_L}[2\alpha - \sin 2\alpha - \pi(2 - \frac{X_L}{X_c})] \tag{23}$$

Where V is the voltage magnitude at the bus being controlled; Vref is the desired voltage setting; I is the capacitive current of the SVC, which becomes negative when the controller is operating in inductive mode; X_d stands for the controller droop; Be represents the equivalent susceptance of the SVC controller which is a function of the firing angle α; and X_C and X_L are the SVC's capacitor and inductor reactance. In this case, the last equation is not explicitly considered in the solution process; this equation is only used to determine the control limits.

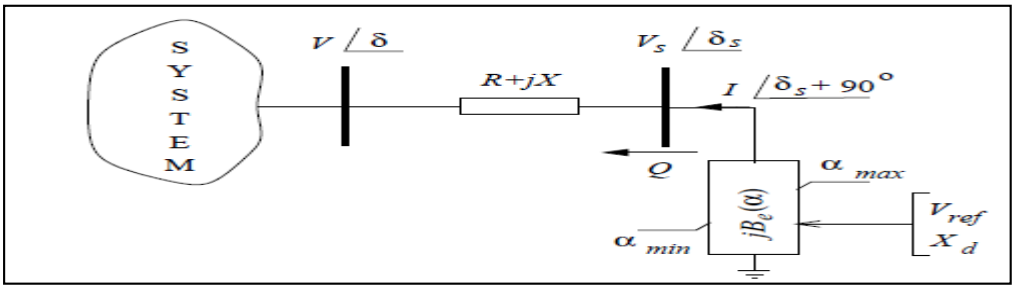


Figure 1-8: SVC steady state model

1.5.2.3 **Static synchronous compensator (STATCOM):**

The STATCOM model in figure (1-9) is a model based on an active power balance between the ac side and dc side of the Static Synchronous Compensator (STATCOM).

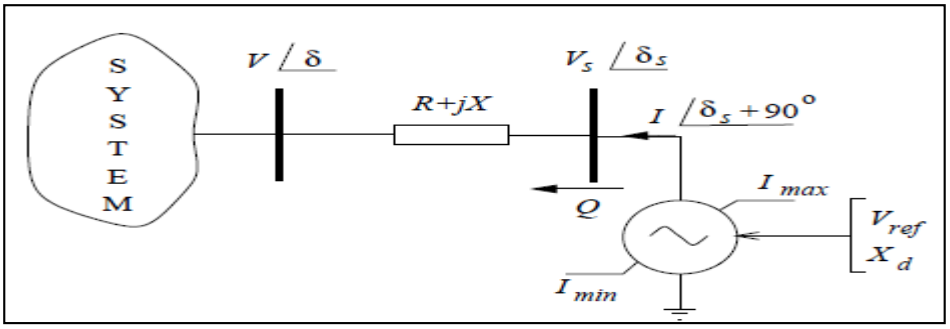


Figure 1-9: STATCOM steady state model

Voltage-sourced converter (VSC), is the main element of a STATCOM. If dc losses in the STATCOM are neglected, as these are typically not very significant, this model can be viewed as a reactive power voltage source model Thus, the STATCOM can be modelled in steady state by means of the following equations when delivering reactive power (operating in capacitive mode):

$$V = V_{ref} - X_d I \quad \& \quad I = Q/V_s$$

$$V_s^2 G - V_s . V . G \cos(\delta_s - \delta) - V_s . V . B sin(\delta_s - \delta) = 0 \tag{24}$$

$$-V_s^2 B - V_s . V . B \cos(\delta_s - \delta) - V_s . V . B sin(\delta_s - \delta) = Q \tag{25}$$

where $G+jB = (R+jX)^{-1}$ represents the step-down STATCOM transformer plus ac active and reactive power losses associated with the solid-state switches operation, which can be significant in PWM control; $V\angle\delta$ and $V\angle\delta$are the voltage phasors at the bus being controlled and the VSC ac bus, respectively; Vref is the desired voltage setting; I is the capacitive current of the STATCOM, which becomes negative when the controller is operating in inductive mode; and X_d stands for the controller droop. Observe that this model is similar to the typical voltage source (synchronous condenser) model used to represent STATCOMs in power flow analysis, since a transformer/line model can be used to represent the R + jX impedance. [2]

Chapter II

2 . Static Var Compensator

2.1 Introduction

SVC is an automated impedance matching device, providing fast acting reactive power on high voltage electricity transmission network, it is a part of flexible AC transmission system (FACTs), regulating the voltage, power factor and stabilizing the system.

2.2 SVC Thyristor controlled reactor -fixed capacitor based (TCR FC)

The SVC of the TCR-FC type consist of a TCR, which absorbs reactive power from the ac power system to which the SVC is connected, and several FCs, which supply reactive power to the system of the TCR-FC type is illustrated in figure(2-1) below.

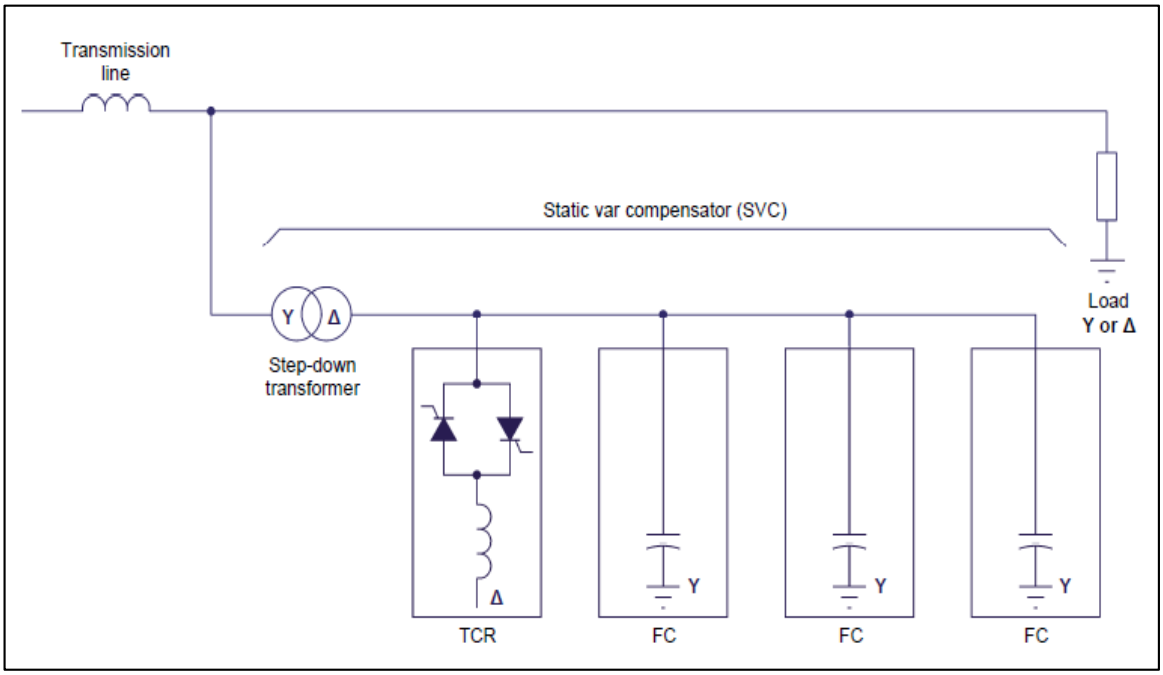


Figure 2-1: Simplified single wire circuit diagram of an SVC of the TCR-FC type [3].

When the SVC has to supply reactive power to compensate the voltage in the ac power system (when the system absorbs reactive power), the TCR firing angle is increased so that the amount of reactive power absorbed by the TCR decreases. The lower the reactive power which the TCR absorbs, the higher the reactive power which the SVC supplies. When the TCR is set to the non-conducting state, the amount of the reactive power supplied by the SVC is maximal. The maximal amount of the reactive power which an SVC of the TCR-FC type can supply is equal to the rated reactive power.

2.3 SVC Thyristor switched capacitor (TSC)

The shunt-capacitor bank is split up into small steps, by using bidirectional thyristor switches. It can be made switched in and out individually. Fig (2-2), shows the single-phase branch, consists of capacitor C and the thyristor switch and a minor component. The reactor L, which is used to limit the rate of rise of the current through the thyristors and also to prevent resonance with the network. The capacitor is switched out through the suppression of the gate trigger pulses of the thyristors.

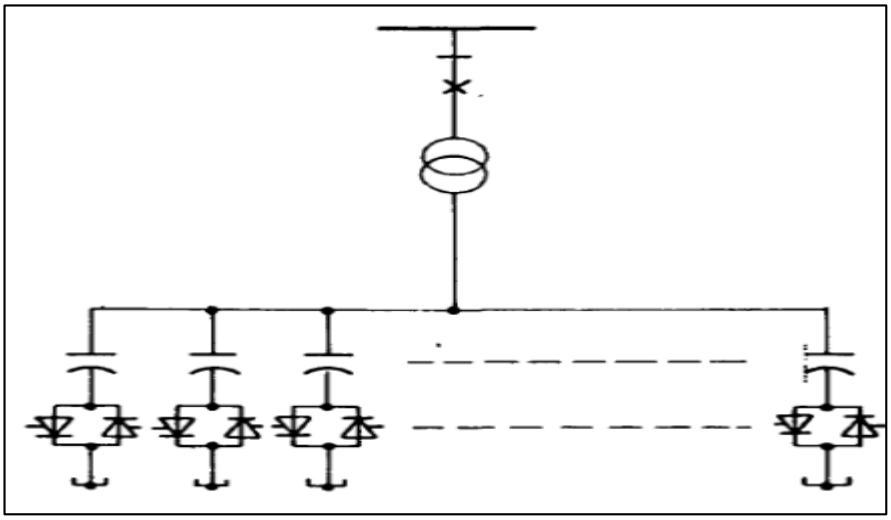


Figure 2-2: Bidirectional thyristor SVC

2.4 SVC (TCR-TSC)

The TCR-TSC type consists of a TCR, which absorbs reactive power from the ac power system connected to the SVC, and several TSCs, which supply reactive power to the ac power system connected to the SVC.

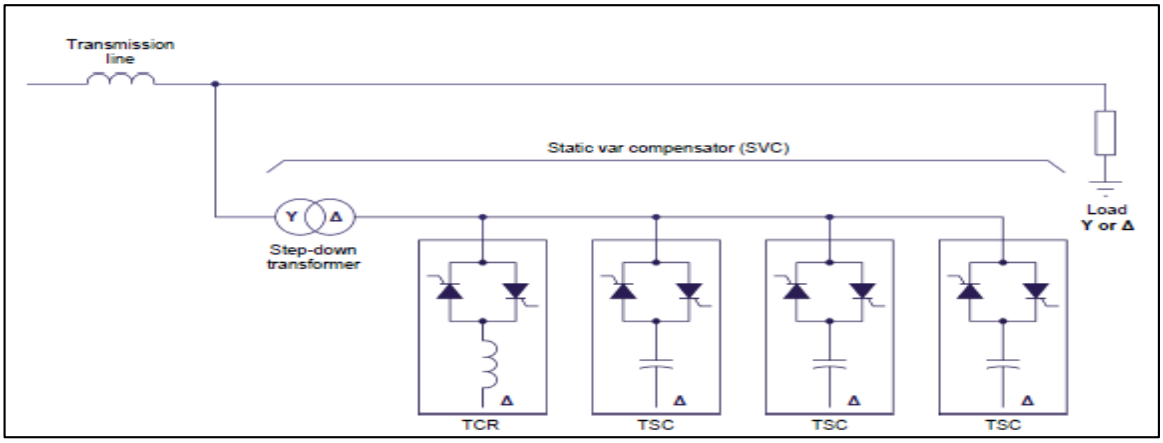


Figure 2-3: Simplified single wire circuit diagram of an SVC of the TCR-TSC [3].

In the thyristor switched capacitor scheme the total reactive power is split into a number of parallel-capacitor banks. The reactive power from the compensator follows the load or terminal voltage variations in a step. Combined TSC and TCR type are characterized by the following properties:

- Continuous control
- Practically no transients
- Low generation of harmonics
- Low losses
- Flexibility in control and operation.

2.5 SVC IGBT based

The SVC treated previously based on thyristor which are hard to turn on and off without forgetting the low order harmonics injected, so we can think on faster low harmonic and more efficient switching method based on hardware design, or in other term we can switch and control in low power.

In this project IGBTs are as switch due to its fastness and resisting to a high power, the figure (2-4) shows a diagram of switching methodology which should be implemented.

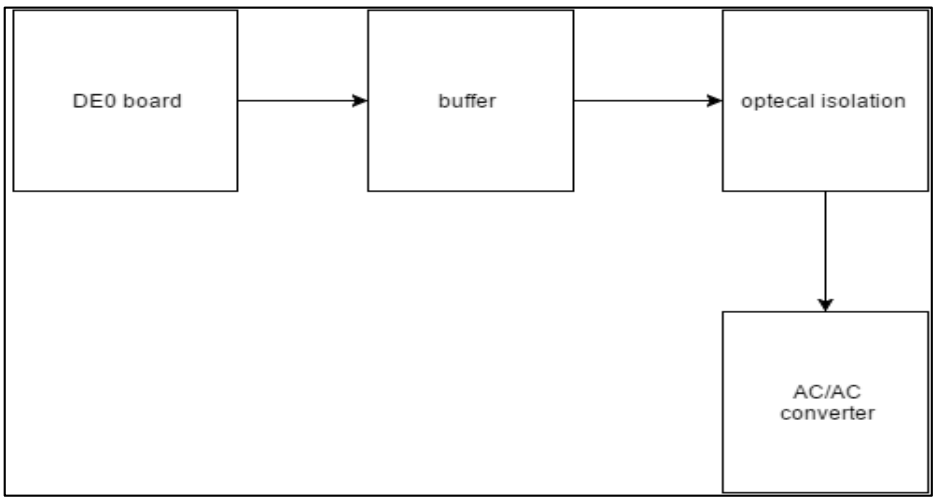


Figure 2-4: Initial design of SVC IGBT based

DE0 board being used to generate the signals which are buffered to an optical isolation which drives the IGBTs of AC /AC converter.

2.5.1 **Circuit development:**

The electronics hardware design based on FPGA board allow to control AC/AC converters by generating signals to switch on or off the IGBTs. The choice of the FPGA comes from it ability to replace the IC's and allow us to create fast low level logic devices with a high speed, Compared to other boards, the FPGAs are more precise, high speed interface. Also a hardware implementation could be done compared to "µcontroller ……" More details on this board are mentioned on the next chapter.

The signals coming from the FPGA cannot be sent directly to the IGBTs gate, therefore signal conditioning circuit must be added.

2.5.2 **Voltage buffer**

A circuit which transfers a voltage from a circuit with high output impedance to a circuit with low input impedance is called a voltage buffer.

The voltage buffer connected between these two circuits prevents the low input impedance circuit from loading the first one. Absolute linearity, high speed are the features of an ideal voltage buffer.

If the voltage is transferred from the first circuit to the second one without any change in amplitude, then such a circuit is called unity gain voltage buffer or voltage follower.

Voltage follower implemented using opamp is shown in Figure (2-5). by connecting the output pin to the inverting input pin. So the equation for gain is given in Eq (26).

$$Av = 1 + (Rf/R1)^2 \quad (26)$$

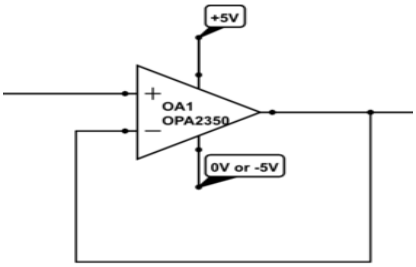


Figure 2-5: Buffer circuit [5]

Since output and inverting input are shorted, Rf=0, and R1 is not connected to ground, it can be considered as an open circuit and so R1 =∞ Therefore (Rf/R1) = (0/∞) = 0 and the gain is one. [4]

2.5.3 **Optical isolation**

It is done by isolating the primary input voltage from the secondary output voltage or the command input side from the load output side by using just light using a very common and valuable electronic component called an Opt coupler.

Opt couplers, “Opt-isolator or Photo-coupler”, are an electronic components that much two separate electrical circuits by an infra-red light.

The basic design of an opt coupler consists of a LED that produces infra-red light and a photo-sensitive semiconductor device that is used to detect the emitted infra-red beam.

When a current between 6 mA and 25 mA enters the anode of the infra-red diode, the latter is activated and delivers a light beam, which turns on to the semiconductor in the other side of the opt coupler. The revers operation cannot take place.

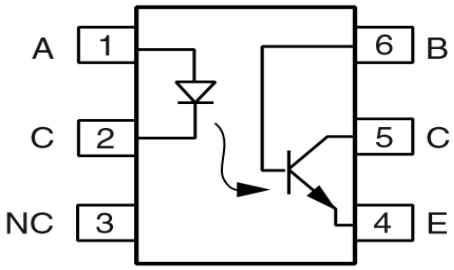


Figure 2-6: 4N34 opt coupler

2.5.4 **MOSFET and IGBT technology**

Today’s Power Electronics uses MOSFETs and IGBTs in most applications for switching, driving …… ect. The most important advantage of MOSFETs is the high frequency switching. Its limit factors are: transit time of electrons across the drift region and the time required to charge and discharge the input Gate and ‘Miller’ capacitances.

The main advantage of IGBT is an injecting region on its Drain side to provide conductivity of the Drain drift region which reduces the losses, when compared to an equally rated high voltage MOSFET.

When using IGBTs or MOSFETs, driving circuit is required to control the turning-on\off. Driver circuits designed for driving MOSFET can be used to drive an IGBT.

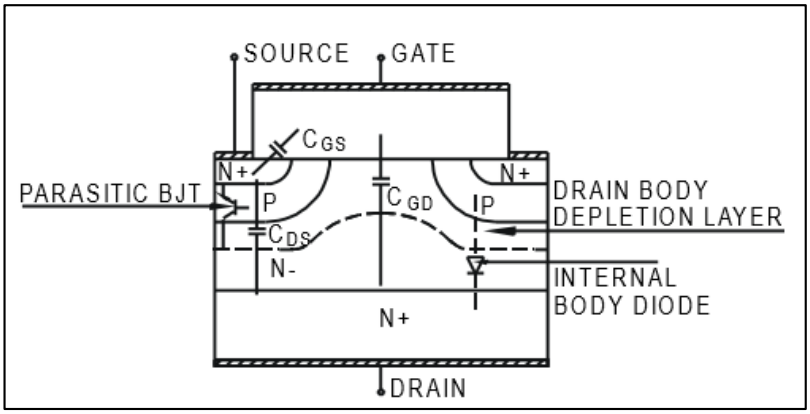


Figure 2-7: Cross section N-Channel MOSFET [6]

The IGBT driver serves to charge the gate of the power electronic device with a sufficient power to turn it on the switch or discharge to turn it off. The power required is calculated as shown in Eq (27)

$$P_G = Q_G * F_{IN} * \Delta V_{Gate} + C_{GE} * F_{IN} * \Delta V_{Gate}^2 \quad (27)$$

Where: F_{IN}: is the switching frequency.

P_G: is the switching power.

Q_G: is the Gate charge.

ΔV_{Gate}: is the swing voltage.

C_{GE} : is the capacitance between gate and emitter to be charged and discharged during a cycle.

2.5.5 **Opt driver**

The opt diver is the most used because it provides an isolation between the command side and high power side which is the case in our project., it is LED diode that activate with a current in between 6mA and 25 mA at the input side, and half bridge of two p-channel transistors at the output side with common input that comes from the light receiver diode, when the input diode is on the upper transistor is on and delivers 15 V brought from source to the IGBTs gate and charge gate-emitter capacitor and the lower is off that's ON state.

When the input LED is OFF, the lower transistor is activated and the upper remain off that provide a short from gate emitter terminal through the gate resistor. One can add a source of -5 to -15 to speed up the switching OFF and keep OFF state when needed. The two transistors are never gated at the same time. Figure (2-8)

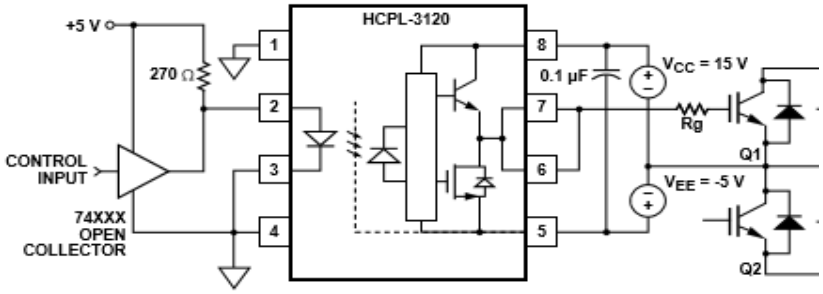


Figure 2-8: HCPL 3120 [7]

2.5.6 **Compensation using bidirectional switch (AC chopper)**

Single phase AC choppers is a power electronics converter with four switches used to control the current and voltage, in this project, it is used to control the voltage and current as switch between an inductor and capacitor to compensate the phase shift between them.

As shown figures (2-9, 2-10) it is composed of series arm and parallel one. Each arm has a two IGBTs emitter to emitter connected in away to provide bidirectional switching. IGBTs of both arms are switched on and off such that no short circuit is provided in the circuit.

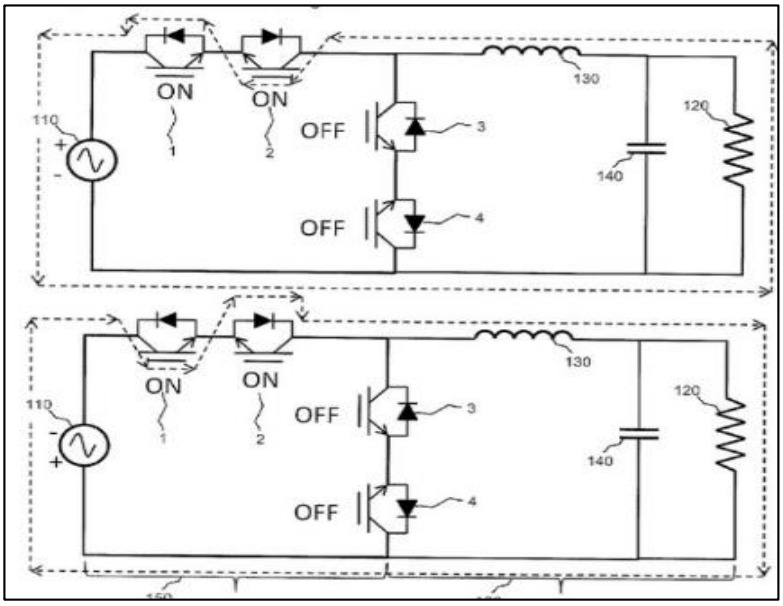


Figure 2-9: Series conduction mode AC chopper [8]

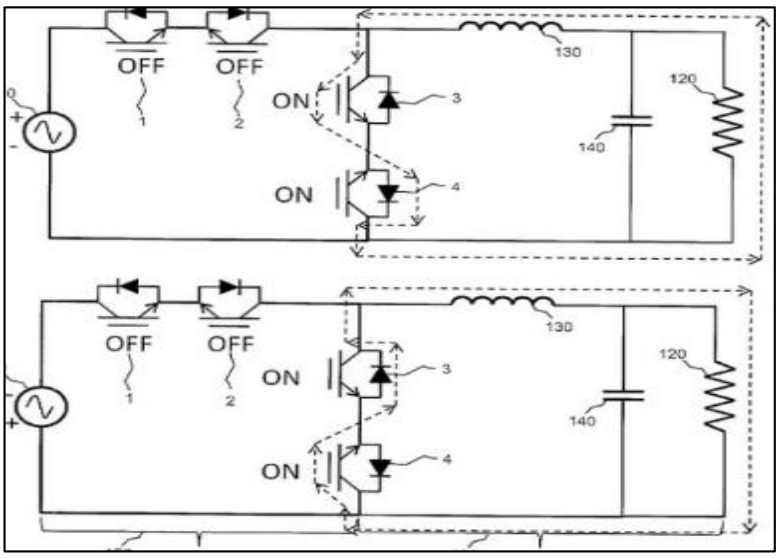


Figure 2-10: Parallel conduction mode [8]

In figure (2-11) Taking an initial state and compensation is required, a switching mode through a specified states is required, otherwise a short circuit is provided. In our case we have two initial states with the direction of current must be taken into consideration. Inductive or capacitive initial states, and negative or positive current. And the time of compensation depends on the duty cycle of the generated PWM.

Inductive to capacitive:

Table 1: switching states for inductive to capacitive compensation positive and negative current

	Positive current				Negative current			
	IGBT1	IGBT2	IGBT3	IGBT4	IGBT1	IGBT2	IGBT3	IGBT4
State 1	ON	ON	OFF	OFF	ON	ON	OFF	OFF
State 2	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF
State 3	ON	OFF	OFF	ON	OFF	ON	ON	OFF
State 4	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF
State 5	OFF	OFF	ON	ON	OFF	OFF	ON	ON

Capacitive to inductive:

Table 2: : switching states for inductive to capacitive compensation positive and negative current

	Positive current				Negative current			
	IGBT1	IGBT2	IGBT3	IGBT4	IGBT1	IGBT2	IGBT3	IGBT4
State 1	0FF	0FF	ON	ON	0FF	0FF	ON	ON
State 2	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON
State 3	OFF	ON	ON	OFF	ON	OFF	OFF	ON
State 4	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF
State 5	ON	ON	OFF	OFF	ON	ON	OFF	OFF

The switching states are built to avoid any short circuit. Taking into consideration the current direction on principle of switching off the IGBT which has an conductive diode in the same direction with present current for the conductive arm first, then switch on the main IGBT that has reversed diode in the other arm to insure the flow of current, after that switch OFF the other IGBT in the main arm and finally switch the last IGBTS.

Operation principle

Beginning by the analogue input that enters the FPGA board then converted to a digital data which represent the signal that must be compared with the carriers signal in the PWM code.

When the PWM signal is generated means that the desired reactive power is adjusted and here comes the AC choppers turn by switching between the inductor and the coil without forgetting the direction of current that should be return from the end of the AC chopper to the FPGA to select the state switching as seen in the tables.

The final circuit: figure (2-11)

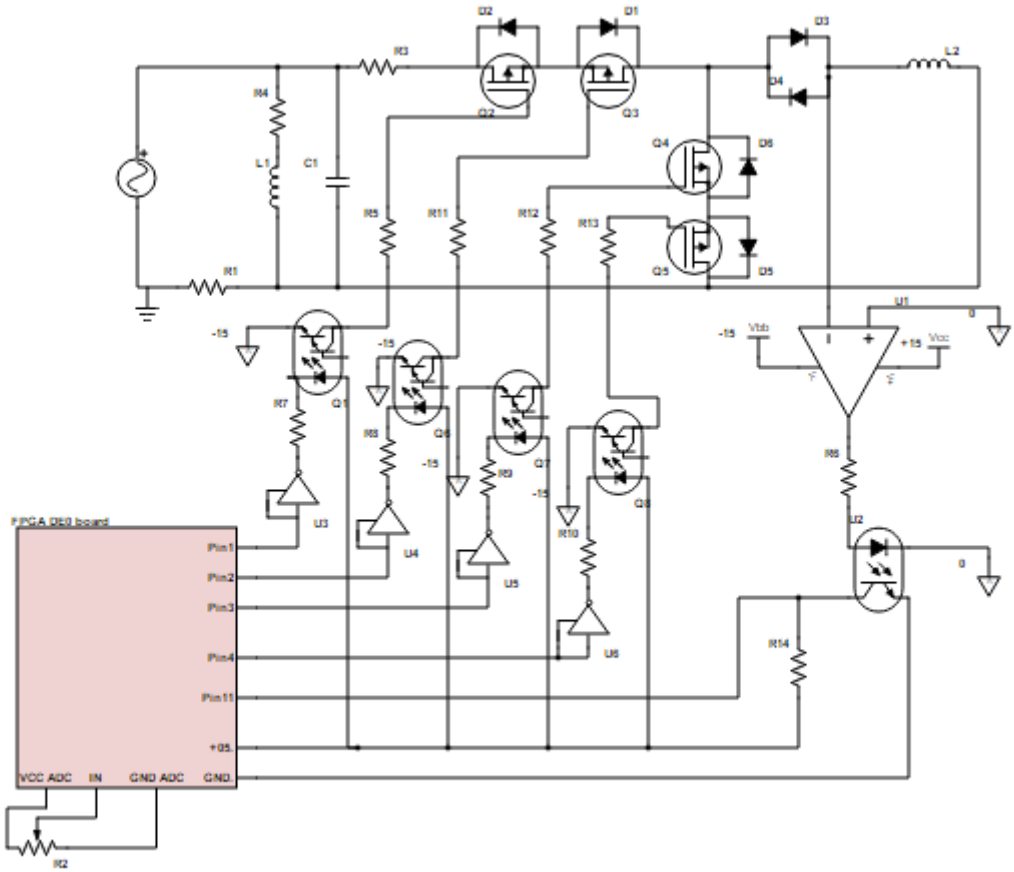


Figure 2-11: SVC based on FPGA control and AC chopper switching

Chapter III

3 .FPGA implementation

As seen in the previous chapter, the project requires PWM generation and signals and control the AC chopper switches.

The embedded systems is one of the precise and accurate method to generate our control signals using a programmable board like FPGA Altera board.

FPGA can replace the IC's and allow to create fast low level logic devices with a high speed, Compared to the other boards, FPGAs are more precise, high speed interfaces "RAM, HDMI, ADC……..", Soft core can be implemented "µcontroller ……" using the logic FPGA. The total control of the board means we can create & implement the process we want then send it to the desired pin on our board without any limitation compared to the µcontroller.

3.1 FPGA

Field Programmable Gate Array are semiconductor devices that are based around a matrix of configurable logic blocks (CLBs) connected via programmable interconnects. FPGAs can be reprogrammed to desired application or functionality requirements after manufacturing.

This feature distinguishes FPGAs from Application Specific Integrated Circuits (ASICs), which are custom manufactured for specific design tasks.

Although one-time programmable (OTP) FPGAs are available, the dominant types are SRAM based which can be reprogrammed as the design evolves.

3.2 FPGA cyclone V DE0 Nano soc board

The Atlas-SoC Software Development Kit presents a robust hardware design built around the Altera System-on-Chip (SoC) FPGA, which combines the latest dual-core Cortex-A9 embedded cores with industry-leading programmable logic for ultimate design flexibility. Users can now leverage the power of tremendous re-configurability paired with a high-performance, low-power processor system.

Altera's SoC integrates an ARM-based hard processor system (HPS) consisting of processor, peripherals and memory interfaces tied seamlessly with the FPGA fabric using a high-bandwidth interconnect backbone.

The Atlas-SoC development board is equipped with high-speed DDR3 memory, analogue to digital capabilities, Ethernet networking, and much more that promise many exciting applications. [9]

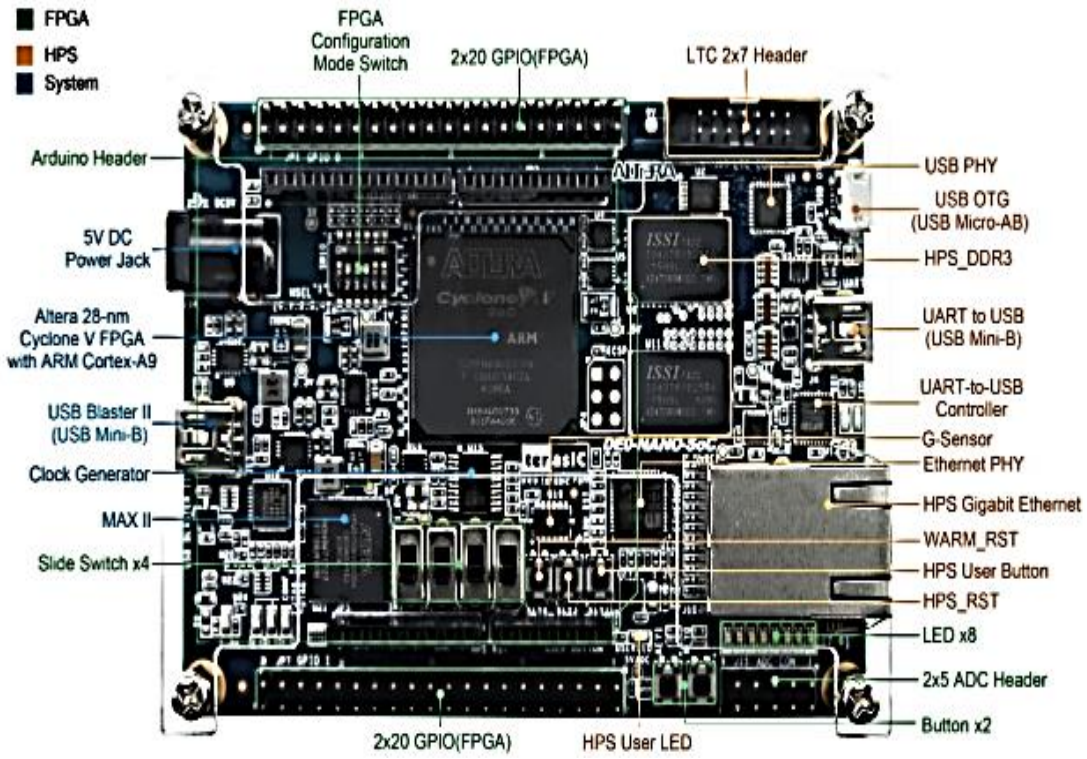


Figure 3-1: Component of DE0 board upper side

3.3 Project implementation on DE0 board

The implementation was made by programing and configuration the component on the board to generate the main signals to switch on our IGBTS, meaning a hardware design.

At the beginning the implementation was an open loop control, consisting on an analogue input varied with potentiometer at the input terminals of the LTC 2308 analogue to digital converter then the digital data should be sent to the PWM code in the FPGA unit to generate the PWM signal.

after that the PWM signal should pass to the state machine for having the four main signals in case of single phase regulation to control the four switches of our AC chopper. Figure 3-2 shows hardware design on DE0 board.

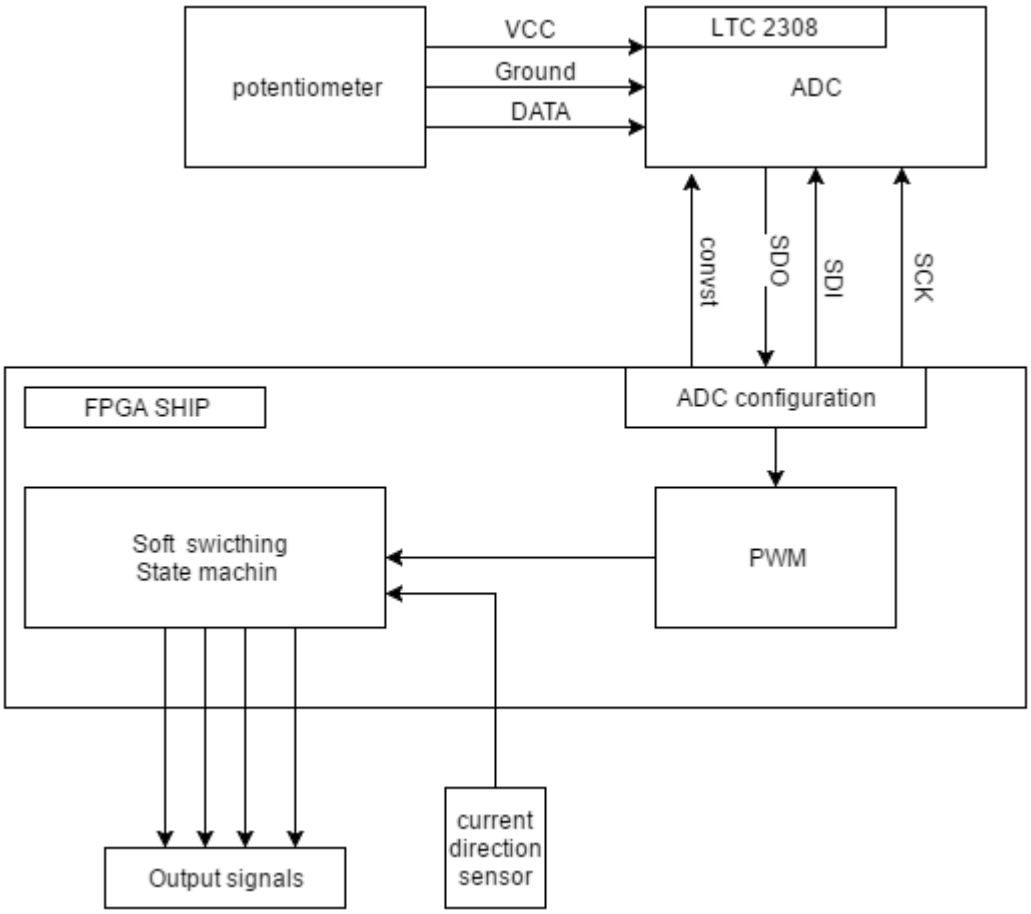


Figure 3-2: Implementation on FPGA

3.3.1 ADC LTC 2308

The LTC 2308 is a low noise, 500ksps, 8-channel, 12-bit ADC with a Serial Peripheral Interface (SPI) MICROWIRE compatible serial interface. This ADC includes an internal reference and a fully differential sample-and-hold circuit to reduce common mode noise.

The internal conversion clock allows the external serial output data clock (SCK) to operate at any frequency up to 40MHz. The LTC2308 operates from a single 5V supply and draws just 3.5mA at a sample rate of 500ksps. The auto-shutdown feature reduces the supply current to 200μA at a sample rate of 1ksps.

The LTC2308 is packaged in a small 24-pin 4mm × 4mm QFN. The internal 2.5V reference and 8-channel multiplexer further reduce PCB board space requirements.

The low power consumption and small size make the LTC2308 ideal for battery operated and portable applications, while the 4-wire SPI compatible serial interface makes this ADC a good match for isolated or remote data acquisition systems. Figure (3-3). [10]

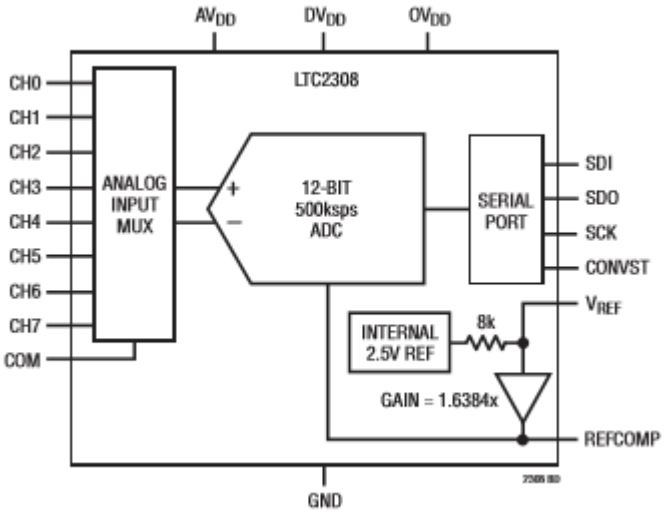


Figure 3-3: LTC 2308 ADC block diagram [10]

AVDD: 5V Analog Supply. The range of AVDD is 4.75V to 5.25V. Bypass AVDD to GND with a 0.1µF ceramic and a 10µF tantalum capacitor in parallel, Pins 12, 13 on the FPGA.

OVDD: Output Driver Supply, Bypass OVDD to GND with a 0.1µF ceramic capacitor close to the pin. The range of OVDD is 2.7V to 5.25V, Pin 19 on the FPGA.

DVDD: 5V Digital Supply, The range of DVDD is 4.75V to 5.25V. Bypass DVDD to GND with a 0.1 µF ceramic and a 10µF tantalum capacitor in parallel, Pin 21.

CH0-CH2: Channel 0 to Channel 2 Analog Inputs, can be configured as single ended or differential input channels, Pins 22, 23, 24.

GND: Exposed Pad Ground, Must be soldered directly to ground plane, Pin 25 on the FPGA.

CONVST: (Conversion Start) A rising edge at CONVST begins a conversion. For best performance, ensure that CONVST returns low within 40ns after the conversion starts or after the conversion ends, Pin 14.

SDI : Serial Data Input. The SDI serial bit stream configures the ADC and is latched on the rising edge of the first 6 SCK pulses, Pin 15.

SCK: Serial Data Clock, SCK synchronizes the serial data transfer, The serial data input at SDI is latched on the rising edge of SCK. The serial data output at SDO transitions on the falling edge of SCK, Pin 16. [10]

3.3.1.1 ADC functionality

The LTC 2308 doesn't need any ADC code because it is implemented hardware on the chip but it must be configured via a code from the FPGA.

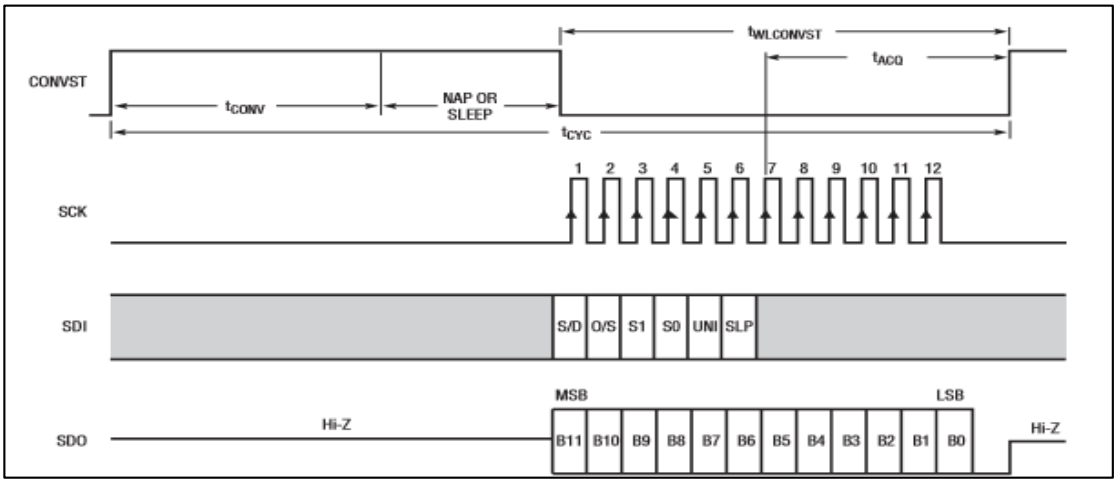


Figure 3-4: SPI ADC configuration [10]

The required configuration must respect the timing seen on Figure (3-4) the data conversion starts when the CONVST signal remains high, once the high edge comes, new data cannot be converted intel the current conversion is completed, this signal should be high during the conversion time which is the SLP bit that must be stet to a logic 1 in this case of configuration and nap time when SLP set to 0 the nap mode between conversions, thereby reducing the average power dissipation as the sample rate decreases.

Once the MSB appears on SDO pin 12 clock are generated from SCK pin and her comes the data exchange between the FPGA and the ADC bit per bit serially at each SCK clock or when the edge appears a configuration is sent and a data is received, Finite State Machine is used to generate the configuration code in our case.

3.3.2 Pulse Width Modulation signal

Is the control signal and the variation depends on the analogue input converted to digital by ADC that gives data from 0 to 255, which are compared to carrier signal of 255 "11111111".

This signal is generated by a code which consists on an up and down counter increases at each clock edge, and when it reaches the maximum "255" value, start decreasing one number each clock cycle until it reaches zero and the pattern repeats again. This will give a triangle waveform. This triangular carrier signal is compared with data brought from the ADC.

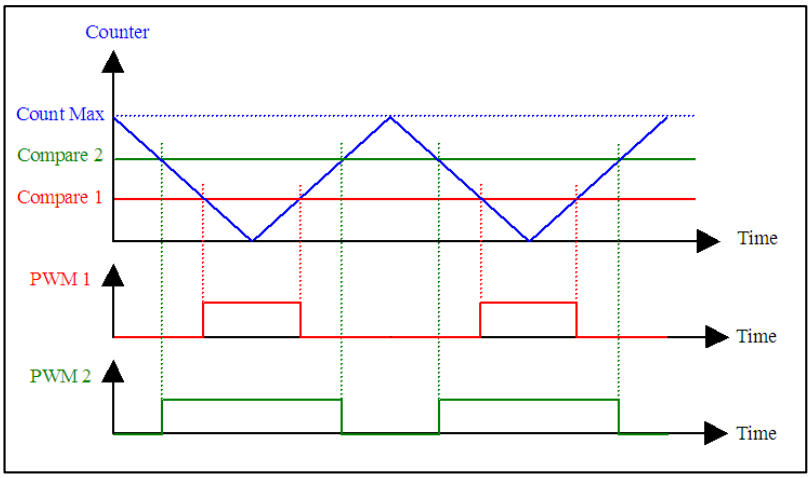


Figure 3-5: PWM triangular carrier signal [10]

3.3.3 Finite state machine FSM

The PWM generated signal cannot control four switches at once in single phase case, due to the current direction signal so we must extract four signal from the PWM treating the cases when the PWM is up and down and taking the direction of current into account.

FSM is sequential logic operation, it uses memory logic and the input change to make transition each clock cycle which makes it very fast. Its structure also makes it less difficult and more optimum.

Finite state machine must be used in this code due to the presence of state transition to make the code smaller and easier to manage. Figure (3-6) shows structural diagram of our FSM.

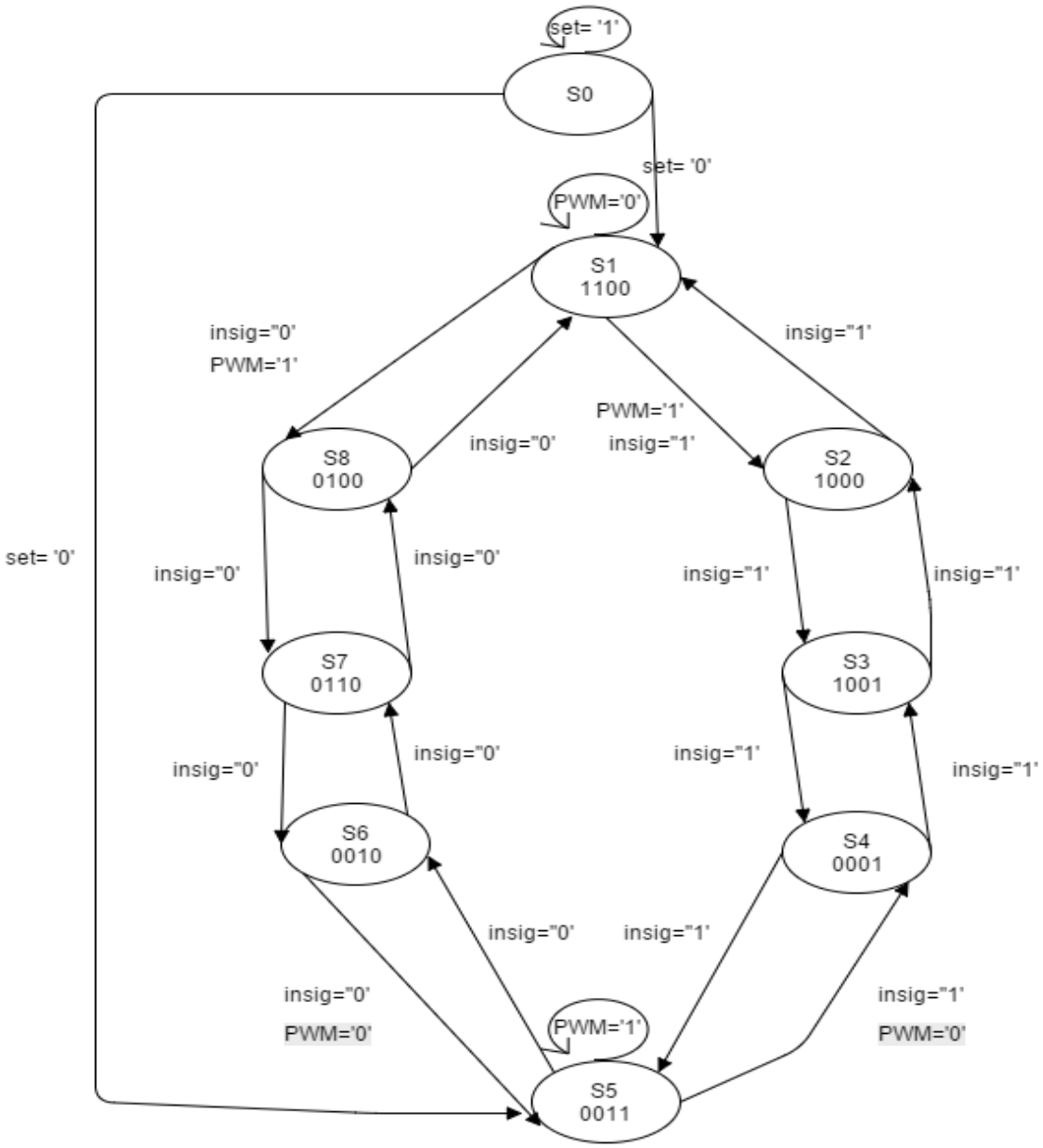


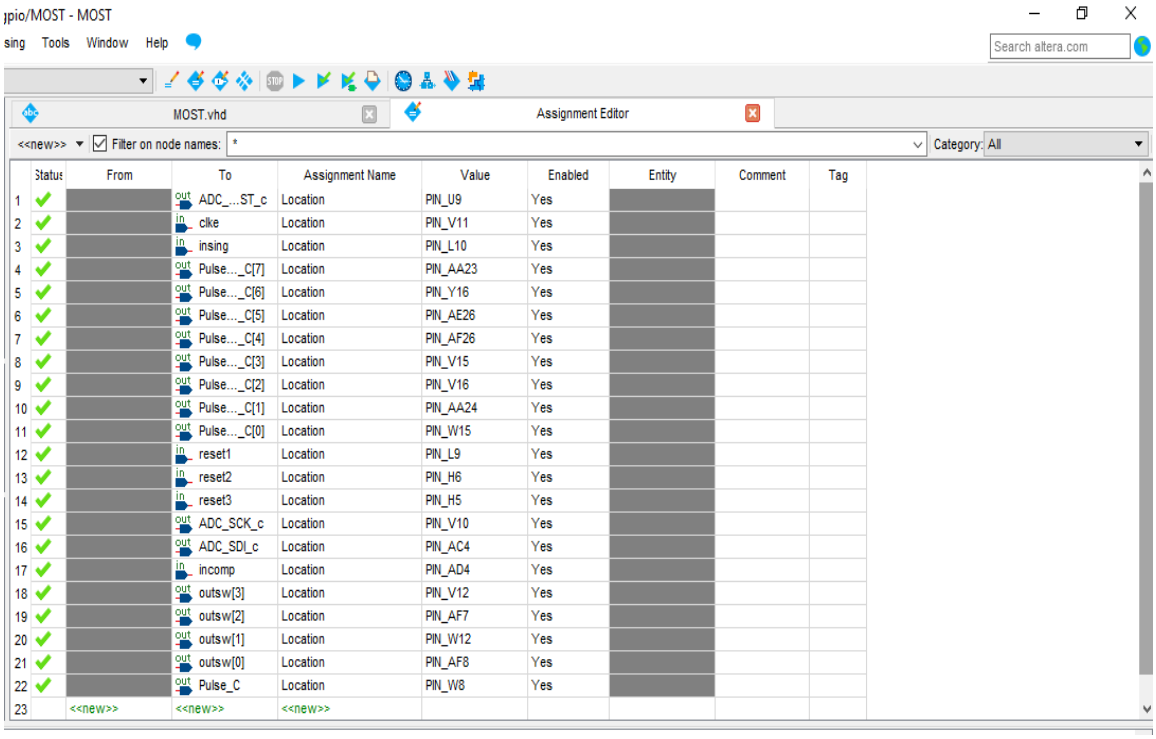
Figure 3-6: FSM block diagram

The S0 state doesn't have an output, it is made to detect our initial state of the switches S1 or S5. We must verify the two transition conditions which are in our case PWM & direction of current to choose our state transition to avoid short circuit.

- For S1 to be an initial state If PWM='0' it keep in S1 until PWM changes to '1'.
- For S1 to be an initial state If PWM='1' & insig='0' path is {S1, S8, S7, S6, S5}.
- For S1 to be an initial state If PWM='1' & insig='1' path is {S1, S2, S3, S4, S5}.
- For S5 to be an initial state If PWM='1' it keep in S1 until PWM changes to '0'.
- For S5 to be an initial state If PWM='0' & insig='0' path is {S5, S4, S3, S2, S1}.
- For S5 to be an initial state If PWM='1' & insig='1' path is {S5, S6, S7, S8, S1}.

3.4 DE0 implementation

As defined previously the codes written in form of one component then compile, assign the pins PWM & switches signals to the GPIO_0 pins and connect the potentiometer at the terminals of ADC.



	Status	From	To	Assignment Name	Value	Enabled	Entity	Comment	Tag
1	✓		out ADC_...ST_c	Location	PIN_U9	Yes			
2	✓		in clke	Location	PIN_V11	Yes			
3	✓		in insing	Location	PIN_L10	Yes			
4	✓		out Pulse..._C[7]	Location	PIN_AA23	Yes			
5	✓		out Pulse..._C[6]	Location	PIN_Y16	Yes			
6	✓		out Pulse..._C[5]	Location	PIN_AE26	Yes			
7	✓		out Pulse..._C[4]	Location	PIN_AF26	Yes			
8	✓		out Pulse..._C[3]	Location	PIN_V15	Yes			
9	✓		out Pulse..._C[2]	Location	PIN_V16	Yes			
10	✓		out Pulse..._C[1]	Location	PIN_AA24	Yes			
11	✓		out Pulse..._C[0]	Location	PIN_W15	Yes			
12	✓		in reset1	Location	PIN_L9	Yes			
13	✓		in reset2	Location	PIN_H6	Yes			
14	✓		in reset3	Location	PIN_H5	Yes			
15	✓		out ADC_SCK_c	Location	PIN_V10	Yes			
16	✓		out ADC_SDI_c	Location	PIN_AC4	Yes			
17	✓		in incomp	Location	PIN_AD4	Yes			
18	✓		out outsw[3]	Location	PIN_V12	Yes			
19	✓		out outsw[2]	Location	PIN_AF7	Yes			
20	✓		out outsw[1]	Location	PIN_W12	Yes			
21	✓		out outsw[0]	Location	PIN_AF8	Yes			
22	✓		out Pulse_C	Location	PIN_W8	Yes			
23		<<new>>	<<new>>	<<new>>					

Figure 3-7: Pins assignment

As discussed previously the figure below shows the switches signals:

a) Positive current:

Falling edge PWM:

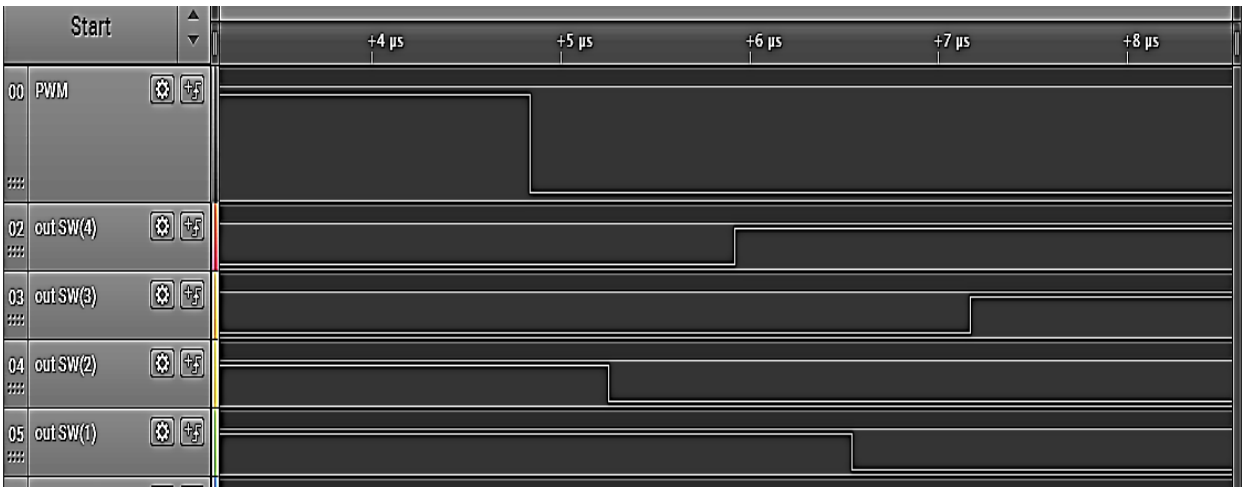


Figure 3-8: Signals at positive current falling edge

Rising edge:

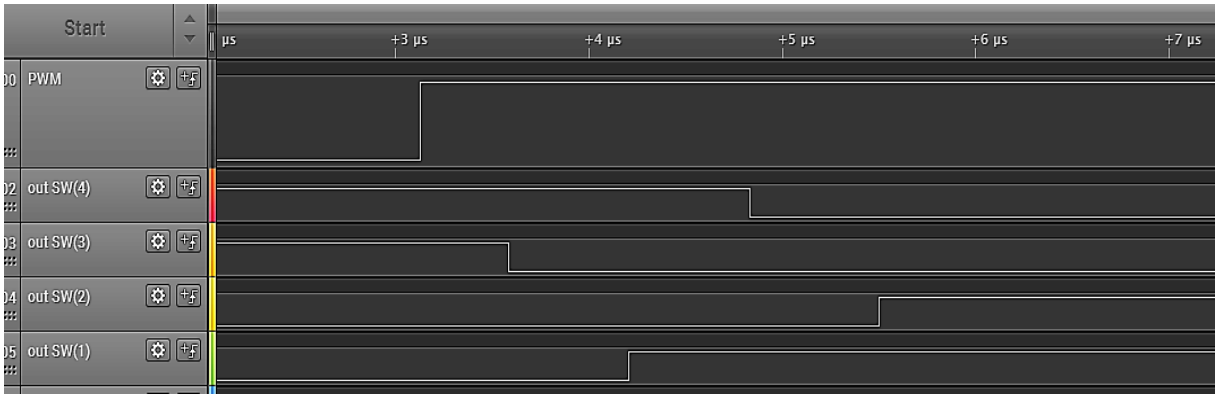


Figure 3-9: Signals at positive current rising edge

b) Negative current:

Rising PWM edge:

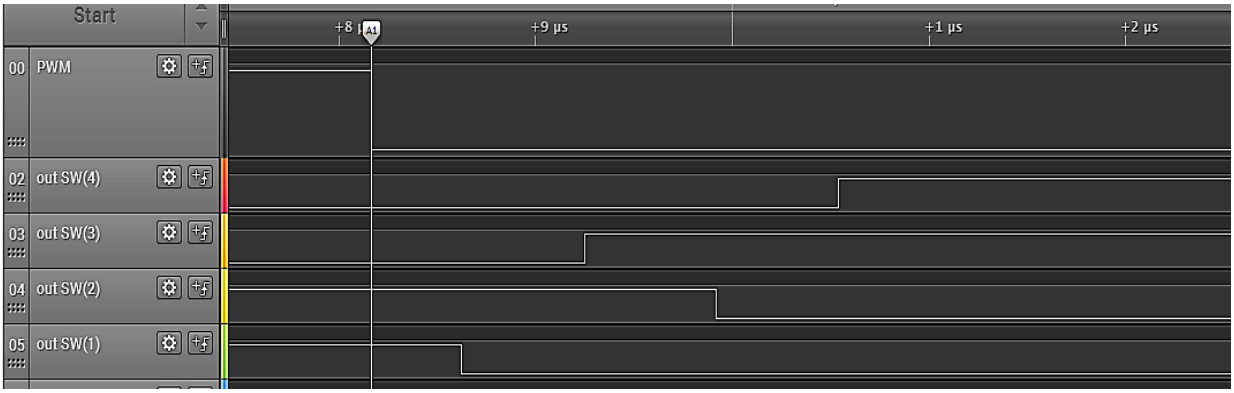


Figure 3-10: Signals at negative current rising edge

Falling PWM edge:

Figure 3-11: Signals at negative current falling edge

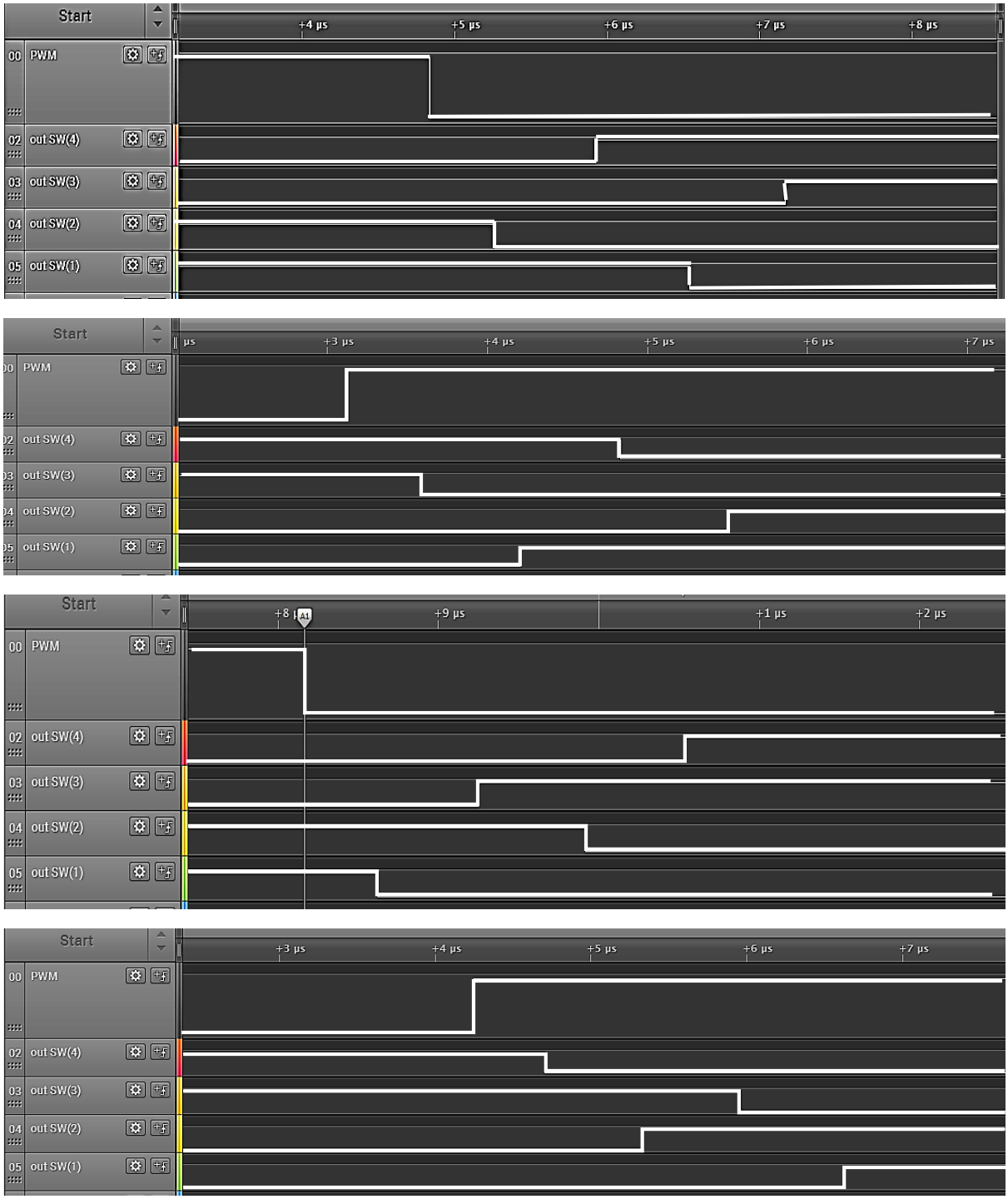


Figure 3-12: Highlighted figures (3-8, 3-9, 10, 3-11)

3.5 **Discussion**

One can notice that at each PWM transition or change in current sign, a state transition change, also the frequency of each signal is 3.01 KHz as shown in figures (3-8, 3-9, 3-10, 3-11), by using the 50 MHZ clock generator of the FPGA and clock divider added in PWM code we get our PWM frequency:50 MHz / 2^4 and the 8 bit up down counter of the PWM, the new frequency will be 3 KHz signal. Means that PWM frequency and switching can be adjusted.

The delay between each switch is around 1.4 µs provided by a counter added on the FSM code 50 MHz / 2^6 that's can give time to IGBTs to take action to prevent any short circuit. This time is very important.

Chapter IV:

4 .Simulation and implementation

4.1 Simulation

For any experiment to test a simulation should be done to minimize the damages especially power electronics circuits based on hard/software signal generation. Two software are used to simulate the circuit based on FPGA in real time which namely MATLAB Simulink and Modelsim. The real interconnection between the two software is known as Co-simulation.

Modelsim is used to create FPGA model with Matlab Simulink using HDL coder library in Simulink. The first step is to create a common folder between Matlab and modelsim. MATLAB command and tap >> vsim to open modelsim.

As necessaire condition we have to put our code on it and save it in the same folder, we compile simulate our work on model sim and we tap >>vsimulink xxx.vhd in modelsim command "xxx is the name of the vhdl file", we re-simulate our project and re-tap >>vsimulink xxx.vhd.

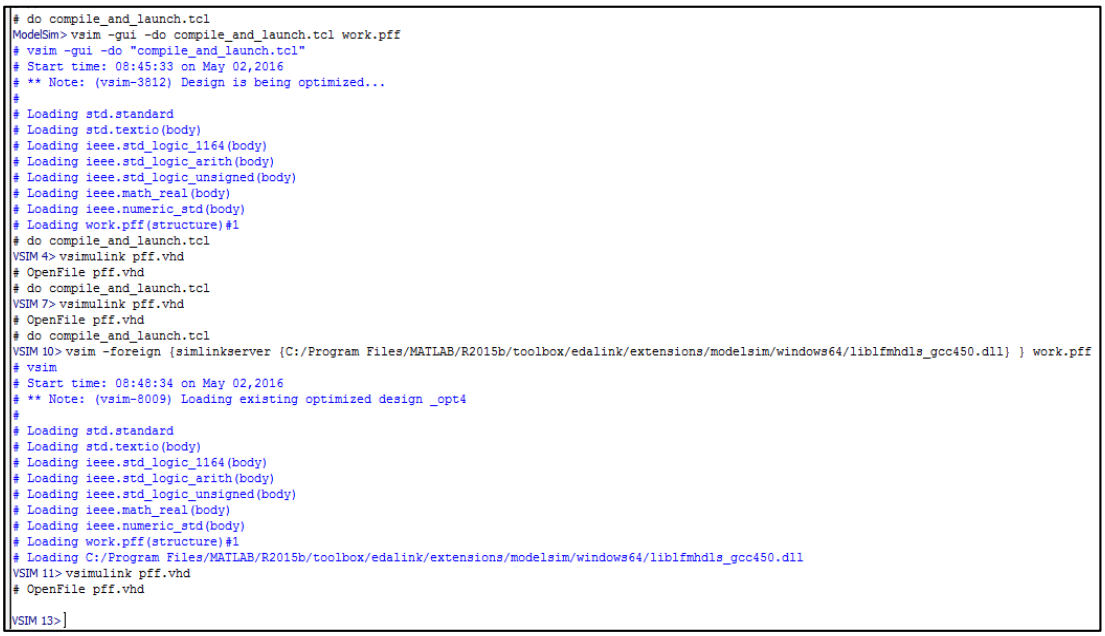


Figure 4-1: Link between MATLAB & Model sim

As seen in figure we can see that model sim succeeded to create a link with Matlab, in this stage we can simulate in real time.

The FPGA block is made just by adding a block from HDL coder mounter graph to our model then set the inputs and outputs.

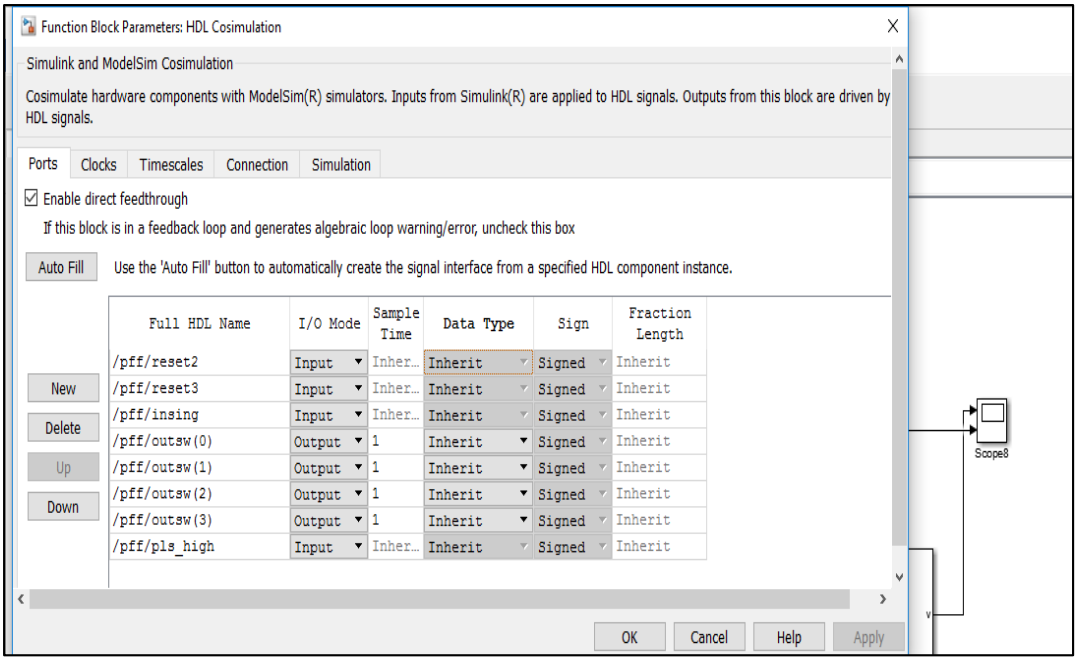


Figure 4-2: Setting inputs & outputs on MATLAB

As the simple time on Matlab is limited to 1 ns. to deal with this frequency source has been reduced to 0.000015 Hz.

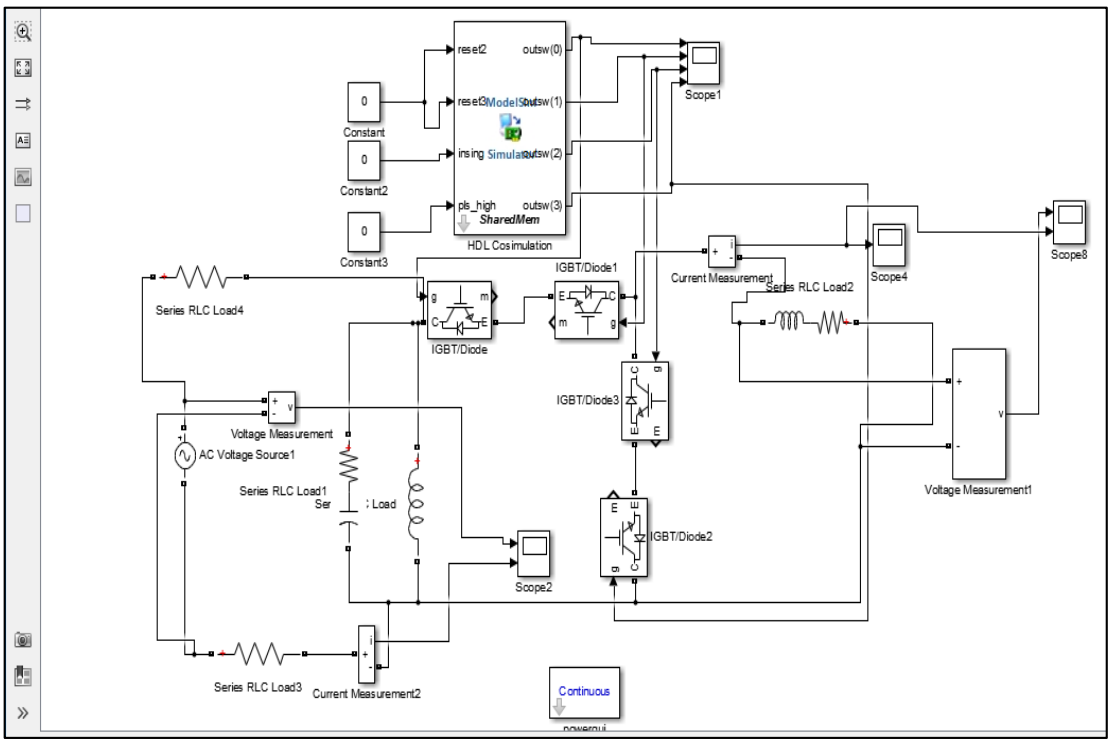


Figure 4-3: Circuit design on MATLAB Simulink

4.1.1 **Simulation outputs**

At duty cycle 0 %:

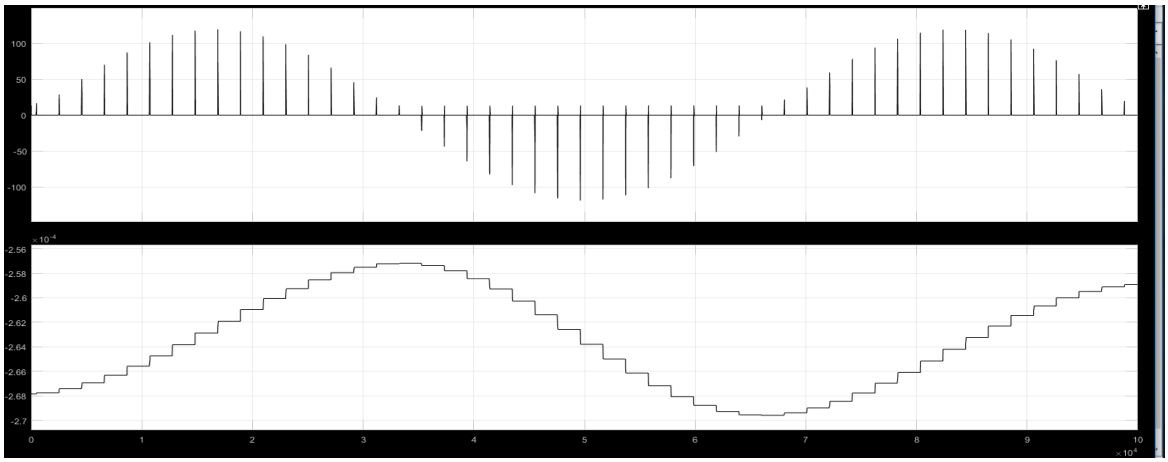


Figure 4-4: AC chopper voltage & coil current at 0% duty cycle

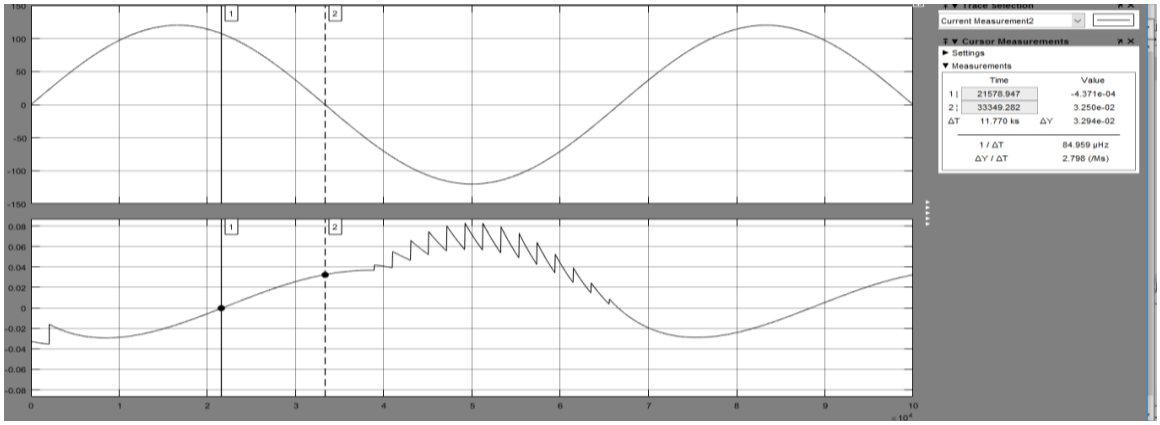


Figure 4-5: Voltage source and current signals at 0% duty cycle

At duty cycle 20 %:

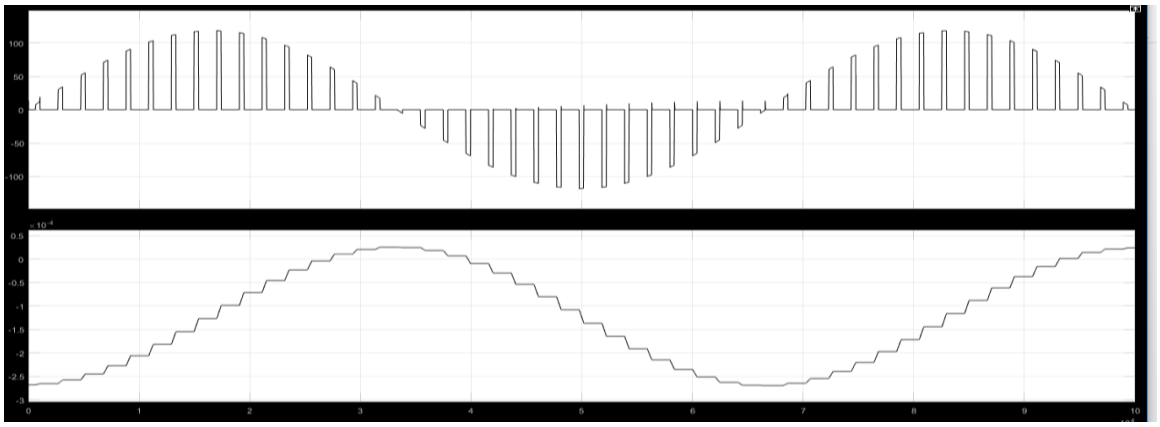


Figure 4-6: AC chopper voltage & coil current at 20% duty cycle

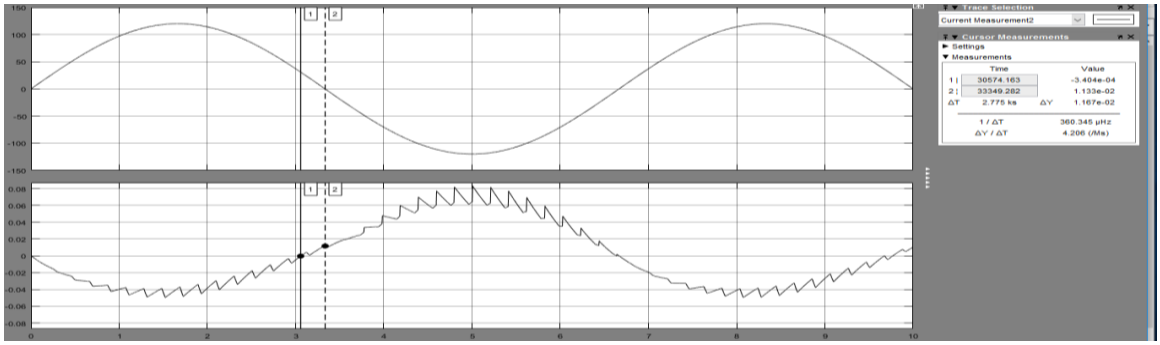


Figure 4-7: Voltage and current signals at20% duty cycle

At 50 %

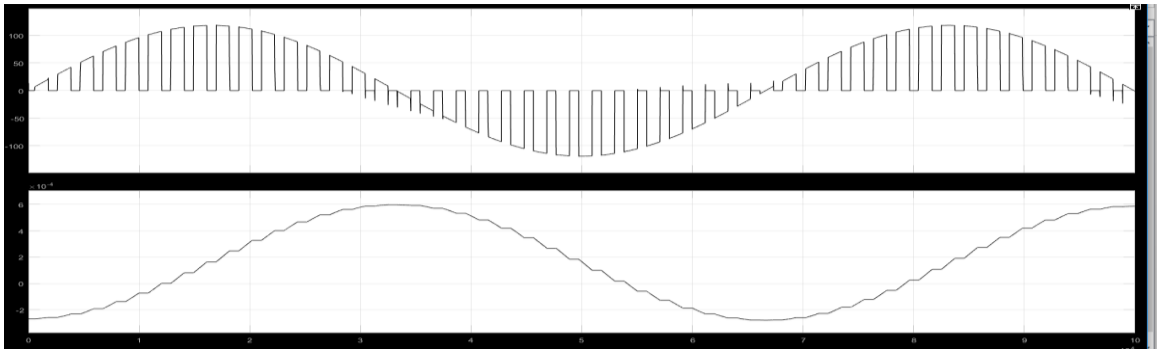


Figure 4-8: AC chopper coil voltage & coil current outputs 50% duty cycle

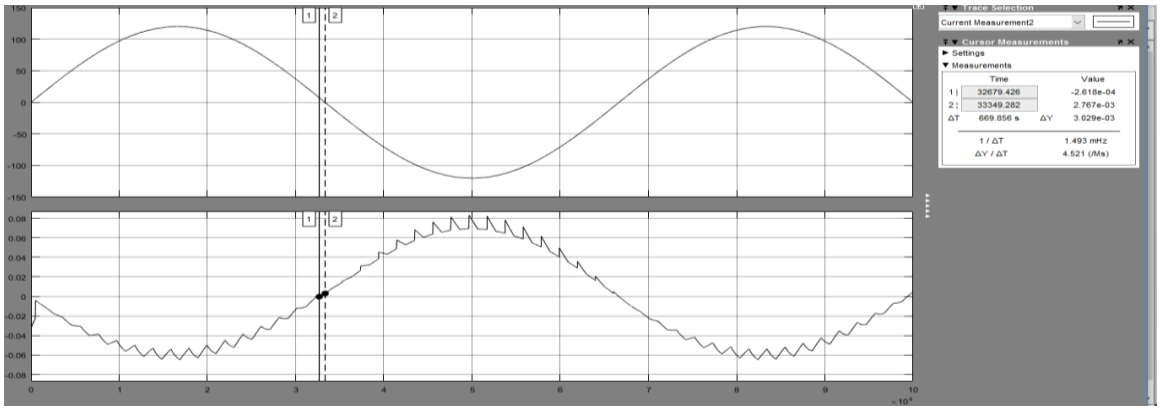


Figure 4-9: Voltage and current signals at 50% duty cycle

4.2 Simulation results and Discussion

In figures (4-4, 4-5) one can see four signals source voltage, the voltage after AC chopper, current of the coil and the current at the second terminal of the source. One can notice that the ac chopper has totally cut the signal vertically depending on duty cycle of 3 KHz PWM signal generated by the FPGA or most of the duty cycle in conduction mode which gives an amplitude of the source and the rest remain zero. Figures (4-4, 4-6, 4-8) shows ac chopper output for different duty cycle.

The current at the coil shown on figures (4-5, 4-9,4-7) has nearly 90° phase shift provided by the coil, also by changing the PWM, that is changing the duty cycle, it is clear that current amplitude at the coil is changing according to duty, cycle is 100% then the current amplitude is at maximum, that allow a good control of current coil.

One can also notice that a kind of stairs provided by the switching states between capacitor that inject current and the coil that absorbs it.

A comparison of voltage and current of the source, it is seen that current has a shift angle of 180° for 100 % PWM meaning a unity power factor. By reducing PWM the current amplitude doesn’t change but the variation of PWM makes the current shifts to the left. For 100% pf is nearly to 0.99 and for 0 % nearly 0.89 this allows us to conclude that the injection of reactive power has been changed.

4.3 Implementation

In the previous chapter, we have seen the duel simulation from both modelsim / MATLAB by using Simulink which called the Co-simulation and quartus vhdl code with the FPGA that is shown in the Logic oscilloscope software, next step is the design and the implementation of the topology in the real time, by identifying the main component that is used to install the circuit. At the end the results are presented and discussed.

4.3.1 Component

a) ASTONIA 12V AC 220V

The main power source is used is 220V AC but the drives need only 12V DC, so we use the 220/12 AC transformer supply source that is connected to the bridge to get the DC source to aluminate the gate driver of the control part of the network.

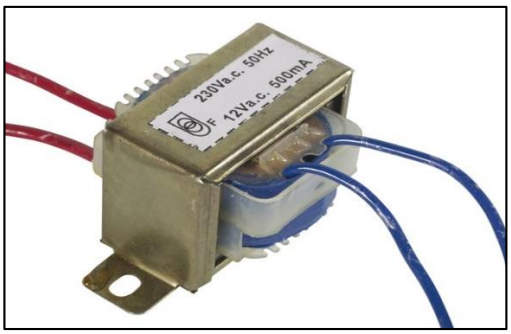


Figure 4-10: Single phase transformer

b) "SEP W06" Bridge

Voltage range is 50 to 1000 V. Maximum Average Forward Rectified Output Current at TA = 25o C. Surge overload ratings to 50 amperes peak.

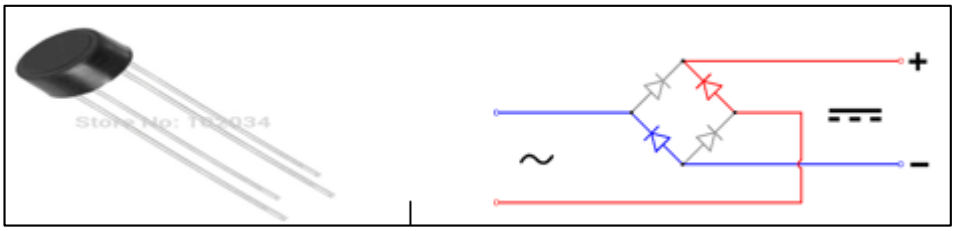


Figure 4-11: SEP rectifier bridge

Rating at 25℃ambient temperature unless otherwise specified. Single phase, half wave, 60 Hz, resistive or inductive load. For capacitive load, de-rate current by 20%.

c) "SFC 2815" and "LM 7915CT" voltage Regulator

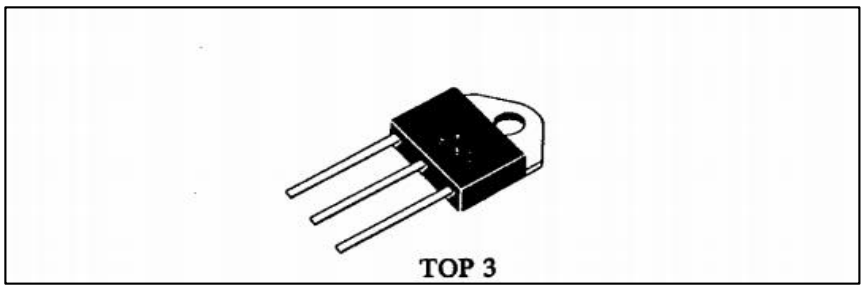


Figure 4-12: Voltage regulator

An automatically voltage regulator maintains a constant voltage level at +15 or -15 to supply the voltage of the OPAMP and the gate driver of the IGBTs, the input range is between 17.5 to 30 V output also 14.4 to 15.6 V.

d) "SN74LS540N" Buffer

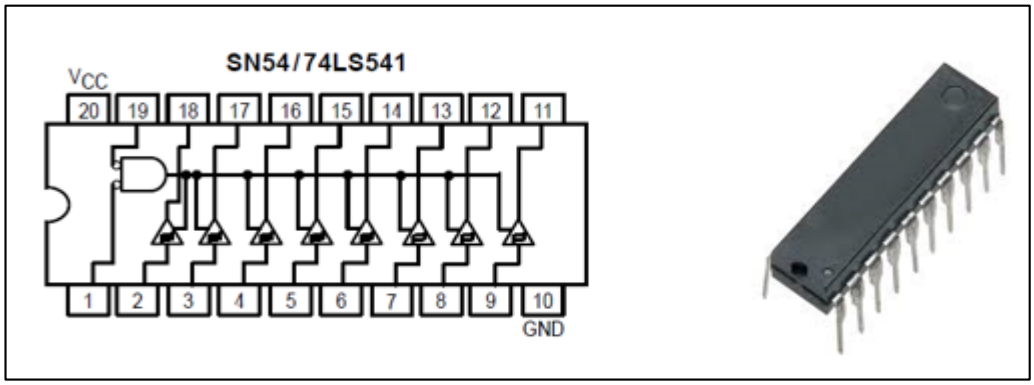


Figure 4-13: Buffer

Octal buffers and line drivers are designed to offer a pinout having the inputs and outputs on opposite sides of the package. The three-state control gate is a 2-input NOR, 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers.

The P-N-P Inputs Reduce D-C Loading.

Hysteresis at Inputs Improves Noise Margins.

INPUTS			OUTPUTS	
E_1	E_2	D	LS540	LS541
L	L	H	L	H
H	X	X	Z	Z
X	H	X	Z	Z
L	L	L	H	L

L = LOW Voltage Level.

H = HIGH Voltage Level.

X = Immaterial.

Z = High Impedance.

Figure 4-14: Buffer operation mode

The main purpose of the buffer in the circuit is to connect the FPGA output data to the gate driver IGBTs by selecting the switches with respect to the state machine cases.

e) "HCNW3120" drive

Gate drive opt coupler **HCPL-3120** contains a Gasp LED. The LED is optically coupled to an integrated circuit with a power output stage. These opt couplers are ideally suited for driving power IGBTs and MOSFETs used in motor control inverter applications.

The high operating voltage range of the output stage provides the drive voltages required by gate controlled devices. The voltage and current supplied by these opt couplers ratings up to 1200 V/100 A. For IGBTs with higher ratings, the HCPL-3120 series can be used to drive a discrete power stage which drives the IGBT gate.

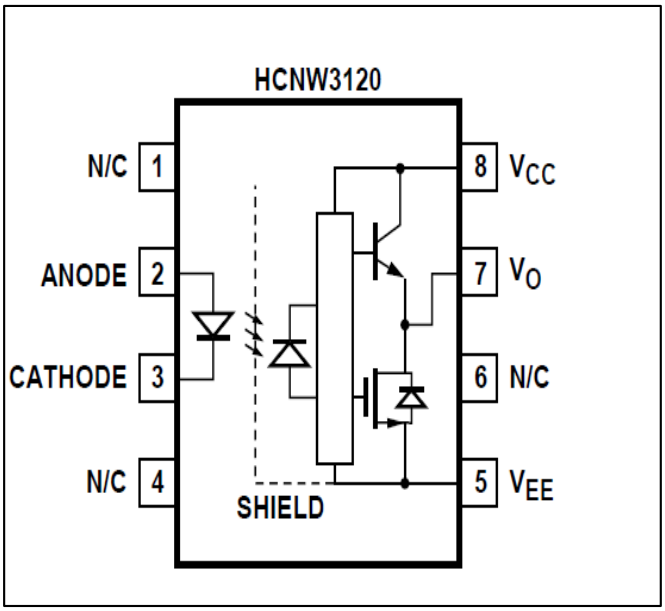


Figure 4-15: Gate drive optocoupler

f) K40T1202 "IGBT"

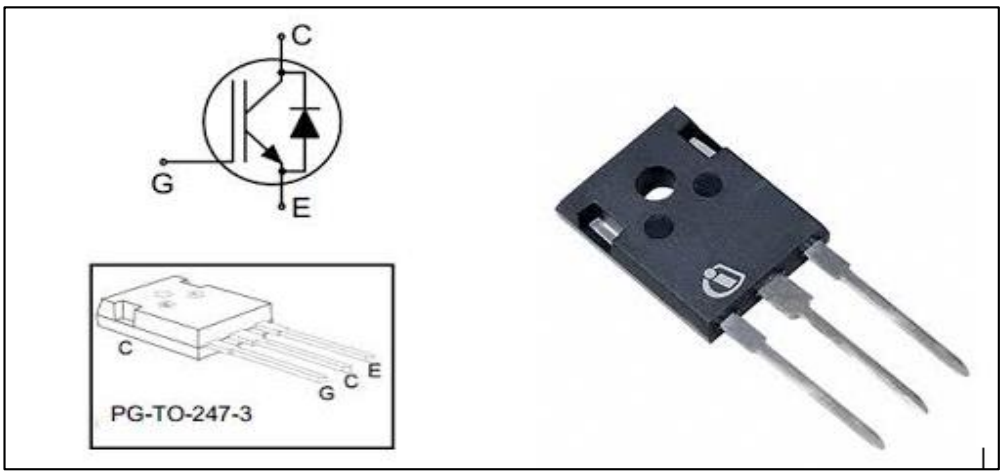


Figure 4-16: Insulated gate bipolar transistor

An insulated-gate bipolar transistor (IGBT) is a three-terminal power semiconductor device primarily used as an electronic switch, came to combine high efficiency and fast switching,

The IGBT has the output switching and conduction characteristics of a bipolar transistor but is voltage-controlled like a MOSFET. In general, this means it has the advantages of high-current handling capability of a bipolar with the ease of control of a MOSFET. However, the IGBT still has the disadvantages of a comparatively large current tail and no body drain diode.

MOSFETs and IGBTs: Similar But Different

In general, high voltage, high current and low switching frequencies favor the IGBT while low voltage, low current and high switching frequencies are the domain of the MOSFET

The IGBT technology is certainly the device of choice for breakdown voltages above 1000V, while the MOSFET is certainly the device of choice for device breakdown voltages below 250V. Between 250 to 1000V, there are many technical papers available from manufacturers of these devices, some preferring MOSFETs, some IGBTs. However, choosing between IGBTs and MOSFETs is very application-specific and cost, size, speed and thermal requirements should all be considered.

MOSFETs are preferred in:

- High frequency applications (>200kHz).
- Wide line or load variations.
- Long duty cycles.
- Low-voltage applications (< 500W output power.

IGBTs have been the preferred device under these conditions:

- Low duty cycle.
- Low frequency (<20kHz).
- Narrow or small line or load variations.
- High-voltage applications (>1000V).
- Operation at high junction temperature is allowed (>100°C).

5kW output power.

Figure 4-17 shows some of the boundaries where it is fairly clear as to what is preferred, the MOSFET or IGBT, because we have the output frequency of the FPGA that represent the PWM frequency. It's about 3 khz and the voltage is clearly above 220V, therefore the IGBT is selected for this work.

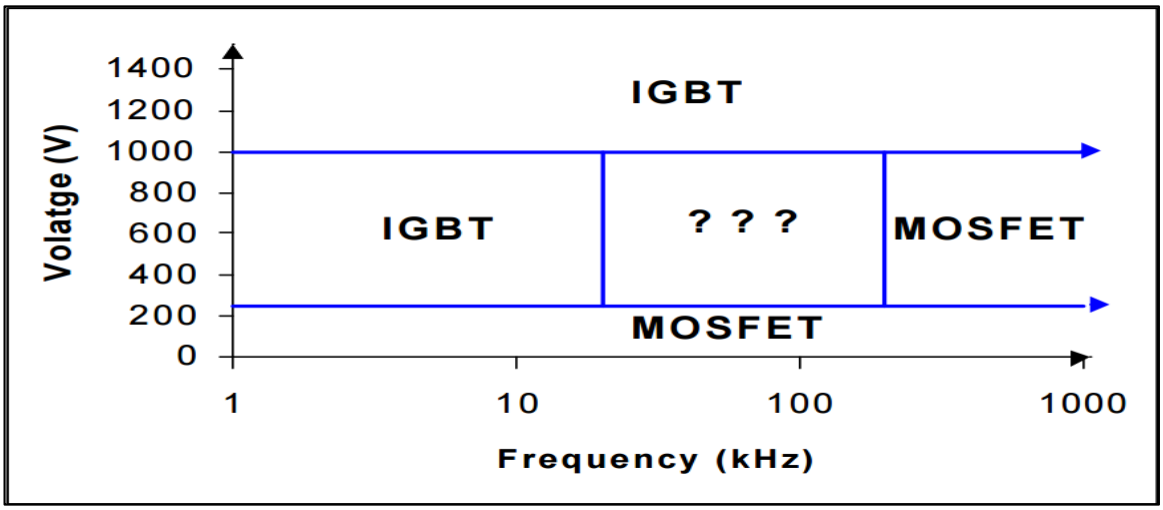


Figure 4-17: Selection of switch

4.3.2 Current sensor equipment

a) "OP27G" opamp

The opamp is used in current sensor to compare direction of the current that comes from bidirectional diodes, if it is in positive direction the output of the amplifier is about +15V else -15V.

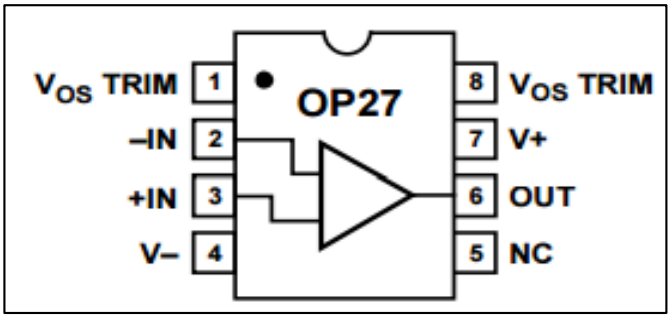


Figure 4-18: Operation amplifier [12].

The 2nd and 3rd pins are connected to the diodes,4th and 7th pins connected to -15, +15V respectively, pin 6 is output of the amplifier.

b) Opt coupler "4n35"

Opt coupler is a component that transfers electrical signals between two isolated circuits by using light, Opt-isolators prevent high voltage from affecting the system receiving the signal, input-to-output voltages up to 10 KV and voltage transients with speeds up to 10 kV/μs.

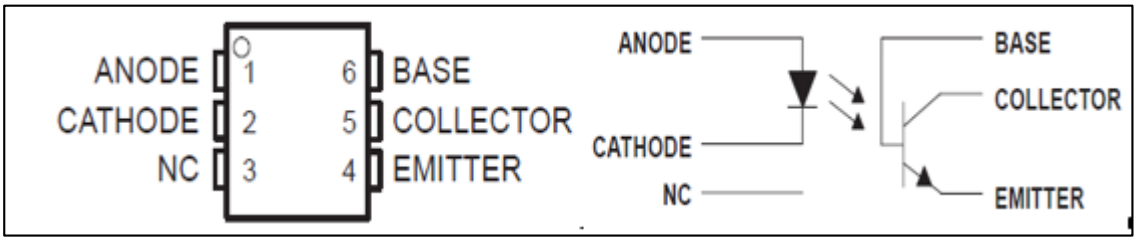


Figure 4-19: 4n35 opt coupler [13]

The cathode is connected to the output of the amplifier, anode linked to the ground of the supply for comparator. Collector and emitter receives voltage from Vcc and ground of GPIO. The output of the opt coupler returns back to the FPGA.

4.4 Circuit interconnection

4.4.1 AC chopper

The DE0 board generates PWM that have duty cycle depending on ADC, then the FSM VHDL code generates four signals depending on the PWM and the direction of the current brought from the circuit to the FPGA.

The four signals enters the "74LS540N" buffer inverter to fix the voltage at 5V and the current at 10 mA, the pins 19,1 and 10 are grounded, 20 is the Vcc brought from FPGA also 2,3,4 and 5 are the input buffer of the FSM signals brought from GPIO output of the FPGA figure(2-11, 3-2).

The buffer output should be connected to a 470 Ω resistor that enters the anode pin of the HCPL. When the signal generated is high the voltage at the output of the buffer should be 5V and the current is 10 mA, which are enough to activate the led and the output remains 15 V from pin 7 pulled by 10 Ω resistor.

10 Ω connected the gate of the IGBT, the emitter to -15 V as reference. At this stage we have four IGBTs ready to be connected as follow, emitter 01 to emitter 02, emitter 03 to emitter 04 and collector 02 to collector 03 building an AC chopper.

4.4.2 **Polarity current sensor**

To parallel diode connected between collector 02 and coil gives 0.5 V for positive current and - 0.5 for negative, taking the two ends of diodes to OP27G opamp at pin 2 & 3 and one of them should be taken to 0 V reference, gives at opamp out pin 6, +12 V when current is positive and – 12 V for negative current using 370 Ω, the signal from the opamp enters to cathode pin of 4n35 opt coupler and the anode to 0 V reference that give 1.2 V and 10 mA to turn on the led. Pin 4 to FPGA GND and pin 5 to 370 Ω then FPGA 5 V our signal is before the resistance figures (4-20).

4.4.3 **Implementation results**

Putting the prob1 on coil and prob2 at resistor of 1Ω prob1 on source and prob2 at collecto04 the oscilloscope shows:

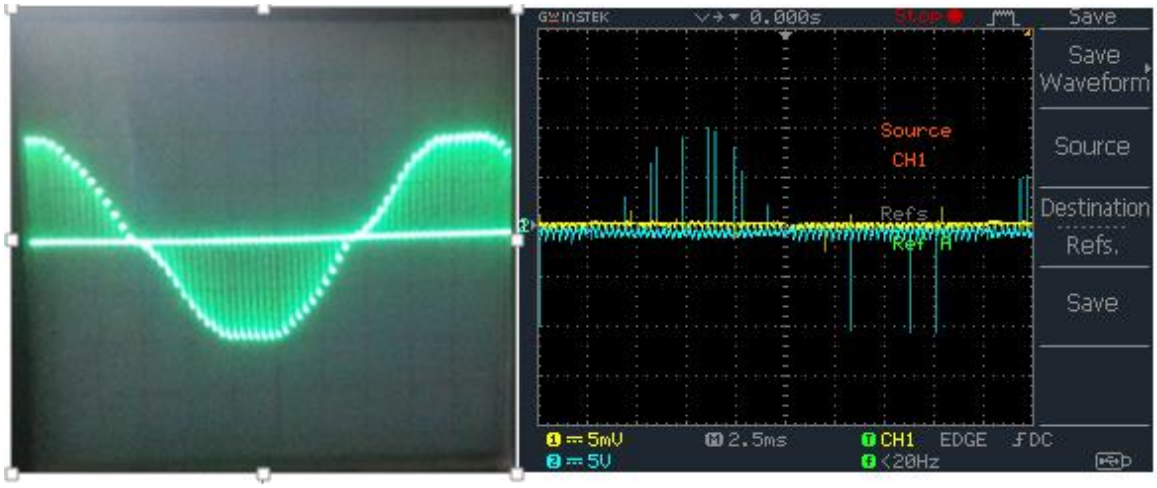


Figure 4-20: AC chopper output for 50% and 0%

a) Polarity sensor:

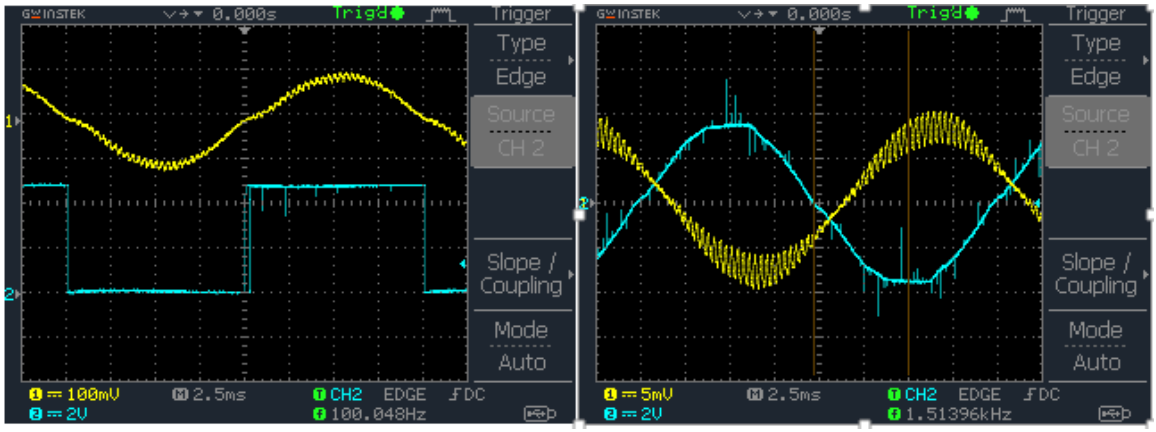


Figure 4-21: Coil current and polarity sensor

b) SVC realization

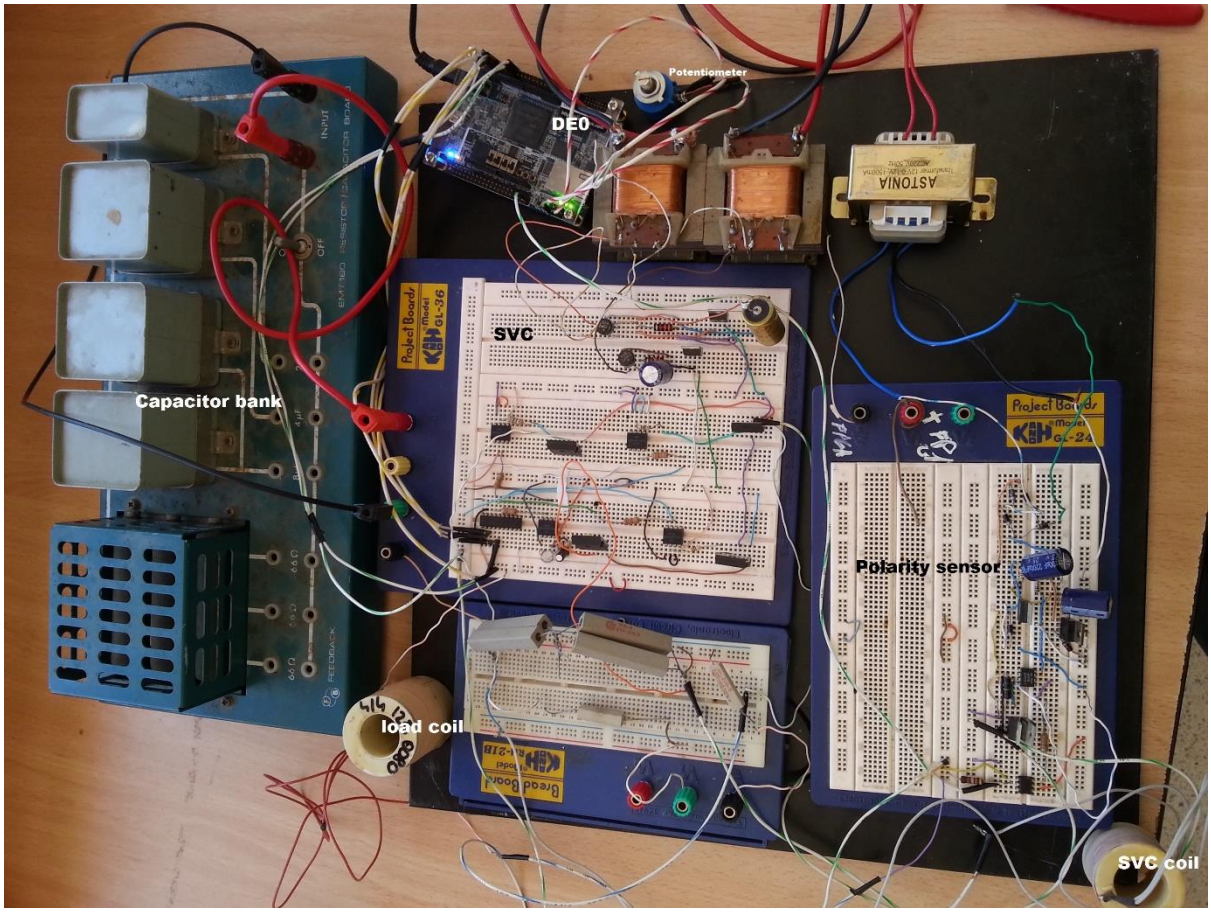


Figure 4-22: The realization circuit of SVC.

Using the previous components to implement this circuit of SVC for one phase in open loop, we check the output of the system many times with different condition, the next figures represents the output of the model.

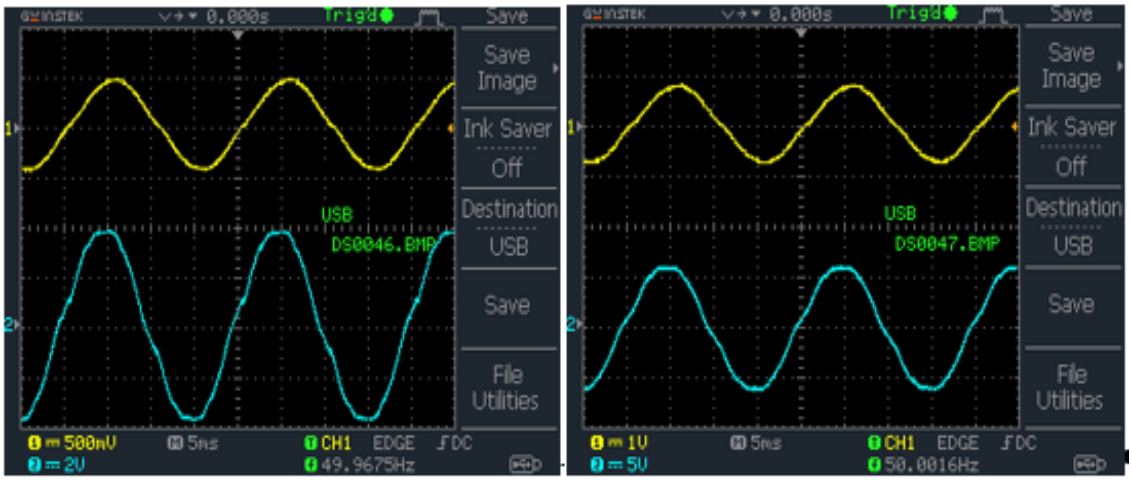


Figure 4-23: Coil voltage and current 100% duty cycle

Figure (4-23) this output of the load without effect of the SVC system. The bleu represents voltage at the coil for 100% and the yellow one is current. The source voltage is about 65 V peak.

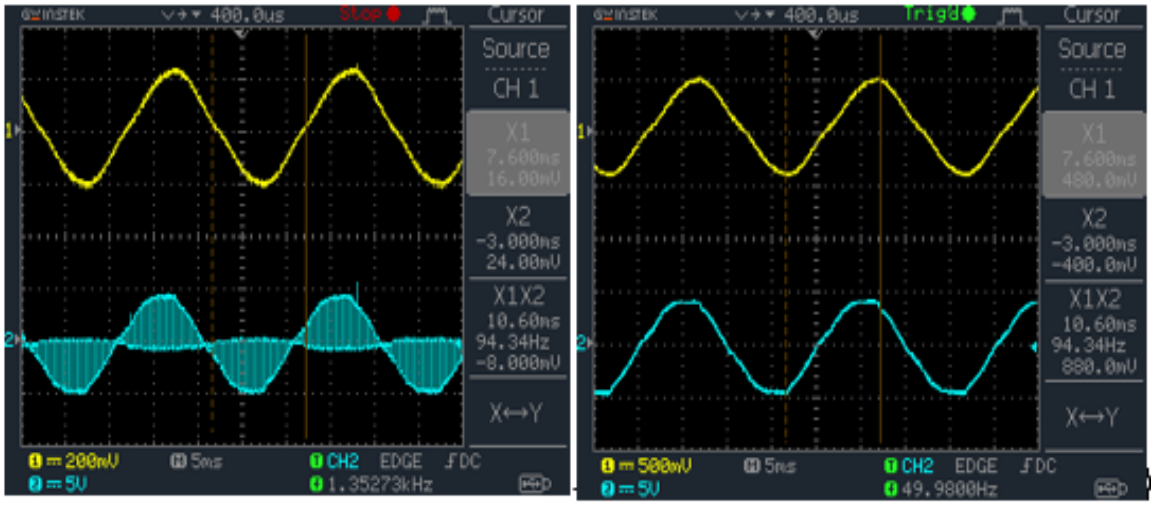


Figure 4-24: The output of the coil 50 %and 100% with SVC effect

The next outputs are displayed with the presence of shunt capacitor with series inductor.

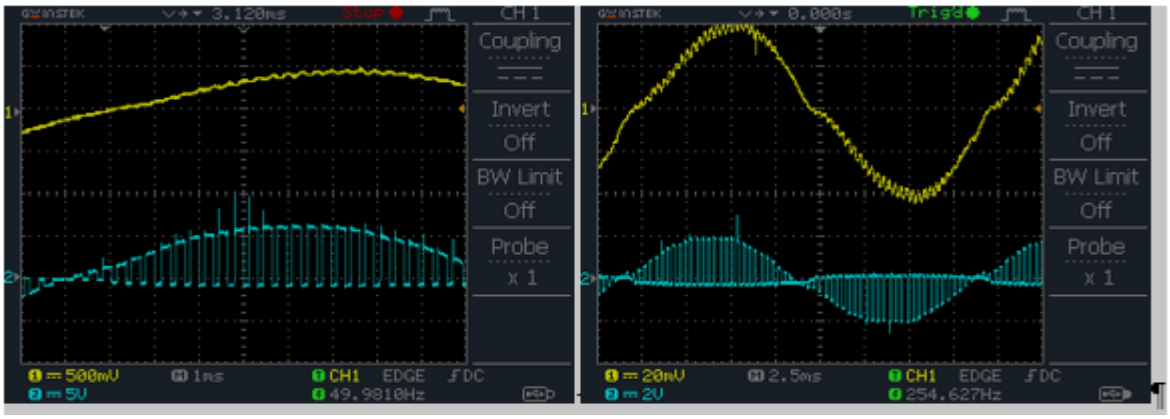


Figure 4-25: Coil current and voltage

Figure. 4-25 shows the load signal after the installation of the coil in series with resistance, ripples on current signal provided by state commutation.

Next step is adding shunt capacitor with inductor to the circuit, output is shown fig. 4-26.

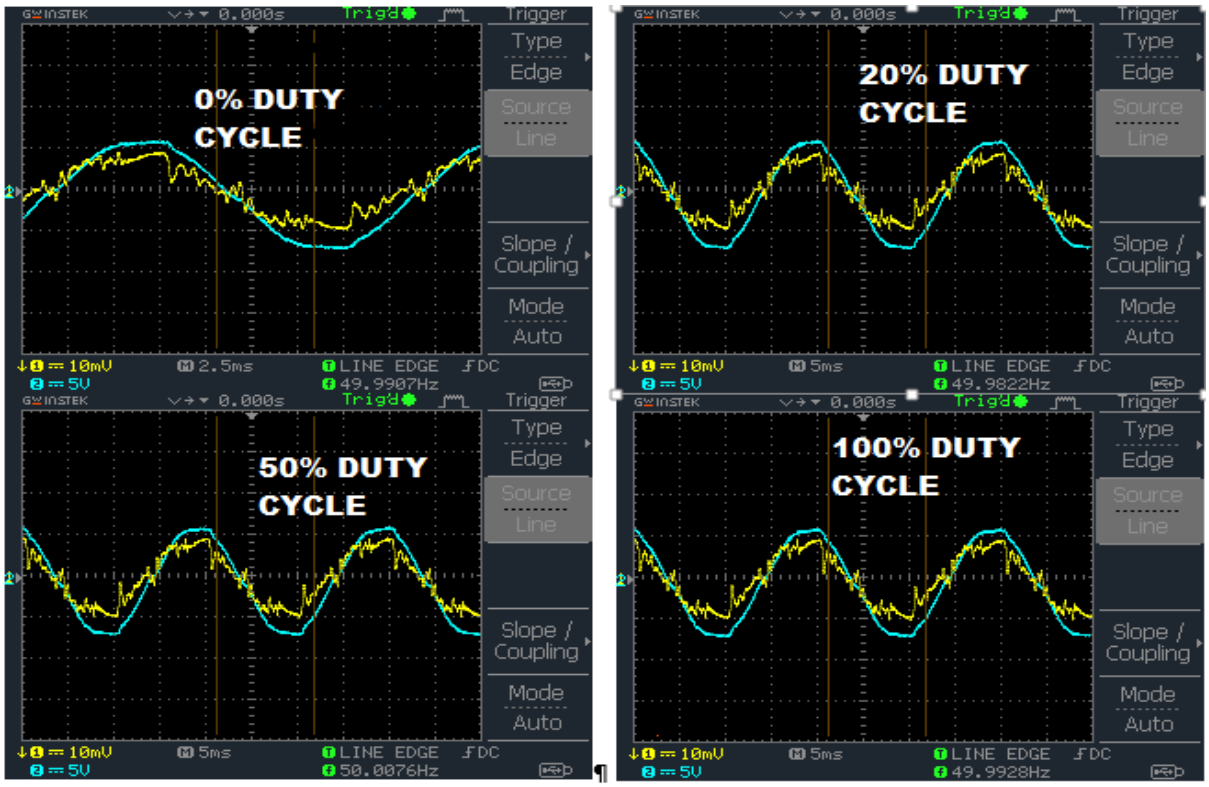


Figure 4-26: Effect of capacitor of 2µF

The changes of phase shift between current and voltage when the duty cycle varies.

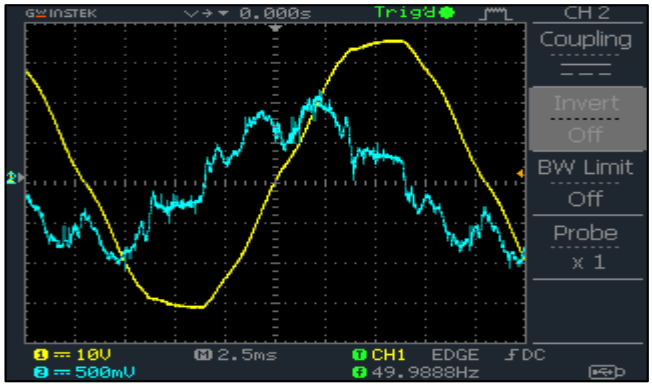


Figure 4-27: Current and voltage source with 8µF capacitor 50% PWM (380 V)

Figure 4-28: The effect of 4µF cap

Varying the duty cycle the current shifts to the left means an absorption of reactive power, and the amplitude of current is greater compared with 2µF from 80 mA to 150 mA.

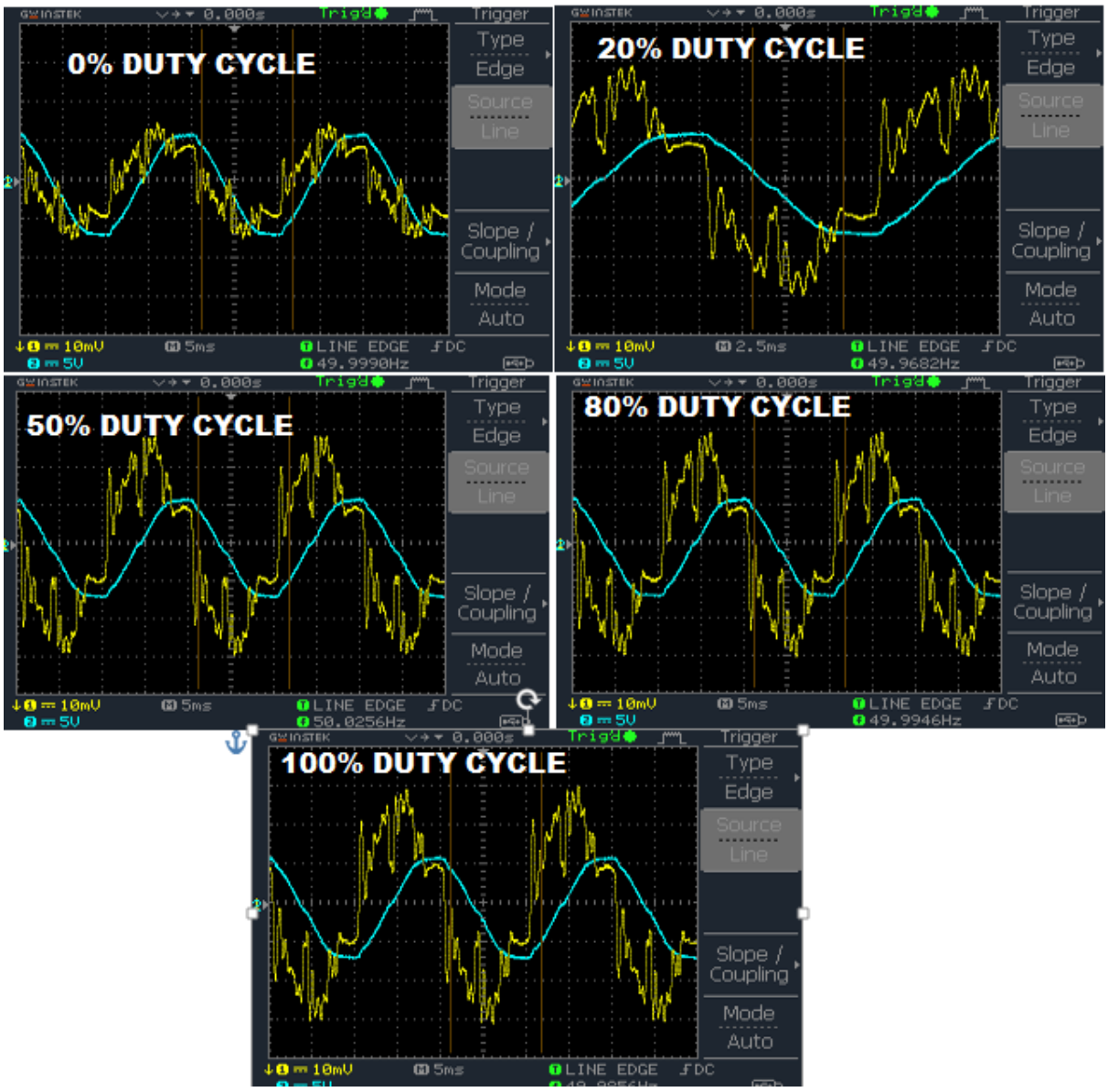


Figure 4-29: 8µF cap

Varying the duty cycle the current shifts to the left means an absorption of reactive power, and the amplitude of current is greater compared with 2 & 4 µF from 80 mA to 300 mA.

4.5 Implementation Discussion

Blue signal in Figures (4-20, 4-23, 4-24, 4-25) shows the output of AC chopper with different duty cycles, the AC chopper chopped the voltage and kept the same amplitude of the source with different duty cycle, the chopped signal is also varying with respect to the duty cycles of the PWM, that allows a control of RMS voltage from 0 to maximum value which is 45 V in our case.

Whereas the yellow signal in figures (4-20, 4-23, 4-24, 4-25) is the inductor current. Also by varying the duty cycle the amplitude of current changes from 0 to 0.5 A for 2 H inductor and 1 H inductive load. Due to the state transitions the coil is connected and disconnected from the source that makes the signal have a form of hysteresis sinusoidal see figures (4-20, 4-23, 4-24, 4-25).

Placing polarity current sensor between collector 02 and the coil allowed as to extract a signal that can be taken to FPGA to have more safe switching as discussed in chapter 03.

When putting a 2µF capacitor figure (4-26) and by varying PWM from 0% to 100 % we can see that the current shift to the left with respect to voltage source but the variation is very small compared with 4µF and 8µF where the variation can be seen on the oscilloscope figures (4-26,4-27,4-28, 4-29).

As the frequency of PWM and size of capacitor increase the variation can be seen clearly. The switching of the AC chopper makes the signal hysteresis and the oldness of the capacitor used makes the signal little noisy.

General Conclusion

The development of compensation methods have allowed to reduce the time to regulate the reactive power in distribution level, without affecting the characteristics in the systems, especially the power quality, which is the goal of developing fast and safe FACTs.

Using the co-simulation has allowed us to have an initial insight of our signals and verified the state transition generated by DE0 board. This is fore the switching operation point of view.

DE0 board generated four signals with adjustable frequency to control IGBTs driven with HCPL opt couplers, which allowed the control of the AC chopper safely with an optical isolation.

With 2 H inductive load, 1 H coil and variable capacitor "2µF to 8 µF" placed on two sides of AC chopper, results shown the successful of the control of the reactive power injected and absorbed as seen on current signal in Co-simulation and implementation. The current amplitude was varying by varying the PWM signal done by changing the ADC input.

Varying PWM makes the impedance of the circuit changes, this entails the shift between current and voltage source varies.

Comparing the simulation and implementation results, one can say that there is some matching. The non-adjusted simple time between MATLAB and Modelsim made the FPGA slower in Simulink which forced us to change the frequency source.

The seizing of coil and capacitor are very important to get better results. As a future work the circuit can be closed by just measuring the voltage, compare it to a reference and plug to the analogue input of FPGA. Also PID can be implemented on FPGA board and the circuit can be extended to three phase system.

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