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MASTER

In **Power Engineering**

Option: **Power Engineering**

Title:

Study and Implementation of Real-Time Testing with Hardware in the Loop for Protection Relays and Power Meters

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Registration Number:………/2020

Abstract

Due to increasing need for power system protection functioning insurance and compliance to system needs for electrical devices protection, and their effect on the power system stability and customer services, protective relays and power meters needs to be tested to ensure compliance of the devices with the power system needs. Real-time simulator-based factory acceptance tests (FAT) are by now a necessary and well-established part of the process of developing and implementing new protection schemes by electric power utilities.

This thesis presents hardware implementation of adaptive protection relay and power meters testing models based on real time simulators. The simulation tool used was Opal-RT OP5600 real time digital simulator. To emulate the actual environment where the test model could be used, a complete phasor network setup is established using actual devices, such as protection relays, power meters and current and voltage amplifier.

A simulation models based on MATLAB/Simulink software were designed to perform real time simulation testing of the protective relays and power meters.

The obtained test results describe the functional states of the tested devices. The results are compared to the standards expected results and limitations.

Dedication

I have a great pleasure to dedicate this modest work

To my Beloved Mother, my Dear Father

To my Dear Brothers, Uncles, Aunts and Cousins

To all my Friends

And to all with whom I spent wonderful moments

Yazid BENTAYEB

Acknowledgement

In the name of Allah, the Most Gracious and the Most Merciful Alhamdulillah, all praises to Allah for the strengths and His blessing in completing this project.

I would like to express my deepest and sincere gratitude to my project Supervisor Dr. Mohammed BOUCHAHDANE. It was a great privilege and honor to work and study under your supervision. Thank you very much.

Last but not least, I am infinitely grateful to my family members, particularly my parents for their patience, unwavering support, continuous encouragement, and belief in me throughout my whole life. I would have never made it this far without them beside me in every step of the way.

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List of Abbreviations & Acronyms

ANSI, American National Standards Institute.

FPGA, Field Programmable Gate Arrays.

HIL, Hardware-In-the-Loop.

HMI, Human Machine Interface.

IEC, International Electrical Commission.

I/O, Input and Output.

LDP, Load Power.

RT-LAB, Real Time Laboratory.

SEL, Schweitzer Engineering Laboratories.

TDS, Time Dial Settings.

TOC, Time Overcurrent.

U.S, United States.

XHP, eXtreme High Performance.

General introduction

Electric system utilities push power systems to operate close to their limits due to the rapid expansion of the power system and to meet the increased consumers demand and with the economic and environmental restrictions. Consequently, system wide disturbances that may lead to outages and blackouts become more likely. At the same time, nature accidents or human-errors causes, such as lightnings, wind damage, ice loading, falling trees, vehicle and bird accidents, human errors, digging into underground cable and many others can initiate system imbalance and lead to disturbances that may lead to system blackouts. Thus, the utilities demand higher reliability and security of the electric service to preserve a stable and secure electric power system. Although it may not be possible to completely prevent the system blackouts due to economical and technological restrictions. It is possible to limit their frequency and intensity with the aid of system control and protection strategies, by developing and testing power system schemes. Today, the major challenging task for an electrical engineer is ensuring a high level of continuity of service to customers even under system disturbance.

The power system protection schemes use protection relays to ensure the protection of the power grids and system equipment's. The protection relays are electrical device that are designed to respond to input conditions in a prescribed manner and, after specified conditions are met, to cause contact operation to trip circuit breaker and isolate fault part of the power system. Hence, ensuring full functionality of the protective relays leads to ensure healthy power transmission and distribution.

The electric system utilities are companies in the electric power industry (often a public utility) that engages in electricity generation and distribution of electricity for sale generally in a regulated market. These companies need to compute the delivered power to the customer for the sale purpose. The power and quality revenue meters are used to perform system's power flow computations. Besides to the Protective relays, meters must be tested to ensure compliance of the device to be used.

This report is divided into four chapters:

- **Chapter 1:** introduces software and hardware used for testing Protective relays and power meters with real time simulators.

- **Chapter 2:** presents theory for the experiment of testing protective relays and power meters using Opal-RT OP5600 real time simulator.

- **Chapter 3:** presents the experimental procedures followed for real time simulation test with hardware in the loop method.

- **Chapter 4:** presents conclusion and Future work.

Chapter 1: Real Time Simulation Software and Hardware

1.1 Introduction:

This chapter introduces the software and hardware used for realising this master thesis. Opal RT-LAB simulator platforms uses MALAB Simulink based models for simulation. Opal RT Technologies integrates RT-Lab software with MATLAB Simulink so that it you can access to Simulink through RT-LAB software. Opal RT simulator platform outputs are used for low-level interface, for tests with high voltage we use amplifiers. F6 Multiple Amplifier Configurator is used to configure F6350 Doble amplifier. Configuration of SEL relays and meters are done through AcSELerator QuickSet software.

1.2 Software:

1.1.1 MATLAB Simulink®:

Simulink is a MATLAB-based graphical programming environment for modelling, simulating and analysing multidomain dynamical systems. Its primary interface is a graphical block diagramming tool and a customizable set of block libraries. It offers tight integration with the rest of the MATLAB environment and can either drive MATLAB or be scripted from it. Simulink is widely used in automatic control and digital signal processing for multidomain simulation and model-based design. In this project Simulink is used for building and simulating the experimental circuit.

1.2.2 RT-LAB®:

RT-LAB is OPAL-RT's real-time simulation software combining performance and enhanced user experience. Fully integrated with MATLAB/Simulink®, RT-LAB offers the most complex model-based design for interaction with real-world environments. It provides the flexibility and scalability to achieve the most complex real-time simulation applications in the automotive, aerospace, power electronics, and power systems industries. RT-LAB handles everything, including code generation, with an easy-to-use interface. With just a few clicks of the mouse, a Simulink® model becomes an interactive real-time simulation application.

RT-LAB's acquisition system acts like a virtual oscilloscope, by allowing the user to visualize waveforms in real-time without glitches and data loss. It can run continuously or based on user-configured triggers to capture specific events. Its core engine provides the accuracy and the bandwidth for the most demanding real-time applications with hundreds of channels and microsecond precision. With the possibility of recording thousands of measurement points, RT-LAB provides users with a complete data history. The format is compatible with other simulation and post-processing software. These advanced acquisition features are done without disturbing the real-time simulation and by keeping a maximal availability for executing the user’s model.

1.2.3 AcSELerator QuickSet® [12]:

AcSELerator QuickSet® SEL-5030 Software is a tool for engineers and technicians to quickly and easily design, deploy, and manage devices for power system protection, control, metering, and monitoring. Through use of this software, you can perform the following:

- ➤ Configure settings for supported devices. For most SEL devices, QuickSet has smart drivers that automatically verify if settings are within an acceptable range. A legacy grid editor driver supports legacy devices.
- ➤ Organize devices in the QuickSet Device Manager. The Device Manager plugin provides a straightforward way to organize devices and to associate connection parameters, documents, device settings, and device parameters.
- ➤ Create and implement Design Templates. The optional Design Templates allow for consistent setup and reduced configuration time. Lock settings so they match your standards, or lock and hide unused settings to reduce entry error.
- ➤ View operational status or device history at your convenience. The customizable human-machine interface (HMI) displays pertinent device data locally or remotely so that verifying and analysing device performance becomes easier.

With the AcSELerator QuickSet Human-Machine Interface (HMI) you are able to obtain pertinent device data locally or remotely with the customizable HMI. Automatic live updates provide fast visual information and eliminate the need to rely on command line inputs. View operational status or history at your convenience, and make adjustments as needed. Verify and analyse device performance with a graphical representation of digital and analog information. HMI interfaces are specific to each device.

1.2.4 AcSELerator Analytic Assistant & SEL SynchroWAVe Event:

AcSELerator Analytic Assistant and SEL-5601-2 synchroWAVe Event Software helps engineers to diagnose a protective relay’s behaviour during a power system fault. It is a powerful yet easy-to-use solution for displaying and analysing SEL relay event reports from SEL devices and COMTRADE files.

The SEL-5601-2 SYNCHROWAVE® Event Software provides the following components and capabilities:

Basic and advanced:

- ➤ Analog and digital charts.
- ➤ Harmonic and spectral analysis.
- ➤ Phasor value derivation and display.
- ➤ Automatic calculation of symmetrical components.
- ➤ Reconfigurable display.
- ➤ ACB or ABC phase rotation support.
- ➤ Searchable signal lists and relay settings.
- ➤ View COMTRADE and SEL ASCII format event reports.

1.2.5 F6 Multiple Amplifier Configurator v5.0.0:

F6 Multiple Amplifier Configurator is a software for configuring and controlling several F6 amplifiers (F6350/e and F6300/e). The software is hosted on one computer and can control/configure up to 16 amplifiers. Configuration of amplifiers is required to enable correct amplification of the low-level signals that are provided by a host simulator. The amplified signal must be of the correct magnitude, based on conversion factors that are selected as part of the configuration process. The configuration software configures both the AC analog outputs of the amplifiers and also the battery output of the F6350s. This software can run on both Windows 7 and Windows XP operating systems.

1.2.6 TeamViewer:

TeamViewer is a comprehensive, remote access, remote control and remote support solution that works with almost every desktop and mobile platform, including Windows, macOS, Android, and iOS. TeamViewer lets you remote into computers or mobile devices located anywhere in the world and use them as though you were there.

1.3 Hardware:

1.3.1 Opal-RT real time simulators [3]:

1.3.1.1 Overview:

OPAL-RT TECHNOLOGIES is the leading developer of open Real-Time Digital Simulators and Hardware-In-the-Loop testing equipment for electrical, electro-mechanical and power electronic systems. OPAL-RT Simulators are used by engineers and researchers at leading manufacturers, utilities, universities and research centres around the world.

OPAL-RT offers a wide range of simulator platforms as shown in table **Table.1.1** to meet all current industry needs and forthcoming challenges. All simulators are based on a modular and flexible design, and are fully customizable and expandable for specific I/O requirements.

Table.1.1: Simulator Platforms Comparison.

Simulator platform	**OP4200**	**OP4510**	**OP5600**	**OP5707**	**OP5031**
Compatible Simulation Systems and Software	RT-LAB eFPGASIM	RT-LAB HYPERSIM eMEGASIM ePHASORSIM eFPGASIM	RT-LAB HYPERSIM eMEGASIM ePHASORSIM eFPGASIM	RT-LAB HYPERSIM eMEGASIM ePHASORSIM eFPGASIM	RT-LAB HYPERSIM eMEGASIM ePHASORSIM
CPU	ARM	INTEL XEON E3	INTEL XEON E5	INTEL XEON E5	INTEL XEON E5
Number of cores	2	4	4,8,16 or 32	4,8,16 or 32	4,8,16 or 32
XILINX FPGA (standard configuration)	ZYNQ (7030)	Kintex 7 (325T)	Spartan 3	Virtex 7 (485T)	n/a
SFP optical interface (GTX 5 Gbits/s)	2	4	0	16	n/a
I/O modules with 16 analog or 32 digital signals	4	4	8	8	n/a
Maximum number of I/O channels	128	128	256	256	n/a

1.3.1.2 OP5600 simulator platform:

The OP5600 real-time simulator is the most adopted simulation platform by OPAL-RT's users in industry and academia. OP5600 combines the performance, versatility and reliability that is ideal for demanding hardware-in-the-loop applications. Whether working within the power systems, aerospace, automotive, oil and gas or other electro-mechanical industries, the OP5600 has the power to simulate systems, while offering all the I/Os required to get your hardware into the loop.

It has two primary sections: an upper section containing analog and digital I/O signal modules, and a bottom section containing the multi-core processor computer and FPGA capable of running the entire OPAL-RT suite of real-time simulation software.

The OP5600 can be configured with up to 32 Intel Xeon E5 processing cores, and comes with a custom-designed Linux operating system, providing the best real-time performance on the market. The OP5600 also provides the option of user-programmable I/O management, handled by a fast Xilinx® Artix®-7 FPGA.

In general, the simulator (target simulator) is connected to a computer (host computer) as illustrated in **Figure 1.1** via ethernet cable with TCP/IP communication protocol. the host computer is supposed to send and control the model, display the graphical results, and receive or read the stored simulation results files in the simulator and some other functions. While the target simulator is supposed to load, build and run the model, during simulation the simulator can store the data without affecting the simulation operation's results and at the end it sends the file to the host computer.

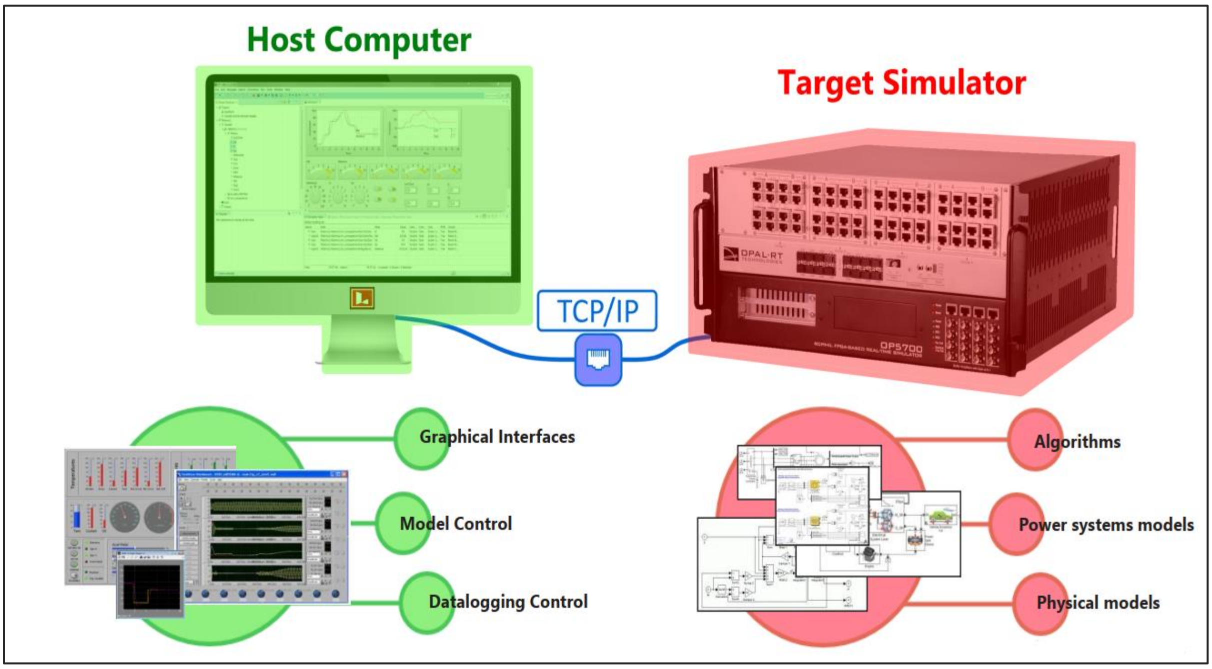

Figure 1.1: Target Simulator to host computer connection.

1.3.1.3 Hardware architecture and components:

i) OP5600 exploded view:

the OP5600 contains five main parts: I/O board, carrier board, FPGA, top section and bottom section as illustrated in **Figure 1.2.**

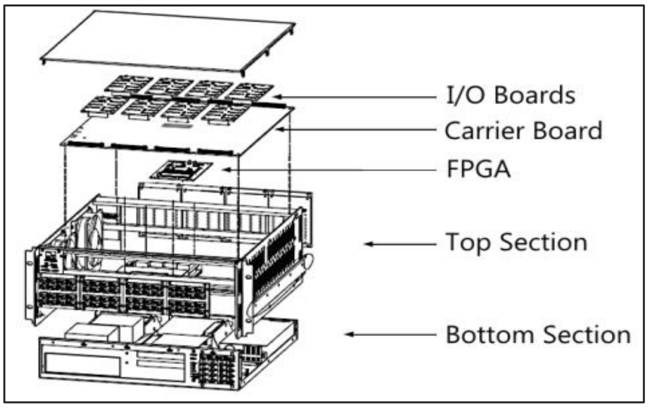

Figure 1.2: OP5600 simulator exploded view.

ii) Spartan-3 FPGA (Field-Programmable Gate Array):

- Can connect with up to 8 swappable OPAL-RT I/O boards (Digital or Analog I/O).
- Highly flexible: Many different IO combinations possible.
- Large Capacity: Up to 256 I/O connections available.
- Sampling time: 100 MHz.

iii) Target Computer – x86 Architecture Platform:

The OP5600 simulator also named the target computer. Its different parts located at the bottom section are shown in **Figure 1.3**.

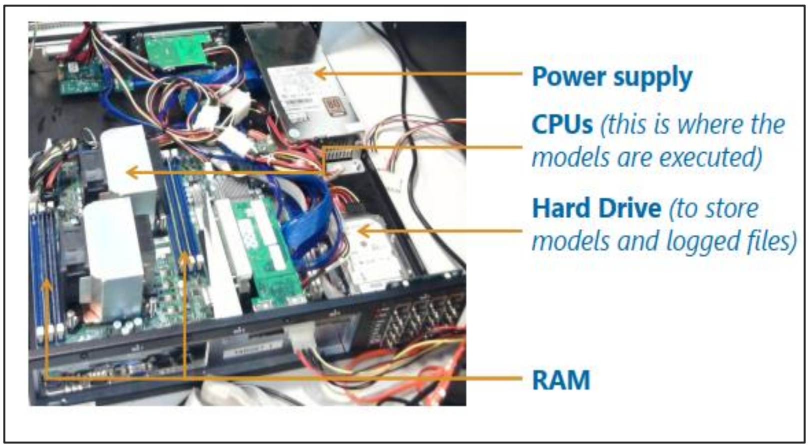

Figure 1.3: Target computer components.

iv) I/O Modules:

(1) Analog Connection Layout:

16 channels per mezzanine card:

▪ OP5330: 16 analog outputs.

▪ OP5340: 16 analog inputs.

Analog outputs:

▪ 16 single-ended channels

▪ Resolution 16 bits

▪ Voltage range +/- 16 V

▪ Conversion time: 1 µs

Analog inputs

▪ 16 differential channels

▪ Resolution 16 bits

▪ Voltage range +/- 20 V

▪ Conversion time: 0.5 or 2.5

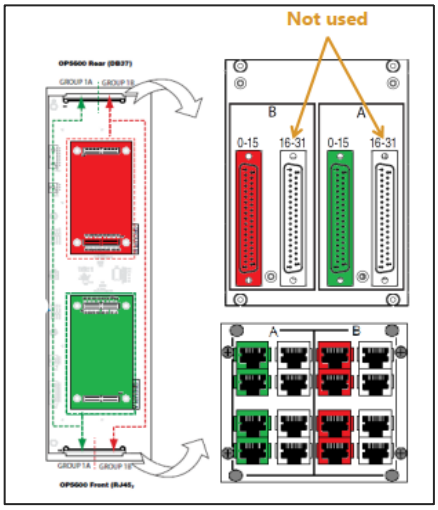

Figure 1.4: OP5600 analog Inputs/outputs cards.

(2) Digital Connection Layout:

32 channels per Mezzanine Card

▪ OP5360: 32 digital outputs.

▪ OP5353: 32 digital inputs.

Digital Outputs:

▪ 32 channels.

▪ Optical isolation.

▪ User-defined output voltage (5 to 30 V).

▪ Max current +/- 50 mA per channel.

Digital Inputs:

▪ 32 channels

▪ Optical isolation

▪ Flexible input voltage (4 to 50 V)

▪ Input current 3.6 mA

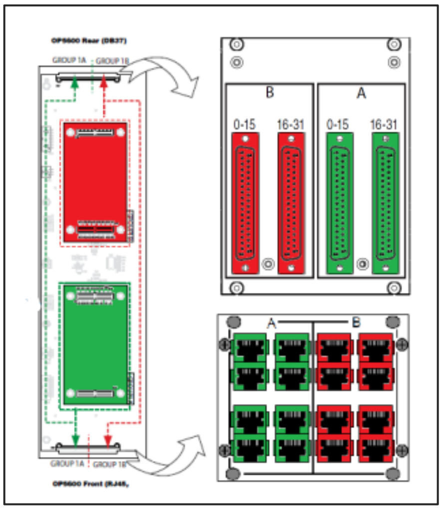

Figure 1.5: OP5600 digital Inputs/outputs cards.

v) Front and back views:

The front and back views are illustrated in **Figure 1.6** and **Figure 1.7** respectively.

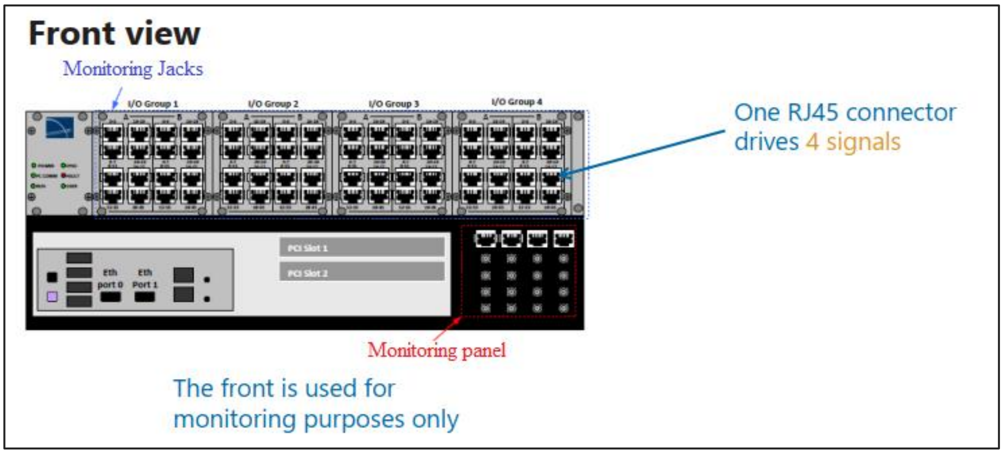

Figure 1.6: OP5600 front view.

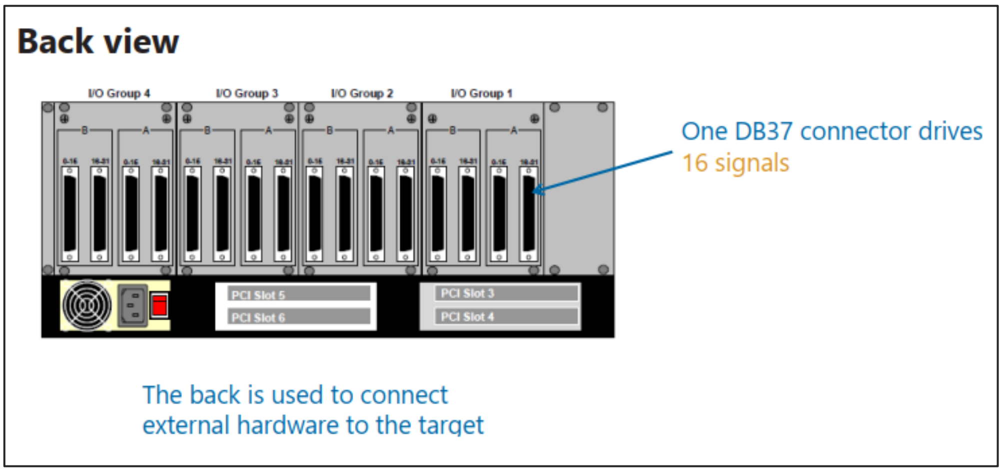

Figure 1.7: OP5600 back view.

1.3.2 Doble F6350 Current / Voltage Amplifier:

Doble's F6350 shown in **Figure 1.8** is used as current/voltage amplifier as shown above. It receives the low-level signal from the real time simulator and supplies the amplified signals to device under test.

The F6350 is designed to accept a range of low-level signals and the output range is selected to conform linearly to the low-level input signals. A 6.7 V rms low level signal will produce a voltage equal to the high end of voltage range selected for the F6350. For example, if the output range is selected as 75V, 6.7V rms will correspond to 75V. If a range of 150V is selected, the 6.7V rms will generate an output of 150V. The three ranges of voltage outputs are 75V, 150V and 300V.

Similarly, the current channels are designed such that a 3.4V rms low level signal will correspond to the high end of the current range selected for the F6350.

The F6350 supports a transient current output. A low-level signal of 6.8V rms corresponds to a transient current output of 1.5 times the normal current range for 1.5 seconds.

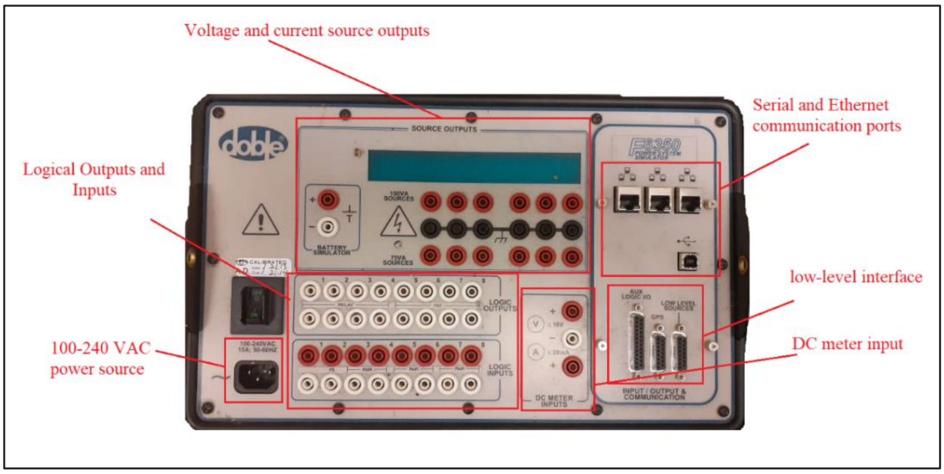

Figure 1.8: Doble F6350 amplifier.

The selection of the ranges and the enabling of the amplifiers are performed via the F6350 software that is installed on the PC. The communication between F6350 and the configuration software is user selectable. This selection is done via the configuration software "F6 Multiple Amplifier Configurator". **Figure 1.9** shows a typical setup using one Doble F6350 Voltage and current amplifier.

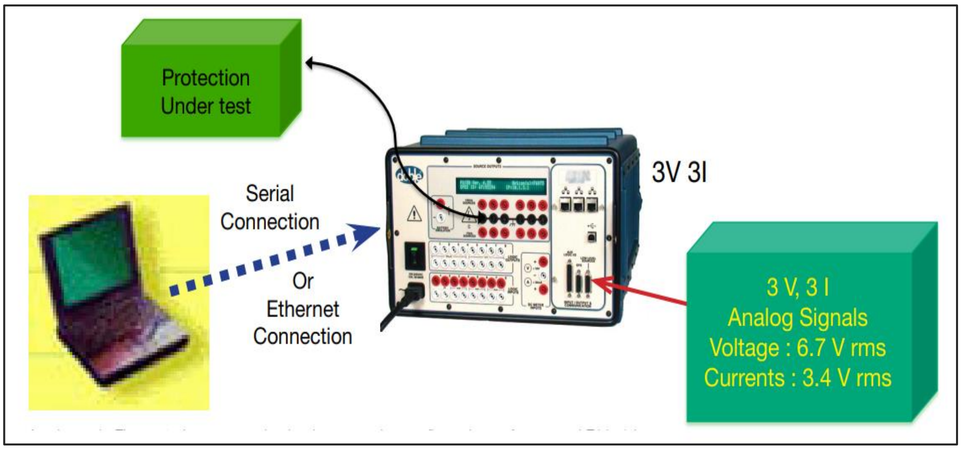

Figure 1.9: Typical test setup utilizing one F6350.

1.3.3 Schweitzer Engineering Laboratories SEL-487E and SEL-411L relays:

i) SEL-487E relay [6]:

The SEL-487E relay shown in **Figure 1.10**, provides a suite of current and voltage elements for the comprehensive protection of power transformers. In total, the relay consists of 24 analog channels, divided into three groups of analog inputs. The first group consists of 15 channels for phase current inputs that are divided into five groups of three-phase inputs. The second group consists of three channels for single-phase (neutral) current inputs, and the third group consists of six channels for two three-phase voltage inputs.

Figure 1.10: SEL-487E relay's front panel.

The SEL-487E contains many protection, automation, and control features. **Table 1.2** presents features and protection functions of the relay.

Table 1.2: Features and protection functions of SEL-487E relay.

ANSI numbers	Function name
16SEC	Access Security (Serial, Ethernet)
24	Volts/Hertz
25	Synchronism Check
27	Undervoltage
32	Directional Power
46	Current Unbalance
49	Thermal
50BF	Breaker Failure Overcurrent
50N	Neutral Overcurrent
50 (P, G, Q)	Overcurrent (Phase, Ground, Neg. Seq.)
51N	Neutral Time-Overcurrent
51 (P, G, Q)	Time-Overcurrent (Phase, Ground, Neg. Seq.)
59	Overvoltage
67 (P, G, Q)	Directional Overcurrent (Phase, Ground, Neg. Seq.)
81 (O, U)	Over- and Underfrequency
85 RIO	SEL MIRRORED BITS® Communications
87 (U, R, Q)	Transformer Differential (Unrestrained, Restrained, Neg. Seq.)
DFR	Event Reports
ENV	SEL-2600
HMI	Operator Interface
LGC	Expanded SELOGIC® Control Equations
MET	High-Accuracy Metering
PMU	Synchrophasors
REF	Restricted Earth Fault
RTU	Remote Terminal Unit
SER	Sequential Events Recorder

ii) SEL-411L relay [5]:

SEL-411L relay shown in **Figure 1.11** is a high-speed transmission line differential, distance, and current protection relay featuring single-pole and three-pole tripping and reclosing with synchronism check, circuit breaker monitoring, circuit breaker failure protection, and series-compensated line protection logic. The relay features extensive metering and data recording including high-resolution data capture and reporting.

Figure 1.11: SEL-411L relay's front panel.

The SEL-411L contains many protection, automation, and control features. **Table 1.3** presents features and protection functions of the relay.

Table 1.3: Features and protection functions of SEL-411L relay.

ANSI numbers	Function name
16SEC	Access Security (Serial, Ethernet)
21	Phase & Ground distance
25	Synchronism Check
27	Undervoltage
49	Thermal
50BF	Breaker Failure Overcurrent
50N	Neutral Overcurrent
50 (P, G, Q)	Overcurrent (Phase, Ground, Neg. Seq.)
51N	Neutral Time-Overcurrent
51 (P, G, Q)	Time-Overcurrent (Phase, Ground, Neg. Seq.)
59	Overvoltage
67 (P, G, Q)	Directional Overcurrent (Phase, Ground, Neg. Seq.)
67	Out-Of-Step trip and/or block
79	Single/Three-pole reclosing
85 RIO	SEL MIRRORED BITS® Communications
87L	Line current differential

DFR	Event Reports
ENV	SEL-2600
HMI	Operator Interface
LGC	Expanded SELOGIC® Control Equations
MET	High-Accuracy Metering
PMU	Synchrophasors
REF	Restricted Earth Fault
RTU	Remote Terminal Unit
SER	Sequential Events Recorder

Schweitzer Engineering laboratories provides relays with a set of communication ports, analogue/digital inputs and outputs and expanded SELOGIC control Equations and graphical functions designs that allows the user to expand relay's functionality and enhance relay's flexibility and reliability.

1.3.4 Schweitzer Engineering Laboratories SEL-735 Power Quality and Revenue Meter [7]:

The SEL-735 Power Quality and Revenue Meter shown in **Figure 1.12** provides high-accuracy revenue metering and power quality metering for electric utilities and industrial applications. The SEL-735 has flexible, user-programmable SELOGIC control equations that include mathematical functions. The metering and control functions are ideal for complete automation applications.

The SEL-735 Power Quality and Revenue Meter Instruction Manual describes common aspects of power quality and revenue meter applications. It includes the necessary information to install, set, test, and operate the meter and more detailed information about settings and commands.

Figure 1.12: SEL-735 Meter front and rear panels.

1.4 Conclusion:

This chapter has dealt with the main software and hardware used for the implementation of this project. These devices are available at the Tennessee’s university laboratory and controlled remotely using TeamViewer software.

In this chapter we presented: MATLAB Simulink, RT-LAB®, AcSELerator QuickSet®, AcSELerator Analytic Assistant & SEL SynchroWAVe Event, F6 Multiple Amplifier Configurator v5.0.0 and TeamViewer, these software are used for the realisation of this project.

In this chapter we presented: OP5600 simulator platform, Doble F6350 Current/Voltage Amplifier, SEL-411L, SEL-487E relays and SEL-735 Meter, these hardware are used for the implementation of this project.

Chapter 2: Real Time Simulation Models For RT-LAB Projects

2.1 Introduction:

This chapter explains the theory for the experiment of testing protective relays and power meters using Opal-RT OP5600 real time simulator and Doble F6350 amplifier. Hardware-In-the-loop method is implemented to interface the hardware directly with the simulation, the calculations and results of the simulation can be injected directly to the connected devices. Another advantage of this method is that in normal testing methods we inject directly a predefined tests values. In reality, the fault currents and voltages differ from these last. For power meters we load all the tests to the model according the ANSII or IEC standards then we run the simulation.

2.2 Creating Simulink models for relay testing:

2.2.1 General relay testing model:

Testing relays with real time digital simulators using Hardware-In-the-Loop (HIL) method gives rise to three main parts to appear in the experiment. The first part is the simulation part where we simulate the power system protected by the relays, which is the part needed to perform the fault analysis to find power system currents and voltages in the different parts of the faulted circuit.

The second part is used to inject the calculated values from the simulation to the relays, in this part we interface relay with simulator via the analog outputs of the simulator. The simulator's analog outputs can inject up to 16V comparing to the normal values in the secondary of voltage transformers it is too small, so either we need to amplify the injected values or; in such cases if available, we use the low-level interface of the relay which is basically the normal input divided by a factor that can be found in the relay's manual.

The third part receives the relay's word-bit which is the decision token by the relay such as trip or a communication signal. These signals are needed to be sent to the simulator in order to trip circuit breakers where needed in the circuit or to communicate with other relays. The simulator uses the digital inputs to read the relay's outputs to open or close circuit breakers or to communicate with other relays by sending the signals via the simulator's digital outputs. In this manner we are implementing HIL method for testing protective relays.

2.2.2 General overview of Opal RT simulator's model [3]:

In general, In RT-LAB platforms, subsystems objectives are to distinguish computation subsystems and graphical user interface (GUI) and Assign computation subsystems to different CPU cores. Opal RT simulator's model consists of two types of subsystems; as shown in **Figure 2.1**, computation and GUI subsystem. A computation subsystem will be executed in real-time on one CPU core of the real-time target, where GUI subsystem will be displayed on the Host PC. The data between the Computation subsystem and GUI subsystem will exchanged asynchronously through the TCP/IP link [3].

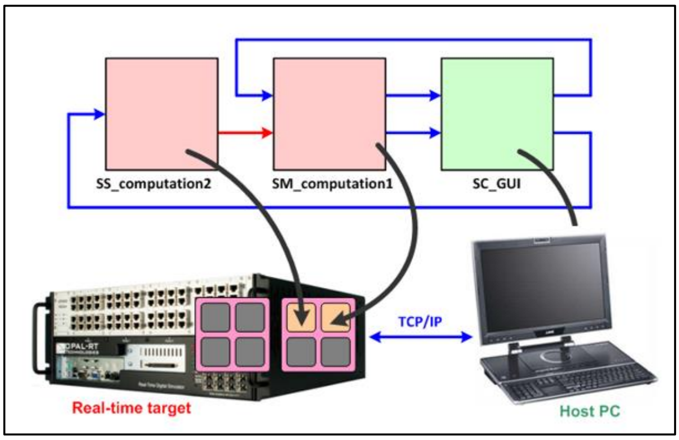

Figure 2.1: Opal RT simulator's model subsystems.

The computation elements of the Simulink Model can be split into different computation subsystems. Each of the computation subsystems will be executed on one CPU core of the real-time target and the data between any two of the computation subsystems is exchanged synchronously onboard the simulator.

Only subsystems are allowed at the top-level of the Simulink model. These ones are assigned to the wright role with a prefix added to the block name separated with an underscore in the form XX_AnyName, the prefix can be either "SC" for GUI subsystem, or "SM" for primary computation subsystem or if only one subsystem is available and "SS" for any additional computation subsystem.

During simulation phase each subsystem will be separated, the communication between subsystems is established with the "OpComm" block, it can be founded in RT-LAB library of the Simulink® library browser, once RT-LAB has been installed. "OpComm" block must be added after creation and naming of the subsystem. All subsystems (SM, SS, SC) inputs must first go through an "OpComm" block before any operations can be done on the signals they are associated with. One "OpComm" block can accept multiple inputs in one subsystem. Double-click on the block to select the number of inputs required.

"Powergui" block is an environment block for Simscape Electrical Specialized Power Systems models allows to choose between one of the different solving methods. "ARTEMIS Guide" also is an environment block from Artemis library they are located on the top-level of the model.

2.2.3 Relay testing model top-level:

In our experiment and as shown **Figure 2.2**, the model consists of two subsystems; the "SM_NETWORK", a computation block contains the power system, analog outputs, digital inputs, and some other blocks needed in simulation. While the "SC_RelayConsole" contains scopes of the signals to be displayed in the host computer during simulation.

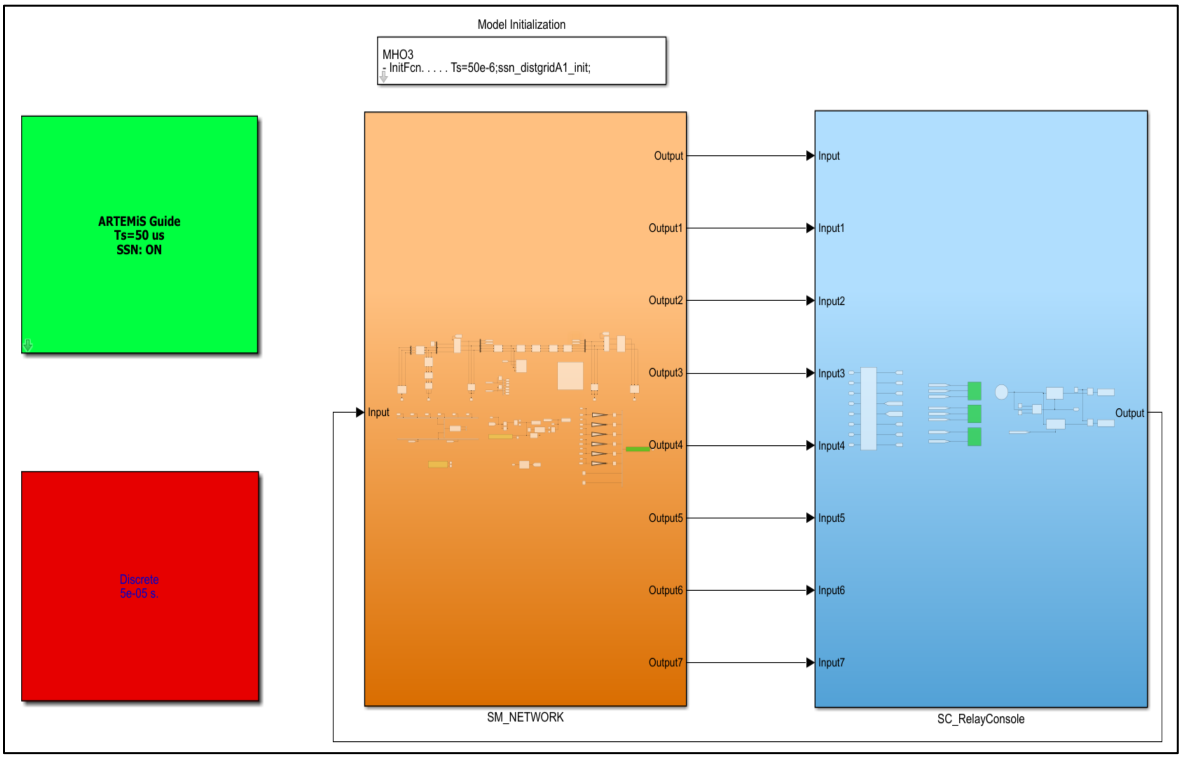

Figure 2.2: Top level view of the relay testing model.

The two blocks on the left of **Figure 2.2** are the "ARETEMIS Guide" and "Powergui" blocks in green and red colours respectively. The white block is the "Model initialization" block, it is linked to a MATLAB code ".m" file in which such constants and parameters are declared.

Each block must be configured to meet the simulations parameters, in the next parts we are going to introduce the configuration needed for the simulation and for the relays testing. Any non-mentioned parameters can be left as default.

i) ARTEMIS Guide and Powergui blocks:

In the “powergui” block, simulation parameters were set with a “Discrete” simulation type , “Tustin/Backward Euler (TBE)” discrete solver type and “ 5e-5” sample time in seconds (in MATLAB “e-5” tends for ten to the power of minus five) or “Ts” if it is declared before in the “Model Initialisation” block, parameters are shown in **Figure 2.3**.

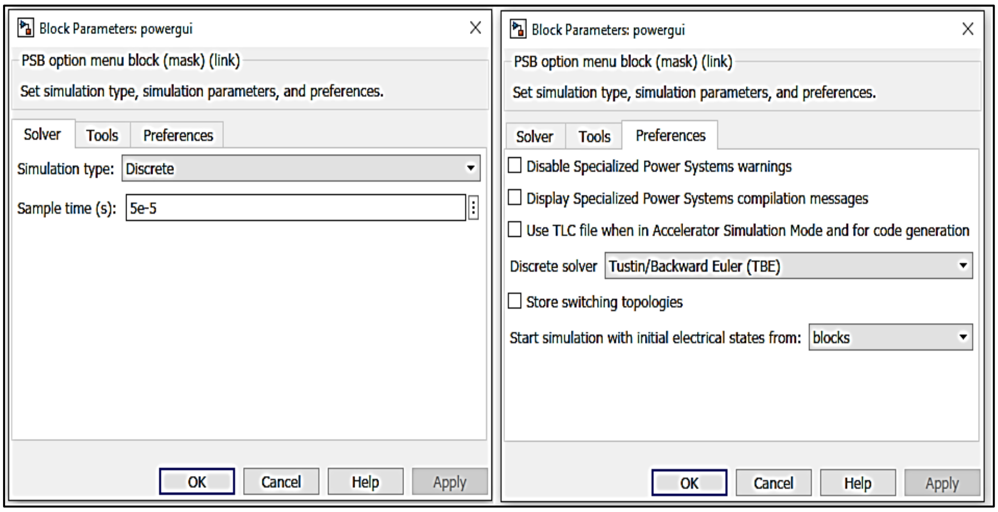

Figure 2.3: “Powergui” block settings.

In the “ARTEMIS Guide” block, the “art5” state-space discretization method was applied and a sample time of “5e-5” seconds. Parameters are shown in **Figure 2.4**.

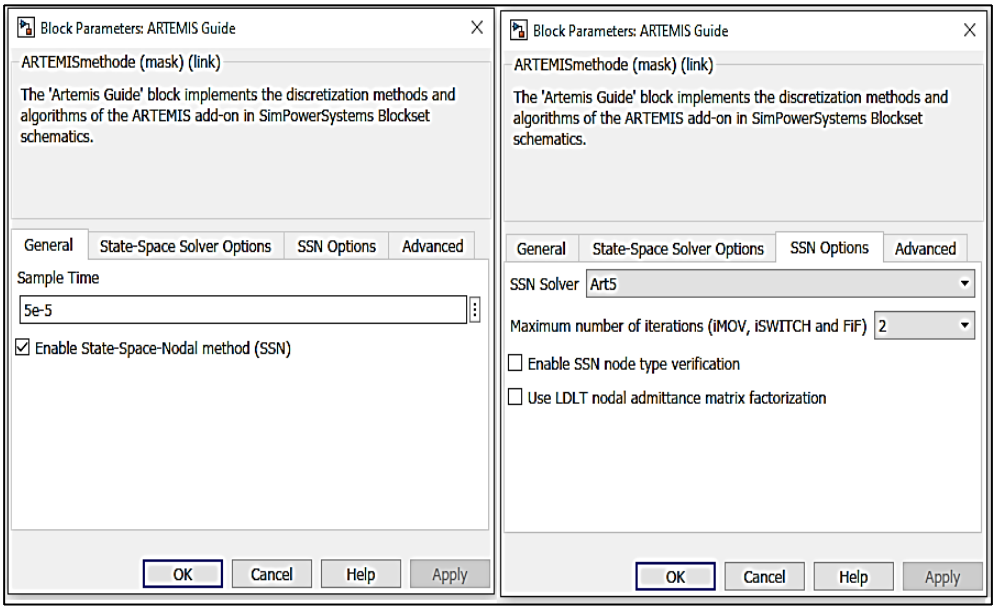

Figure 2.4: “ARTEMIS Guide” block settings.

ii) Model Initialisation block:

In the “Model Initialisation” block we directly declare constants for example “Ts=5e-5”, or we link the block with a “.m” file that contain list of declared constant. The MATLAB code file must be saved in the same location where the models is located and named same as in the “Model Initialisation” block. We should separate each constant or file name with a semicolon. Each time we set a parameter to “Ts” MATLAB assign the value of “5e-5” to that parameter and so on. **Figure 2.5** shows the block parameters used.

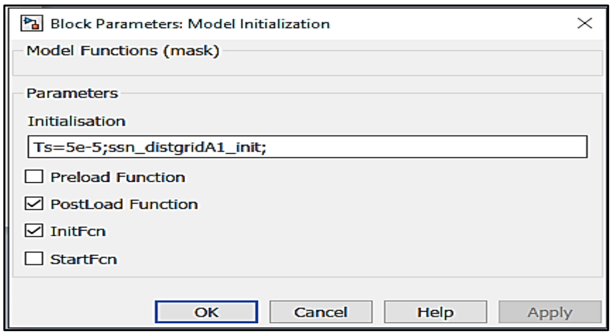

Figure 2.5: “Model Initialisation” block settings.

In this block “Ts” is set to “5e-5” and MATLAB code “.m” file named “ssn_distgridA1_init” is declared. This file is located in the model folder and named the same, it contains a list of constants and circuit parameters as shown in **Figure 2.6.**

```
ssn_distgridA1_init.m

% Source/Generator GENE_0 Parameters Jeu 1
Resis_directe_A_jeu1 = 0.16; %Ohms
Resis_inverse_A_jeu1 = 0.16; %Ohms
Resis_homo_A_jeu1 = 0.16; %Ohms
Induc_directe_A_jeu1 = 19.2e-3; %H
Induc_inverse_A_jeu1 = 19.2e-3; %H
Induc_homo_A_jeu1 = 19.2e-3; %H

% Source/Generator GENE_0 Parameters Jeu 2
Resis_directe_A_jeu23 = 0.16; %Ohms
Resis_inverse_A_jeu23 = 0.16; %Ohms
Resis_homo_A_jeu23 = 0.48; %Ohms
Induc_directe_A_jeu23 = 19.1e-3; %H
Induc_inverse_A_jeu23 = 19.1e-3; %H
Induc_homo_A_jeu23 = 57.3e-3; %H

% Source/Generator GENE_1 Parameters Jeu 1
Resis_directe_B_jeu1 = 1.27; %Ohms
Resis_inverse_B_jeu1 = 1.27; %Ohms
Resis_homo_B_jeu1 = 1.27; %Ohms
Induc_directe_B_jeu1 = 63.5e-3; %H
Induc_inverse_B_jeu1 = 63.5e-3; %H
Induc_homo_B_jeu1 = 63.5e-3; %H

% Source/Generator GENE_1 Parameters Jeu 2
Resis_directe_B_jeu23 = 1.27; %Ohms
Resis_inverse_B_jeu23 = 1.27; %Ohms
Resis_homo_B_jeu23 = 3.84; %Ohms
Induc_directe_B_jeu23 = 63.5e-3; %H
Induc_inverse_B_jeu23 = 63.5e-3; %H
Induc_homo_B_jeu23 = 190.5e-3; %H


freq=60; %Hz
Vnom=225e3; %kV

%Line parameters
%note: with C1_line=C0_line=0.00001e-9 the model becomes unstable
%C1_line= 0.00001e-9; %F/km
%C0_line= 0.00001e-9; %F/km
C1_line=12.74e-9;  %these parameter taken from power_3phseriescomp.mdl SPS
C0_line=7.751e-9;  % hope it's better!
R1_line= 0.01273; %Ohms/km
R0_line=  0.3864; %Ohms/km
L1_line= 0.9337e-3 ; %H/km
L0_line=  4.1264e-3; %H/km


% Load Parameters
R=10000; %Ohms
L=0;     %H
C=0;     %F

% Breaker parameters.  Modeled as perfect breaker
Ron= 0.00001; %Ohms
Rsnub = 1e6; %Ohms
```

Figure 2.6: “ssn_distgridA1_init.m” file settings.

2.2.4 Relay testing model computation subsystem:

The “SM_NETWORK” computation block shown in **Figure 2.7** can be divided into six (6) parts:

- Power system circuit.
- Fault initiation circuit.
- Inputs/outputs card programming circuit.
- Voltages and Currents injection circuit.
- Trip and signals receiving circuit.
- Data acquisition circuit.

i) Power system circuit:

The power system used in this simulation has two generators; one at each end and two loads with a transmission line that connects the substations where generators are located. This power system can be found in the RT-Lab Simulink model library named “ssn_distributiongrid_A1” with the system parameters shown in **Figure 2.6**.

The tested relay is connected at “Bus 2” with distance main protection to protect the transmission line between the two substations and supposed to trip the circuit breaker on the left.

ii) Fault initiation circuit:

The “Three-phase fault” block is used to simulate a fault (short circuit) between any phase and the ground. We can simulate any type of fault by selecting the right block. The switching time is set to “External” as shown in **Figure 2.8**, this allows the block to be triggered externally through an input signal. The fault block is controlled by the “SC_RelayConsole” subsystem, therefore we should use an “OpComm” to establish communication between subsystems during simulation.

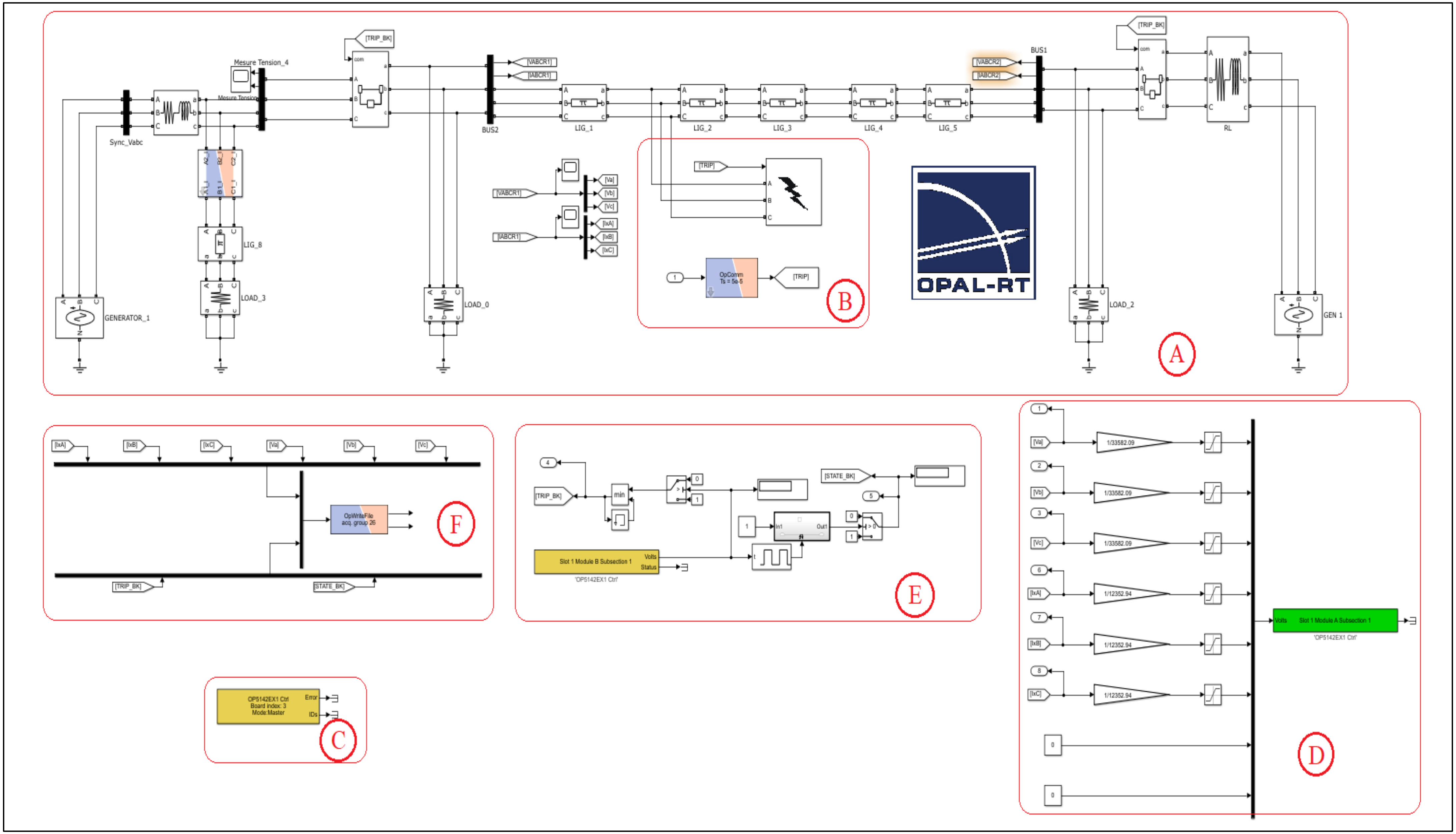

Figure 2.7: "Sm_NETWORK" computation block: A) Power system circuit. B) Fault initiation circuit. C) Inputs/outputs card programming circuit. D) Voltages and Currents injection circuit. E) Trip and signals receiving circuit. F) Data acquisition circuit.

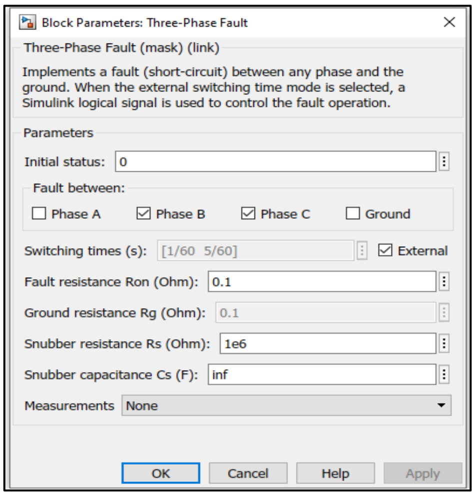

Figure 2.8: "Three-phase fault" block settings for BC fault type.

iii) Inputs/outputs card programming circuit:

The OP5600 simulator has an OP5142 (**Appendix A)** card with 32 analog inputs, 32 analog outputs, 32 digital inputs and 32 digital outputs, this card needs to be programmed in the model. The RT-LAB I/O library contains a set of blocks for each card type, to configure and control the OP5142 card we must add an "OpCtrlOP5142EX1" block. In this block, "OP5142EX1 Ctrl" controller name was selected, later this name will be used to point input output blocks to this controller. The board ID and Bitstream FileName are manufacturer selected and can be found in the simulator files or can be extracted from simulator during build phase if using a wrong setting, the error shown in **Figure 2.9** will appear and the correct settings can be found in the error report.

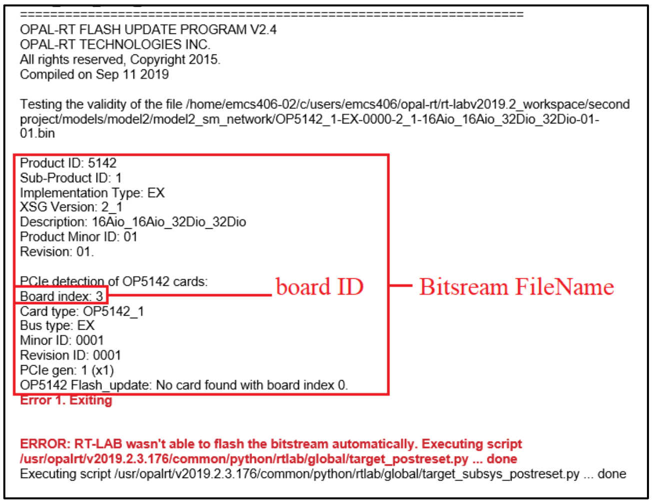

Figure 2.9: Build error report with wrong board ID and Bitstream FileName settings.

The two files in **Figure 2.10** with ".bin" and ".conf" extensions and having the same name are provided with each card by manufacturer. These files must be copied to the location of the model, their name is used as Bitstream FileName in order to program the input and output cards.

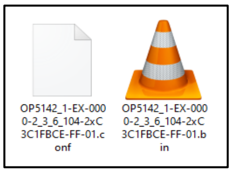

Figure 2.10: ".bin" and ".conf" files.

The ".conf" file contains a table that defines each slot in the simulator's front panel, where its divided into four groups, each one has two sections A and B and each section has two subsections P1 and P2. **Figure 2.11A** shows ".conf" file configurations, settings of the "OpCtrlOP5142EX1" block are shown in **Figure 2.12B**.

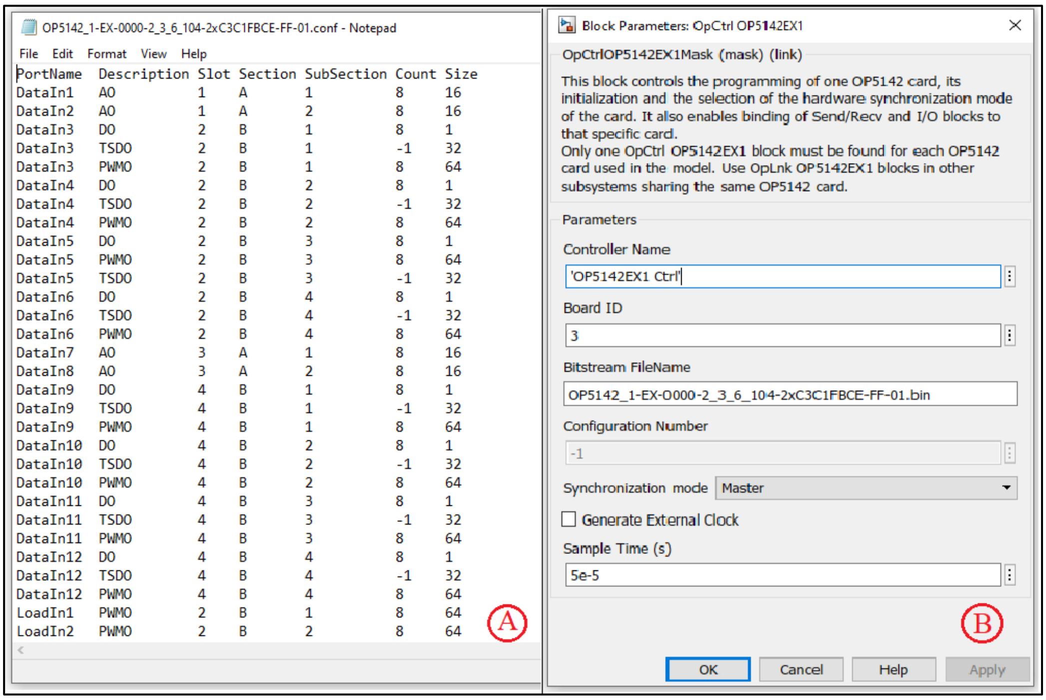

Figure 2.11: A) ".conf" file configurations. B) "OpCtrlOP5142EX1" settings.

iv) Voltages and Currents injection circuit:

Voltages and currents calculated during simulation at "BUS1" are to be injected in the simulator's outputs. The values are too large to be injected from a digital simulator, hence we need to transform each value by a corresponding factor. Since the OP5600 simulator can output +/-16V so we need to map the reading of currents and voltages to this range. Another limitation is that if the amplifier or low-level interface has a nominal value that should be token in consideration, or as in our case the conversion factors of the amplifier are preselected by manufacturer, then the amplifier can be considered as a step-up transformer with a fixed turns ratio. The solution for this problem is by adding a factor (gain) in the model to correct the total conversion factor of the equipment and a saturation block to make sure that the simulator cannot output any larger value than the selected one in this block. **Figure 2.7D** shows different parts of the circuit.

Calculation of the conversion factor takes in consideration the current transformer (CT) or voltage transformer (VT) ratios, amplifier factor and any other factor can be used in the circuit. Let's consider voltage case, Vp is the primary voltage of the system, PTR is the voltage transformer ratio, Vn/Vs is the amplifier ratio where Vn is the nominal input voltage. Hence, the saturation block must limit the voltage to Vn and the conversion factor CF can be calculated using the formula:

$$CF = \frac{Vs}{PTR \times Vn} \qquad \text{Eq.2.1}$$

We use the "OpFcnOP5142EX1AnalogOut" block collected from the "RT-LAB®/ I/O/ Opal-RT => OP5142EX1" library to transmit to one OP5142 card the voltage values to be applied to the analog output channels. We set the controller name to "OP5142EX1 Ctrl" that is the name of the "OpCtrlOP5142EX1" controller and the Number of AOut channels to 8 out of 32 since we need three voltages and three currents, the other two additional outputs can be connected to a constant "0". And any other settings can be left as default. Once you select the analog output block and enter the proper controller name you can notice the slot info is changed from "Slot 0 Module X Subsection 0" to "Slot 1 Module A Subsection 1" if it is the first block, these information are obtained from ".conf" configurations file.

v) Trip and signals receiving circuit:

Once the relay detects a fault the outputs states change either to trip circuit breaker, trigger an alarm, or communicate with other relays. In order to complete the circuit to simulate real case, the simulator must receive the signals through the digital inputs to isolate the faulted part of the system. **Figure 2.7E** describe the tripping circuit of the breaker, an "OpFcnOP5142EX1AnalogIn" block collected from the "RT-LAB®/ I/O/ Opal-RT => OP5142EX1" library is used to return the trip signal to the circuit breaker. We set the controller name to "OP5142EX1 Ctrl" and the number of Ain channels to 1 out of 32 since we have only one circuit breaker and no communication is configured in the relay. Once you select the analog output block and enter the proper controller name you can notice the slot info is changed from "Slot 0 Module X Subsection 0" to "Slot 1 Module B Subsection 1" if it is the first block, these information are obtained from ".conf" configurations file.

vi) Data acquisition circuit:

A great feature the OP5600 simulator can provide is saving any simulation signal during simulation without affecting the results. Opal RT-LAB simulators contain a hard drive to store the signals and results during simulation, and once the simulation ends it will be sent to the host computer in format ".m" MATLAB file.

"OpWriteFile" block collected from RT-LAB library is used to save the input signals where the first row is the simulation time, the second row is the first input and so on.We set the FileName to any name followed by ".mat" extension (Name.mat), also we choose Variable name a that will appear in MATLAB workspace when opening the file. Select the Acquisition group to 26, select "Write in Simulink Mode", and set the file size name to any larger value in bytes according to the data stored and simulation time. **Figure 2.12** shows the configuration of the "OpWriteFile" block.

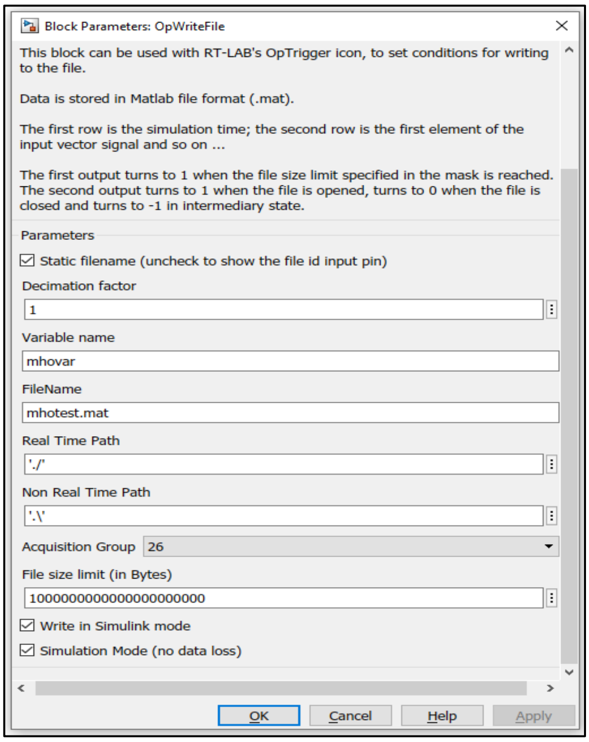

Figure 2.12: "OpWriteFile" block settings.

2.2.5 Relay testing model GUI subsystem:

The “SC_RelayConsole” shown in **Figure 2.13** can be divided into two parts:

- Fault timing control circuit.
- Graphical user interface circuit.

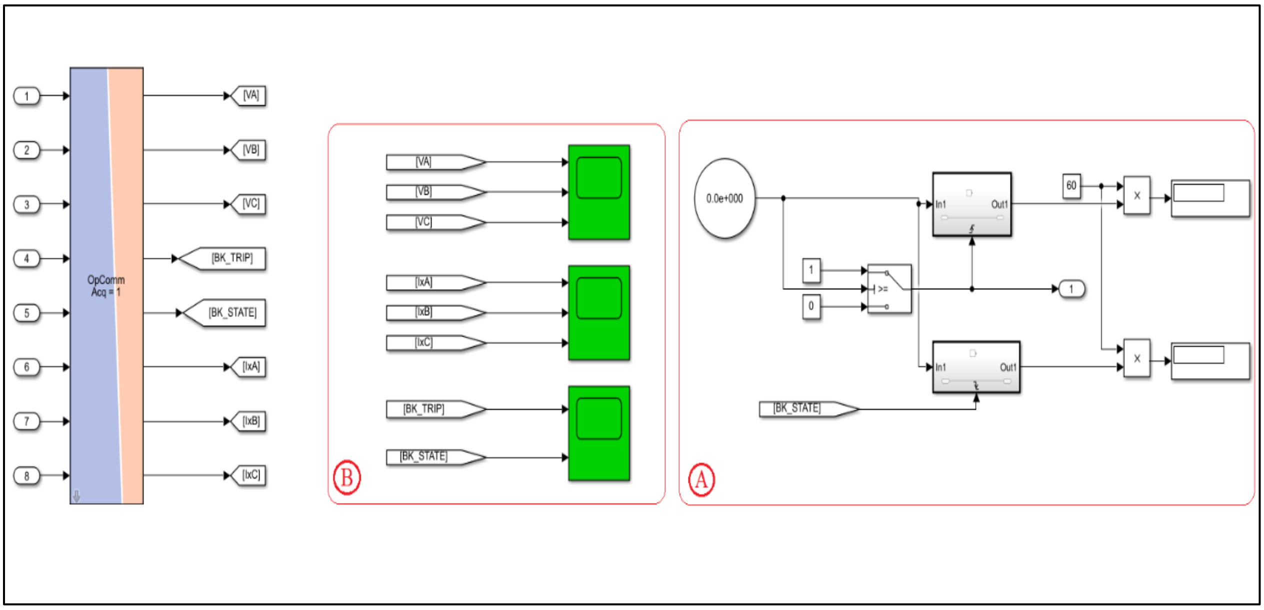

Figure 2.13: A) Fault timing control circuit. B) Graphical user interface circuit.

i) Fault timing control circuit:

Faults can be delayed in order to simulate three states: prefault, fault and postfault states. These three states give a better experiment for testing relays. The two displays show the time in cycle when the fault start and when the breaker state has changed. In this manner we can notice the response time of the relay.

ii) Graphical user interface circuit:

During simulation, simulator displays the “SC_RelayConsole” subsystem on the host computer where you can follow the reading and plots of the different signals during the three states. In this experiment we used scopes to display signals. The “OpComm” block is used to establish communication between the two subsystems.

2.3 Implementing distance Mho function in Simulink model:

2.3.1 Mho distance protection theory:

Distance mho protection function is one of the main protections used for transmission lines power system protection. With its impedance plot-based principle it can be implemented in a model to test relay's functionality with respect to theoretical result. This model can be added to the main model in an additional computation subsystem or it can be run in a separate model.

Distance mho function depends on the calculation of fault currents and voltages to find their respective impedance. The impedance is directly proportional to the length of wire, so according to the fault impedance we can deduce the relative fault location in distance units and this explains where the name comes from. It is used as a main or backup function.

Distance protection schemes are mainly designed to protect power system against two types of faults symmetrical and unsymmetrical faults. These two types can be further divided into Line-to-Ground, Line-to-Line-to-Ground, Line-to-Line and Three-Phase faults.

In general, distance protection schemes have six units of fault detection, three units for detection of faults between any two phases, while the other three units detects faults between any phase and ground. Different equations of fault detection are explained in **Table 2.1**. Settings of distance relay are always calculated on the basis of positive sequence impedance [13].

When a phase to ground fault occurs, the single line voltage at the fault location is zero. it would appear that the voltage at the relaying point is the product of the fault current and impedance, this is only true if earth resistance is zero. However, the fault current depends on the number of earthing points, the method of earthing and sequence impedances of the fault loop. [8][9][10] the voltage drop is the sum of the sequence voltage drops between the relaying point to the fault location. The voltage drop to the fault and current in the fault loop are:

$$VA = I1 \times Z1 + I2 \times Z2 + I0 \times Z0 \qquad \text{Eq.2.2}$$

$$IA = I1 + I2 + I0 \qquad \text{Eq.2.3}$$

$$IN = IA + IB + IC = 3I0 \qquad \text{Eq.2.4}$$

Where 1,2 and 0 are positive, negative and zero sequence components.

By considering Z1=Z2, a constant K where: $K = \frac{Z0}{Z1}$ and replacing in Eq.2.2:

$$VA = Z1\{IA + (IA + IB + IC) \times \frac{K-1}{3}\} = Z1\{IA + I0 \times k\} \qquad \text{Eq.2.5}$$

Where : $k = \frac{K-1}{3}$

The impedance seen by the relay comparing IA and VA is:

$$ZR = \frac{VA}{IA} = \left(1 + \frac{K-1}{3}\right) \times Z1 = (1 + k) \times Z1 \qquad \text{Eq.2.6}$$

From equation Eq.2.6 we can notice that the impedance is incorrect due to factor m. to find real value of fault impedance Zf we need to correct the currents and voltages entering relay, this is known as compensation. The compensated current for phase A is

$$IAcompensated = (IA + kI0) \qquad \text{Eq.2.7}$$

Hence:

$$ZR = \frac{VA}{IA} = Z1 \qquad \text{Eq.2.8}$$

Table 2.1: Fault Impedance Calculation on different fault situations

Faults	**Fault impedance equation**
Phase A – Ground	ZA = VA / (IA + 3 k I0)
Phase B – Ground	ZB = VB / (IB + 3 k I0)
Phase C – Ground	ZC = VC / (IC + 3 k I0)
Phase A – Phase B	ZAB = VAB / (IA – IB)
Phase B – Phase C	ZBC = VBC / (IB – IC)
Phase C – Phase A	ZCA = VCA / (IC – IA)

Where:

VA, VB, VC and IA, IB, IC are phase voltages and currents respectively.

VAB, VBC and VCA are phase to phase voltages.

k is the zero sequence or residual compensation factor.

I0 is zero sequence current.

Mho distance scheme apply a circle on an R-X plane; where R-axis is the resistance axis and the X-axis is for reactance, that passes through the reference point with a reach in percentage of the line positive sequence impedance and polarized with its angle. If the fault impedance plot is inside the circle; also named zone, then the relay asserts a trip signal, otherwise the fault does not belong to that protected zone. Relay applies different zones in cascade and delayed to enhance protection scheme reliability and security. **Figure 2.14** shows mho circle diagram, where ZR is zone reach and Zsc short circuit or fault impedance point location on the R-X plane.

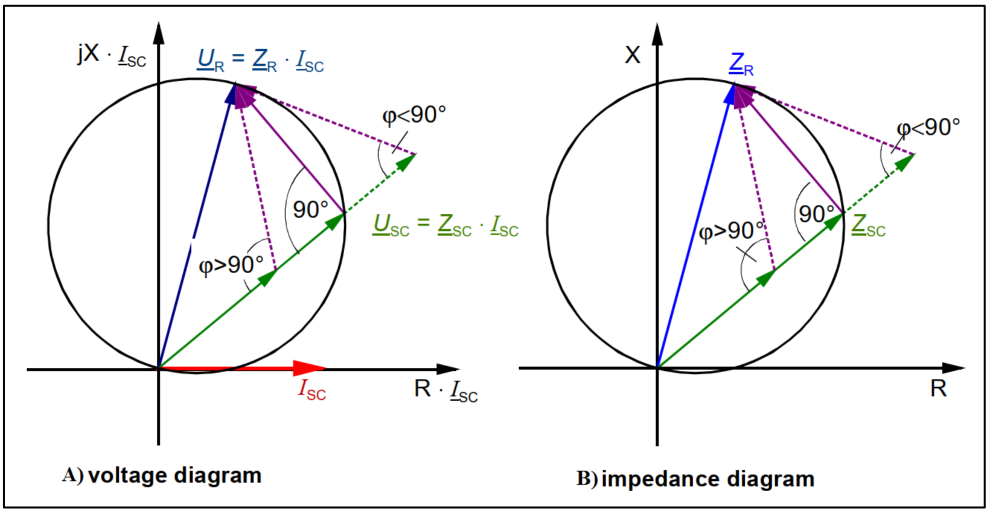

Figure 2.14: A) mho circle voltage diagram. B) mho circle impedance diagram.

It can be shown mathematically that the angle between the vector $\overrightarrow{Zsc}$ and the vector $\overrightarrow{(ZR - Zsc)}$ defines the location of the point Zsc with respect to the Mho circle, where $\overrightarrow{Zsc}$ is defined by point Zsc and the plane reference and $\overrightarrow{ZR}$ is defined by mho zone reach and angle. If $\varphi > 90°$ then point Zsc is inside the circle, if $\varphi < 90°$ then Zsc is outside the circle and if $\varphi = 90°$ then Zsc is on the circle. This logic can be implemented to simulate the mho protection scheme.

2.3.2 Mho model "SC_NETWORK" computation subsystem:

Top-level view of Mho model looks similar to any other RT-LAB model it may differ only in inputs and outputs or number of computation blocks and this is shown in **Figure 2.15**.

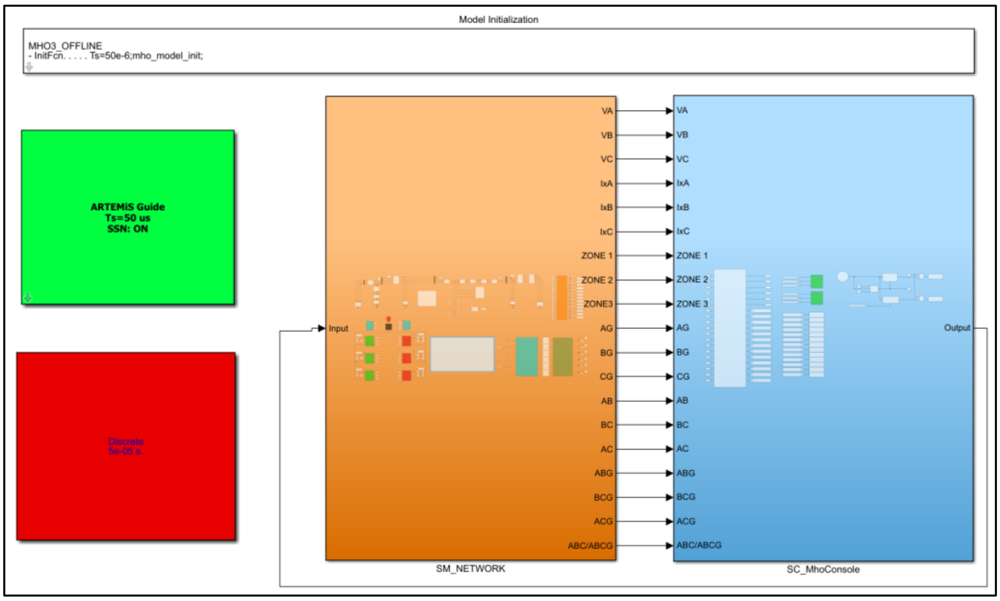

Figure 2.15: Mho model top-level view.

Mho model "SM_NETWORK" computation subsystem shown in **Figure 2.16** applies the theoretical calculations for fault detections and type selection logic. The results are displayed on the "SC_MhoConsole" GUI subsystem during simulation. The computation block can be divided into four (04) parts:

- Power system and fault initiation circuits.
- Harmonics removal and filters circuits.
- Fault detection circuit.
- Fault type and zone selection logic circuit.

i) Power system and fault initiation circuits:

The power system in **Figure 2.16A** is similar to the one used in the previous section for relay testing. This power system can be found in the RT-Lab Simulink model library named "ssn_distributiongrid_A1" with the system parameters shown in **Figure 2.6**.

While the fault initiation is controlled by the "SC_MhoConsole" subsystem and the fault type is select by "Three-phase fault" block.

ii) Harmonics removal and filters circuit:

When a fault occurs on a transmission line, currents and voltages are severely distorted due DC decaying components, presence of transient higher order frequencies. So, signals must be filtered to deal with fundamental frequency without affecting it. The filtering block is divided into three parts, Low pass filter, fundamental frequency extractor, and DC component remover.

Higher frequency components can be eliminated using low pass filters, with appropriate cut-off frequency. In this experiment a low pass FIR filter is used with settings shown in **Figure 2.17**. the low pass filter response is shown in **Figure 2.18.**

After removal of higher order frequency, we need to extract the fundamental frequency from the lower order frequencies in the distorted signals. One of the best methods for extracting the fundamental frequency is using Fourier analysis. The "Fourier analysis" block can be found in Simulink library. We set the fundamental frequency to 60 Hz, harmonic numbers to 1, since the fundamental frequency is the only needed frequency and the sample time is set to the simulation sample time for discrete-time Fourier analysis. The settings are shown in **Figure 2.19**.

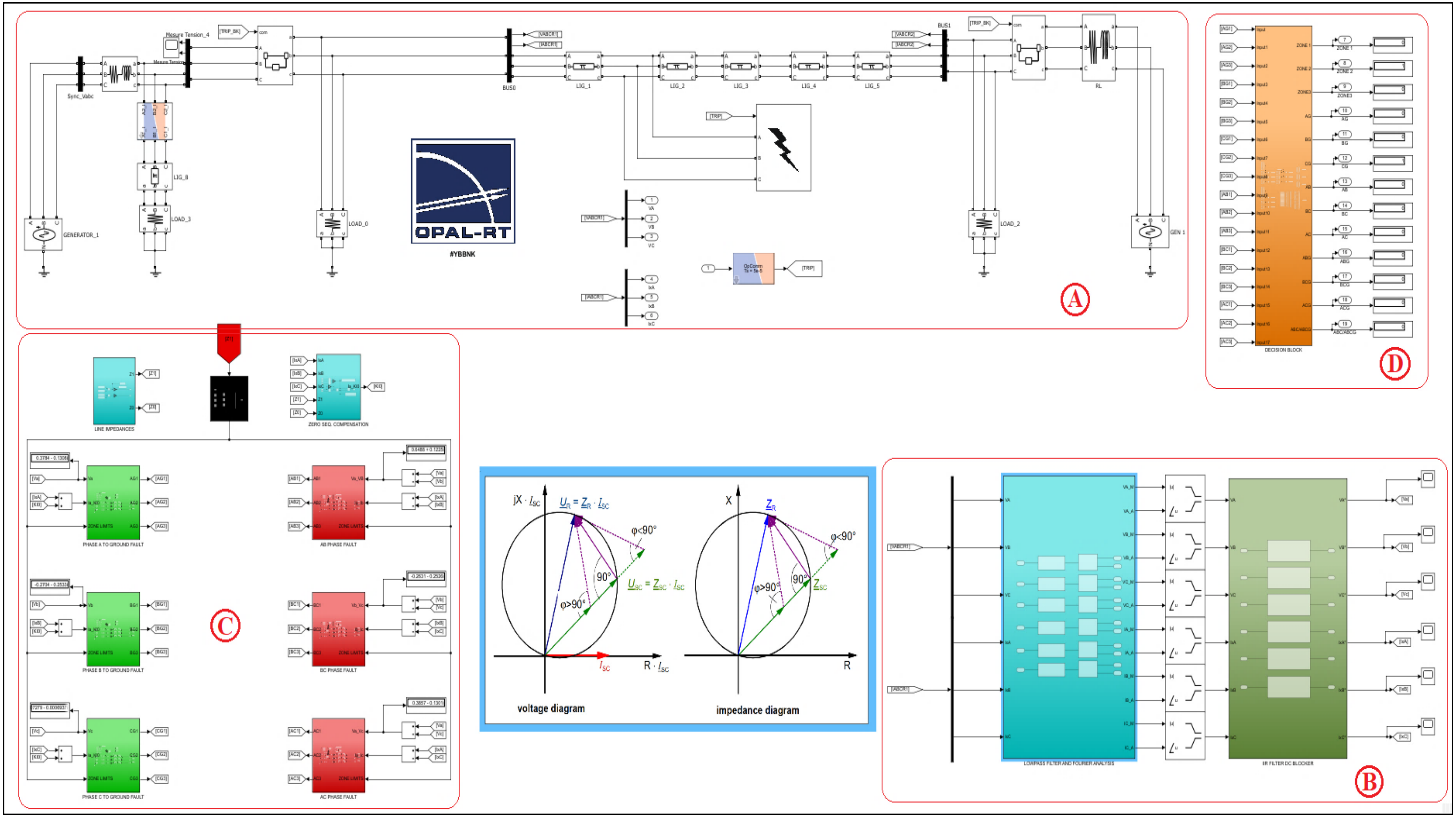

Figure 2.16: A) Power system and fault initiation circuits. B) Harmonics removal and filters circuits. C) Fault detection circuit. D) Fault type selection logic circuit.

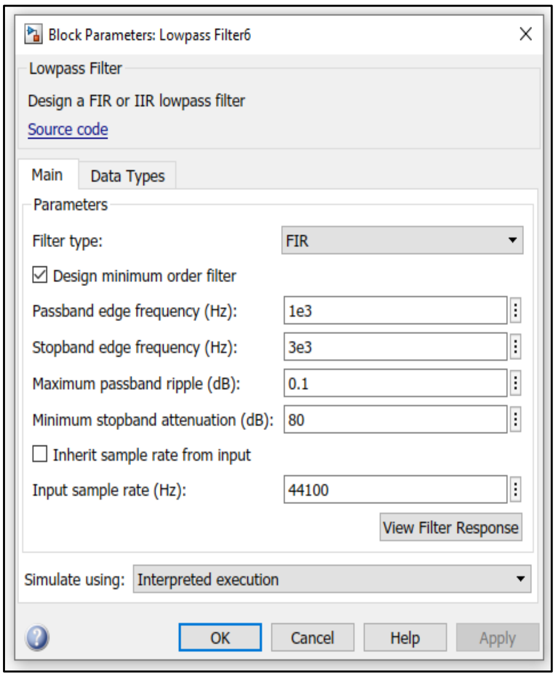

Figure 2.17: low pass filter settings.

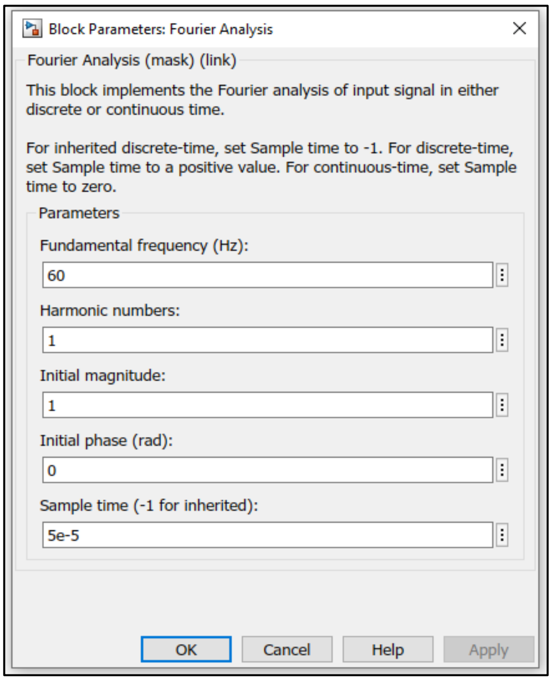

Figure 2.19: Fourier analysis block settings.

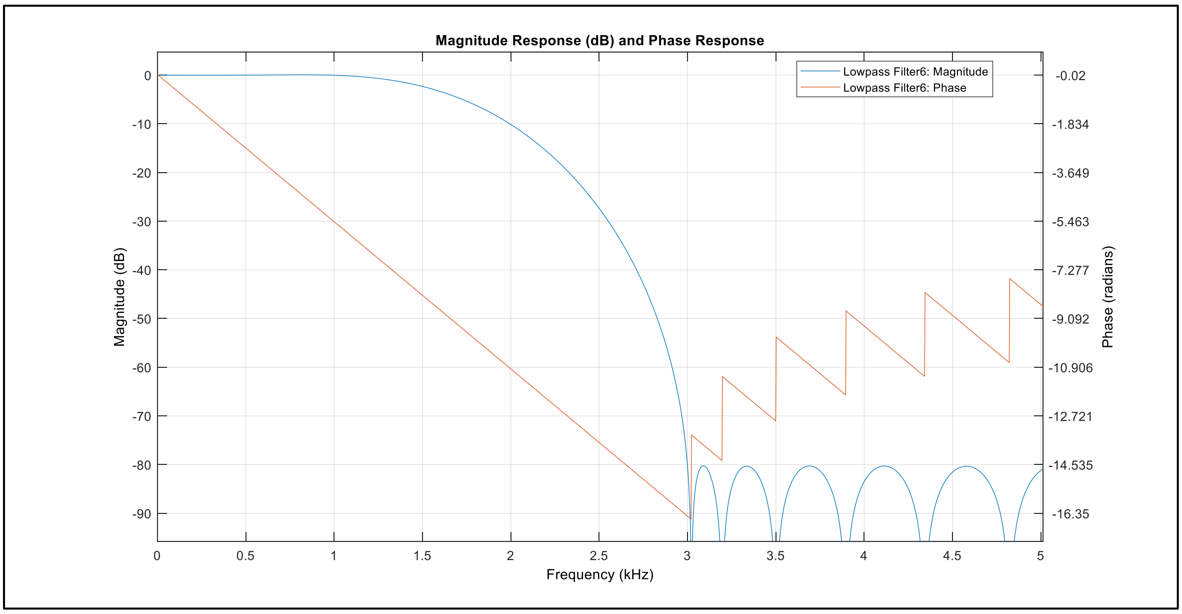

Figure 2.18: low pass filter phase and magnitude response.

Discrete Fourier Transform (DFT) has immunityfrom harmonic components and has a relatively fast response time for the fundamental component calculation. However, the DFT is not immune from the DC component, the decaying DC component in the fault current can cause undesirable oscillations in the DFT results. To eliminate the DC components we need another stage of filtering, the “DC Blocker” block collected from Simulink library is used to eleminate decaying dc component. The IIR algorithm is set to remove DC offset with a normalized bandwidth of 0.001 and the order of the lowpass IIR eliptic filter is set to 6 as shown in **Figure 2.20**.

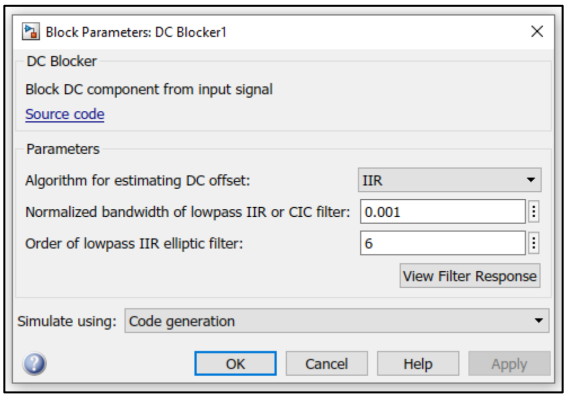

Figure 2.20: "DC blocker" block settings.

iii) Fault detection circuit:

The theory discussed before in the previous section is now applied, six blocks or subsystems, with one for each equation in **Table 2.1**. each block is configured to three zone Mho distance protection, it can be expanded to any n number of zones by simply adding their respective zone reach limits.

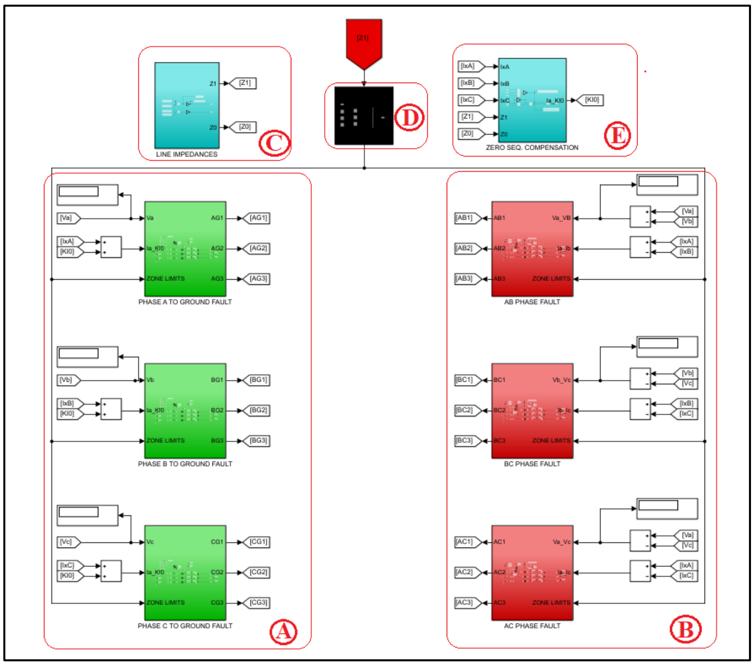

Figure 2.21: Fault detection circuit.

In **Figure 2.21** block A contains subsystems for single line to ground fault detection of the three phases. The three blocks are similar since the equations are the same, while they differ only in the phase voltage and compensated current inputs. Each one of the blocks applies one of the equations from **Table 2.1**. the circuit is shown in **Figure 2.22**.

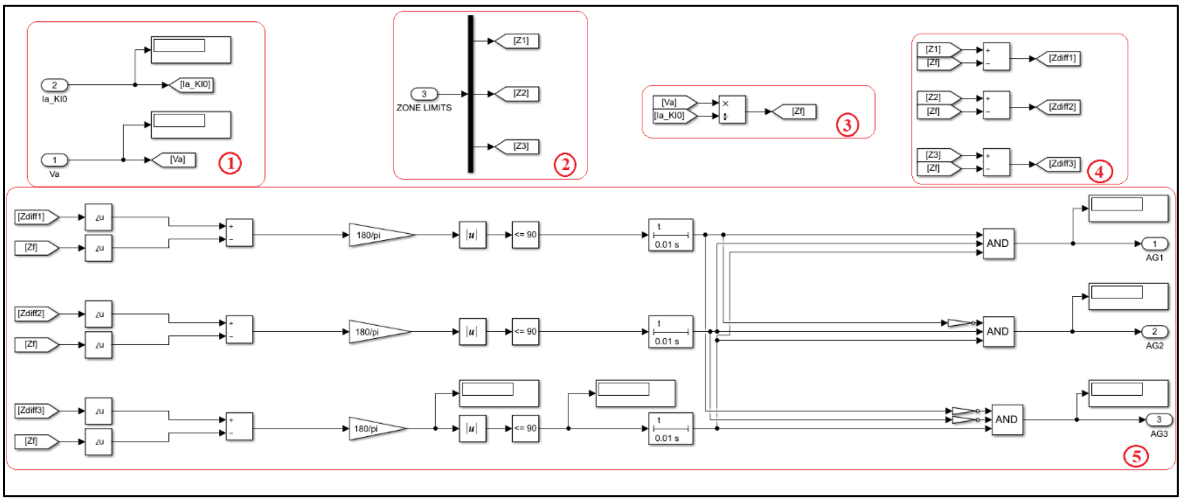

Figure 2.22: Phase A to ground fault detection circuit.

Circuit in **Figure 2.22** can be divided into five parts, part 1 contain input voltage and compensated current. Part 2 inputs the three zones reach or limits. Part 3 calculates the fault impedance seen from the relaying point and using the corresponding equation. Part 4 calculate the vector $\overrightarrow{(ZR - Zsc)}$ angle and magnitude as a complex number. While part 5 decides to which zone the fault corresponds. One can notice that if the fault is in zone 1, all higher reach zones will detect the fault. So, in order to select the proper zone, an "AND" gate logic circuit will detect the faulted zone, if the fault is in zone 2 all higher reach zones than zone 2 will detect the fault and any lower reach zones must not detect the fault, hence we can conclude that the fault belongs to zone 2.

Block B (in **Figure 2.21**) contains subsystems for double line fault detection of any two of the three phases. Each subsystem is divided into five parts as in **Figure 2.22**. The difference between the blocks in A and B is in the input voltages and currents. Block B input voltages are line to line voltages, while current are uncompensated phase currents. The same faulted zones detection logic applies.

In Block C (in **Figure 2.21**) we declare positive and zero sequence impedances as shown in **Figure 2.23**. since settings of transmission line shown in **Figure 2.6** are in Ohms per Km so we need to multiply the impedances by line length.

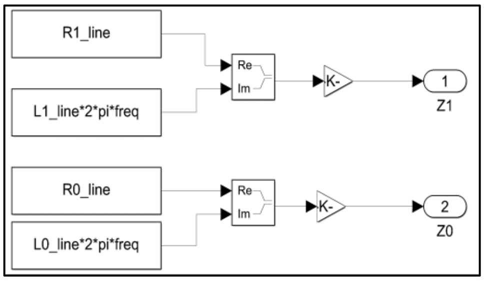

Figure 2.23: positive and zero sequence impedances calculation.

Block D (in **Figure 2.21**) contains circuit for declaring protection zone limits or reaches, the circuit in **Figure 2.24** shows zone limits in per unit values multiplied by the line positive sequence impedance. This circuit contains three zones, zone 1 at 80%, zone 2 at 140% and zone 3 at 220% of the line impedance. This scheme can be expanded to cover any n number of the protected zones.

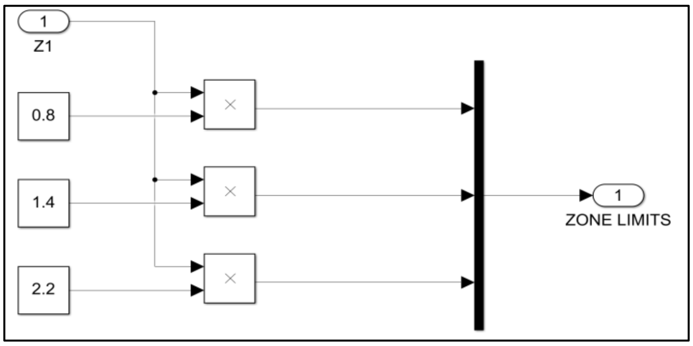

Figure 2.24: Mho model zone limits.

Block E (in **Figure 2.21**) calculates the needed amount of zero sequence current (kI0) for the compensation of the phase to ground fault current in equation Eq.2.7. **Figure 2.25** shows the circuit of block E.

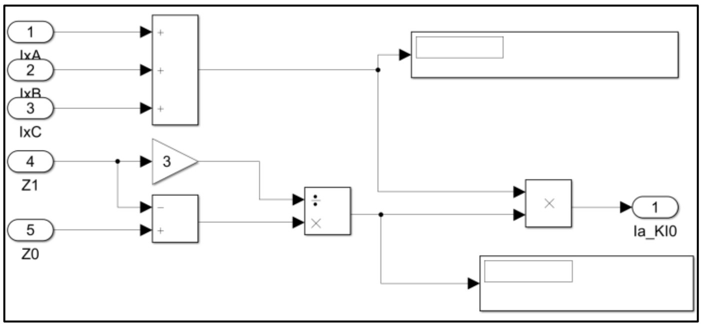

Figure 2.25: Zero sequence compensation circuit.

iv) Fault type and zone selection logic circuit:

Outputs of block A and B of **Figure 2.21** are fairly enough to make a decision of the fault type and zone. For any type there are a set of outputs that will assert a logical 1 and other blocks will assert logical 0, so according to the outputs of these blocks or subsystems we can design a logical circuit that that filters fault types and zones. **Figure 2.26** shows the logical circuit used.

The block will assert logical 1 of the zone 1 fault if any of the outputs:AG1, BG1, 1CG1, AB1, BC1 or AC1 asserts logical 1. Similar logic applies for other zones.

The block will assert logical 1 of the phase A to ground fault if any of the outputs: AG1, AG2 or AG3 asserts a logical 1 and all the outputs: AB1, AB2, AB3, BC1, BC2, BC3, AC1, AC2 and AC3 should assert logical 0 (only phase A to ground fault detection block should assert logical 1). Similar logic applies for phase B and C to ground faults.

The block will assert logical 1 of the phase A and B line to line fault if any of the outputs: AB1, AB2, or AB3 asserts logical 1 all the outputs: AG1, AG2, AG3, BG1, BG2, BG3, CG1, CG2 and CG3 should assert logical 0 (only phase A to phase B fault detection block should assert logical 1). Similar logic applies for other line to line faults.

The block will assert logical 1 of the B and C double line to ground fault if any of the outputs: BC1, BC2 or BC3 assert logical 1 and outputs BG1and CG1, BG2 and CG2 or BG3 and CG3 asserts logical1 respectively. Any other outputs should assert logical 0. Similar logic applies for other double line to ground faults.

The block will assert a logical 1 of the three-phases fault if all outputs assert logical 1.

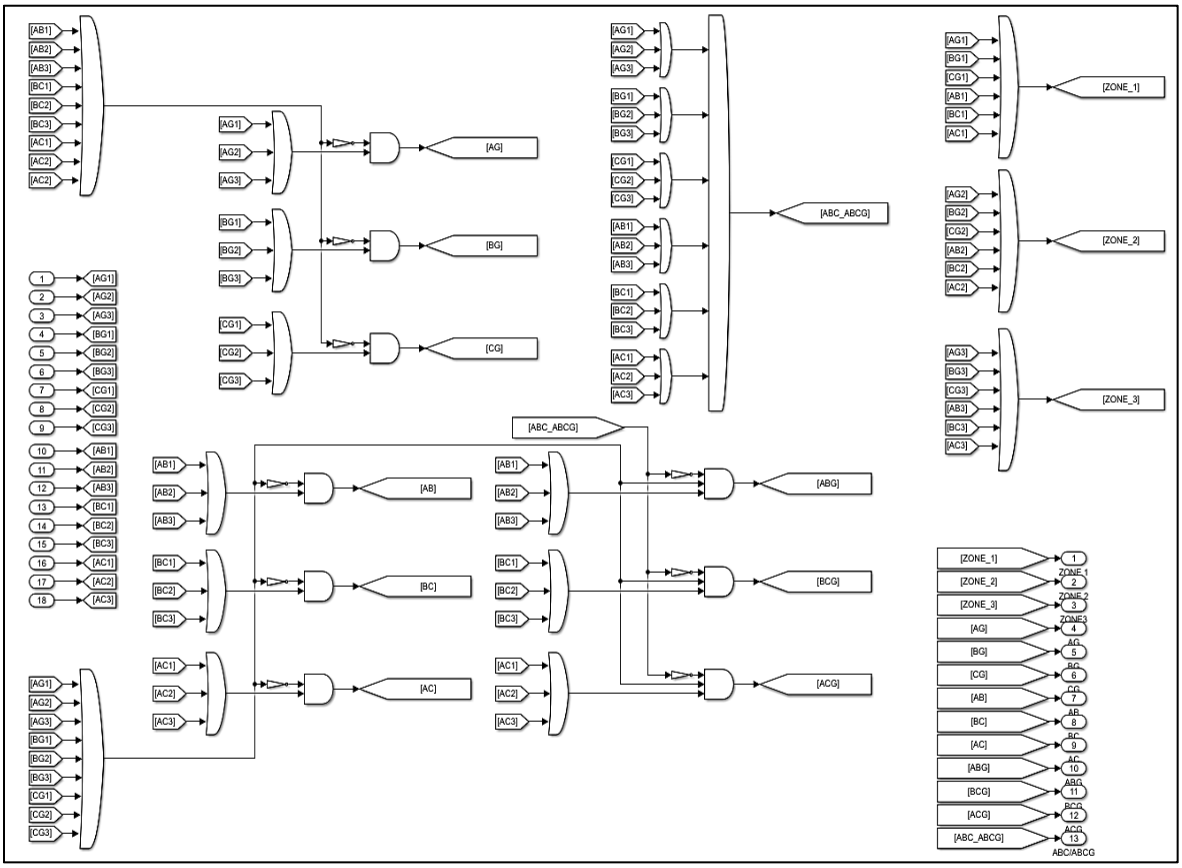

Figure 2.26: Fault type and zone selection logic circuit.

2.3.3 Mho model "SC_MhoConsole" GUI subsystem:

The graphical user interface block is similar to the one used for relay testing. It controls the fault timing, displays simulation real time currents and voltages on scopes and displays the Mho function results on a set of display blocks. The "OpComm" block is set to 19 inports since the "SM_NETWOR" block has 19 outputs. **Figure 2.27** shows components of "SC_MhoConsole" subsystem.

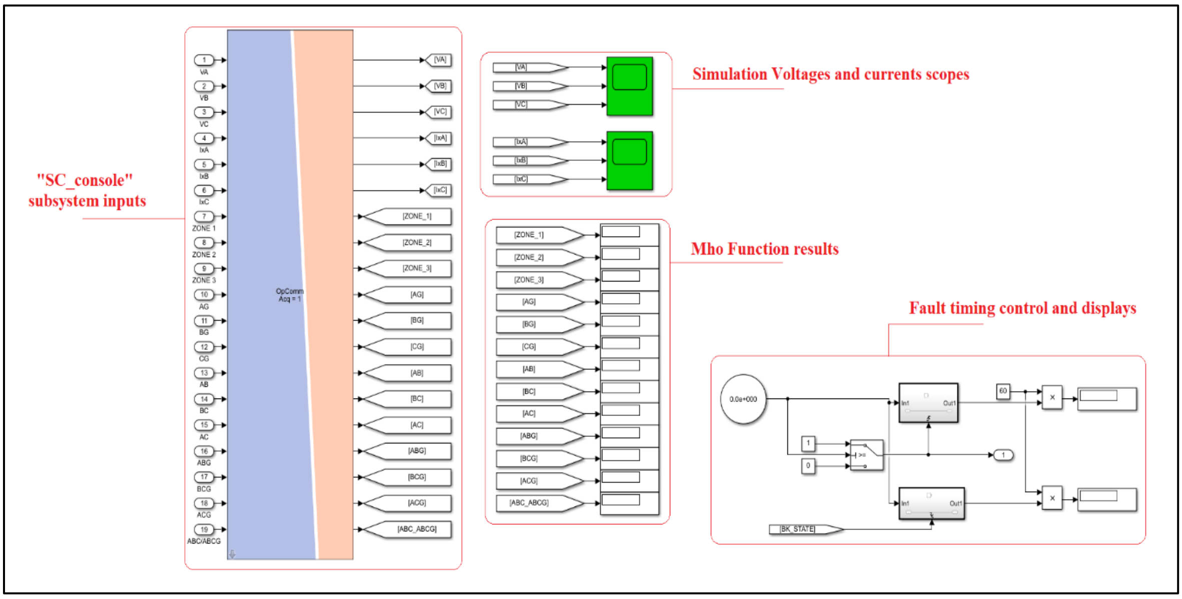

Figure 2.27: "SC_MhoConsole" GUI subsystem.

2.4 Implementing Time overcurrent Function in Simulink model:

2.4.1 Time Overcurrent (TOC) protection theory [9]:

Protection against excess current was naturally the earliest protection system to evolve. From this basic principle, the graded overcurrent system has been developed. Among the various possible methods used to achieve correct relay co-ordination are those using either time or overcurrent, or a combination of both. The common aim of all three methods is to give correct discrimination. That is to say, each one must isolate only the faulty section of the power system network, leaving the rest of the system undisturbed.

Discrimination by Time method, gives an appropriate time setting to each of the relays controlling the circuit breakers in a power system to ensure that the breaker nearest to the fault opens first. Discrimination by current relies on the fact that the fault current varies with the position of the fault because of the difference in impedance values between the source and the fault. Hence, typically, the relays controlling the various circuit breakers are set to operate at suitably tapered values of current such that only the relay nearest to the fault trips its breaker.

Each of the two methods described so far has a fundamental disadvantage. In the case of discrimination by time alone, the disadvantage is due to the fact that the more severe faults are cleared in the longest operating time. On the other hand, discrimination by current can be applied only where there is appreciable impedance between the two circuit breakers concerned. It is because of the limitations imposed by the independent use of either time or current co-ordination that the inverse time overcurrent relay characteristic has evolved. With this characteristic, the time of operation is inversely proportional to the fault current level and the actual characteristic is a function of both 'time' and 'current' settings. **Figure 2.28** shows the characteristics of two relays given different current/time settings. For a large variation in fault current between the two ends of the feeder, faster operating times can be achieved by the relays nearest to the source, where the fault level is the highest. The disadvantages of grading by time or current alone are overcome.

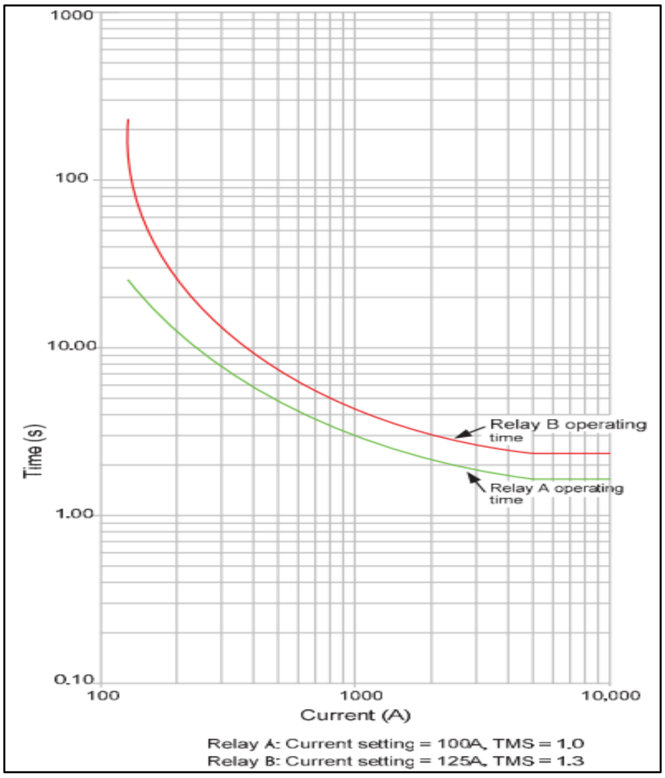

Figure 2.28: Inverse time overcurrent characteristic curve.

Overcurrent relays are also provided with elements having independent or definite time characteristics. These characteristics provide a ready means of co-ordinating several relays in series in situations in which the system fault current varies very widely due to changes in source impedance, as there is no change in time with the variation of fault current more than pickup current.

IDMT curves with stand for inverse-definite minimum time overcurrent protection uses combination of inverse time and definite time curves with relay trip for minimum time.

A wide set of curves are set according to international standards such as U.S and IEC standards. Each curve has its corresponding operating and reset times equations with a variable setting. **Table 2.2** and **Table 2.3** shows U.S and IEC curves equations. [5]

Table 2.2: U.S. Time-Overcurrent Equations.

Curve Type	Operating Time	Reset Time
U1(Moderately Inverse)	$Tp = TD.(0.0226 + \frac{0.0104}{M^{0.02} - 1})$	$Tr = TD.(\frac{1.08}{1 - M^2})$
U2 (Inverse)	$Tp = TD.(0.180 + \frac{5.95}{M^2 - 1})$	$Tr = TD.(\frac{5.95}{1 - M^2})$
U3 (Very Inverse)	$Tp = TD.(0.0963 + \frac{3.88}{M^2 - 1})$	$Tr = TD.(\frac{3.88}{1 - M^2})$
U4 (Extremely Inverse)	$Tp = TD.(0.02434 + \frac{5.64}{M^2 - 1})$	$Tr = TD.(\frac{5.64}{1 - M^2})$
U5 (Short-Time Inverse)	$Tp = TD.(0.00262 + \frac{0.00342}{M^{0.02} - 1})$	$Tr = TD.(\frac{0.323}{1 - M^2})$

Table 2.3: IEC. Time-Overcurrent Equations.

Curve Type	Operating Time	Reset Time
C1(Standard Inverse)	$Tp = TD.(\frac{0.14}{M^{0.02} - 1})$	$Tr = TD.(\frac{13.5}{1 - M^2})$
C2 (Very Inverse)	$Tp = TD.(\frac{13.5}{M - 1})$	$Tr = TD.(\frac{47.3}{1 - M^2})$
C3 (Extremely Inverse)	$Tp = TD.(\frac{80}{M^2 - 1})$	$Tr = TD.(\frac{80}{1 - M^2})$
C4 (Long-Time Inverse)	$Tp = TD.(\frac{120}{M - 1})$	$Tr = TD.(\frac{120}{1 - M})$
C5 (Short-Time Inverse)	$Tp = TD.(\frac{0.05}{M^{0.04} - 1})$	$Tr = TD.(\frac{4.85}{1 - M^2})$

Where: TP is the Operating Time.

TR is the Reset Time.

TD is the Time-Delay Setting also named TDS or Time Dial Settings

M is the ratio of the Measured Current over the Pickup Current.

With each pickup current or time dial setting we get a different characteristic curve corresponding to the settings selected.

2.4.2 TOC model "SM_DirectInj" computation subsystem:

The top-level view for the TOC model is shown in **Figure 2.29**, "SM_DirectInj" injects the voltages and currents of the test through the analog outputs of the simulator, and receives a trip signal from the analog input to stop the injection.

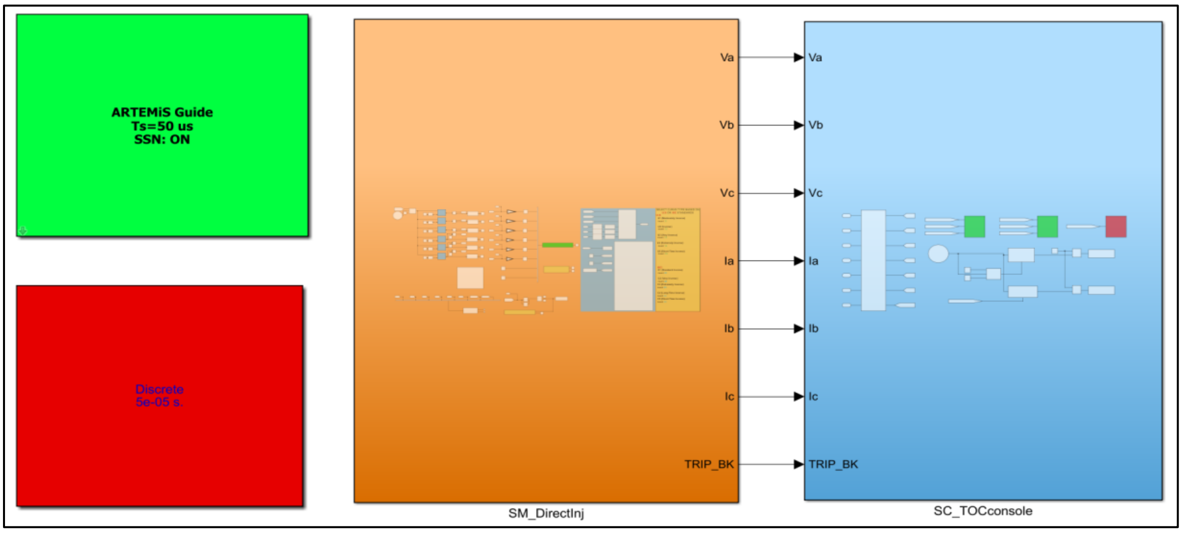

Figure 2.29: TOC model top-level view.

The "SM_DirectInj" computation block shown in **Figure 2.30** can be divided into 5 parts:

- Voltages and Currents selection circuit.
- TOC function block.
- Voltages and Currents injection circuit.
- Trip signal receiving circuit.
- Data acquisition circuit.

i) Voltages and Currents selection circuit:

The TOC function block can be added to relay test model to function with real time simulation currents and voltages of the power system in order to test relay's functionality with the theoretical results of the TOC protection function block. Instead of simulating power system we used a circuit that injects directly the test values of currents and voltages. **Figure 2.30A** shows the circuit that consists of six independent single-phase ac voltage sources, each one is connected in series with a single-phase circuit breaker and a 1 Ohm resistance. This circuit allows the injection and measurement of each phase current or voltage independent from the other phases. And for each value of current or voltage magnitude or phase we can set the power supply to inject the specific values.

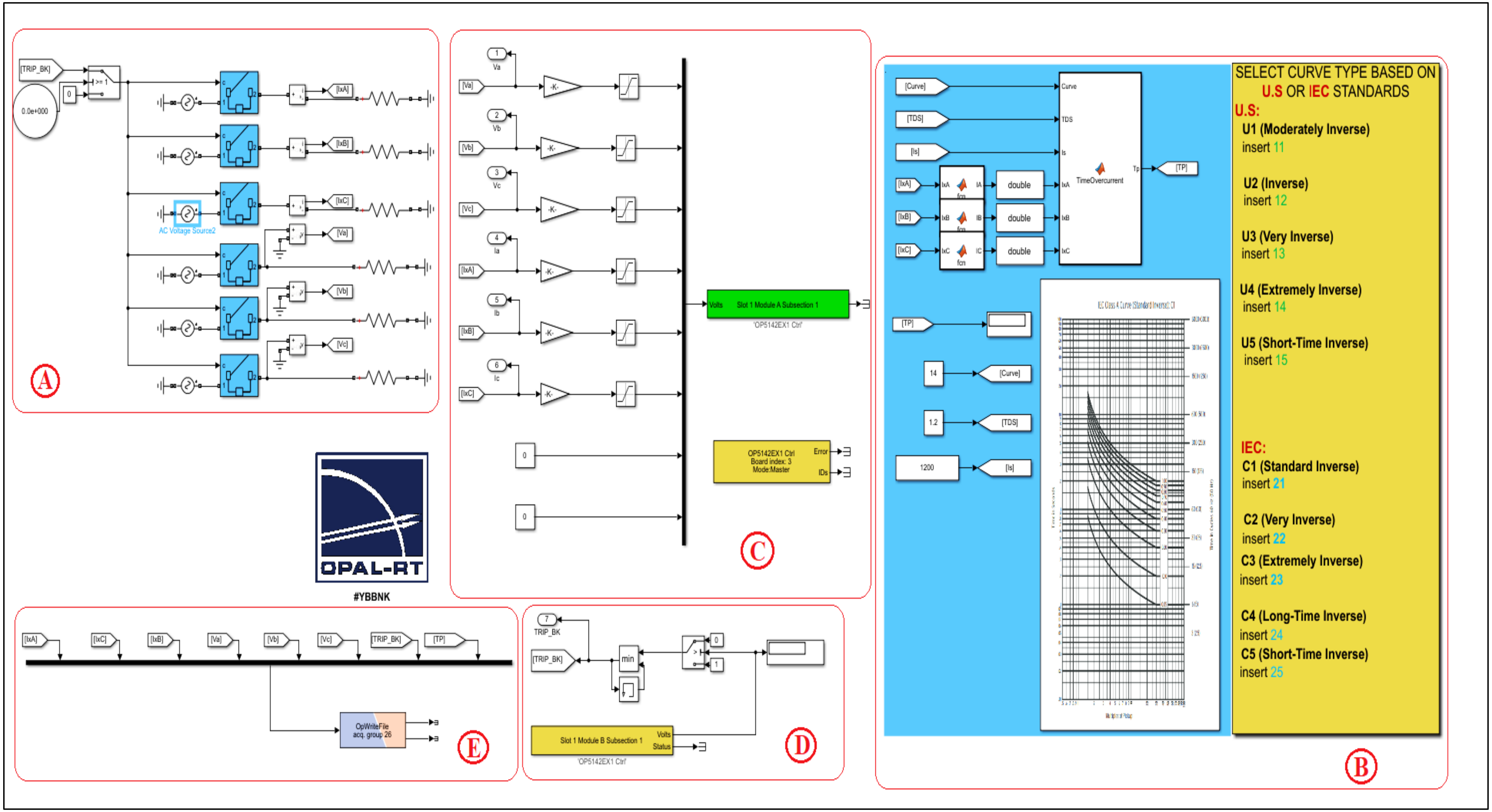

Figure 2.30: A) Voltages and Currents selection circuit. B) TOC function block. C)Voltages and Currents injection circuit. D) Trip signal receiving circuit. E) Data acquisition circuit.

ii) TOC function block:

The TOC function block applies the operating time equation in **Table 2.2** and **Table 2.3** to the measured values of phase currents and with the selected Is which is the setting or pickup current, TDS time dial setting and the selected curve type. The equations are used in a "MATLAB function" block in the program code shown below:

```
function Tp= TimeOvercurrent(Curve,TDS,Is,IxA,IxB,IxC)
%Curve is a two-digit variable used to select type of the curve.
%The first number is used to specify the standards of the curves.
%Curve=1X => US-- Curve=2X => IEC
%TDS:time dial settings
%M = Measured Current / Pickup Current
TpA=0;
TpB=0;
TpC=0;
persistent T
if isempty(T)
    T=0;
end
M3=[IxA,IxB,IxC];
Tp=[TpA,TpB,TpC];
   %U.S CURVES:
   for i=1:3
       M=M3(1,i)/Is;
if (Curve==11)
    T= TDS*(0.0226+0.0104/(M^0.02-1));

elseif (Curve==12)
    T= TDS*(0.180+5.95/(M^2-1));

elseif (Curve==13)
    T= TDS*(0.0963+3.88/(M^2-1));
elseif (Curve==14)
    T= TDS*(0.02434+5.64/(M^2-1));
elseif (Curve==15)
    T= TDS*(0.00262+0.00342/(M^0.02-1));

  %IEC CURVES:
elseif (Curve ==21)
    T= TDS*(0.14/(M^0.02-1));
elseif (Curve==22)
    T= TDS*(13.5/(M-1));
elseif (Curve==23)
    T= TDS*(80/(M^2-1));
elseif (Curve==24)
    T= TDS*(120/(M-1));
else
    T= TDS*(0.05/(M.^0.04-1));
end
 Tp(1,i)=T;
   end
```

This code calculate the "Tp" which is the trip time or operating time for the given inputs "Curve"," TDS" and "Is" for the measured phase currents "IxA", "IxB" and "IxC".

For the circuits: Voltages and Currents injection circuit (C), Trip signal receiving circuit (D) and Data acquisition circuit (E) of **Figure 2.30** we set the circuit blocks according to settings used in part "2.2.4".

2.4.3 TOC model "SC_TOCconsole" GUI subsystem:

The graphical user interface Block shown in **Figure 2.31** displays the injection time of the computation block, and displays the real time simulation current and voltage on scopes, the breaker trip time is also displayed on a scope. The "OpComm" block is set to 7 inports.

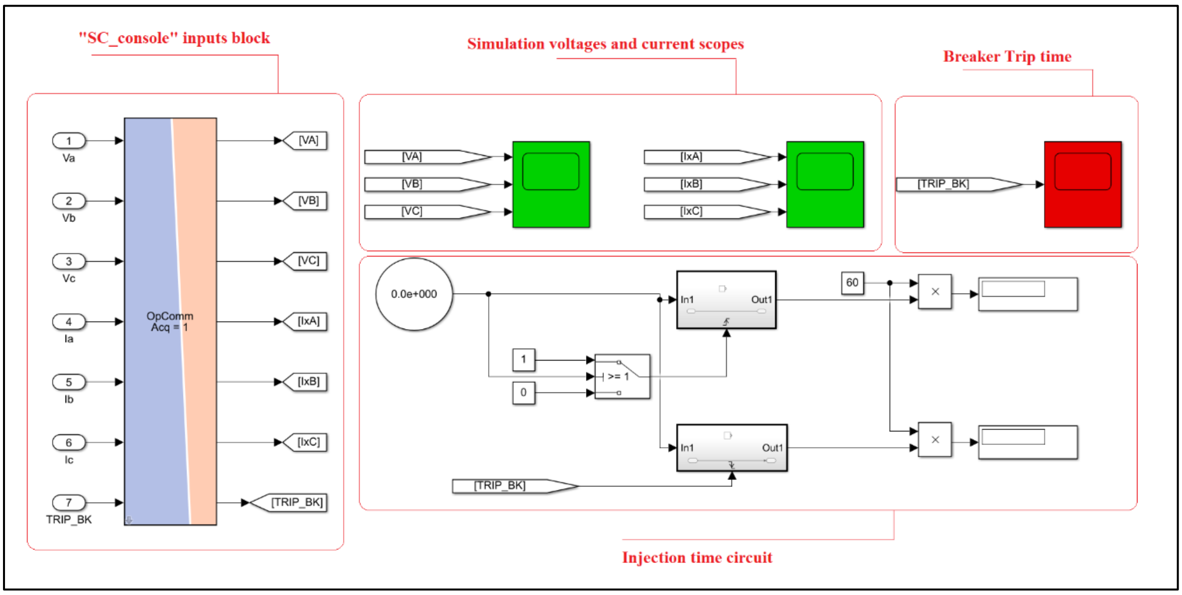

Figure 2.31: "SC_TOCconsole" GUI subsystem.

2.5 Creating Simulink models for Power Meters testing:

2.5.1 General overview of Power meters model:

Modern power systems are experiencing an increasing number of distorted waveforms caused by fast-switching circuits and nonlinear elements. These distorted waveforms decrease the efficiency of systems and end equipment and can also negatively affect revenue metering accuracy. The most important function of revenue meters is accurate metering under all system conditions, but not all revenue-grade meters can accurately and precisely measure the full spectrum of energy consumption in all conditions.

Power and quality revenue meters are one the most important devices that needs to be periodically tested and calibrated. The IEC and ANSI standards are a well-selected set of tests according to the devices specifications that ensures the well working states. Nowadays, any power meter is firstly calibrated and tested in laboratories according to the "IEC 62052-11:2002, 62053-22:2003, 62053-23:2003, IEC 61000-4-7:2002 and IEC 61000-4-15:2003" IEC standards or to the "C12.20-2015" ANSI standards [11].

Testing power meters with real time digital simulator can make maters calibration a lot easier than before, building a model with full compliance to the standards to test meters can be realised with a Simulink model with a program code that include the voltage and current amplitudes, phases, and test time. The power meters are set to be tested in closed loop (HIL method). This allows the simulator to collect the reading of the meters and compare it with the standards.

2.5.2 Meter testing model "SM_Meter" computation subsystem:

Meter testing model shown in **Figure 2.32** consists of two subsystems: "SM_Meter" computation subsystem that injects the test values through the analog outputs and receives the meter readings through the analog inputs. The "SC_MeterConsole" GUI subsystem displays the real simulation time tests values of currents and voltages and the percentage error.

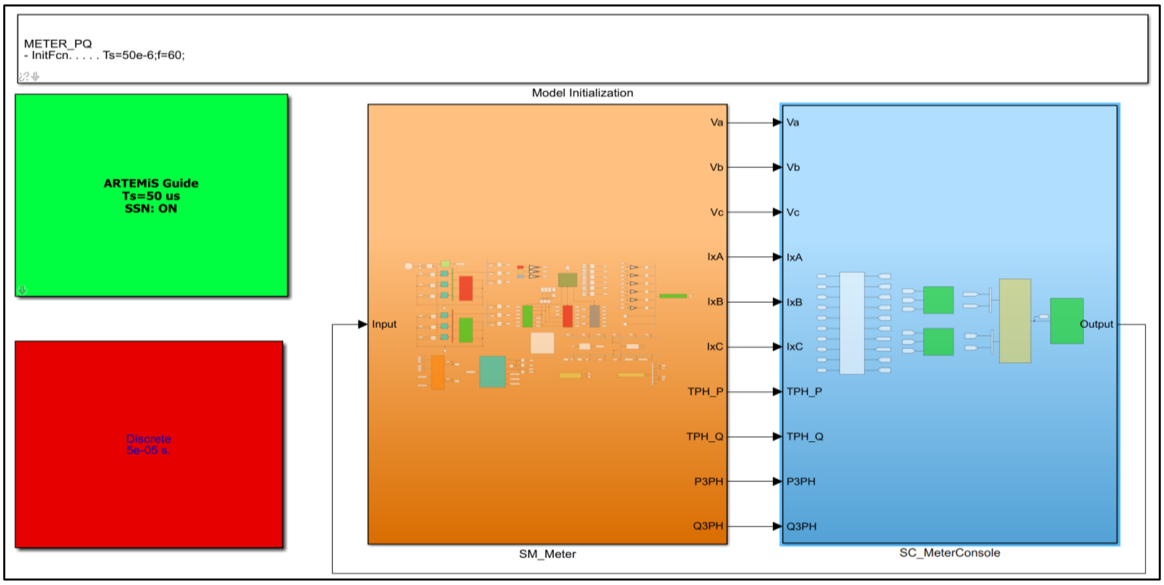

Figure 2.32: Meter test model top-level view.

The "SM_Meter" computation block shown in **Figure 2.33** can be divided into seven parts:

- ANSI/IEC standards test block.
- Phase shift applying circuit.
- Test Voltages and Currents selection circuit.
- Test Voltages and Currents injection circuit.
- Three phase real and reactive power calculation block.
- Three phase meter's power reading circuit.
- Data acquisition circuit.

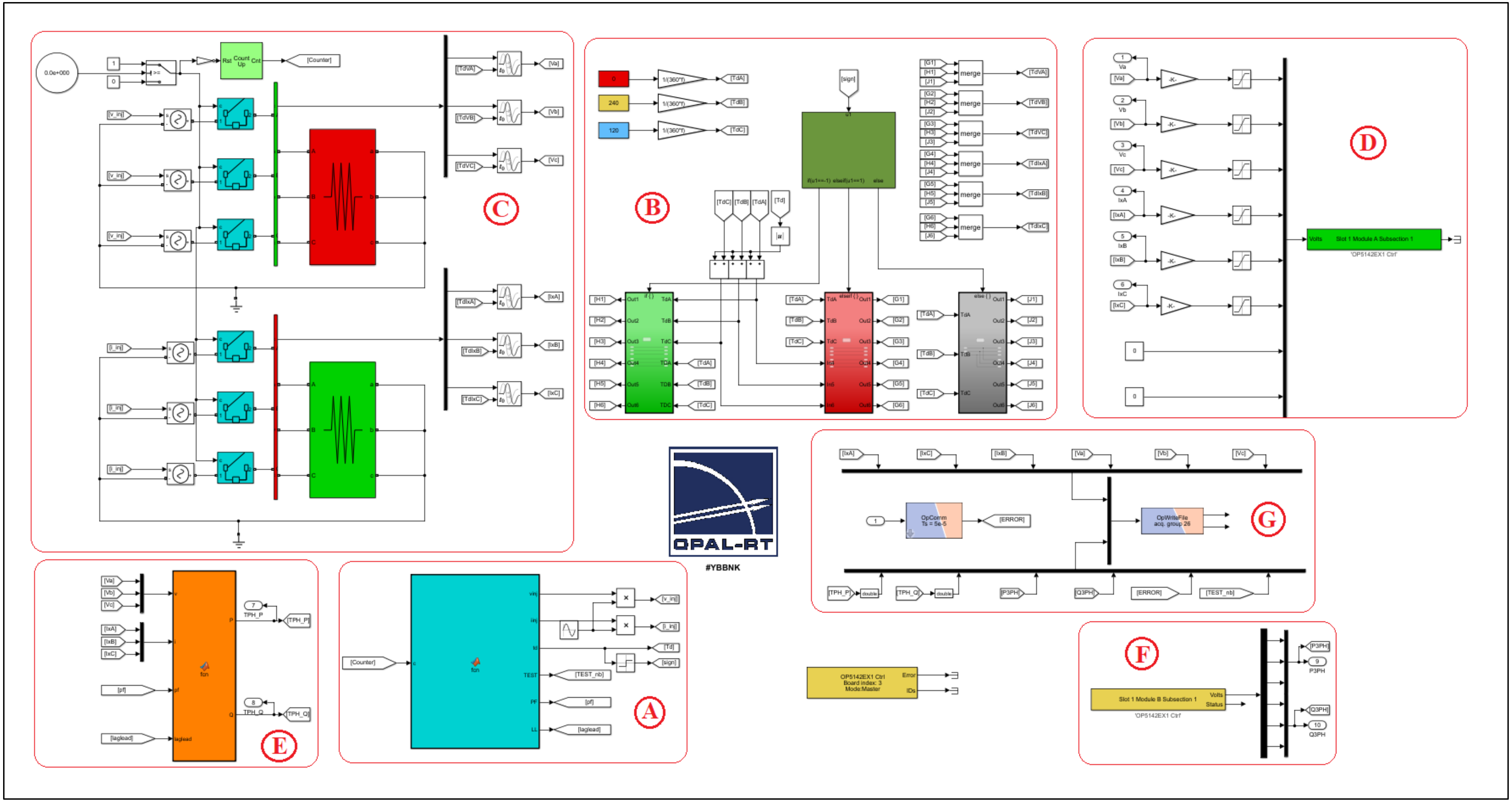

Figure 2.33: A) ANSI/IEC standards tests block. B) Phase shift applying circuit. C) Test Voltages and Currents selection circuit. D) Test Voltages and Currents injection circuit. E) Three phase real and reactive power calculation block. F) Three phase meter’s power reading circuit. G) Data acquisition circuit.

i) ANSI/IEC standards test block:

ANSI/IEC standards test block consist of a “MATLAB function” block. The input of this block is a counter with steps in seconds. It contains the ANSI/IEC standards test values of currents and voltages magnitude and power factor. The block computes the phase shift in term of a delay in seconds.

Power system signals are sinusoidal, so currents and voltages can be written in the form:

$$V(t) = Vm \times \sin(\omega t + \varphi) \qquad \text{Eq.2.9}$$

$$I(t) = Im \times \sin(\omega t + \varphi) \qquad \text{Eq.2.10}$$

Where: Vm, Im are peak values, $\omega = 2\pi f$ is angular speed in radians, and φ is the phase shift of the signal.

Since φ represents an angle in radians and we have the angular speed ω so we write Eq2.9 and 2.10 as:

$$V(t) = Vm \times \sin(\omega(t + Td)) \qquad \text{Eq.2.11}$$

$$I(t) = Im \times \sin(\omega(t + Td)) \qquad \text{Eq.2.12}$$

Where: $Td = \frac{\varphi}{\omega}$ in seconds.

Since the phase shift is a relative relationship between currents and voltages, we can fix one as reference and shift the other by the angle of the power factor. The “MATLAB function” block computes the time delay using the Eq.2.13:

$$Td = \pm\frac{cos^{-1}(PF)}{\omega} = \pm\frac{cos^{-1}(PF)}{2\pi f} \qquad \text{Eq.2.11}$$

Where: Pf is the power factor, f is the system frequency and +sign for lead power factor and -sign for lag power factor.

We can assign a test for each values of the counter or a range of counter steps to reach test time through the “MATLAB function” block configuration code. The “Matlab function” was configured with the following code:

```
function [vinj,iinj,td,TEST,PF,LL] = fcn(c)
f=60; %system frequency.
%define test values based on the counter values.
%FIRST TEST VALUES:
if c==1
     v=205;
     i=2.5;
     pf=1;
     laglead=0;
     Td=-1*laglead*acos(pf)/(2*pi*f);
     test=100;
```

```
elseif c==3
     v=205;
     i=5;
     pf=0.5;
     laglead=1;
     Td=-1*laglead*acos(pf)/(2*pi*f);
     test=200;
     elseif c==5
     v=205;
     i=5;
     pf=0.5;
     laglead=-1;
     Td=-1*laglead*acos(pf)/(2*pi*f);
     test=300;
     elseif c==7
     v=205;
     i=5;
     pf=0.9;
     laglead=-1;
     Td=-1*laglead*acos(pf)/(2*pi*f);
     test=400;
     elseif c==9
     v=205;
     i=5;
     pf=0.9;
     laglead=1;
     Td=-1*laglead*acos(pf)/(2*pi*f);
     test=500;
else
     v=0;
     i=0;
     pf=1;
     laglead=0;
     Td=-1*laglead*acos(pf)/(2*pi*f);
     test=1;
end

vinj=v;
iinj=i;
td=Td;
TEST=test;
PF=pf;
LL=laglead;
```

ii) Phase shift applying circuit:

For the different tests we have three states, leading, lagging or unity power factor tests. So, a phase shift of current or voltage signal must be applied. For a leading power factor test, instead of shifting the current to the left we can shift the voltage with a positive amount of time delay. While for lagging power factor test, we can shift the current signal with a positive amount of time. The time delay or phase shift is added to the symmetrical phase shift of the power system. Using and "If" block with three "If switch case subsystem" blocks we can demonstrate the three states of tests, the merge block id used to output the available signal of any of the three switch cases. **Figure 2.33B** shows the used circuit.

iii) Test Voltages and Currents selection circuit:

The voltage and current amplitude outputs of Block A of **Figure 2.33** are MATLAB signals, we multiply those signals by a sine wave with the nominal frequency of 60Hz in order to sinusoidal signal. These signals are going to drive a "Controlled voltage source" blocks to generate the proper test voltages and currents. This block is collected from Simscape fundamental electrical sources. We set the voltage source to AC. Then we apply the proper time delay for the measurement circuit with "Time delay" block controlled by the outputs of Block B of **Figure 2.33.**

iv) Three phase real and reactive power calculation block:

This block is used to calculates the real and reactive powers for each test. The values are to be stored in a ".m" file and it will be used to calculate the percentage error in the GUI subsystem. The "MATLAB function" block is configured to calculate three phase powers; the configurations code is shown below:

```
function [P,Q] = fcn(v,i,pf,laglead)

P=v.*i.*pf;
Q=laglead*v.*i.*sin(acos(pf));
```

The configuration of the circuits D, G and F in **Figure 2.33** are similar to the configurations in part 2.2.4, while the analog input signals are six (6) inputs for the three phases real and reactive powers instead of one trip signal.

2.5.3 Meter testing model "SC_MeterConsole" GUI subsystem:

"SC_MeterConsole" GUI subsystem in **Figure 2.34** displays the currents and voltages and calculates the percentage error between the meter measurement received from the analog inputs and the calculated values of simulation in the three-phase real and reactive power calculation block.

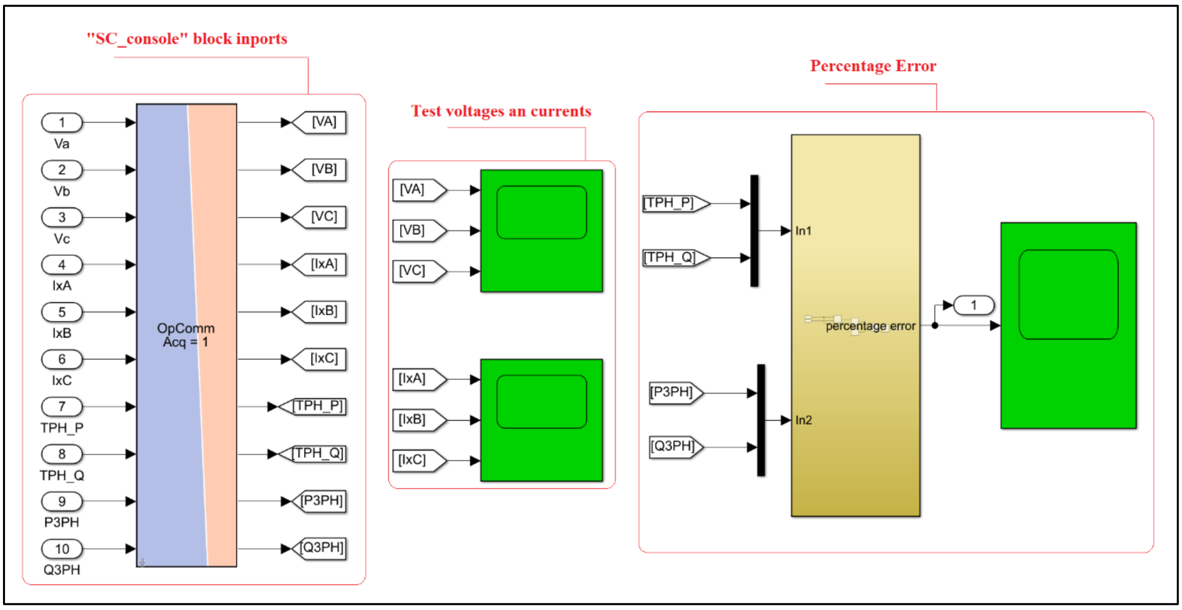

Figure 2.34: "SC_MeterConsole" GUI subsystem.

2.5.4 Conclusion:

This chapter has dealt with the main steps for creating Simulink models for the Opal RT-LAB target platforms to test relays and power meters with HIL method.

In this chapter, we configured the SM computation and SC GUI subsystems for Opal RT-LAB simulation models. The SM subsystem simulated the fault and test currents and voltages of the model. The SC GUI is configured to display the simulation voltages and currents.

This chapter explained the basic theory of Mho distance and Time Overcurrent used for the creation of Simulink models of these protection functions.

Chapter 3: Experimental Results and Discussion

3.1 Introduction:

This chapter presents the experimental procedures followed for real time simulation test with hardware in the loop (HIL). Test steps consists of six phases: Configuration (1), Edition (2), Preparation (3), Compilation (4), Execution (5) and Collection (6) phase. The tests start with configuration of hardware and ends with Collection of report files from both hardware and simulator. At the end of a collection phase we can run a new test by starting again; if hardware settings change is needed, from the Configuration phase, otherwise we can start from the Edition phase.

3.2 Configuration phase:

In the configuration phase we set the hardware to match the power system settings. In most of the time the relay is pre-configured or provided with the configuration file based on a study of the power system. Setting relay to power system configurations gives a great opportunity to match real case faults during real time simulation.

In this experiment we used SEL-411L and SEL-487 relays and SEL-735 power meter of the Schweitzer Engineering Laboratories. SEL products are configured by a single software SEL-5030 AcSELerator QuickSet that provides a list of products each one is specified by a part number. If a device is not found on the list an update is needed. The AcSELerator QuickSet software is opened by a double clicking the icon shown in **Figure 3.1A**, **Figure 3.1B** will be shown on the screen while preparing the software to start.

Figure 3.1: A) AcSELerator QuickSet software icon. B) starting window.

Once the software starts, the home screen shown in **Figure 3.2** will be displayed. On this home page you can click on “New” to select a device from the list available to create a new file that hold the settings of the device, click on “Read” to read settings that are stored on the device or you can click on "Open" to get access to a settings file stored in the computer.

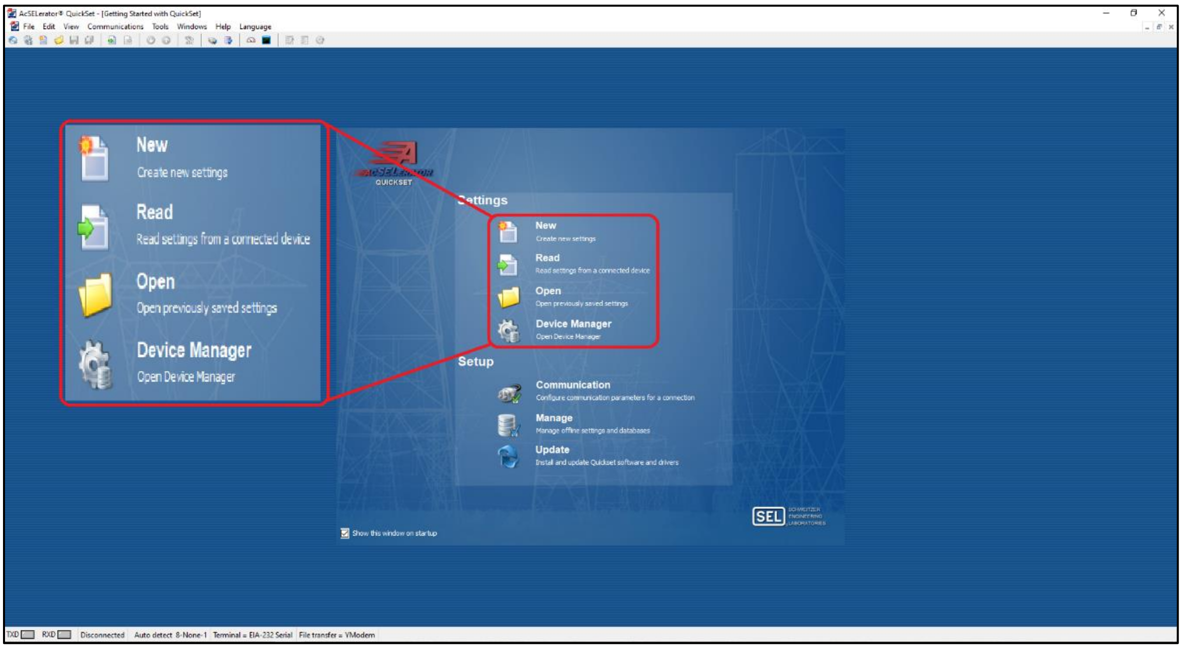

Figure 3.2: AcSELerator QuickSet Home page.

To establish communication with relay, click on "Communication" then the pop-up window in **Figure 3.3** will appear to set the settings of the communication types available (Serial, Network, Modem). Once you enter settings click on "Apply" then "OK". If settings are correct the connection is established, otherwise a pop-up window will indicate the error.

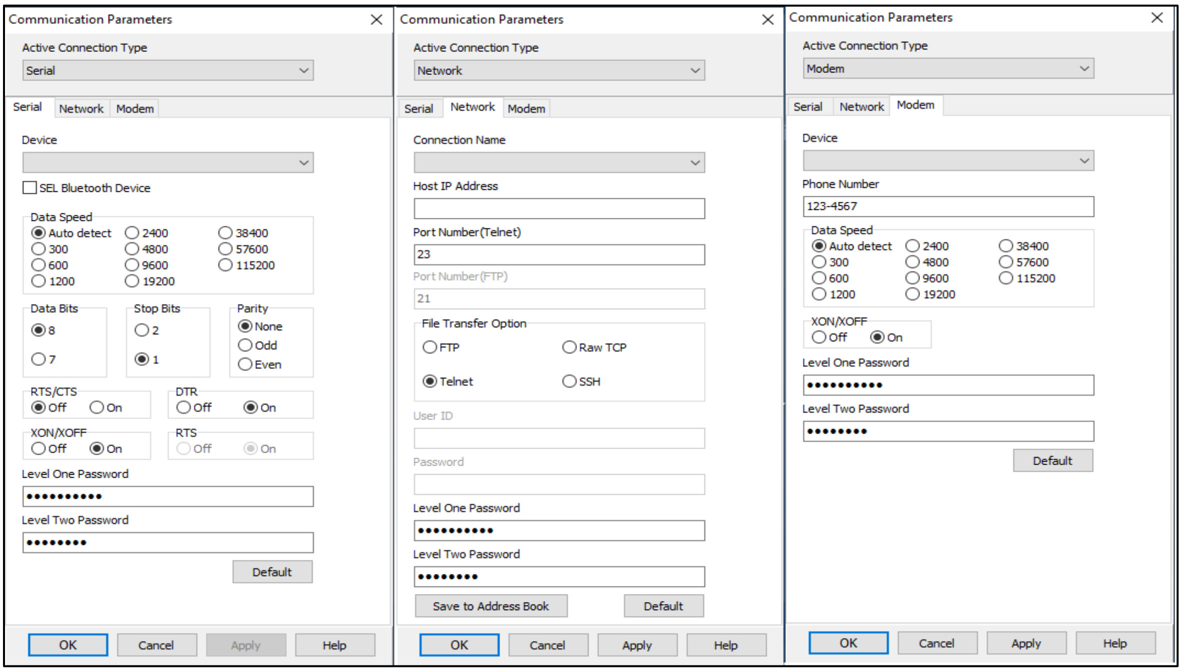

Figure 3.3: AcSELerator QuickSet communication types.

3.2.1 Configuration of SEL-411L [1]:

SEL-411L relay shown is a high-speed transmission line differential, distance, and current protection relay. In this experiment, distance protection element of SEL-411L relay is set to be tested with three zones of protection set at 80%, 140%, and 220% of the positive-sequence impedance of the line. The protection line protected by the relay has the following settings: positive-sequence line impedance magnitude $Z1M = 3.29\Omega$, positive-sequence line impedance angle $Z1ANG = 87.93°$, zero-sequence line impedance magnitude $Z0M = 8.98\Omega$, zero-sequence line impedance angle $Z0ANG = 76.05°$ and line length of 100 Miles. We enable three zones for ground and phase protection and we disable all other function by setting elements to "N". Relay settings are shown in **Appendix B**.

3.2.2 Configuration of SEL-487E [1]:

SEL-487E relay is used for power transformer protection, it provides a suite of current and voltage elements of protection. In this experiment, Time overcurrent protection element of the relay is to be tested. We selected one element of inverse time overcurrent at each time we change the element pickup "51P01", curve type "51C01", and time dial setting "51TD01". Setting of the relay are shown in **Appendix C**.

3.2.3 Configuration of Doble F6350 Current / Voltage Amplifier:

Doble amplifier F6350 is used to amplify voltage signals that are coming out of the simulator analog outputs to the inputs of the protection relays. The amplification is needed since the simulator outputs a maximum of 16V while the rated relay input is 67V.

Doble F6350 offers three voltage amplification gains: 6.7V/75V, 6.7V/150V and 6.7V/300V and two current amplification gains: 3.4V/7.5A and 3.4V/15A. The selection of a specific gain is determined by the amplifier input voltage which comes from the simulator output port and also by the required voltage at the relay's terminals.

After selection of the amplification gain, we need to calculate the MATLAB model output gains using equation Eq.2.1.

3.3 Edition phase [4]:

In the edition phase, the computation subsystem of the model created by Simulink is edited based on the real time test, we can insert changes for the power system, fault location, fault type and fault resistance settings. To edit the model, we need to move it to the workspace of the RT-Lab software then we carry out the modification needed. First, double click on the RT-lab software to open it, a pop-up window will ask you to select the workspace folder, we can select a location folder as a workspace or you can save it in the default address "C:/Users/User_name/RT-LAB workspace/".

To add a project to the workspace, in the "Project Explorer" window click on "Create a new Project" select a project name and description and press next. In the new window select "Empty project" and click on finish. The selected project folder will be shown in the "Project Explorer" window, in the project folder right click on "Models" to add or create new Simulink model. Once you add or create a model, right click on the model and select "Edit" to edit the model, steps are described in **Figure 3.4**.

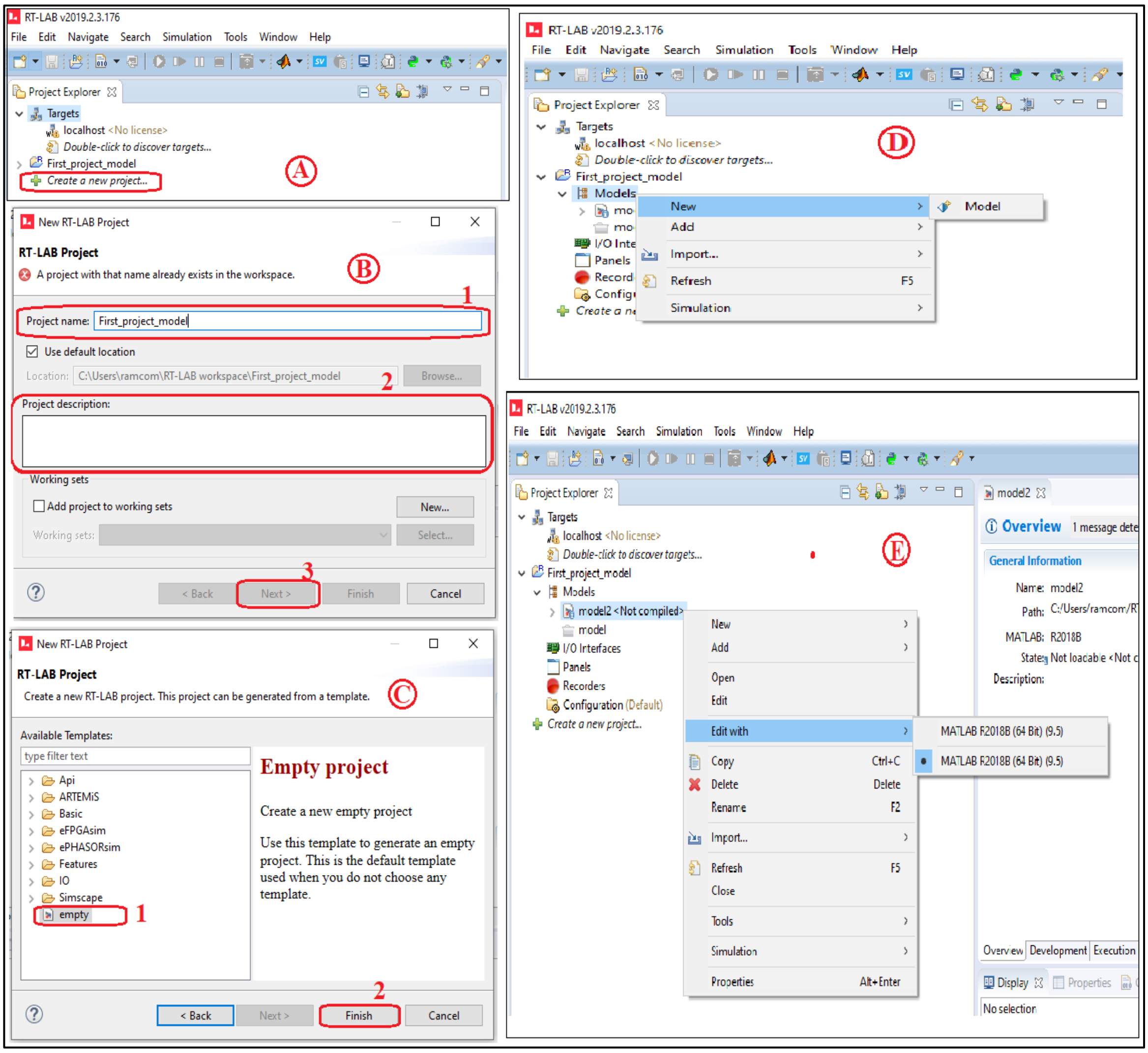

Figure 3.4: Edition phase steps.

3.4 Preparation phase [4]:

In the preparation phase, the OPAL-RT Linux (x64-Based) ® target platform is selected, to communicate with host and target computers during the RTS experiment tests. **Figure 3.5** shows the selected target platform in the development settings.

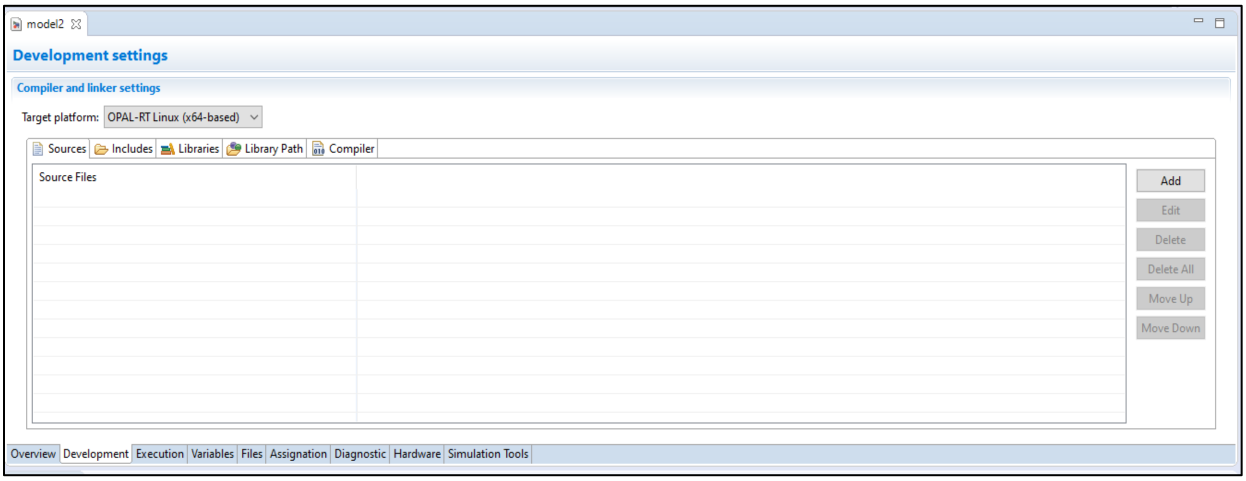

Figure 3.5: Development settings window.

When we select the “Target platform” we can build the model in the simulator, right click on the model and select “Simulation” then click on “Build configurations” as shown in **Figure 3.6**.

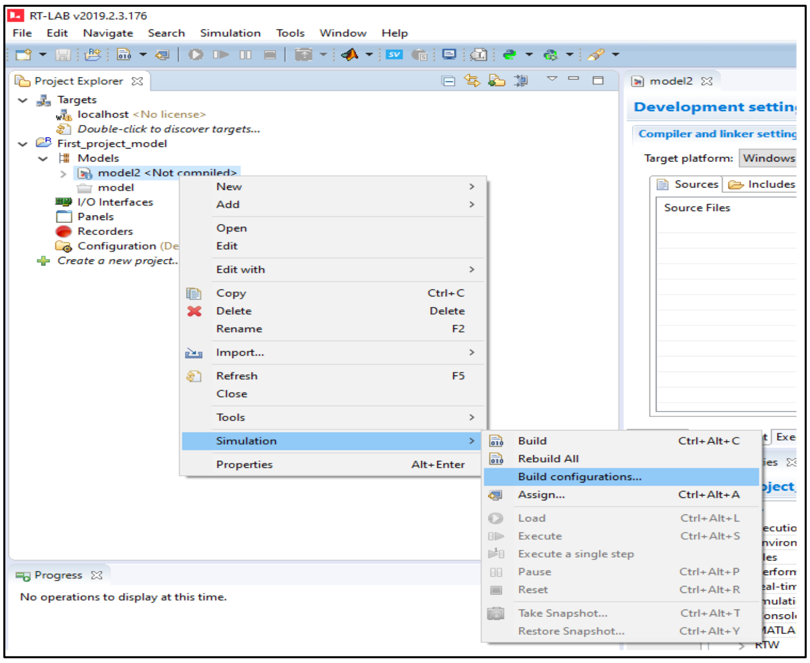

Figure 3.6: Building the model.

3.5 Compilation phase [4]:

In the compilation phase, the results from the compilation view are consulted and the target computer is assigned. However, if the model is built satisfactorily in the Preparation phase, the model is compiled successfully with no errors. Otherwise, compilation errors are shown in the “Display” Window of the software. After the correction of errors, we need to build again the model. **Figure 3.7** shows the “Assignation” window settings.

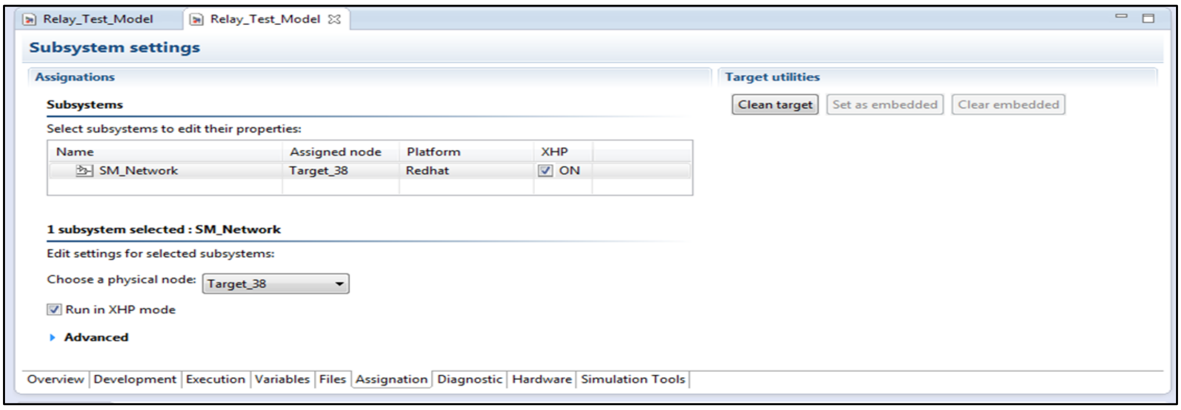

Figure 3.7: Assignation window settings.

In real-time simulation, the OP5600 (target computer) is connected to the host computer in order to run the real-time test. **Figure 3.7** shows subsystem settings. In the real-time tests, we choose a physical node from the available in the list, and the subsystems are set to run in eXtreme High Performance (XHP) mode.

3.6 Execution phase [1]:

In the Execution phase, execution properties to run the test are set, and the model is loaded into the target computer and executed. The "Execution Properties" settings are set as shown in **Figure 3.8**, "Target platform" is set to OPAL-RT Linux (x64-Based), "Simulation mode" is set to Hardware synchronised, "Real time communication link type" is set to UDP/IP, "Time Factor" is set to 1.0 to perform real time test, "Stop Time" and "Pause Time" are set according to the simulation time and the tripping time.

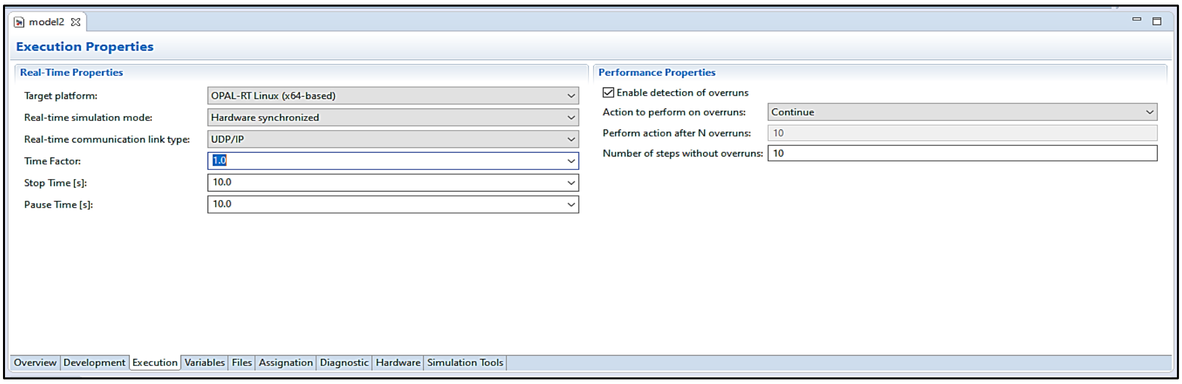

Figure 3.8: Execution window settings.

After selecting the execution settings, we can load the model to the OP5600 simulator. in the Quick access bar of the RT-LAB software click on Load icon to load the model to the simulator, the process takes a few seconds to complete. At the end of the load process the GUI subsystem will open in a new window separated from the model as shown in **Figure 3.9**.

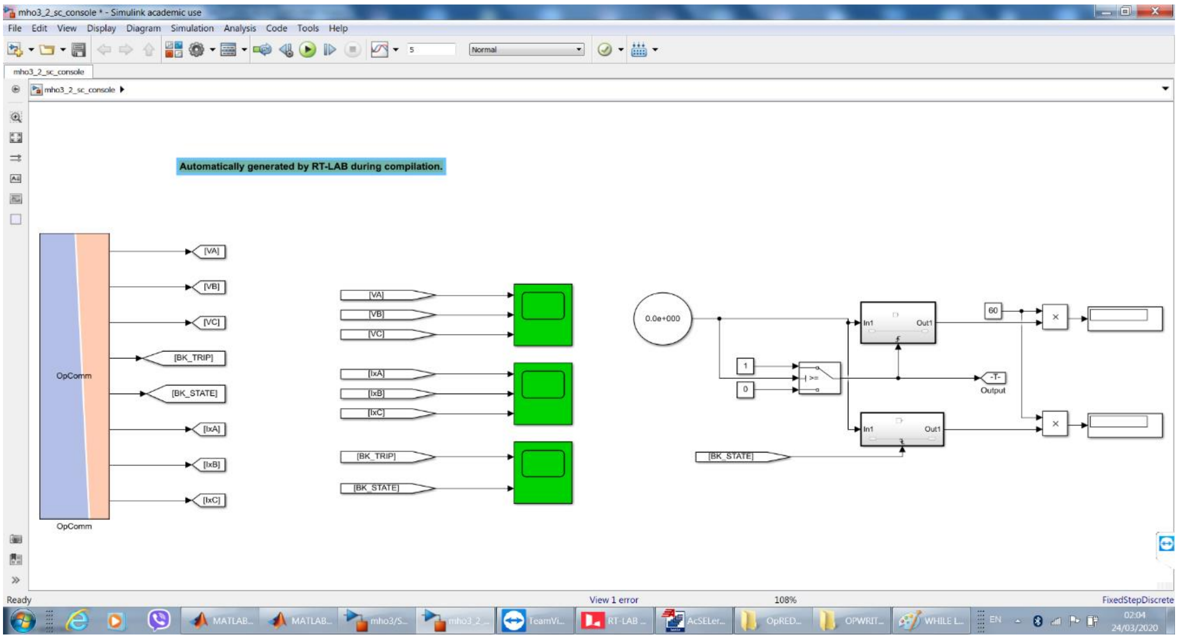

Figure 3.9: “SC_console” GUI subsystem displayed at the end of load process.

If the process ends successfully, we can now run the real time simulation by clicking on Execute icon. Currents and votages and all signals of the simulation are shown in real time, double click on the scopes to consult simulation signals. The communication between target platform and host computer is established by ethernet cable, the “OpComm” bloc collects data from the computation block.

3.7 Collection phase [1]:

In the collection phase, the simulator collects the bus currents and voltage, breaker states and trip signals. The OP5600 target platform records the events under a MATLAB “.m” file stored in the hard drive; this file will be sent to the host computer at the end of the simulation. This process enhances test results by allowing the simulation to run almost with no interruption time.

At the end of simulation, the host computer receives the MATLAB files that holds the test current, voltages and trip signals. The host computer saves the file of each test in “OpREDHAWKtarget” folder that can be found in the project folder. Double click on the file to open it in MATLAB, in the window shown in **Figure 3.10** click on finish to copy data to the workspace.

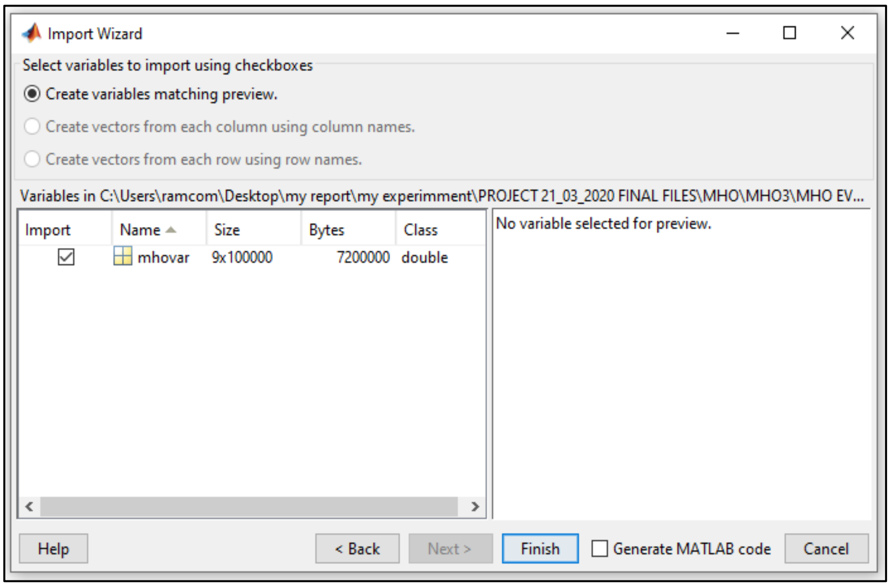

Figure 3.10: "OpWrite" file opened with MATLAB.

In MATLAB workspace, a new variable will appear with the same name of the "OpWrite" file variable name. this variable is divided by rows. The first row represents the simulation time, the next rows represents test variables in the order of the multiplexer signals. We can select a row or a set of rows to create a new MATLAB variable stored in the workspace, for example we select the first row, right click and select "New variable from selection" and click on "New numeric array". Variable creation steps are shown in **Figure 3.11**.

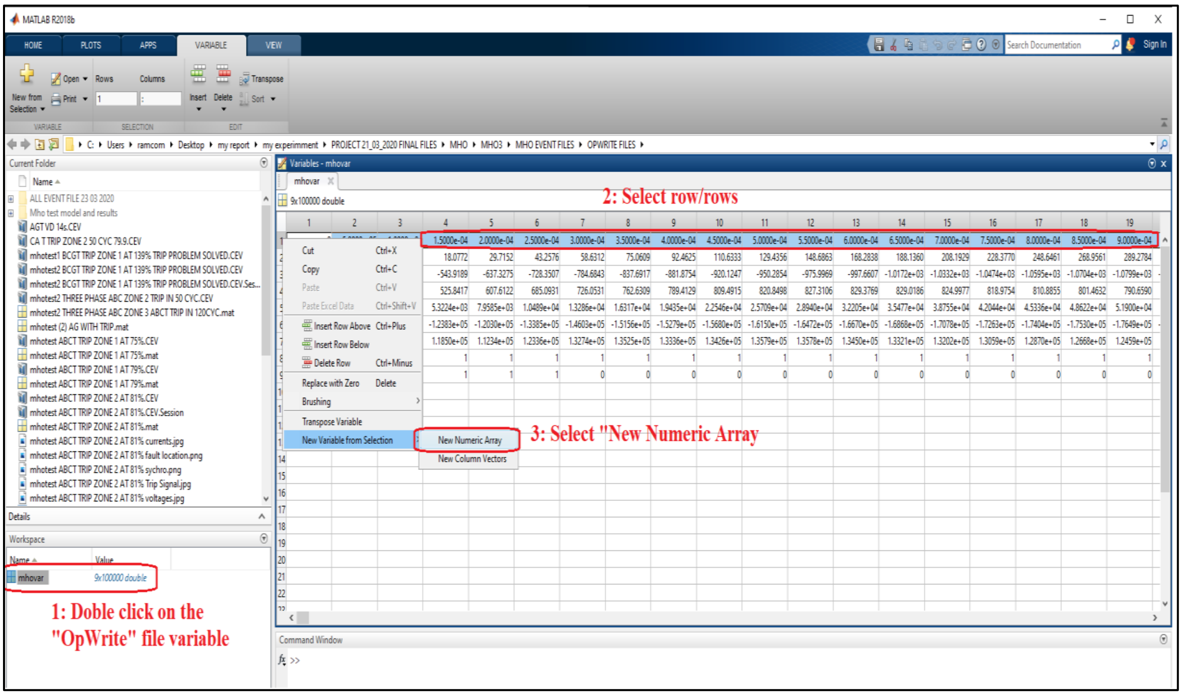

Figure 3.11: Variable creation step from MATLAB variable.

3.8 Simulation tests and results:

3.8.1 Mho model test results:

The SEL-411L relay connected at “Bus 2” (see **Figure 2.7**) is supposed to protect the transmission line between the two buses. The readings of the measurement bus are injected to the relay. When the relay detects a fault a trip signal is asserted to open circuit breaker located at “Bus 2”. Different tests carried out for the Mho distance protection are shown in **Table 3.1**:

Table 3.1: Distance relay protection function tests.

Tests	Fault Type	Zone	Location	Trip Time
1	Phase A-Ground	Zone 1	49%	0 s
2	Phase A–Phase B-Ground	Zone 2	139%	0.833 s
3	Phase B–Phase C-Ground	Zone 3	141%	1.333 s
4	Phase A–Phase C	Zone 1	79%	0 s
5	Phase B–Phase C	Zone 3	142%	1.333 s
6	Three Phase ABC	Zone 2	81%	0.833 s

The tests results are shown in **Table 3.2.** From the test results we can deduce the working state of the relay based on the test standards:

Table 3.2: Distance relay protection function test results.

Tests	Detected Fault Type	Detected Zone	Location	Location Error	Trip Time	Time Error
1	Phase A-Ground	Zone 1	48.02%	2.00%	17.00 ms	--
2	Phase A–Phase B-Ground	Zone 2	138.15%	0.61%	0.867 s	4.08%
3	Phase B–Phase C-Ground	Zone 3	139.75%	0.88%	1.364 s	2.32%
4	Phase A–Phase C	Zone 1	78.60%	0.51%	12.50 ms	--
5	Phase B–Phase C	Zone 3	140.38%	0.11%	1.367 s	2.55%
6	Three Phase ABC	Zone 2	80.24%	0.94%	0.850 s	2.04%

Figures below shows the fault currents and voltages obtained from the plot of data saved in the “OpWrite” file extracted from simulator at the end of the simulation of each fault. The event file figures show the response of the relay to the simulation currents and voltages injected to the relay analog inputs, the relay word bits and faults location are shown in these last.

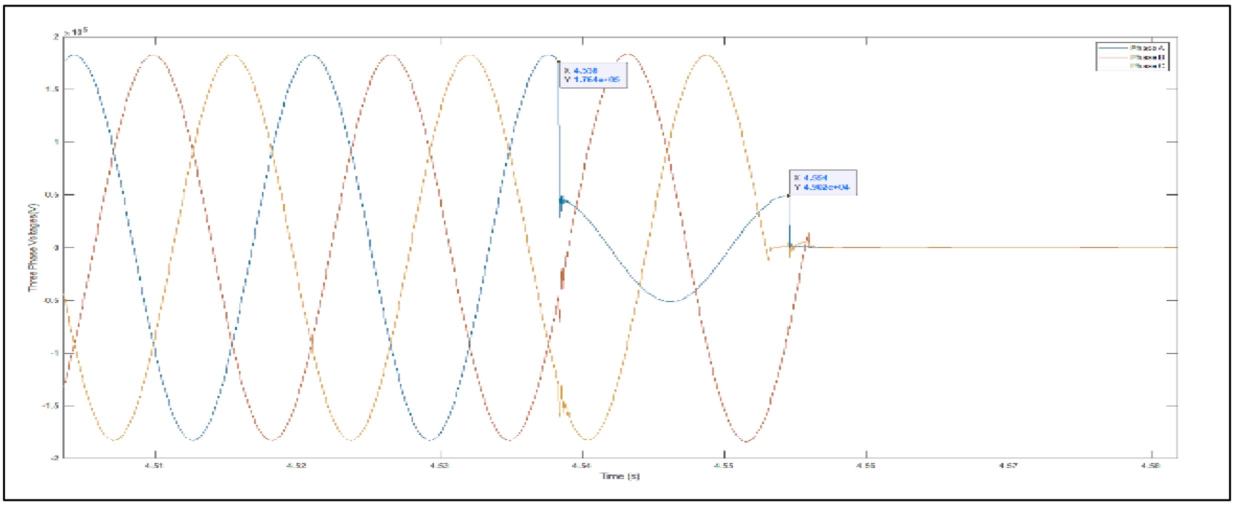

Figure 3.12: Phase A-Ground zone 1 fault Voltages.

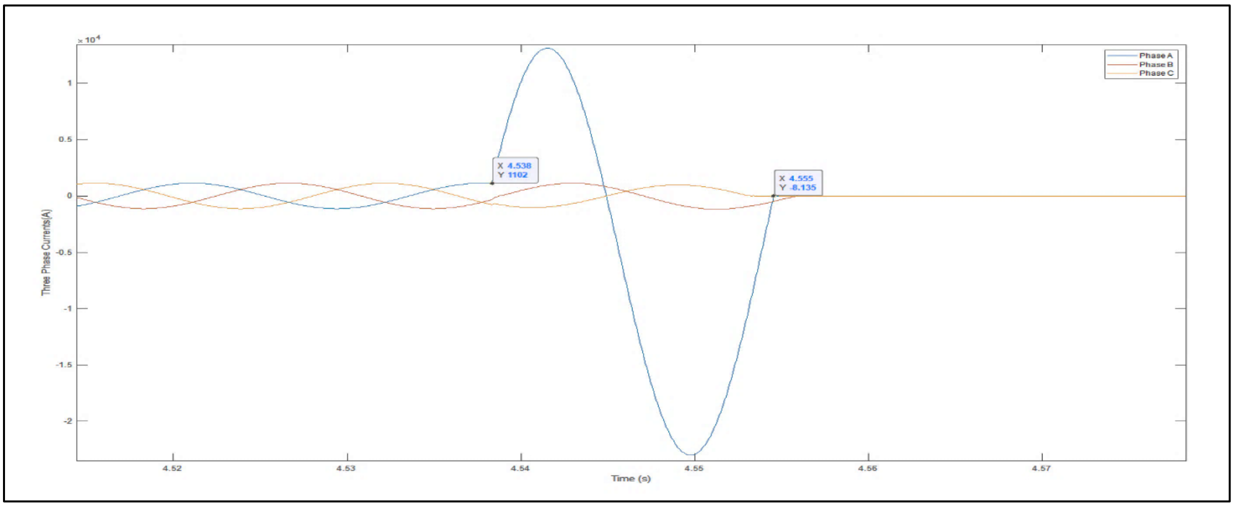

Figure 3.13: Phase A-Ground zone 1 fault Currents.

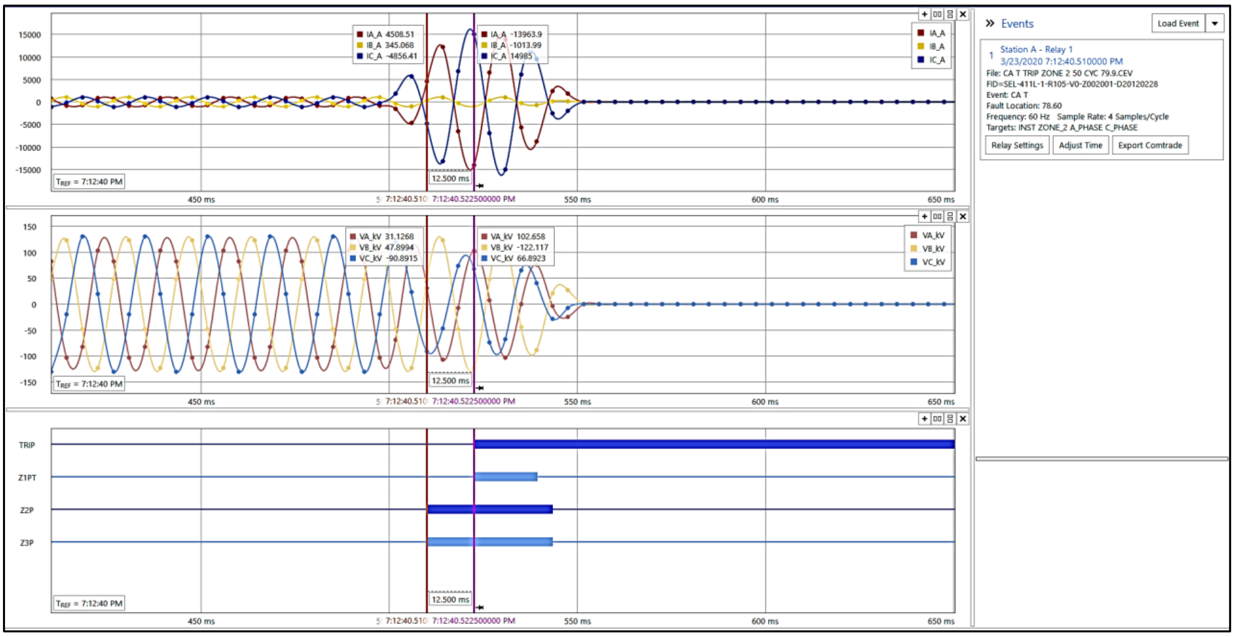

Figure 3.14: Phase A-Ground zone 1 fault Event file.

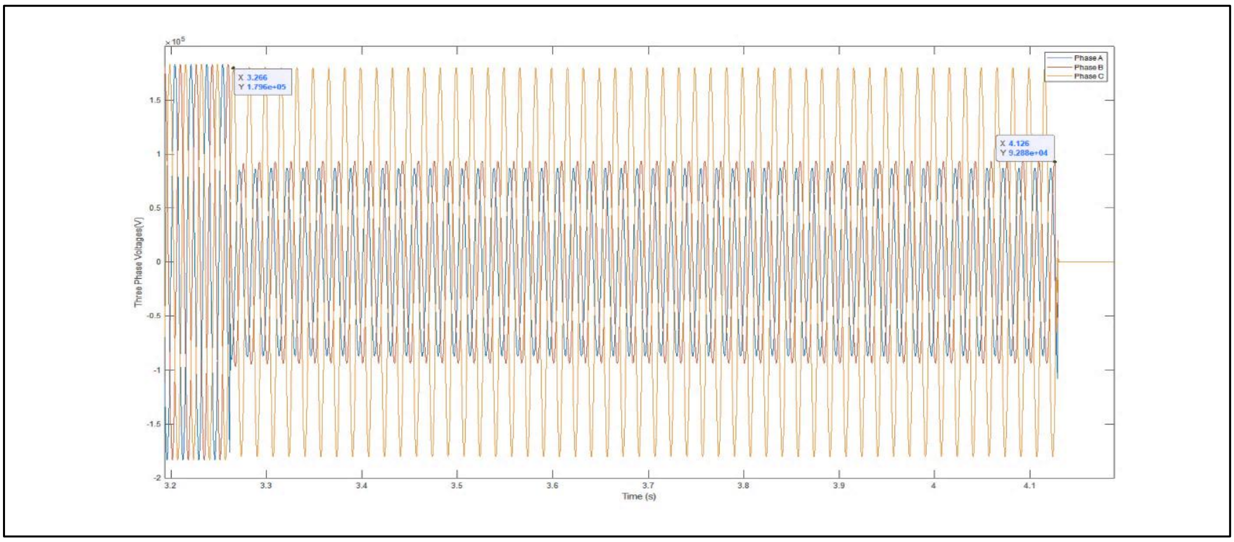

Figure 3.15: Phase A–Phase B-Ground zone 2 fault Voltages.

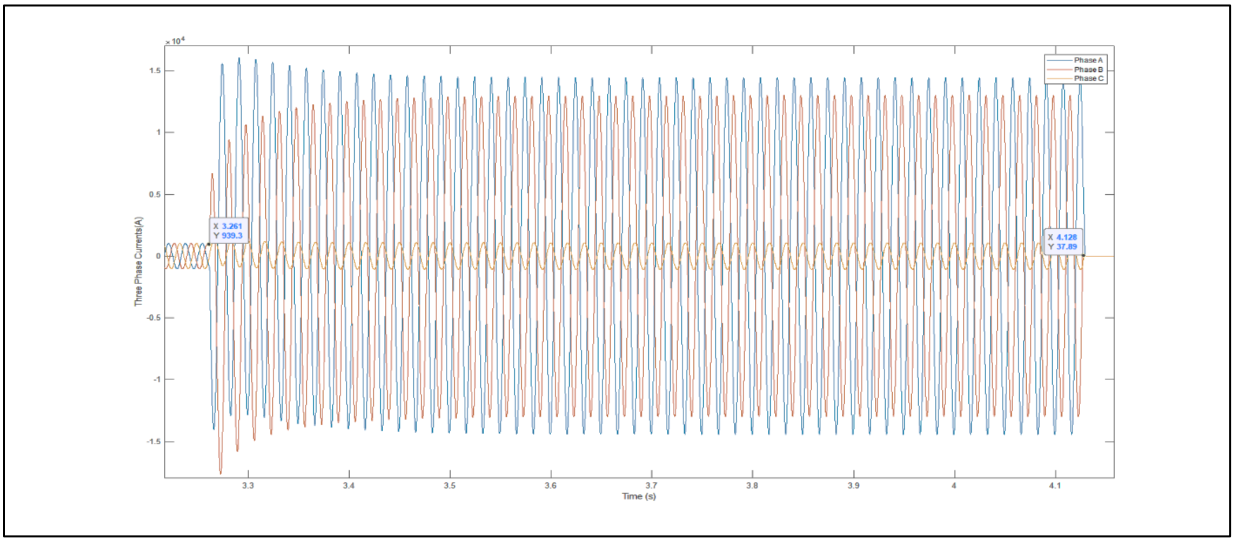

Figure 3.16 Phase A–Phase B-Ground zone 2 fault Currents.

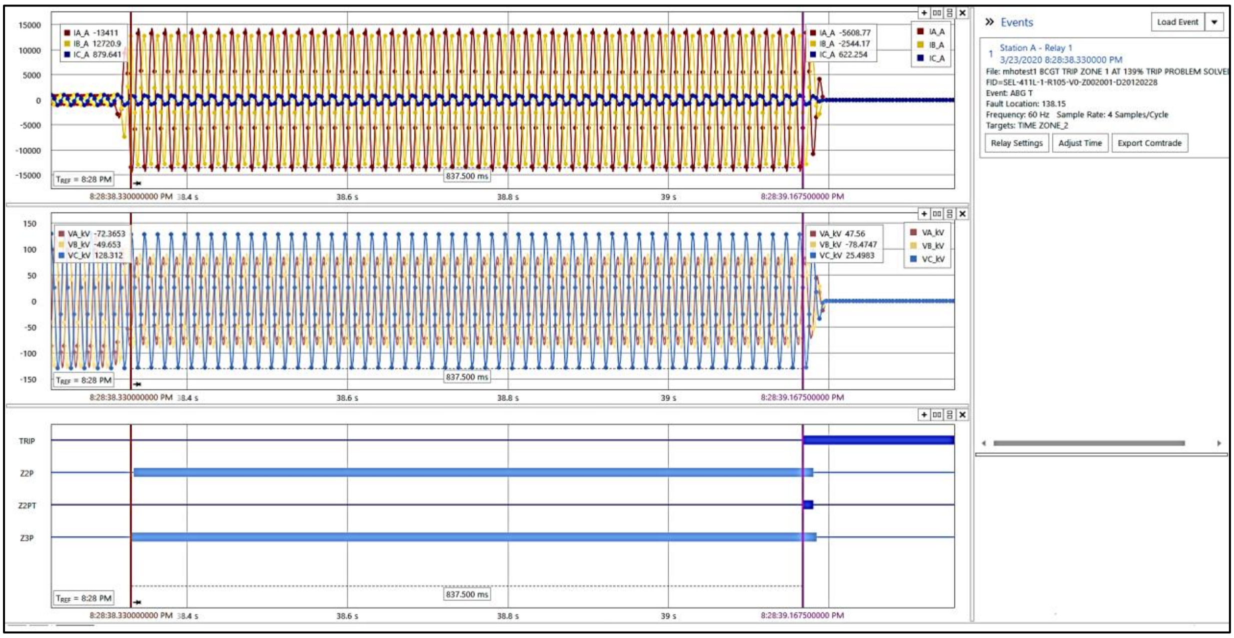

Figure 3.17: Phase A–Phase B-Ground zone 2 fault Event file.

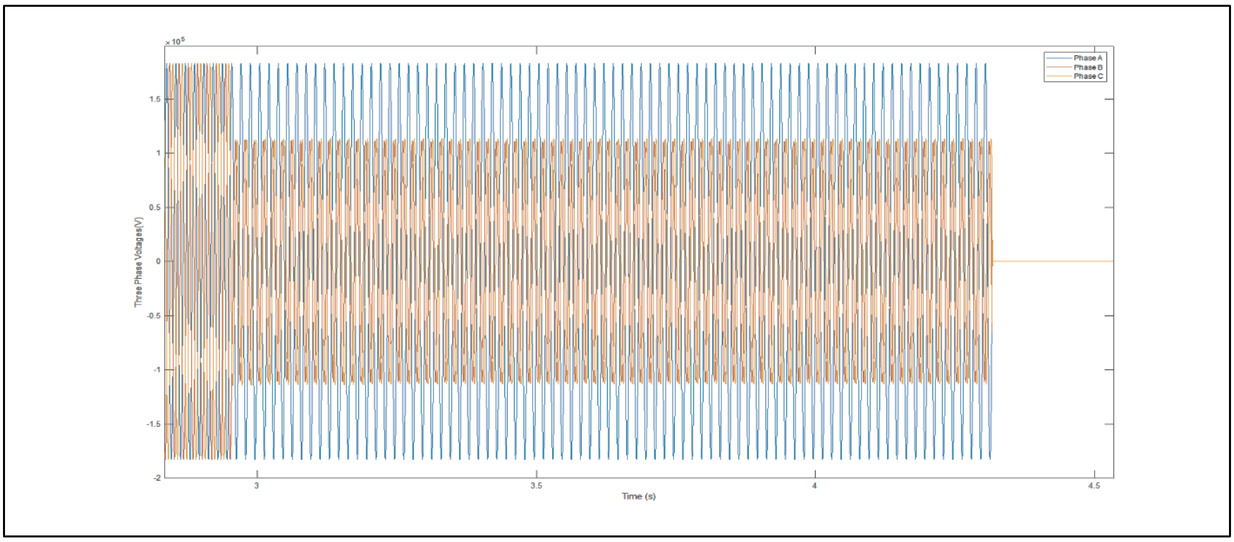

Figure 3.18: Phase B–Phase C zone 3 fault Voltages.

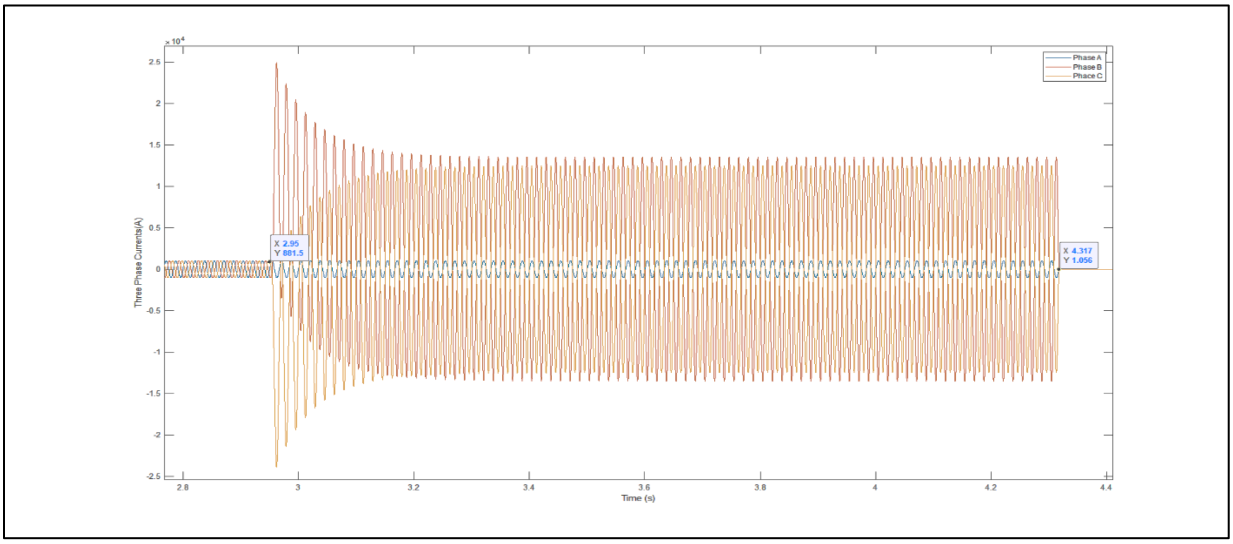

Figure 3.19: Phase B–Phase C zone 3 fault Currents.

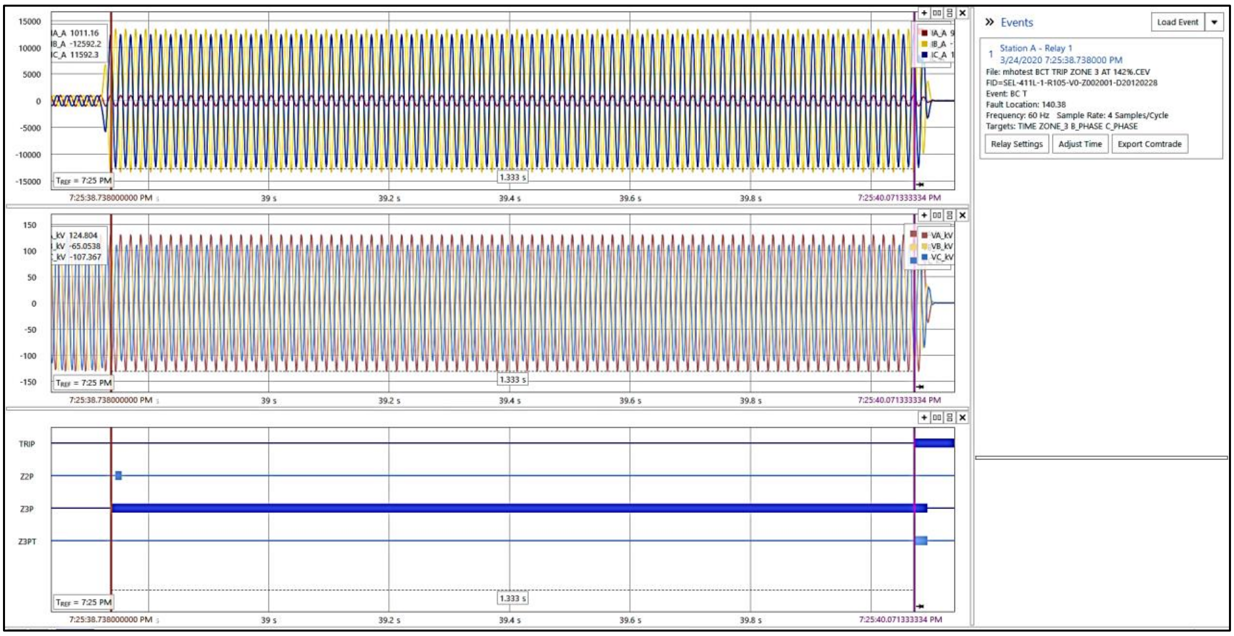

Figure 3.120: Phase B–Phase C zone 3 fault Event file.

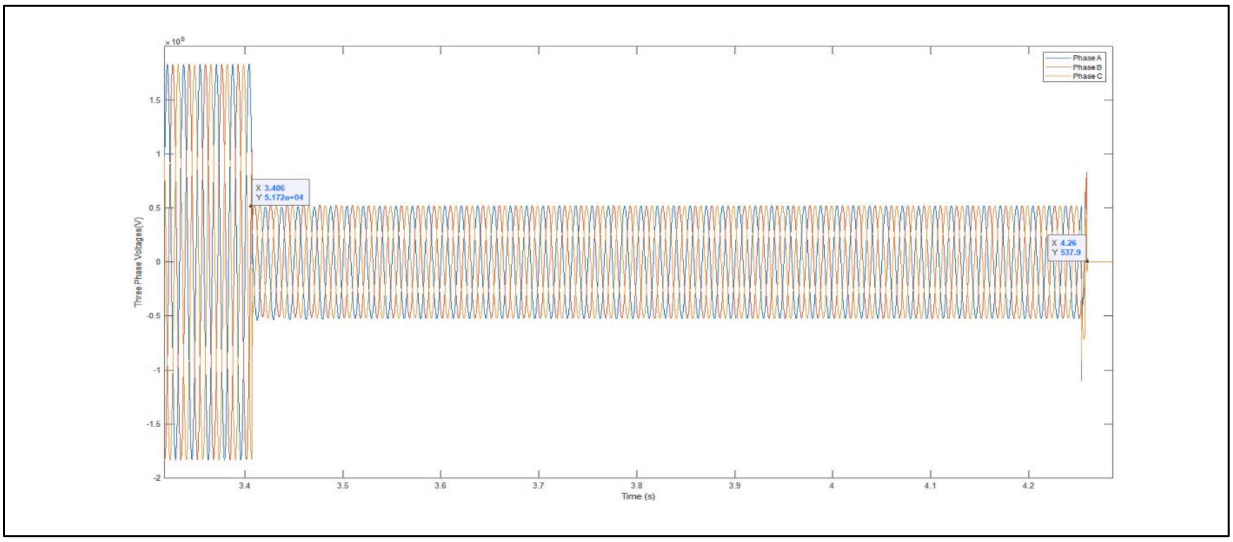

Figure 3.21: Three Phase ABC zone 2 fault Voltages.

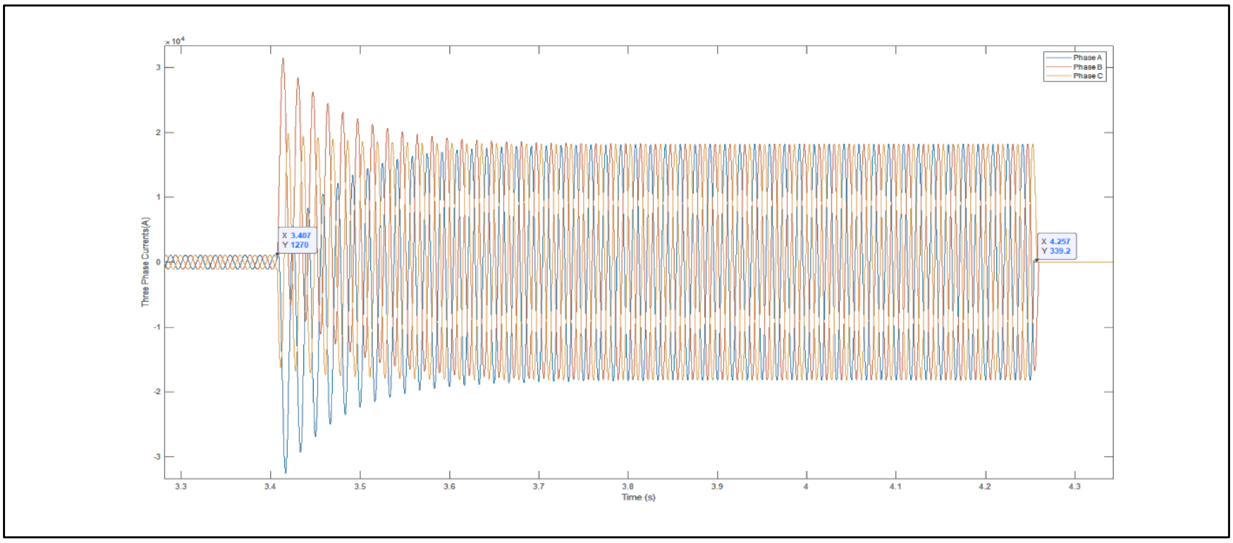

Figure 3.22: Three Phase ABC zone 2 fault Currents.

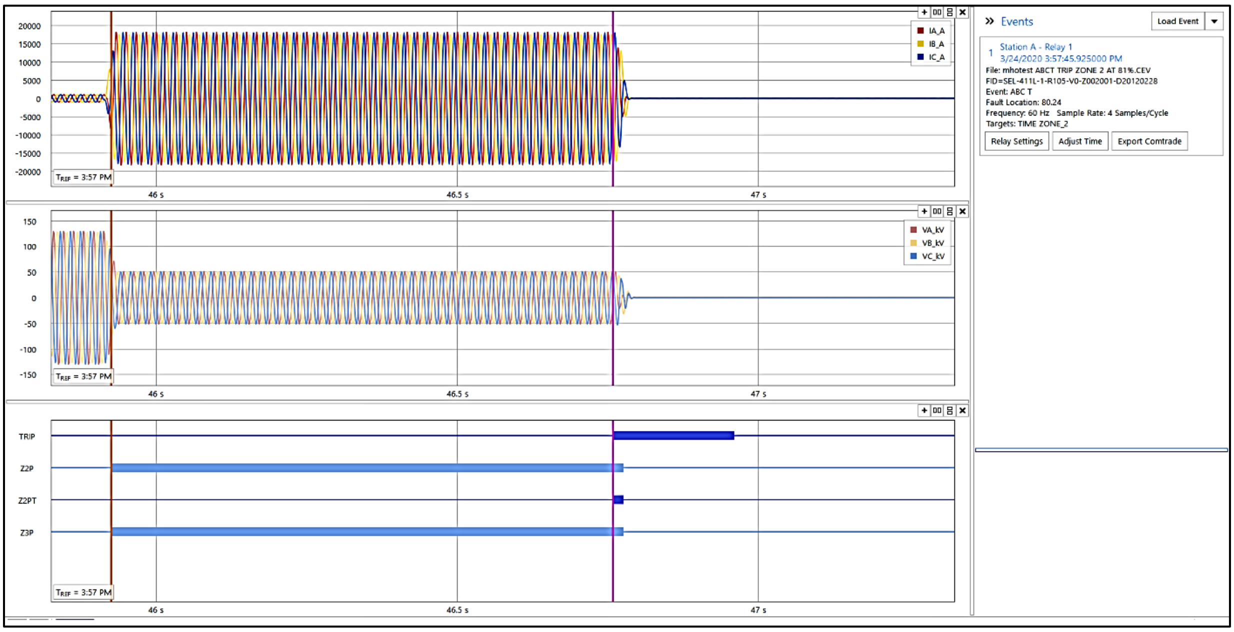

Figure 3.23: Three Phase ABC zone 2 fault Event file.

3.8.2 TOC model test results:

Test currents and voltages are directly injected from the voltage and current sources through the analog outputs of the simulator. **Table 3.3** shows different test values, protection function settings and expected and test trip times:

Table 3.3: TOC relay protection function tests.

Tests	TOC Pickup	TDS	Curve	Primary Test Current	Expected Trip Time	Test Trip Time	Error
1	6.1	1.2	U1	1505 A	3.141 s	3.170 s	0.92%
2	6.1	1.2	U4	2505 A	2.190 s	2.201 s	0.5%
3	6.1	1	U4	2505 A	1.825 s	1.844 s	1.04%

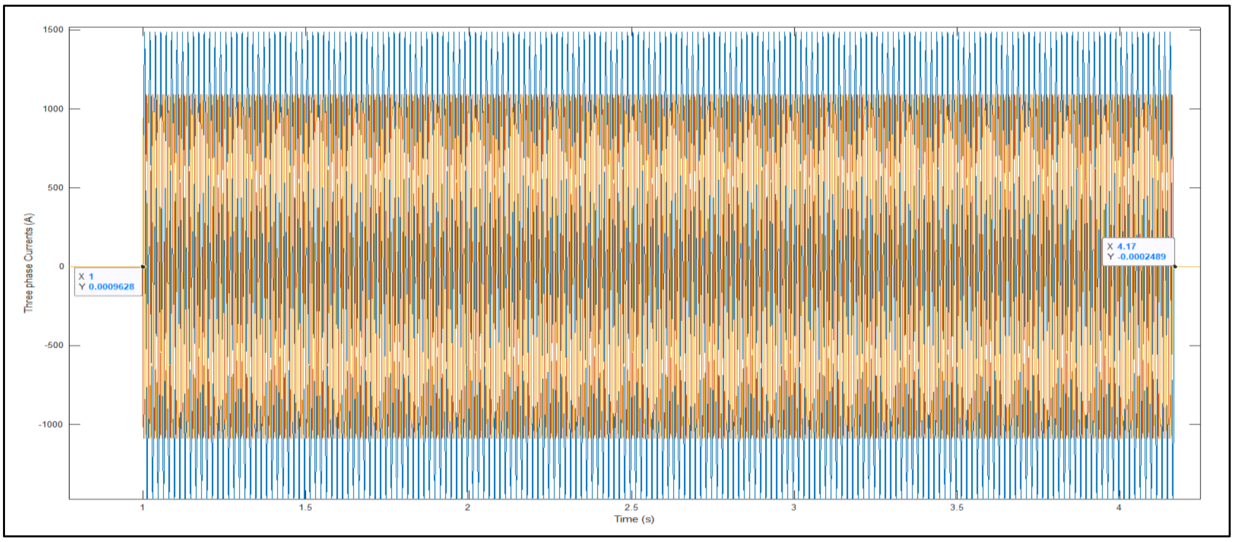

Figure 3.24: 1505A Overcurrent fault with TDS= 1.2, Pickup=6.1 and U1 curve.

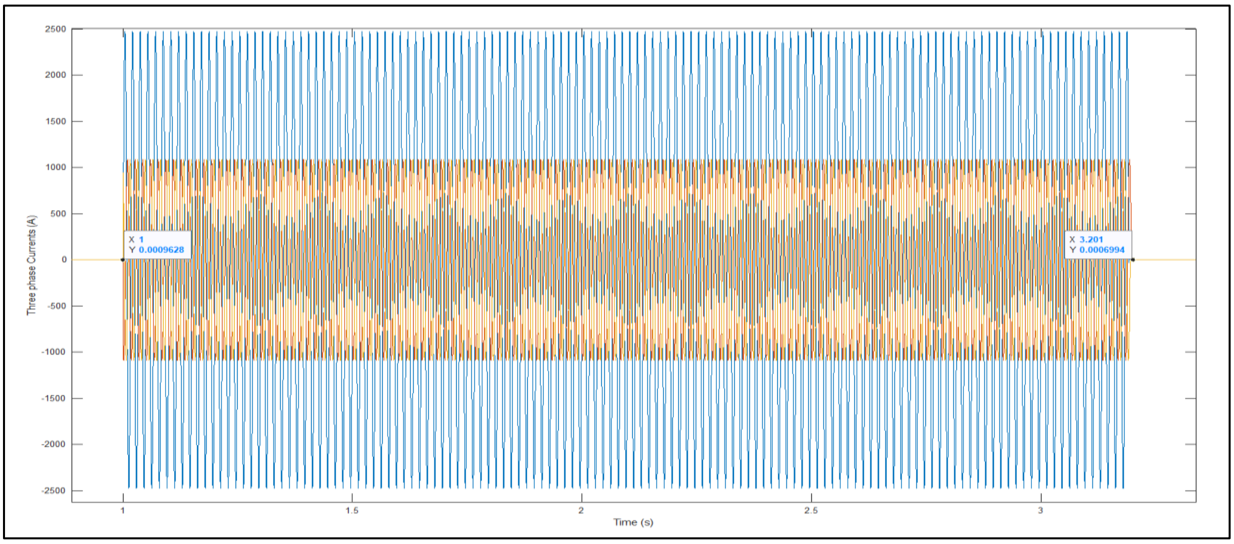

Figure 3.25: 2505A Overcurrent fault with TDS= 1.2, Pickup=6.1 and U4 curve.

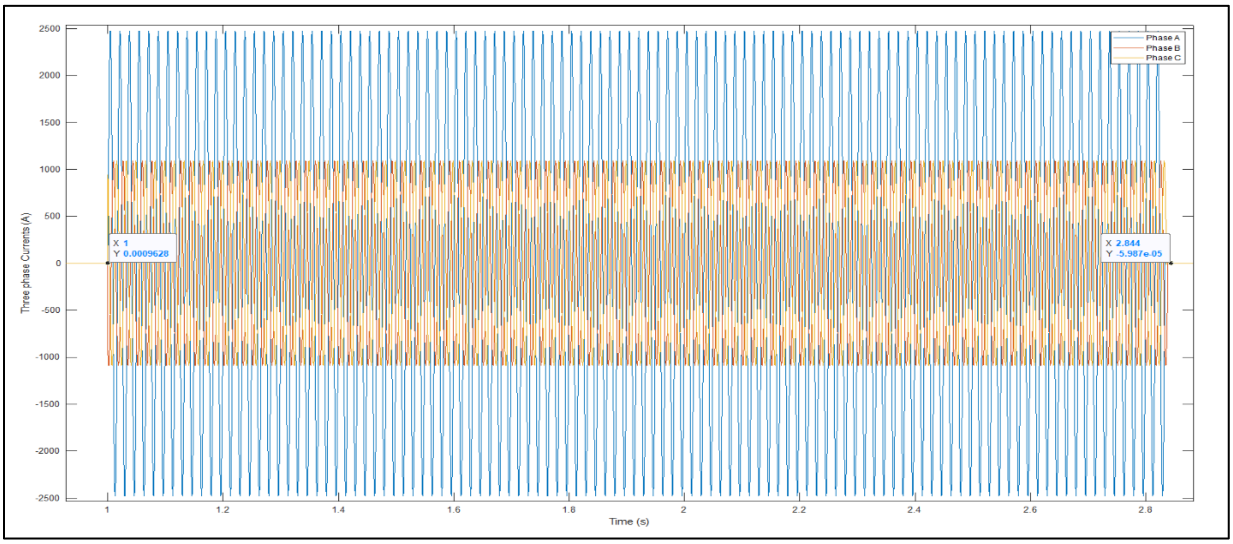

Figure 3.26: 2505A Overcurrent fault with TDS= 1, Pickup=6.1 and U4 curve.

3.8.3 Meter model test results:

The SEL-735 Power Quality and Revenue Meter is set to be tested with the model described in part 2.5.2. The meter is connected to a Doble F6350 amplifier, with three phase voltages and three phase currents. The model is set to carry out a set of tests numerated by the counter. Test values and meter readings are described in **Table 3.4:**

Table 3.4: Meter model test values and meter readings.

Tests	Voltage Amplitude (V)	Current Amplitude (A)	Power Factor
1	205	2.5	Unity
2	205	5	0.5 Lead
3	205	5	0.5 lag
4	205	5	0.9 lag
5	205	5	0.9 lead

The per-phase active and reactive powers injected to the meter are calculated in **Table 3.5** and **Table 3.6** respectively, while readings of the meter are obtained in the form of an LDP (Load Profile) file. The model is supposed to receive the meter readings through the analog inputs card of the simulator. **Table 3.5** and **Table 3.6** shows the meter readings and the calculated error of each test. **Figure 3.27**, **Figure3.28** and **Figure 3.29** shows 'OpWrite' file voltages and currents of the simulator, instantaneous real and reactive powers injected by the simulator and LDP plot of the meter (or meter readings) respectively.

Table 3.5: Per-phase real powers.

Tests	Simulator Voltage (V)	Simulator Current (A)	Meter Voltage (V)	Meter Current (A)	Simulator Power (W)	Meter Power (W)	Error (%)
1	205.90	2.47	205.22	2.48	508.57	508.94	0.073
2	205.90	4.95	205.17	4.97	509.60	509.85	0.049
3	205.90	4.95	205.26	4.97	509.60	510.07	0.092
4	205.90	4.95	205.26	4.97	917.28	918.13	0.092
5	205.90	4.95	205.21	4.97	917.28	917.90	0.068

Table 3.6: Per-phase reactive powers.

Tests	Simulator Voltage (V)	Simulator Current (A)	Meter Voltage (V)	Meter Current (A)	Simulator Power (VAR)	Meter Power (VAR)	Error (%)
1	205.90	2.47	205.22	2.48	0	0	--
2	205.90	4.95	205.17	4.97	-882.66	-883.08	0.048
3	205.90	4.95	205.26	4.97	882.66	883.47	0.092
4	205.90	4.95	205.26	4.97	444.26	444.67	0.092
5	205.90	4.95	205.21	4.97	-444.26	444.56	0.068

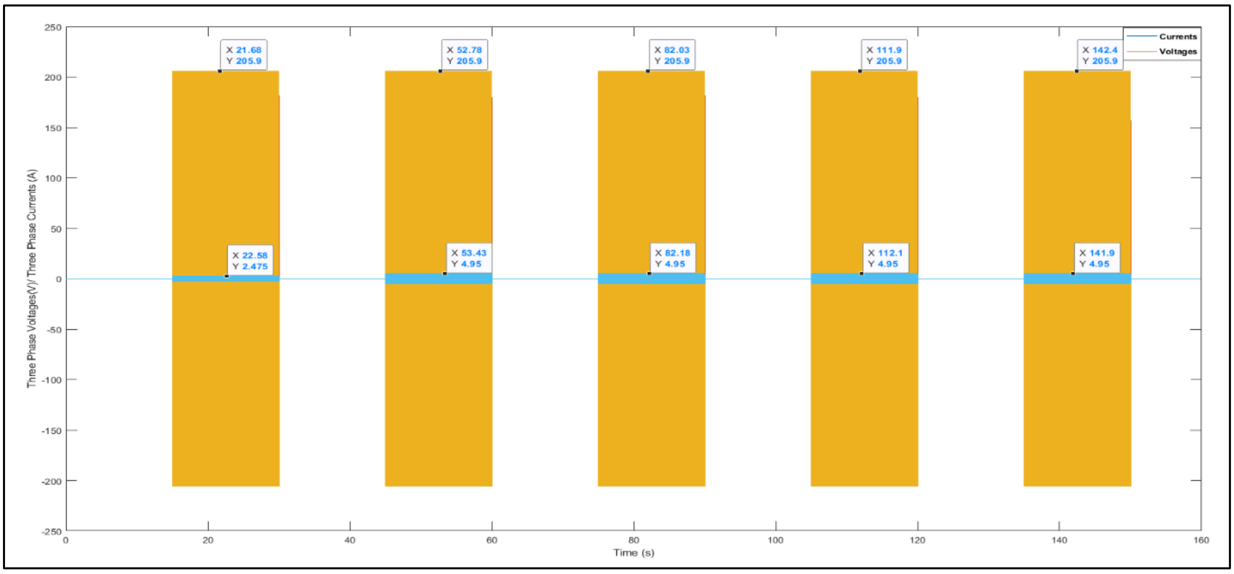

Figure 3.27: Simulator three phase currents and voltages.

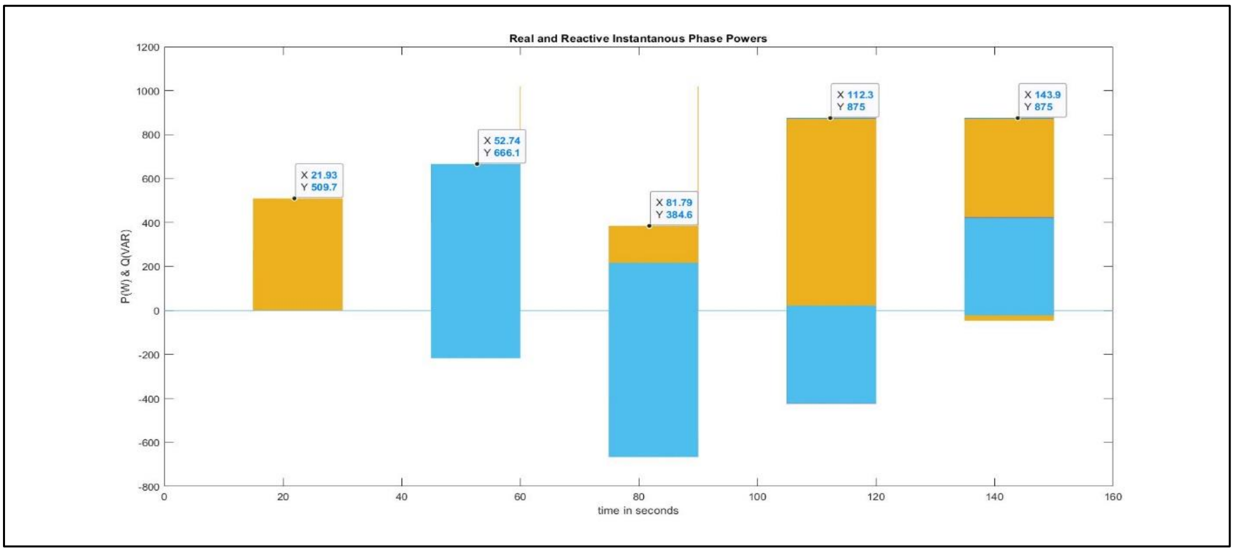

Figure 3.28: Simulator instantaneous real and reactive powers.

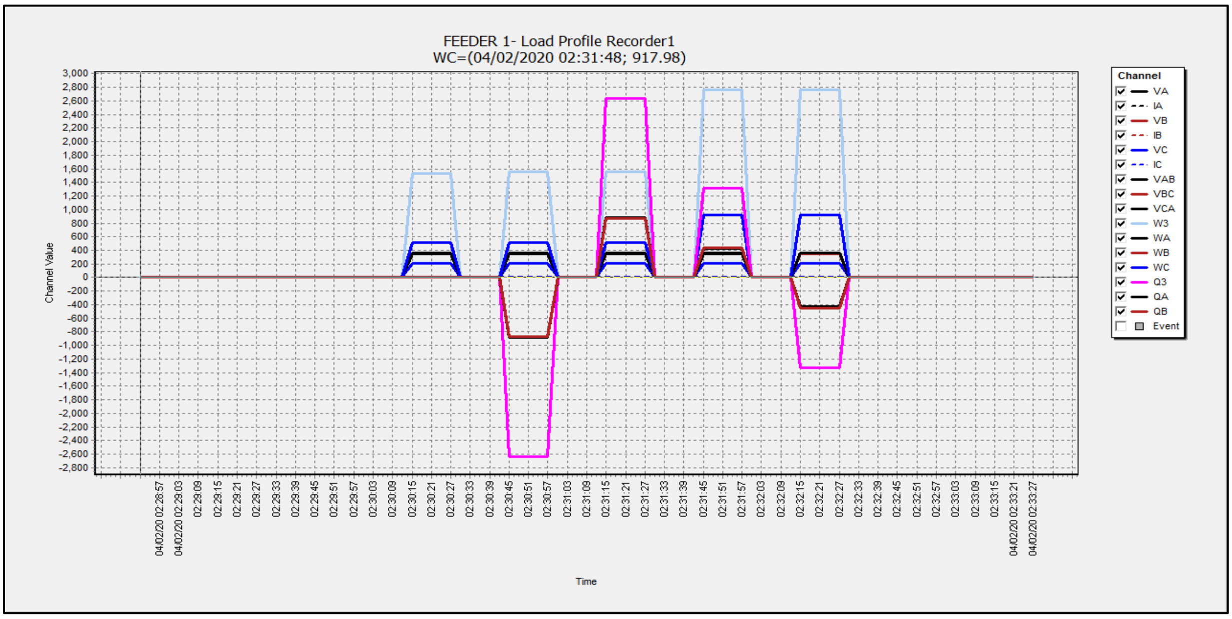

Figure 3.29: LDP file plot from meter HMI.

3.8.4 Test results Discussion:

Analysing test results shown in previous figures and tables can show that results are generally as expected theoretically for protective relays and power meters. From the test results, the following points can be concluded:

- The simulation results comply with the theoretical expectation and results. Relay tripping times are as expected.
- The chosen fault type and location in the Mho distance model can be selected from the three-phase fault block and its location of connection in power system. We carry out one type of fault per simulation.

- Relay response for different type of faults with distance protection indicates the good functional state of the relay.
- The chosen relay pickup, curve type and time dial setting can be selected in the overcurrent function block in the model according to settings of the relay.
- Relays response and timing for the different fault levels and settings of overcurrent protection indicates the good functional state of the relay.
- The meter tests obtained from the IEC or ANSI standards can be added to the ANSI/IEC standards test block.
- The SEL-735 is 0.2 class meter, errors calculated from tests result indicates the compliance of the meter to its class type.
- Better test results of meter can be obtained by carrying out tests according to standards conditions.

3.9 Conclusion:

This chapter has dealt with the experiments and tests carried out to test protective relays and power meters. The SEL-411L and SEL-487E relays and SEL-735 meter are tested.

In this chapter we have explained the main steps for simulating MATLAB/Simulink based model on the RT-LAB OP5600 simulation platform. Configuration, Edition, Preparation, Compilation, Execution and Collection phases must be applied with order and with no error to carry out the tests.

This chapter discussed the test results of the protective relays and power meters. The test results show the well working states of the devices. These tests are tests applied in testing and commissioning of the power system devices.

Chapter 4: General Conclusion & Future Work

4.1 General Conclusion:

The main objective of this thesis was to test and evaluate the performance of the protective relays and power meter with Opal RT-Lab real time simulator, with a MATLAB/Simulink based model were we simulate the power systems for testing protection relays with real time testing Hardware-In-the-Loop method and designing a test circuit for the power meter to apply the IEC/ANSI standards test to ensure full compliance of devices to the standards.

Real time measurements of power system voltages and currents are crucial for real time testing of protection devices, in this thesis, the Opal-RT OP5600 simulator platform is used to provide test voltages and currents in real time that can be injected directly to the connected hardware. Furthermore, Real time simulation provides three test states, pre-fault, fault and post-fault that are almost similar real case states of power system faults.

Building MATLAB/Simulink model with power system parameters can lead to simulating real power system analysis. The MATLAB software is one of the mostly used software for simulation with its ability of calculation and estimation of power system flow of power and measurements.

Power meters and quality revenue devices can be tested using a MATLAB/Simulink model provided with the standards test to ensure compliance of the meters. The Meter model can be configured with all different tests and tested at once.

4.2 Future Work:

Developing models with large power systems and all protections function was one of the major objectives of this study. These models could be used to test all power system protection relays in research works. Moreover, this model can be developed to perform research on the renewable energy and HVDC systems integration with the power grids and testing response of the protection scheme to faults on any part of these systems. This model can be developed to perform various studies on protection of the renewable energy and HVDC grids.

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[12] https://selinc.com/products/5030/

[13] Kunal K. Joshi, M. R. Hans, ‘Development of Mho Type Distance Relay for Protection of Long Transmission Line using MATLAB/Simulink Environment’, International Journal of Engineering Research & Technology IJERT 2016, ISSN:2278-0181, Vol. 5 Issue 04, April 2016.

Appendix A: PF311-249_hardware_overview_rev4_PF314-098

Appendix B: SEL-411L Settings

Group 1
Line Configuration
CTRW := 2800 CTRX := 2800 PTRY := 3000.0 VNOMY := 115
PTRZ := 3000.0 VNOMZ := 115 Z1MAG := 3.29 Z1ANG := 87.93
Z0MAG := 8.98 Z0ANG := 76.05 EFLOC := Y
Relay Configuration
E87L := N E21MP := 3 E21XP := N E21MG := 3
E21XG := N ECVT := N ESERCMP := N ECDTD := N
ESOTF := N EOOS := N ELOAD := N E50P := N
E50G := N E50Q := N E51 := N E81 := N
E27 := N E59 := N E32 := AUTO ECOMM := N
EBFL1 := N E25BK1 := N E79 := N EMANCL := N
ELOP := N EDEM := N EADVS := N
Mho Phase Distance Element Reach
Z1MP := 2.63 Z2MP := 4.60 Z3MP := 7.23
Phase Distance Element Time Delay
Z1PD := 0.000 Z2PD := 50.000 Z3PD := 80.000
Mho Ground Distance Element Reach
Z1MG := 2.63 Z2MG := 4.60 Z3MG := 7.23
Zero-Sequence Compensation Factor
k0M1 := 0.486 k0A1 := -13.30
Ground Distance Element Time Delay
Z1GD := 0.000 Z2GD := 50.000 Z3GD := 80.000
Zone/Level Direction
DIR3 := F
Directional Control Element
ORDER := 'QV'
50FP := 0.60 50RP := 0.40 Z2F := 1.64 Z2R := 1.75
a2 := 0.10 k2 := 0.20 Z0F := 4.49 Z0R := 4.59
a0 := 0.10
E32IV := 1
Pole Open Detection
EPO := 52 SPOD := 0.500 3POD := 0.500
Fault Locator
LLR := 100.00
Trip Logic
TR := Z1GT OR Z1PT OR Z2GT OR Z2PT OR Z3GT OR Z3PT
DTA := NA
DTB := NA
DTC := NA
BK1MTR := OC1 OR PB12PUL
ULTR := TRGTR
ULMTR1 := NOT (52AA1 AND 52AB1 AND 52AC1)
TOPD := 2.000 TULO := 3 Z2GTSP := N 67QGSP := N
TDUR1D := 6.000 TDUR3D := 12.000
E3PT := 1
E3PT1 := 1
ER := R_TRIG Z2P OR R_TRIG Z2G OR R_TRIG 51S01 OR R_TRIG Z3P OR \
R_TRIG Z3G
Global
General Global Settings

```
SID     := 'Station A'
RID     := 'Relay 1'
NUMBK   := 1
BID1    := 'Breaker 1'
NFREQ   := 60       PHROT   := ABC
FAULT   := 50P1 OR 51S01 OR Z2P OR Z2G OR Z3P OR Z3G OR 87LP OR \
           87LQ OR 87LG
Global Enables
EDCMON  := N        EICIS   := N        EDRSTC  := N        EGADVS  := N
EPMU    := N
Control Inputs
IN2XXD  := 0.1250
Settings Group Selection
SS1     := 1
SS2     := 0
SS3     := 0
SS4     := 0
SS5     := 0
SS6     := 0
TGR     := 180
Time-Error Calculation
STALLTE := NA
LOADTE  := NA
Current and Voltage Source Selection
ESS     := N
Time and Date Management
DATE_F  := MDY      IRIGC   := NONE     UTCOFF  := -8.0
BEG_DST := '2,2,1,3'
END_DST := '2,1,1,11'
DNP
EVELOCK := 0        DNPSRC  := UTC
Output
Interface Board #1
OUT201  := 3PT OR TRIP
OUT202  := NA
OUT203  := NA
OUT204  := NA
OUT205  := NA
OUT206  := NA
OUT207  := NA
OUT208  := NA
OUT209  := NA
OUT210  := NA
OUT211  := NA
OUT212  := NA
OUT213  := NA
OUT214  := NA
OUT215  := NA
Protection 1
1: PLT01S := PB1_PUL AND NOT PLT01 # 87L ENABLED
2: PLT01R := PB1_PUL AND PLT01
3: PLT02S := PB2_PUL AND NOT PLT02 # COMM SCHEME ENABLED
```

4: PLT02R := PB2_PUL AND PLT02
5: PLT04S := PB4_PUL AND NOT PLT04 # RELAY TEST MODE
6: PLT04R := PB4_PUL AND PLT04
7: PLT06S := PB6_PUL AND NOT PLT06 # MANUAL CLOSE ENABLED
8: PLT06R := PB6_PUL AND PLT06
9: PLT07S := PB7_PUL AND NOT PLT07 # RECLOSE ENABLED
10: PLT07R := PB7_PUL AND PLT07
Port 87
87 Channel Enable
E87CH := 2SS
87 Channel Configuration
87PCH := 1 87TADR := 2 87R1ADR := 1
87 Channel Monitoring
87CH1SN := C 87CH1MT := OFF 87CH1MD := OFF 87CH1MA := OFF
87CHTRG := 0
87CHWP := N 87CH1PC := OFF
87 Communications Bits De-bounce Time Delay
87R11PU := 0 87R11DO := 0 87R21PU := 0 87R21DO := 0
87R31PU := 0 87R31DO := 0 87R41PU := 0 87R41DO := 0
Alias
Relay Aliases
(RW Bit or Analog Qty. 7 Character Alias [0-9 A-Z _])
1: EN,"RLY_EN"
2: TLED_1,"INST"
3: TLED_2,"TIME"
4: TLED_3,"COMM"
5: TLED_4,"SOTF"
6: TLED_5,"ZONE_1"
7: TLED_6,"ZONE_2"
8: TLED_7,"ZONE_3"
9: TLED_8,"ZONE_4"
10: TLED_9,"A_PHASE"
11: TLED_10,"B_PHASE"
12: TLED_11,"C_PHASE"
13: TLED_12,"GND"
14: TLED_13,"87L"
15: TLED_14,"87L_LST"
16: TLED_15,"87L_ALM"
17: TLED_16,"N_A"
18: TLED_17,"79_RST"
19: TLED_18,"79_LO"
20: TLED_19,"79_CYC"
21: TLED_20,"25_SYNC"
22: TLED_21,"50PICUP"
23: TLED_22,"51PICUP"
24: TLED_23,"LOPTN"
25: TLED_24,"IRIGLCK"

Appendix C: SEL-487E Settings

Group 1
Relay Configuration
ECTTERM := "T" EPTTERM := "V" E87 := OFF EREF := N
E50 := OFF E51 := 1 E46 := OFF E59 := N
E27 := OFF E81 := N E24 := N EBFL := OFF
EPCAL := OFF EDEM := N
Current Transformer Data
CTRT := 100 CTCONT := Y
Potential Transformer Data
PTRV := 1000 PTCONV := Y PTCOMPV := 0.00 VNOMV := 110
Voltage Reference Terminal Selection
VREFT := OFF
Inverse Time Overcurrent Element 01
51O01 := IMAXTF
51P01 := 1.000000
51C01 := U1
51TD01 := 1.000000
51RS01 := N
51TC01 := PLT09
Under Voltage (27) Element 1
27O1 := VNMINVF 27P1P1 := 20.00
27TC1 := 1
27P1D1 := 10.00 27P1P2 := 15.00
Trip Logic
TRXFMR := 51S01 OR 51T01 OR 271P1T
ULTXFMR := 0
TRT := 51S01 OR 51T01 OR 271P1T
ULTRT := 0
TDURD := 5.000
ER := R_TRIG 87U OR R_TRIG 87R
FAULT := 50SQ1 OR 50TQ1
Close Logic
CLT := LB10
ULCLT := 52CLT
CFD := 4.00
Global
General Global Settings
SID := "Station A"
RID := "Relay 1"
NFREQ := 60 PHROT := ABC
Global Enables
EICIS := N EPMU := N
Control Inputs
IN1XXD := 2.0 IN2XXD := 2.0
Settings Group Selection
SS1 := 0
SS2 := NA
SS3 := NA
SS4 := NA

SS5 := NA
SS6 := NA
TGR := 180
Frequency Estimation
EAFSRC := NA
VF01 := VAV VF02 := VBV VF03 := VCV
Time and Date Management
DATE_F := MDY IRIGC := NONE UTCOFF := -5.0
BEG_DST := "2,2,1,3"
END_DST := "2,1,1,11"
Data Reset Control
RST_DEM := NA
RST_PDM := NA
RST_ENE := NA
RSTTRGT := NA
RSTDNPE := TRGTR
RST_HAL := NA
DNP
EVELOCK := 0 DNPSRC := UTC
Output
Main Board
OUT101 := TRIPT OR 51S01 OR 51T01 OR TRIPS
OUT102 := 0
OUT103 := PCT02Q
OUT104 := PCT04Q
OUT105 := NA
OUT106 := NA
OUT107 := NA
OUT108 := NOT (SALARM OR HALARM)
Interface Board #1
OUT201 := NA
OUT202 := NA
OUT203 := NA
OUT204 := NA
OUT205 := NA
OUT206 := NA
OUT207 := NA
OUT208 := NA
OUT209 := NA
OUT210 := NA
OUT211 := NA
OUT212 := NA
OUT213 := NA
OUT214 := NA
OUT215 := NA

Protection 1
1: # BREAKER S OPEN AND CLOSE CMD
2: PCT01IN := PB1 AND 52CLS #CMD TO OPEN BKR S
3: PCT01PU := 60.000000
4: PCT01DO := 0.000000
5: PCT02IN := PB7 AND NOT 52CLS #CMD TO CLOSE BKR S

6: PCT02PU := 60.000000
7: PCT02DO := 0.000000
8: # BREAKER T OPEN AND CLOSE CMD
9: PCT03IN := PB2 AND 52CLT #CMD TO OPEN BKR T
10: PCT03PU := 60.000000
11: PCT03DO := 0.000000
12: PCT04IN := PB8 AND NOT 52CLT #CMD TO CLOSE BKR T
13: PCT04PU := 60.000000
14: PCT04DO := 0.000000
15: PLT03S := PB3_PUL AND NOT PLT03 # DIRECTIONAL OVERCURRENT ENABLED
16: PLT03R := PB3_PUL AND PLT03
17: PLT04S := PB4_PUL AND NOT PLT04 # BREAKER WEAR LEVELS RESET
18: PLT04R := (PB4_PUL AND PLT04) OR RST_BKS OR RST_BKT
19: PLT09S := PB9_PUL AND NOT PLT09 # ADAPTIVE OVERCURRENT ENABLED
20: PLT09R := PB9_PUL AND PLT09
21: PLT13S := TRXFMR
22: PLT13R := TRGTR
Alias
Relay Aliases
(RW Bit or Analog Qty. 7 Character Alias [0-9 A-Z _])
1: EN,"EN_RLY"