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MASTER

In **Electrical and Electronic Engineering**
Option: **Computer Engineering**

Title:

Design and Implementation of FPGA-Based Power Inverters

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Abstract

This project describes the design, simulation, and implementation of a Field-Programmable Gate Array (FPGA) based single-phase full-bridge voltage source power inverters. The implementation of Sinusoidal Pulse Width Modulation (SPWM) technique is used to compute the switching of pulse widths to drive Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) used as power switches. In the first part, MATLAB/Simulink is used to design and simulate square wave, bipolar, and unipolar inverters. In the second part, Very High-Speed Integrated Circuit Hardware Description Language (VHDL) is used to implement a digital controller housed in an FPGA Cyclone IV family. Quartus II development software is used to synthesize these digital controllers. A prototype is built in the laboratory to validate our work.

Dedication

We would like to dedicate this work to our beloved families and friends, whose unwavering support, encouragement, and understanding have been instrumental in our academic journey.

Acknowledgment

First and foremost, we express our gratitude to Allah for granting us patience, and determination to go through these years. We would like also to extend our gratitude to our project advisor, Dr. BENZEKRI Azzouz, for his invaluable guidance and support throughout the research process. His expertise, feedback, and encouragement have been instrumental in shaping the outcomes of this work. A special thanks go to all those who contributed to the accomplishment of this project.

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Chapter 1

Introduction

1.1. Introduction

DC to AC inverters, also referred to as power inverters, are electronic devices that convert direct current (DC) electricity into alternating current (AC). They are essential in scenarios where AC power is required, but only DC power sources, such as batteries or solar panels, are available [1]. This power conversion enables the utilization of a DC power source to operate AC-powered devices.

DC to AC inverters comprise various components, including a DC input source, an inverter circuit, control electronics, and an AC output stage. The DC input source supplies the initial DC power, which is then processed by the inverter circuit. This circuit employs electronic switches such as Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) and Insulated-Gate Bipolar Transistors (IGBTs) to convert the DC input into an AC output. The control regulates the switching of these switches to generate the desired AC output waveform and frequency. Finally, the AC output stage filters and amplifies the inverter output to meet the desired voltage and power requirements [2].

1.2. Applications of Power Inverters

- **Standalone power systems**: They are used in remote or off-grid locations where connection to the utility grid is limited. DC to AC inverters convert DC power from renewable energy sources like solar panels or wind turbines into AC power, enabling the operation of household appliances and lighting systems [2][3].
- **Emergency power backup**: During power outages or emergencies, DC to AC inverters coupled with batteries provide backup power for critical appliances, medical equipment, and communication systems [4].
- **Renewable energy systems**: In grid-connected renewable energy systems, the DC power from solar panels or wind turbines is converted into AC power using power inverters. This allows energy to be fed into the utility grid or used locally to offset electricity consumption [4].
- **Electric vehicle charging**: DC to AC power converters are used in electric vehicle (EV) charging stations to convert AC power from the grid into DC power for charging the vehicle's battery. They are also employed onboard chargers for converting AC power from residential outlets into DC power for EV charging [2][4].
- **Industrial applications**: DC to AC inverters are utilized in various industrial settings, including motor drives, uninterruptible power supplies (UPS), welding equipment, and

adjustable speed drives. These applications require AC power to operate, while DC power sources offer advantages such as efficiency, reliability, or cost-effectiveness [2].

- **Telecommunications**: In remote or off-grid telecommunication installations power inverters are used to convert DC power from batteries or solar panels into AC power for operating communication equipment like cellular base stations, satellite systems, and microwave links [2].
- **Recreational and marine**: Power inverters are employed in recreational vehicles, boats, and yachts to convert DC power from batteries or generators into AC power for running appliances, entertainment systems, air conditioning units, and other electrical devices [4].

1.3. Voltage Source Inverters Versus Current Source Inverters

1.3.1. Voltage Source Inverters

Figure 1 shows the topology of a voltage source inverter (VSI). This circuit converts DC voltage to adjustable AC voltage using switches (e.g., IGBTs, MOSFETs) and control circuitry. By controlling the switch activation pattern, typically with PWM (which will be covered later), the VSI generates a smooth AC output waveform. The VSI circuit is widely used in applications such as motor drives, renewable energy systems, and uninterruptible power supplies (UPS) [5].

1.3.2. Advantages of Voltage Source Inverters

- Voltage source inverters are easier to control because of the less complex design and fewer components [6].
- Very low conduction losses [6].

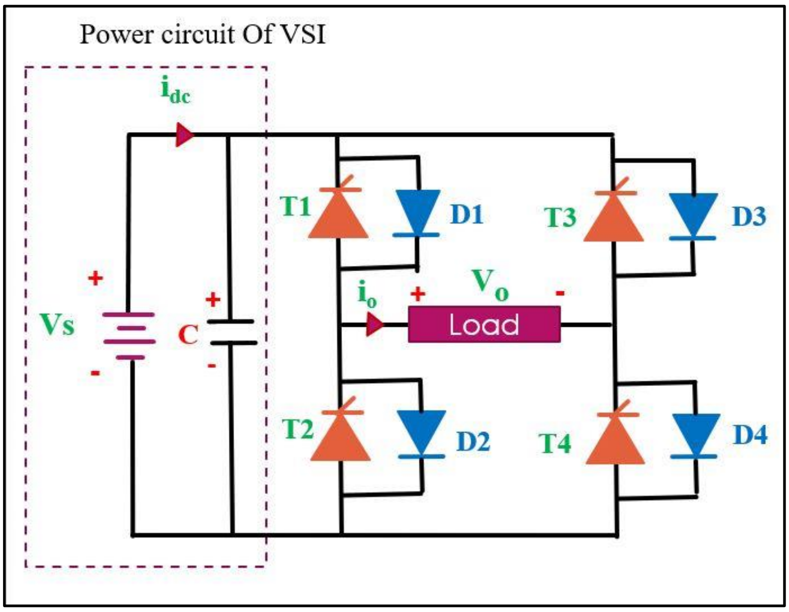


Figure 1. Voltage source inverter topology

Retrieved from: quick-learn.com [7]

1.3.3. Current Source Inverters

The current source inverter (CSI) circuit, as shown in Figure 2, works using a current source which is obtained by a voltage source and a large inductor (ideally infinite impedance) connected in series. The switches (usually thyristors) work similarly to the VSI circuit, i.e., controlling the switching pattern to reach the desired waveform in the end. The CSI circuit is used extensively for applications such as induction heating and welding systems [8].

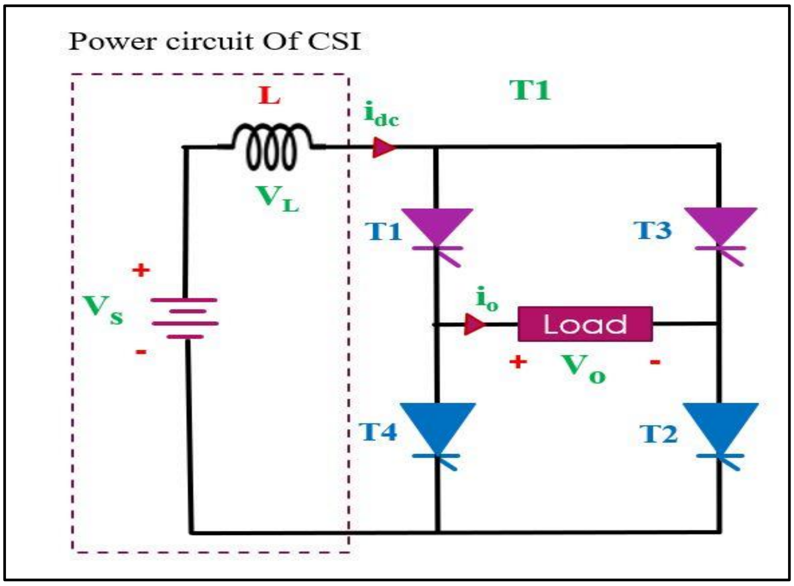


Figure 2. Current source inverter topology

Retrieved from: quick-learn.com [7]

1.4. Power Inverters Topologies

1.4.1. Single-Phase Topologies

1.4.1.1. Single-Phase Half-Bridge Topology

The single-phase half-bridge inverter is a widely used configuration that consists of two switches arranged in a half-bridge configuration as shown in Figure 3. It converts DC input voltage into AC output through a precise control of the switches states. This topology is known for its simplicity and versatility in generating AC power from DC sources. Recent advancements have improved performance and efficiency, resulting in higher switching frequencies, reduced losses, and enhanced reliability. The half-bridge inverter finds applications in renewable energy systems, motor drives, UPS, and electric vehicle powertrains, providing a cost-effective solution with excellent power conversion capabilities [9].

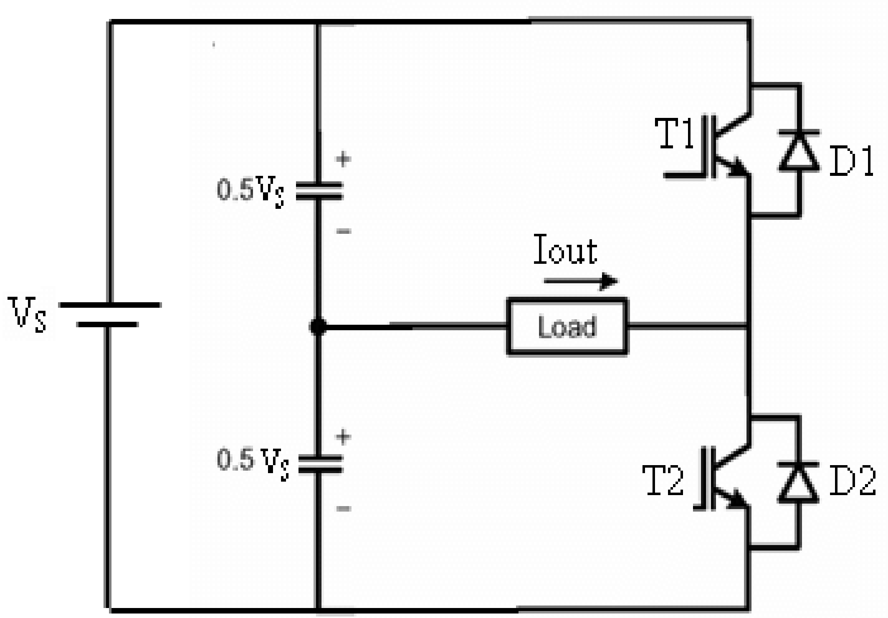


Figure 3. Single-phase half-bridge topology

Retrieved from: Simulation and implementation of two-level and three-level inverters by MATLAB and RT-LAB [9]

1.4.1.2. Single-Phase Full-Bridge Topology

The full bridge configuration, also known as the "full H-bridge" or simply "H-bridge," is also a widely used power electronics topology that consists of four power switching devices, typically MOSFETs or IGBTs. The four switches are arranged in a bridge-like structure, forming two series-connected pairs. Each pair consists of one high-side switch and one low-side switch, and the load is connected between the junction of the two pairs. The full bridge configuration allows for bidirectional current flow and precise control of the output voltage polarity. By selectively switching the high-side and low-side switches, the full bridge can generate an alternating current (AC) output from a direct current (DC) source or control the speed and direction of a motor. This configuration is commonly used in applications such as motor drives, where precise control of motor characteristics is required, as well as in various power conversion systems, including DC to AC inverters and switch-mode power supplies. The full bridge configuration offers flexibility, efficient power conversion, and precise control, making it a popular choice for a wide range of power electronics applications [10].

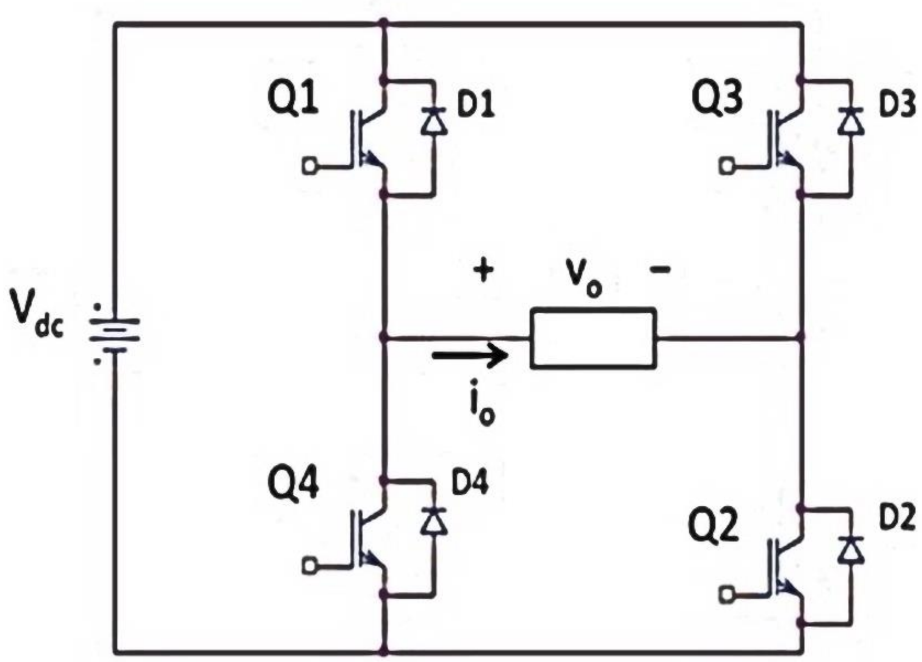


Figure 4. Single-phase full-bridge topology

Retrieved from: 2016 IEEE Student Conference on Research and Development (SCOReD) [10]

1.4.2. Multilevel Topology

The multilevel inverter topology involves the combination of multiple single-phase inverters to achieve higher voltage or power levels. It is commonly used in high-power applications and in situations where the available DC voltage is insufficient for a single inverter. The cascaded configuration can be implemented using either the half-bridge or full-bridge topology for each inverter module. The outputs of the individual inverters are connected in series to obtain the desired output voltage. Cascaded inverters offer scalability and flexibility in terms of voltage and power ratings [11].

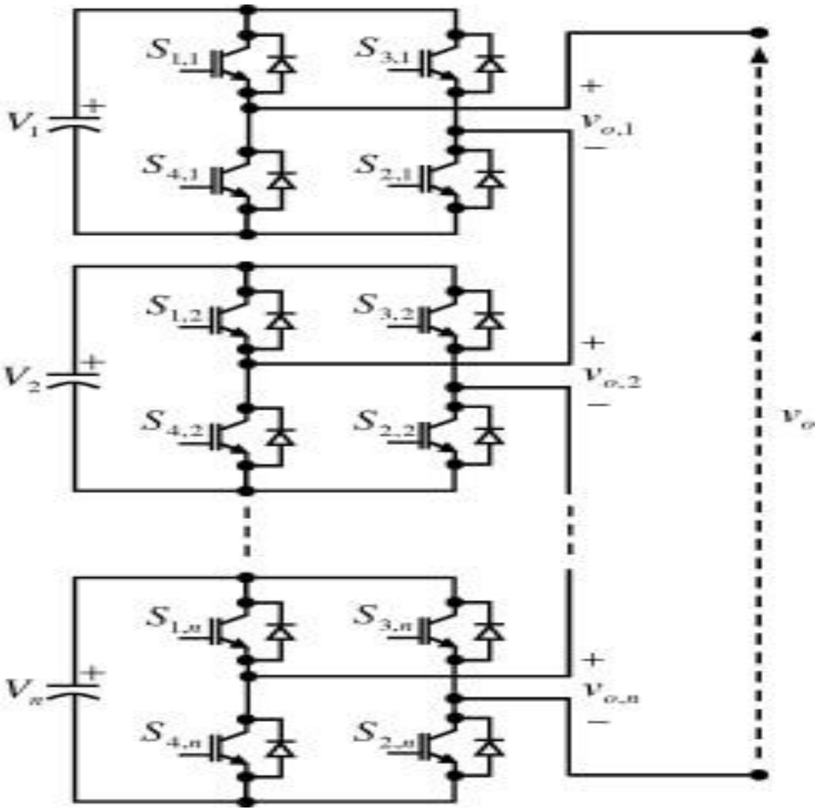


Figure 5. Multilevel topology

Retrieved from: Energy Conversion and Management, Volume 50 [11]

1.4.3. Three-Phase Topology

Figure 6 shows the topology of a three-phase inverter. Three-phase inverters are designed to convert direct current (DC) into three-phase alternating current (AC) waveforms. The topology consists of semiconductor switches, arranged in a specific configuration. By carefully controlling the switching patterns of these switches, the inverter generates three separate AC output voltages, each phase being 120 degrees out of phase with the others. This enables efficient power distribution and utilization in three-phase electrical systems. Three-phase inverters are widely used in motor drives, renewable energy systems, grid-connected applications, and industrial automation, providing reliable and precise power conversion for a variety of industrial and commercial applications [12].

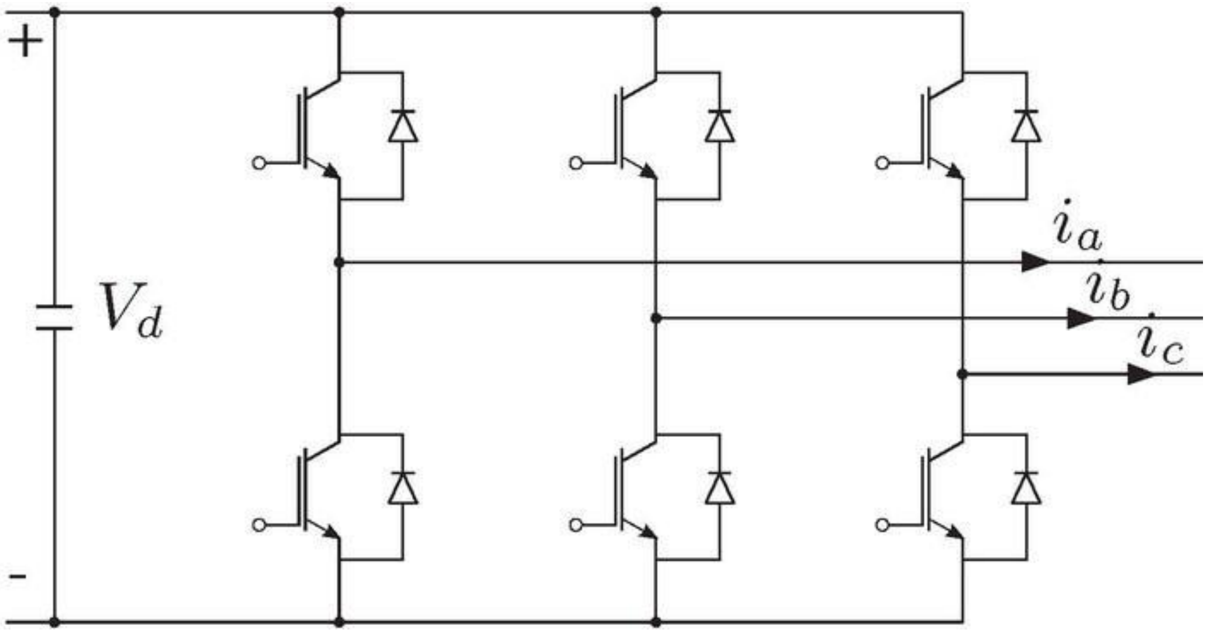


Figure 6. Three-phase topology

Retrieved from: Comparison between a Double Excitation Synchronous Machine and a Permanent Magnet Synchronous Machine According to Various Constant Power Speed Ranges [13]

1.5. Types of Inverters

There are various types of inverters. The types handled in this work are mainly the square wave inverter and the sinusoidal pulse width modulation (SPWM) inverter.

1.5.1. Square Wave Inverter

A square wave inverter generates an output waveform that resembles a square wave. It has a simple design and is relatively inexpensive. However, square wave inverters produce a high amount of harmonic distortion and can cause issues with sensitive electronic devices. Figure 7 illustrates a square wave inverter output waveform (full-bridge configuration) [14].

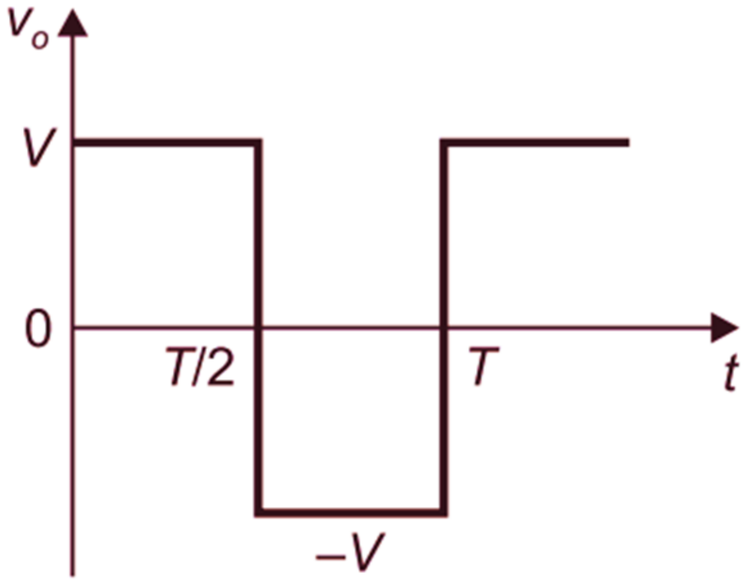


Figure 7. Square inverter output waveform

Retrieved from: electricalworkbook.com [14]

1.5.2. Pulse Width Modulation Inverter

Pulse width modulation is the most popular method of controlling the output voltage of a power inverter. In PWM, the pulses are divided into multiple segments during a half period of the inverter output waveform, and the width of each pulse is controlled. The unfiltered PWM output will have a relatively high THD, but the harmonics will be at much higher frequencies than for a square wave, making filtering easier.

PWM techniques include conventional and advanced methods. Conventional methods contain Single Pulse Width Modulation (SPWM), Multiple Pulse Width Modulation (MPWM), and Sinusoidal Pulse Width Modulation (SPWM). On the other hand, advanced methods contain trapezoidal modulation, staircase modulation, stepped modulation, Harmonic Injected Modulation, delta modulation, and. Space vector pulse width modulation (SVPWM).

In SPWM (Sinusoidal Pulse Width Modulation), control signals are generated by comparing a sinusoidal reference signal (also called a modulating signal) with a high-frequency triangular carrier wave at the intersection points. The width of each pulse varies proportionally to the amplitude of the sine wave. The modulating signal represents the desired waveform shape and determines the amplitude and frequency of the output signal. The carrier, on the other hand, sets the PWM switching frequency. SPWM comprises two switching schemes: bipolar and unipolar.

1.5.2.1. Relevant Consideration

The ratio of the carrier wave frequency to the reference signal frequency is defined as the frequency modulation index (mf):

$$m_f = \frac{f_{carrier}}{f_{reference}} = \frac{f_{tri}}{f_{sine}} \qquad \text{..} (1)$$

Increasing the carrier frequency (i.e., increasing mf) in PWM switching leads to an increase in the frequencies at which harmonics occur. Since high-frequency voltage harmonics are easier to filter out, it is desirable to set the switching frequency as high as possible for better harmonic mitigation. However, one disadvantage of operating at high switching frequencies is the higher losses encountered in the switches used to implement the inverter. Therefore, it is important to consider the trade-off between improved filtering and increased switching losses when selecting the optimal operating frequency for a PWM inverter [15].

The ratio of the reference signal amplitude to the carrier signal amplitude is defined as the amplitude modulation index (ma):

$$m_a = \frac{V_{p,reference}}{V_{p,carrier}} = \frac{V_{p,\sin e}}{V_{p,tri}} \qquad \text{..} (2)$$

If $m_a \leq 1$, the amplitude of the fundamental frequency of the PWM output voltage is linearly proportional to ma thus it can be controlled by ma. This is significant in the case of an unregulated dc supply voltage because the value of ma can be adjusted to compensate for variations in the dc supply voltage, producing a constant-amplitude output.

1.5.2.2. Bipolar PWM Inverter

In Figure 8, the upper and lower switches within a single inverter leg operate in a complementary manner, where one switch is turned on while the other is turned off. As a result, the focus is narrowed down to two independent gating signals, V_{g1}, and V_{g3}, which are derived from the comparison of a sinusoidal modulating wave V_m, with a triangular carrier wave, V_{cr}. The inverter generates terminal voltages, V_{AN}, and V_{BN}, and the resulting output voltage is denoted as $V_{AB} = V_{AN} - V_{BN}$. This specific modulation scheme is referred to as bipolar Pulse Width Modulation due to the oscillation of the V_{AB} waveform between positive and negative DC voltages [16].

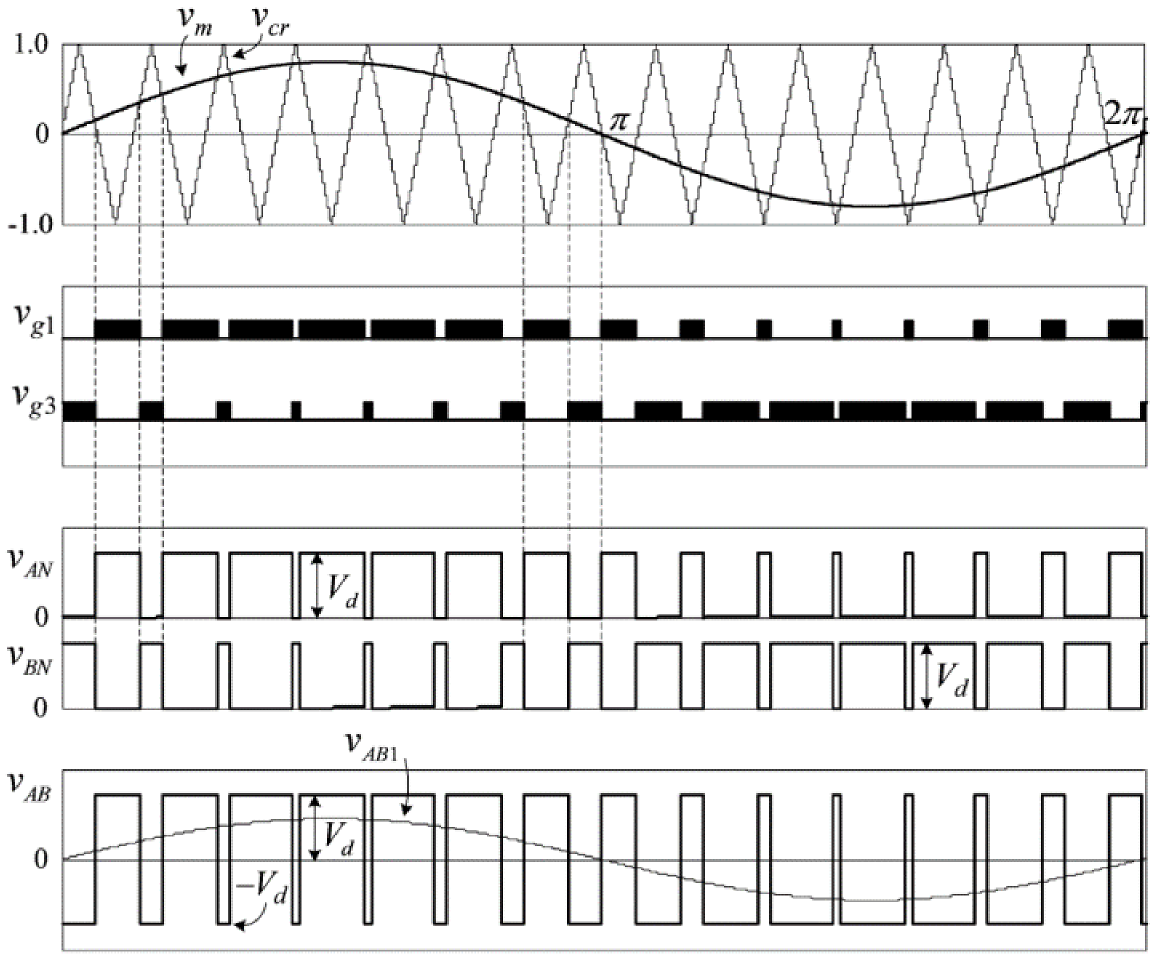


Figure 8. Bipolar modulation technique waveforms

Retrieved from: Unipolar and Bipolar PWM Inverter [16]

1.5.2.3. Unipolar PWM Inverter

The unipolar modulation technique employs two sinusoidal modulating waves, V_m, and V_m-, which have the same magnitude and frequency but are 180 degrees out of phase, as seen in Figure 9. These modulating waves are compared with a common triangular carrier wave, V_{cr}, resulting in the generation of two gating signals, Vg1 and Vg3, for the upper switches S1 and S3. The output voltage of the inverter alternates between zero and $+V_d$ during the positive half cycle, and zero and $-V_d$ during the negative half cycle of the fundamental frequency. This modulation scheme is known as unipolar modulation. The unipolar inverter offers advantages such as reduced switching losses, lower electromagnetic interference (EMI) generation and improved harmonic content [16].

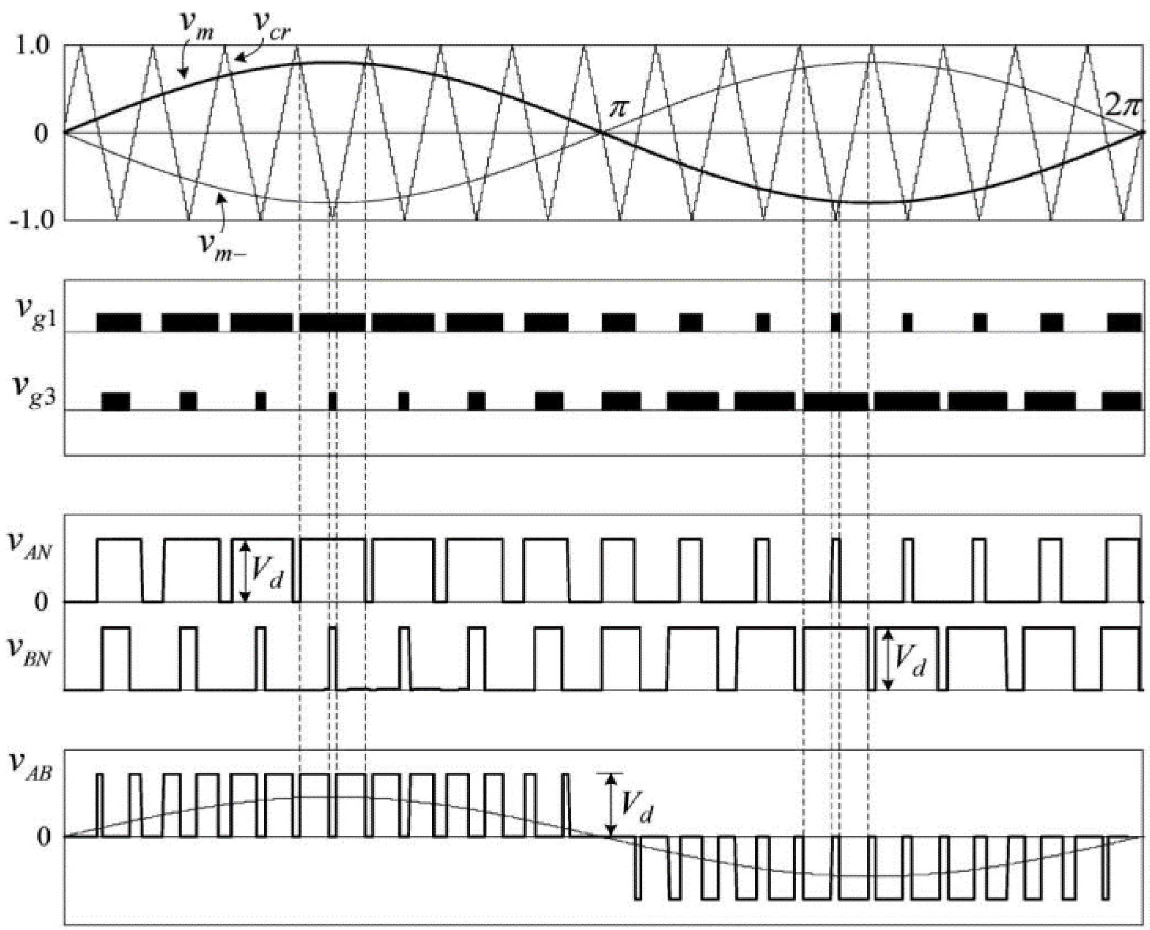


Figure 9. Unipolar modulation technique waveforms

Retrieved from: Unipolar and Bipolar PWM Inverter [16]

1.6. Literature Review

The development of inverters has a rich history dating back to the late 19th century. Visionary inventors such as Charles F. Scott, William Stanley, and Nikola Tesla played pivotal roles in pioneering AC power transmission and the rotary converter, laying the foundation for future advancements in inverter technologies. Scott's experiments with transformer-coupled induction regulators and Stanley's innovations in alternating current systems significantly contributed to the understanding of AC power conversion. Tesla's remarkable inventions, including the polyphase induction motor and his work on high-frequency power, propelled the development of inverter technologies and AC power transmission [17][18]. In the mid-20th century, square wave inverters emerged as early power electronic converters, thanks to the efforts of Frederick Terman, Alan Blumlein, and Donald G. Fink. These inverters utilized switches and transformers to convert DC power into AC power with a square waveform [19]. Such inverters found applications in early UPS systems and standalone power generation, laying the groundwork for future advancements in inverter technology [20]. A significant breakthrough came in the 1970s with the development of Pulse-Width Modulation (PWM) techniques, revolutionizing inverter technology. This advancement greatly enhanced the efficiency and performance of inverters. Among PWM-based carrier techniques, sinusoidal PWM is the most popular. PWM-based inverters gained widespread adoption across various applications, including motor drives, renewable energy systems, and uninterruptible power supplies (UPS) [21]. Many studies were conducted in this area including Muhamad Rusdi, Faizal Arya Samman, and Rhiza S. Sadjad’s research: ”FPGA-Based Electronic Pulse Generator for Single-Phase DC/AC Inverter” where they stated:

> *[22]” This paper is focused on the development of a signal generator Sinusoidal Pulse Width Modulation (SPWM) which is used to control a full wave power switch on a single phase inverter based on a Field Gate Array Programmable (FPGA).”*

A.B. Afarulrazi, M. Zarafi, W. M. Utomo, and A. Zar also contributed with a similar work entitled:” FPGA Implementation of Unipolar SPWM for Single Phase Inverter”, where they stated:

[23]" This project presents development of a Unipolar Sinusoidal Pulse Width Modulation (SPWM) for single phase full bridge inverter using Field Programmable Logic Array (FPGA).

Our project aimed to design and implement a DC to AC power converter utilizing a full bridge configuration, in conjunction with a field-programmable gate array (FPGA) as the control platform as depicted in Figure 10. The full bridge configuration offers several advantages, including improved voltage conversion efficiency, higher power handling capacity, and reduced harmonic distortion. By using the FPGA's flexibility and computational capabilities, precise control of the inverter operation was achieved. The FPGA allowed for the implementation of complex modulation techniques, providing a fine level of control over the output waveform.

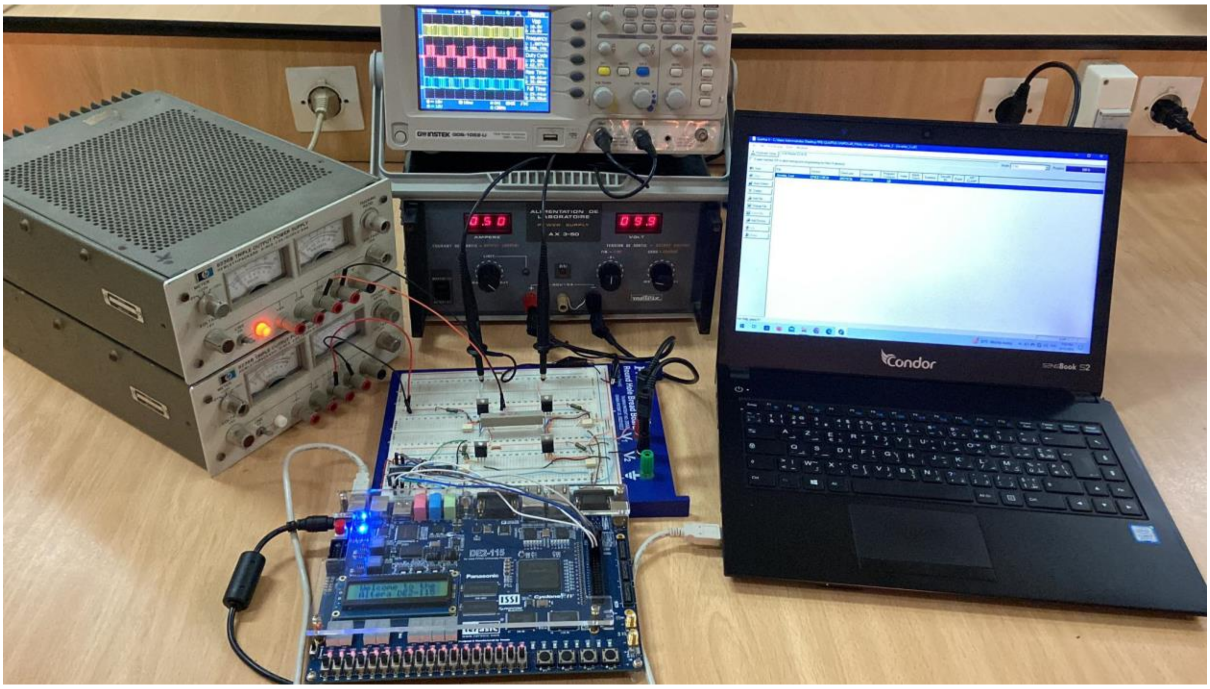


Figure 10. Prototype of a unipolar single phase voltage source power inverter built in the institute laboratory

Chapter 2

Theoretical Background

2.1. Components Overview

2.1.1. IRFZ44N Metal-Oxide-Semiconductor Field-Effect Transistor

Figure 11 illustrates the conventional schematic of a common n-channel Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET), a widely used semiconductor device valued for its ability to regulate current flow in electronic circuits. A MOSFET consists of a three-terminal structure comprising a source, a drain, and a gate. It operates by modulating the conductivity of a semiconductor channel between the source and drain regions via a voltage applied to the gate terminal. This voltage establishes an electric field that controls the flow of current in the channel. MOSFETs offer several advantages, including high switching speed, low power consumption, and excellent noise performance. They find application in a wide range of electronic systems, serving as key components in amplifiers, voltage regulators, power supplies, and digital logic circuits [24].

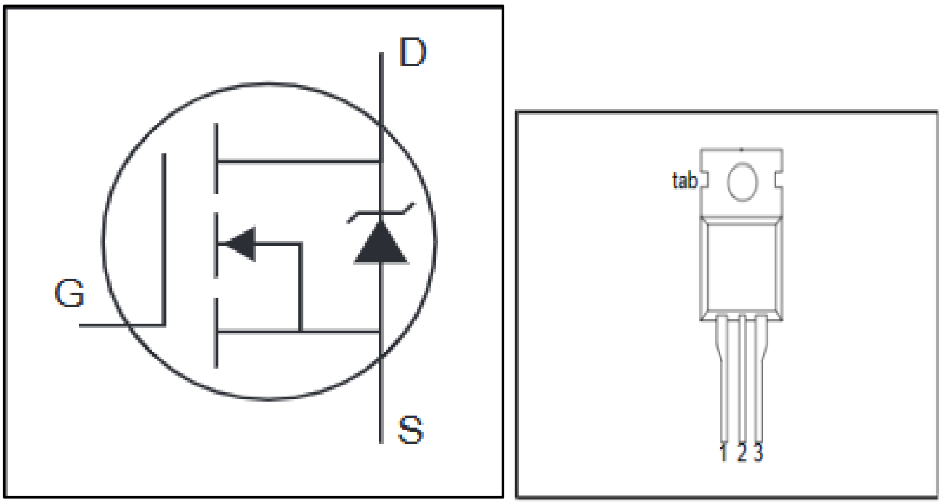


Figure 11. Metal-oxide-semiconductor field-effect transistor schematic

Retrieved from: infineon.com [25]

2.1.2. SN54LS04 Hex Inverter

The SN54LS04 is a popular inverter integrated circuit (IC) belonging to the TTL logic family. As shown in Figure 12, the inverter IC consists of six individual inverters within a single package. It is commonly used in digital logic applications to convert input logic signals into their complementary outputs using the NOT operation. With its reliable performance and compatibility with TTL logic levels, the SN54LS04 is widely used in various electronic projects and educational settings. Its compact design, simplicity, and availability make it a convenient choice for signal inversion and logical complementation needs in digital circuits [26].

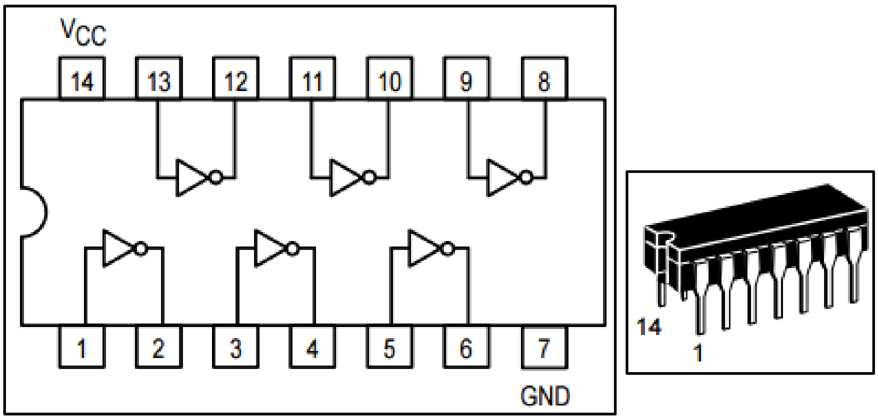


Figure 12. SN54LS04 Hex inverter schematic diagram

Retrieved from: alldatasheet.com [27]

2.1.3. SN54LS240 Buffer

The SN54LS240 illustrated in Figure 13 is a widely used octal buffer/line driver IC in the TTL logic family. It features eight buffer gates with high current drive capabilities. The SN54LS240 is commonly employed for signal buffering and line driving in digital circuits. Its enable input allows for control over the operation of each buffer gate, providing flexibility in signal isolation and transmission [28].

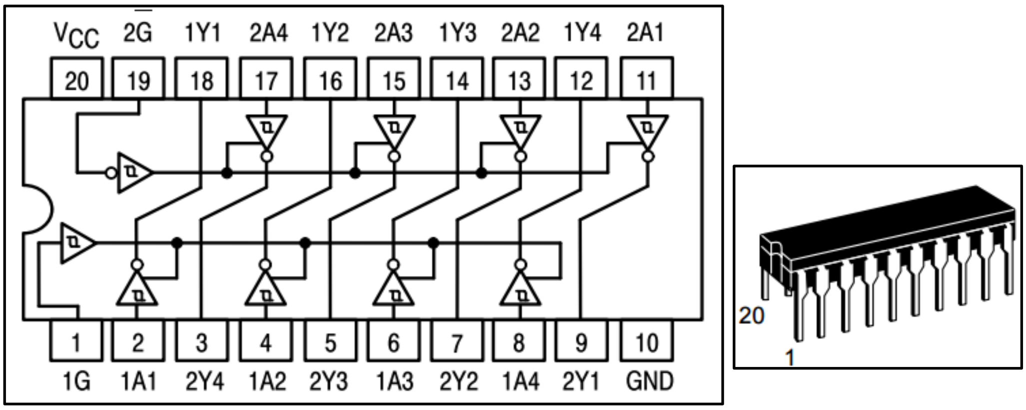


Figure 13. SN54LS240 Buffer schematic diagram

Retrieved from: ti.com [29]

2.1.4. H11D1M Photocoupler

The H11D1M as illustrated in Figure 14 is a commonly used optocoupler IC designed for signal isolation and voltage level shifting applications. It consists of an infrared emitting diode (LED) and a phototransistor within a single package. The LED emits infrared light, which is then detected by the phototransistor, providing electrical isolation between the input and output circuits. The H11D1M optocoupler is known for its reliable performance and fast switching characteristics. It is often used in industrial control systems, communication interfaces, and other applications where electrical isolation and noise immunity are required. With its compact size and ease of integration, the H11D1M is a popular choice for ensuring safe and reliable signal transmission in various electronic circuits [30].

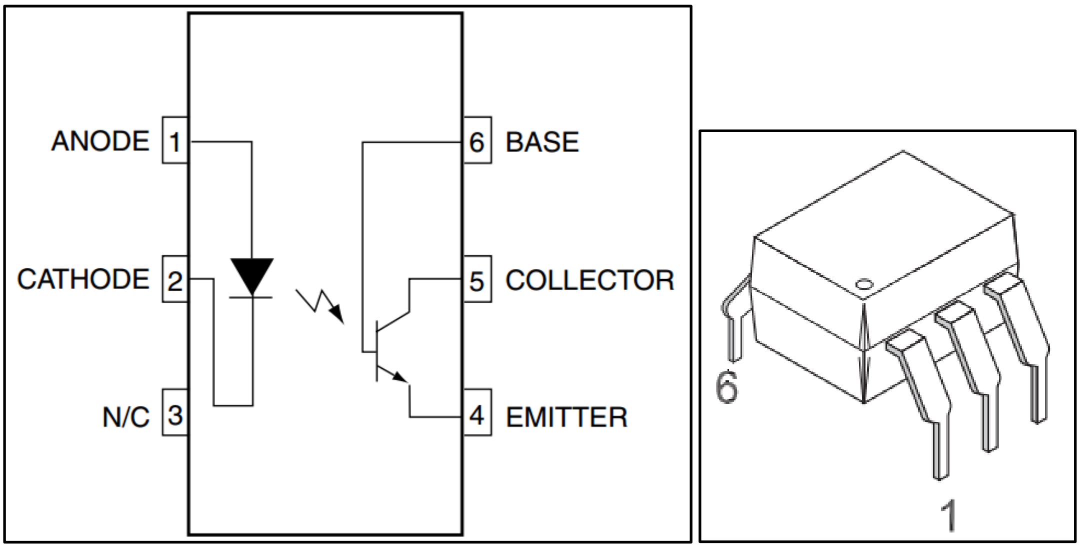


Figure 14. H11D1M Photocoupler schematic diagram

Retrieved from: onsemi.com [31]

2.2. Field-Programmable Gate Arrays

Integrated circuits renowned for their versatility and transformative impact on digital design and implementation. FPGAs comprise an array of configurable logic blocks and programmable interconnects, enabling users to create and deploy customized digital circuits and systems. Unlike fixed Application-Specific Integrated Circuits (ASICs), FPGAs offer the unique advantage of post-manufacturing re-programmability, ensuring adaptability to evolving design requirements. FPGAs offer notable advantages such as high processing speeds, parallel processing capabilities, low power consumption, and the ability to accommodate complex digital functions. Their widespread adoption spans diverse industries including telecommunications, automotive, aerospace, industrial automation, and scientific research. FPGAs empower designers to swiftly prototype and develop innovative solutions, reducing time-to-market while optimizing system performance. By seamlessly handling diverse computational tasks and accommodating evolving design needs, FPGAs have emerged as a pivotal tool in the development of advanced digital systems and embedded applications [32].

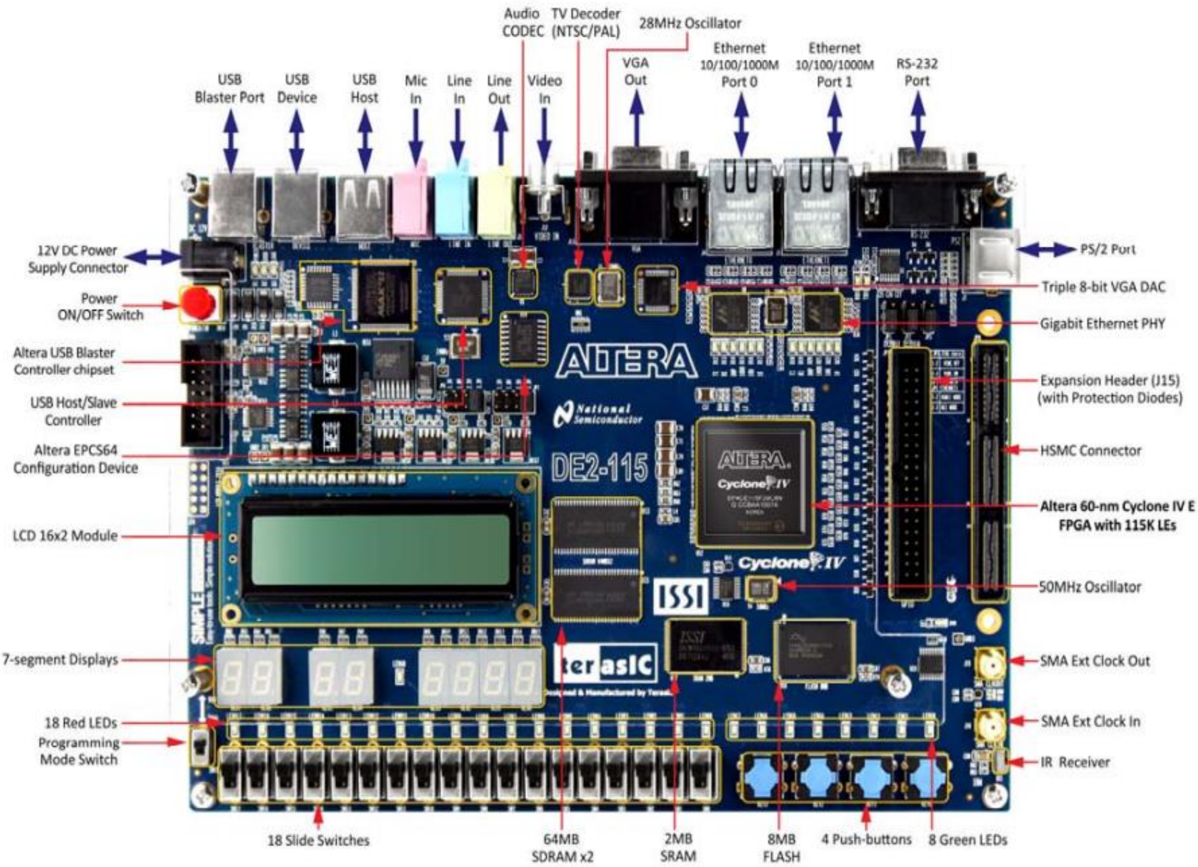


Figure 15. FPGA DE2-115 Cyclone IV board

Retrieved from: DE2-115 User Manual [33]

2.2.1. Field-Programmable Gate Array Hardware

- [33] Altera Cyclone® IV 4CE115 FPGA device
- Altera Serial Configuration device – EPCS64
- USB Blaster (onboard) for programming; both JTAG and Active Serial (AS) Programming
- modes are supported.
- 2MB SRAM
- Two 64MB SDRAM
- 8MB Flash memory
- SD Card socket
- 4 Pushbuttons
- 18 Slide switches
- 18 Red user LEDs
- 9 Green user LEDs
- 50MHz oscillator for clock sources
- 24-bit CD-quality audio CODEC with line-in, line-out, and microphone-in jacks
- VGA DAC (8-bit high-speed triple DACs) with VGA-out connector
- TV Decoder (NTSC/PAL/SECAM) and TV-in connector
- 2 Gigabit Ethernet PHY with RJ45 connectors
- USB Host/Slave Controller with USB type A and type B connectors
- RS-232 transceiver and 9-pin connector
- PS/2 mouse/keyboard connector
- IR Receiver
- 2 SMA connectors for external clock input/output
- One 40-pin Expansion Header with diode protection
- One High-Speed Mezzanine Card (HSMC) connector
- 16x2 LCD module

2.3. Very High-Speed Integrated Circuit Hardware Description Language

The VHSIC Hardware Description Language (VHDL) is a versatile hardware description language utilized for modeling the behavior and structure of digital systems at various levels of abstraction. VHDL serves as a means for design entry, documentation, and verification purposes, allowing designers to describe complex systems from the system level down to the level of logic gates. Its standardization by the Institute of Electrical and Electronics Engineers (IEEE) in 1987 as IEEE Std 1076, with the latest version being IEEE Std 1076-2019, has established it as a widely adopted industry standard. Additionally, to accommodate the modeling of analog and mixed-signal systems, an IEEE-standardized HDL known as VHDL-AMS (officially IEEE 1076.1) has been developed [34].

Chapter 3

Design and Simulation of Single-Phase Voltage Source Power Inverters in MATLAB/Simulink

In this chapter, we will use MATLAB/Simulink software to design and simulate three modes of a power inverter: Square Wave, Bipolar SPWM, and Unipolar SPWM. The simulation results obtained will serve as a valuable guide for the hardware design and implementation that will be discussed in Chapter 4. MATLAB/Simulink offers a comprehensive and efficient platform equipped with a wide range of built-in tools and libraries. This platform enables us to design, simulate, and analyze the behavior of the power inverter under various test control strategies.

3.1.Square Wave Inverter

3.1.1. System Design

Figure 16 shows a simplified Simulink model of a square wave inverter. This model comprises an ideal DC voltage source, an H bridge with 4 ideal IGBTs with antiparallel diodes, and two pulse generators. Each pulse generator generates a control signal that drives one pair of opposite diagonal switches. Specifically, signal A drives the gate inputs of S1H and S2L, while signal B drives the gate inputs of S1L and S2H.

In our design, we have used Ideal “IGBT\DIODE” blocks that Implement a MOSFET and antiparallel diode to ensure perfect switching behaviors, i.e., no switching losses, no voltage drops, and no conduction losses when the switches are on, ideal DC source to maintain a fixed voltage output regardless of the load connected to it. Moreover, in the H-bridge topology where there is a need for reverse conducting capabilities, it is essential to include an anti-parallel diode, commonly referred to as a fast recovery diode. Generally, when driving inductive loads, the fast recovery diode allows the inductive current to continue flowing when the power switch devices switch off, preventing voltage spikes and protecting the power devices from excessive voltage stress. This helps minimize the risk of device failure and improves the system’s overall efficiency. Typically, this diode is co-packaged with the power switch [35].

Figures 17.a and 17.b illustrate that signals A and B exhibit a 90° phase difference and share similar characteristics. Both signals have a 50% duty cycle, a frequency of 50 Hz, corresponding to a period of 20 milliseconds, and a 1V amplitude equal to the forward voltage drop of the MOSFETs.

The consideration of dead time was intentionally omitted during the design of the control system to simplify the system analysis. Dead time prevents short circuits by ensuring that no two transistors on the same leg will be on simultaneously. However, Chapter 4 addresses this issue by incorporating a time delay through hardware programming.

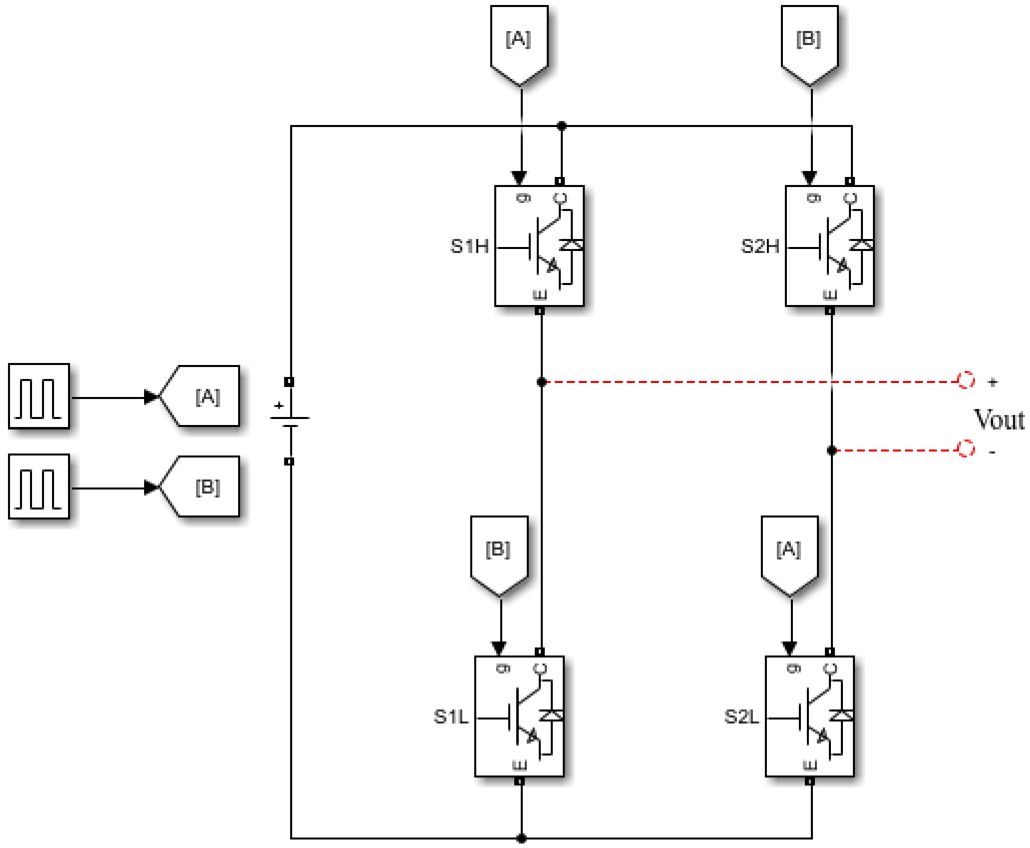
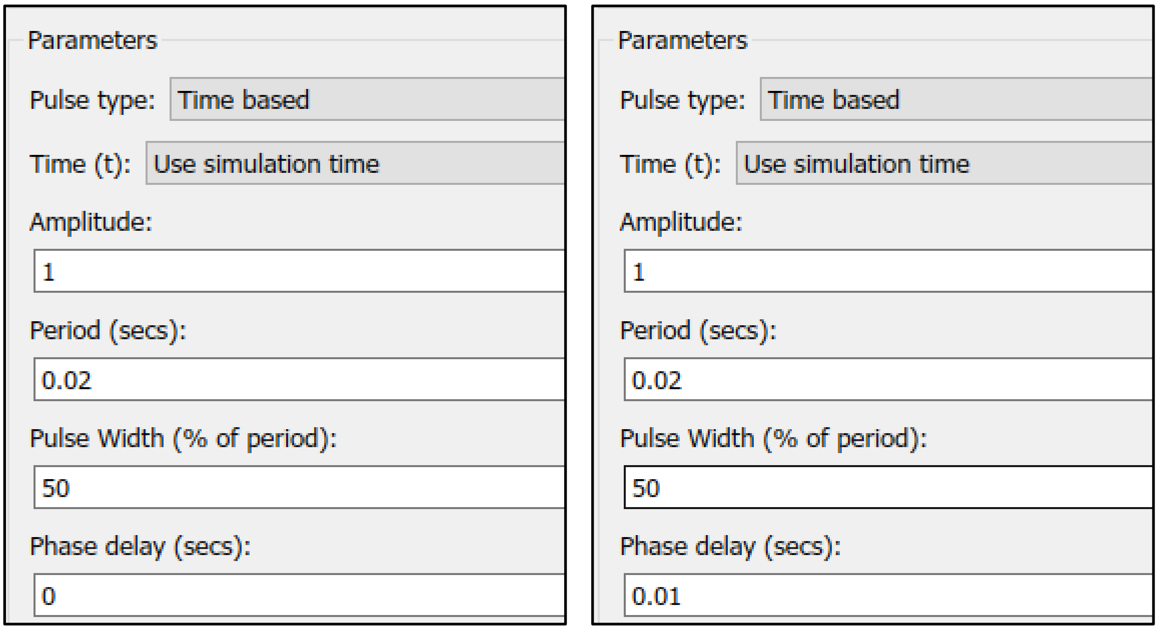


Figure 16. MATLAB/Simulink model of square wave inverter



(a) **(b)**

Figure 17. (a)(b) Block parameters of the pulse generators generating signals A and B, respectively

3.1.2. Simulation Results

The value of the DC source was selected to be +10 volts and the load was selected to be resistive with a value of 10 Ohms. This configuration ensures a matching setup between the components used in the simulation and the hardware implementation. Consequently, it enables a direct comparison and validation of the results obtained from both approaches.

The simulation was extended to two cycles of the inverter output waveform to enhance clarity. This extended timeframe allows for the observation of any repetitive patterns that may occur over multiple cycles, so a more comprehensive understanding of the waveform's characteristics and behavior can be attained.

Figure 18 depicts the control signal A, and B and the inverter output. The output waveform alternates between two voltage levels: +10V for half a cycle and -10V for the second half, corresponding to $+V_{DC}$ and $-V_{DC}$, respectively. Moreover, each complete cycle of the inverter output waveform matches the frequency of the control signals, i.e., the 50 Hz control signals frequency generates a corresponding 50 Hz output waveform from the inverter. This synchronization between the control signals frequency and the inverter output frequency allows for clear visual confirmation of the frequency relationship between the two.

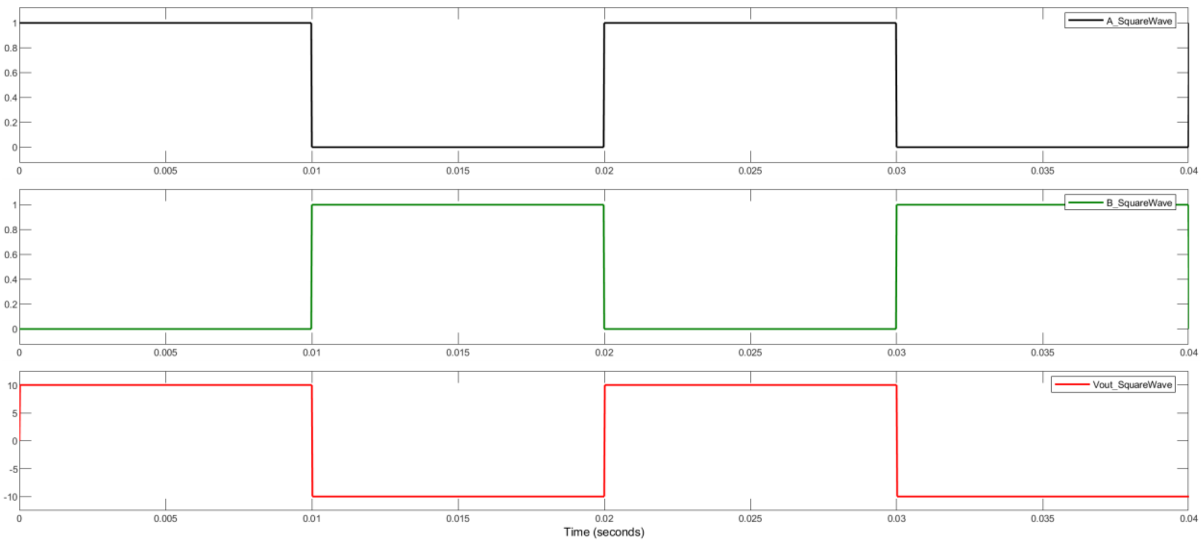


Figure 18. Control signals and square wave inverter output

Observing and analyzing the inverter voltage output waveform under different scenarios is possible. Figure 19 shows three distinct scenarios, each highlighting variations in the DC power supply value and the control parameters. It is worth mentioning that the magnitude of the voltage output can only be changed by adjusting the magnitude of the input DC power source. Conversely, the output frequency can be controlled by modifying the input frequency of the square pulse generators. Therefore, in the square-wave switching scheme, the control is limited to the inverter output frequency. This limitation in control in terms of adjusting the output voltage magnitude is inherent to the square-wave switching technique. On the other hand, other switching schemes, such as PWM, offer more advanced control capabilities over both the output voltage magnitude and frequency, allowing for more flexible and efficient inverter operation.

Figure 19. (a) V_{DC}= +10V, $V_{Control}$ = +15V and f= 50Hz; (b) V_{DC}= +20V, $V_{Control}$ = +1V and f= 50Hz; (c) V_{DC}= +10V, $V_{Control}$ = +1V and f= 100Hz

The FFT analysis decomposes a waveform into its constituent pure sine wave components, where each sinusoid has a frequency that is an integer multiple of the fundamental. These multiples are known as harmonics (see Figure 20).

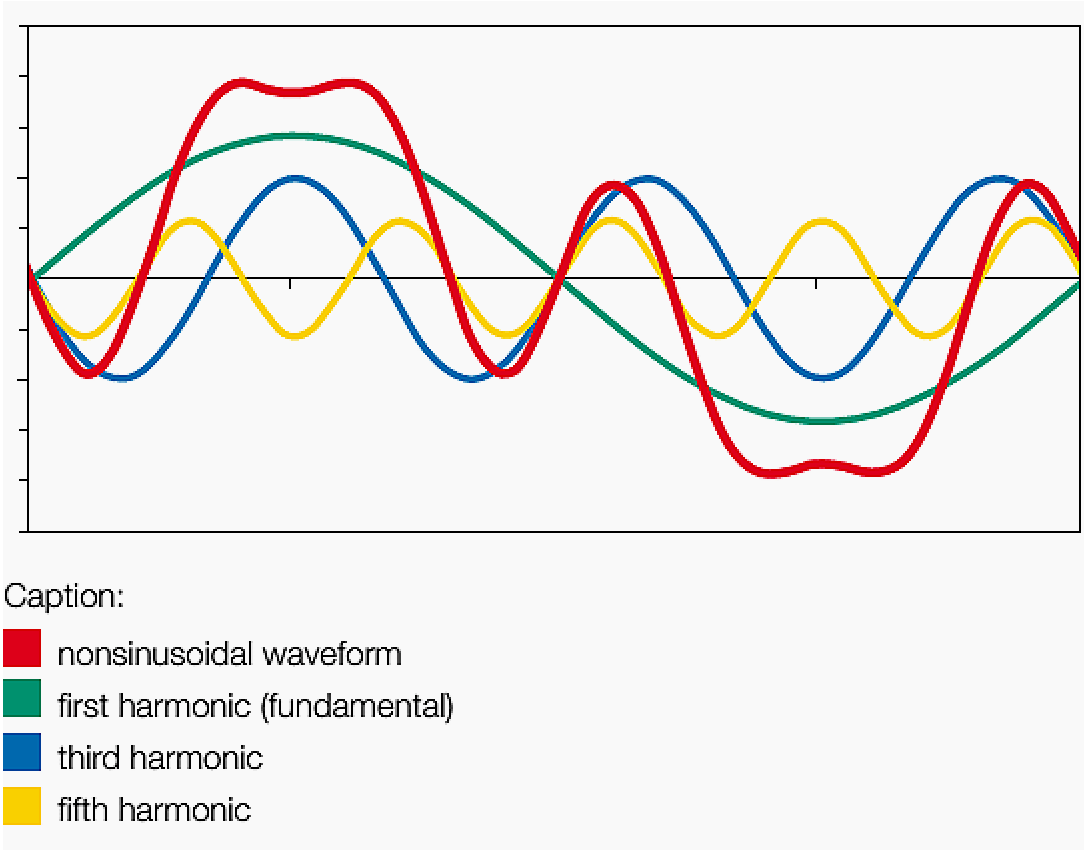


Figure 20. Graphical representation of harmonics

Retrieved from: electrical-engineering-portal.com [36]

While harmonics can be analyzed up to the 40th multiple, it is the early odd harmonics, specifically the 3rd, 5th, and 7th components, that have a more pronounced impact on the system [37]. One way to quantify the overall impact of harmonics is through the calculation of total harmonic distortion (THD). THD is a measure of the distortion present in a waveform causing deviations from the ideal sinusoidal shape. and is expressed as a percentage. It represents the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency.

When harmonics are present in the output voltage waveform of a square wave inverter, the THD value tends to be higher which indicates a greater level of distortion in the output voltage. This can result in various issues such as increased heating, reduced efficiency, and interference with other electrical equipment. Therefore, it becomes essential to address these harmonics and mitigate their effects through appropriate techniques such as filtering, modulation strategies, and control algorithms.

Figures 21 and 22 depict the FFT analysis of the square wave inverter output waveform, highlighting both the THD and the magnitudes of early lower odd harmonics.

The analysis reveals a THD value of 48.22% indicating a significant level of distortion. Among the harmonics, the odd harmonics stand out. The 3rd harmonic component has a magnitude of 33.33% relative to the fundamental frequency, the 5th harmonic has a magnitude of 20%, and the 7th harmonic has a magnitude of 14.29%.

According to IEEE Standard 519 states that the THD measurement should be less than 5% and no one harmonic can be more than 3% of the fundamental frequency. Given these standards, the presence of voltage harmonics in the square wave inverter output, especially those with lower-order components, requires significant filtering to achieve an acceptable sinusoidal waveform and comply with power grid standards. Consequently, investing in bulky filtering equipment becomes imperative.

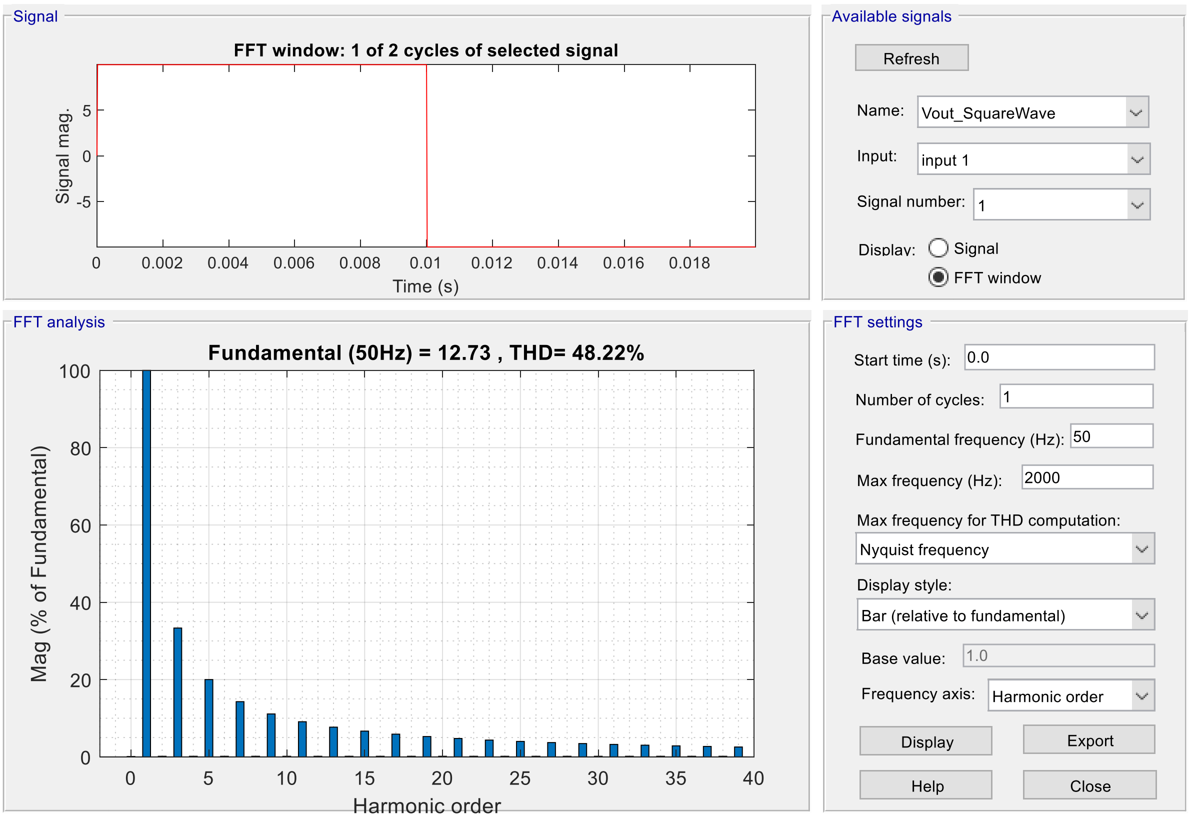


Figure 21. THD is displayed as a list relative to the fundamental frequency

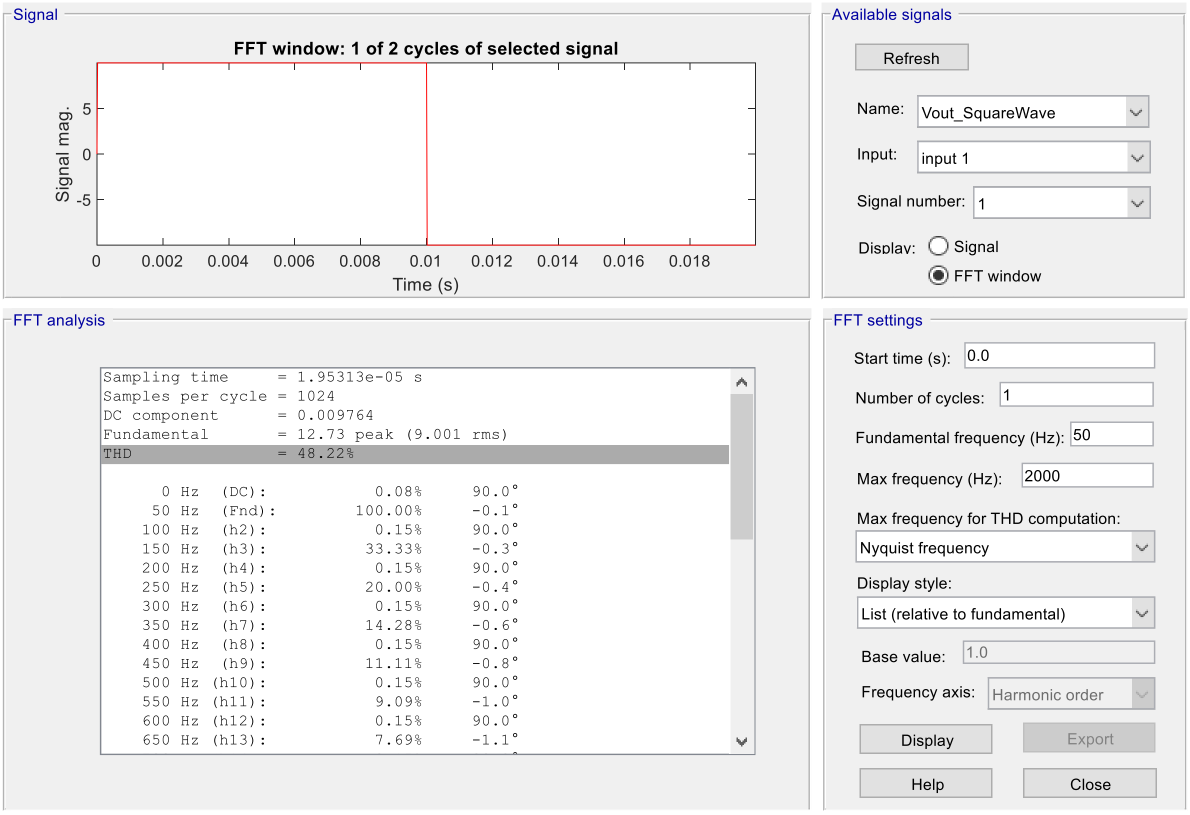


Figure 22. THD displayed as bars relative to the fundamental frequency

3.2.Sinusoidal Pulse Width Modulation Inverter

3.2.1. Bipolar Inverter

3.2.1.1. System Design

Figure 23 shows a simplified Simulink model of a bipolar inverter circuit. This model comprises the H-bridge, power supply, and switches control configuration (i.e., signal A controls switches S_{1H}/S_{2L}, while signal B controls switches S_{1L}/S_{2L}) used in the Simulink model of the square wave inverter, a sine wave, a triangle generator, and two relational operators.

As illustrated in Figure 24, the triangle generator generates a high-frequency carrier signal of 1kHz phased out by 180° and has a peak amplitude of 1V. The phase shift is introduced to get the carrier waveform starting from its peak value rather than from its negative peak value. This phase shift serves a specific purpose, which will be highlighted and explained in detail in the design and implementation chapter. On the other hand, the reference signal has a frequency of 50 Hz and a peak amplitude of 0.8V.

Our design aims to satisfy a modulation index (m_a) value of 0.8. and a frequency modulation index (f_m)value of 20.

$$m_a = \frac{V_{p,ref}}{V_{p,tri}} = \frac{0.8}{1} = 0.8 \quad \text{.......................} (3) \qquad f_m = \frac{f_{tri}}{f_{ref}} = \frac{1000}{50} = 20 \quad \text{.......................} (4)$$

The relational operators depicted in Figure 23 are used to compare the reference and carrier signals. When the instantaneous value of the modulating signal is greater than the carrier signal, the control signal A is high, and the output voltage is at +Vdc. Conversely, when the reference is lower than the carrier signal, control signal B is high and output voltage is at -Vdc. This comparison helps to determine the appropriate ON and OFF timing of the switches to get the desired output voltage waveform:

S_{1H} and S_{2L} are on	$V_{ref} > V_{tri}$	$V_o = +V_{DC}$
S_{1L} and S_{2H} are on	$V_{ref} < V_{tri}$	$V_o = -V_{DC}$

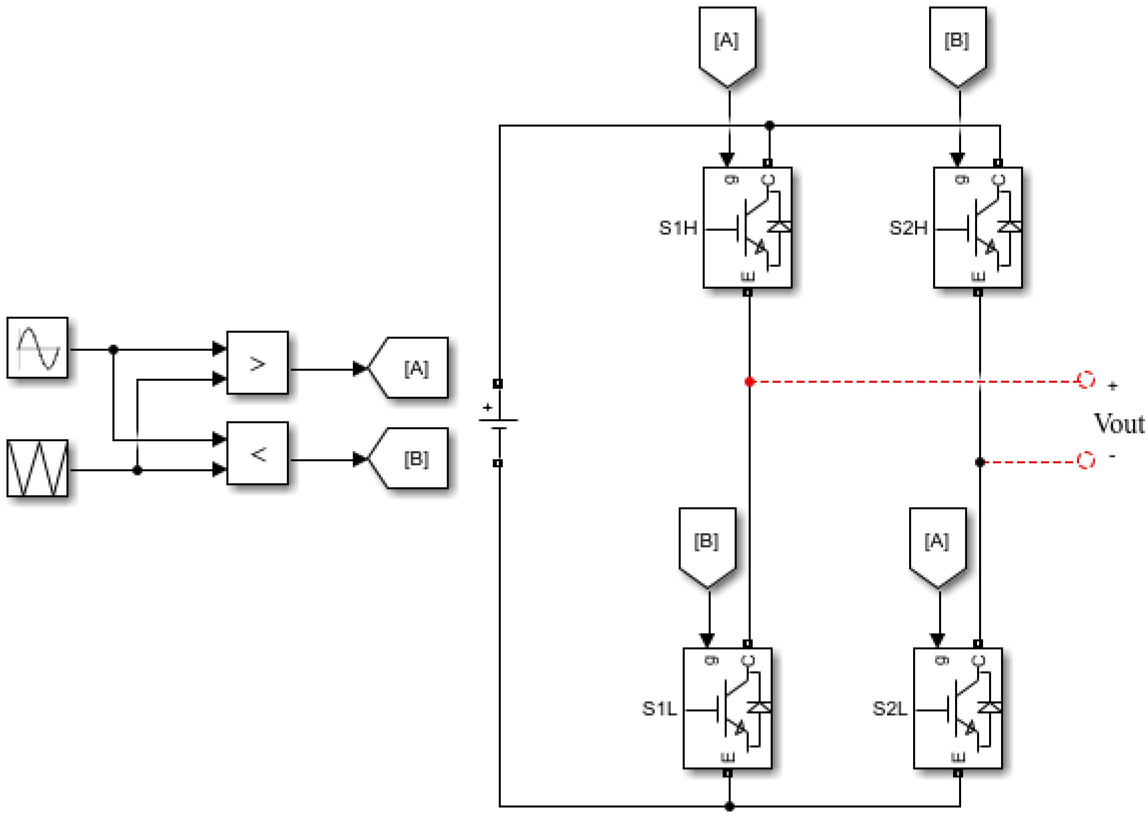
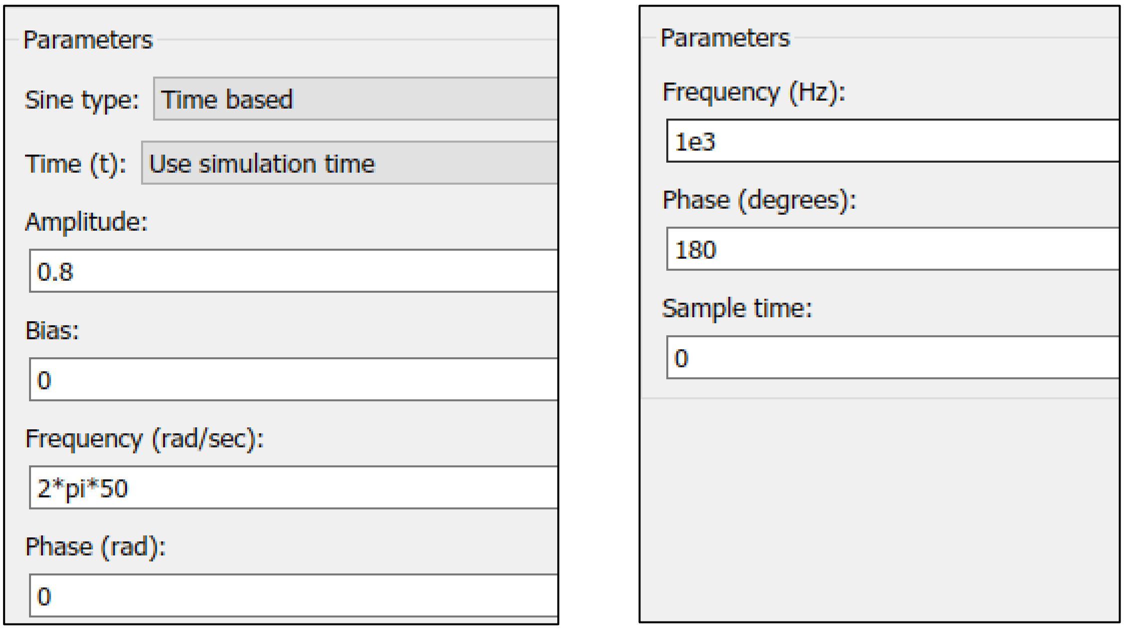


Figure 23. MATLAB\Simulink model of bipolar inverter



(a) *(b)*

Figure 24. (a)(b) Parameters of carrier and reference signals, respectively for bipolar inverter

To generate a sinusoidal waveform that closely resembles a pure sine wave, it is necessary to include an LC filter in our design, as depicted in Figure 25. The following equations are utilized to calculate the suitable combination of capacitor and inductor for the filter [38]:

$$f_{ref} = \frac{1}{2\pi\sqrt{LC}} \quad \text{......................} (5)$$

$$\Delta I_{L\max} = \frac{V_{DC}}{4Lf_{tri}} \quad \text{......................} (6)$$

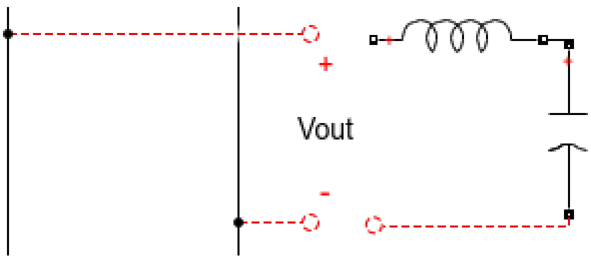


Figure 25. LC filter coupled to the inverter output

3.2.1.2. Simulation Results

The value of the DC source was selected to be +10 volts and the load was selected to be resistive with a value of 10 Ohms.

The simulation results were focused on two cycles of the output frequency waveform to ensure better visualization and analysis of the switching patterns and the inverter output voltage waveform.

The carrier and reference signals are multiplexed into a single trace on the scope as shown in Figure 26.a. Setting the modulation index frequency to 20, leads to 20 switching pulses per cycle with a switching frequency of 1 kHz. The control signals A and B are complementary to each other, as depicted in Figures 26. b and 26. c, respectively. The duty cycle of the switching pulses in control A starts around 50% and gradually increases until reaching the halfway point of the cycle. Afterward, it decreases until completing a full cycle. The unfiltered and filtered inverter outputs are combined into a single trace on the scope, as depicted in Figure 25.d. This figure demonstrates that the unfiltered output is bipolar, exhibiting two voltage levels: $+V_{DC}$ and $-V_{DC}$, and pulsates based on the summation of the two control signals. Furthermore, the filtered output appears as a sine wave with some degree of distortion.

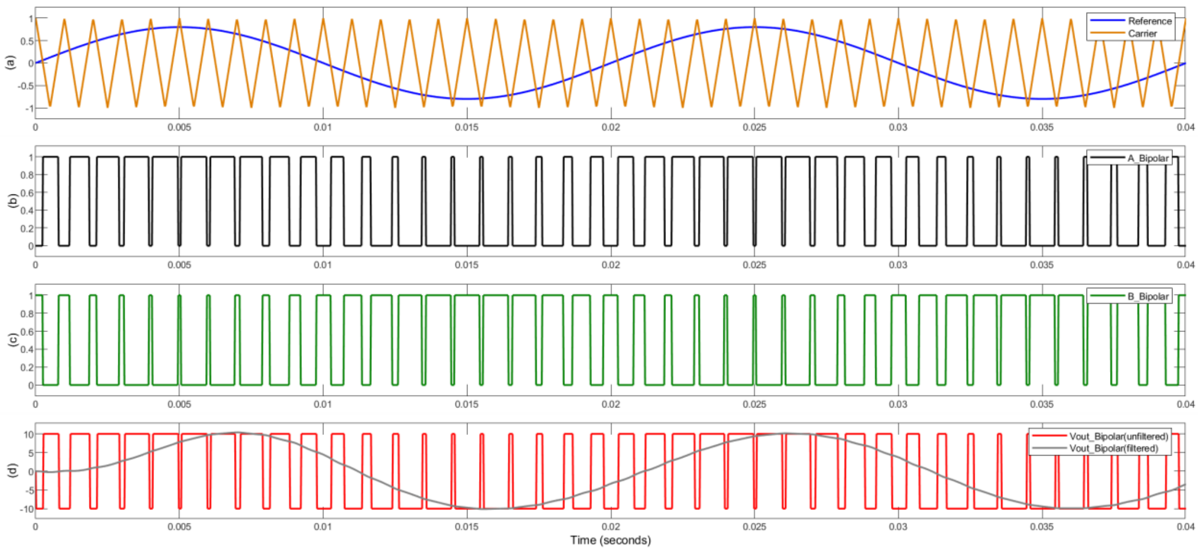


Figure 26. (a) Sine-triangle; (b) Control pulses for S_{1H} S_{2L}; (c) Control pulses for $S_{1L}S_{2H}$; (d) Unfiltered and filtered bipolar inverter outputs

Figure 27 shows the FFT analysis of the unfiltered bipolar inverter output waveform, revealing a THD value of 146.22% and highlighting a significant level of distortion. However, it is noteworthy that lower-order harmonics have been effectively eliminated. This underscores the advantage of a bipolar PWM inverter over a square wave inverter, as it offers the ability to reduce or eliminate early odd harmonics, leading to enhanced overall performance. Although higher-order harmonics are still present, they can be further mitigated as illustrated in Figure 28 by coupling the filter presented in the design section to the resistive load. The LC filter parameters were selected to be 8.865 mH and 286uF, respectively.

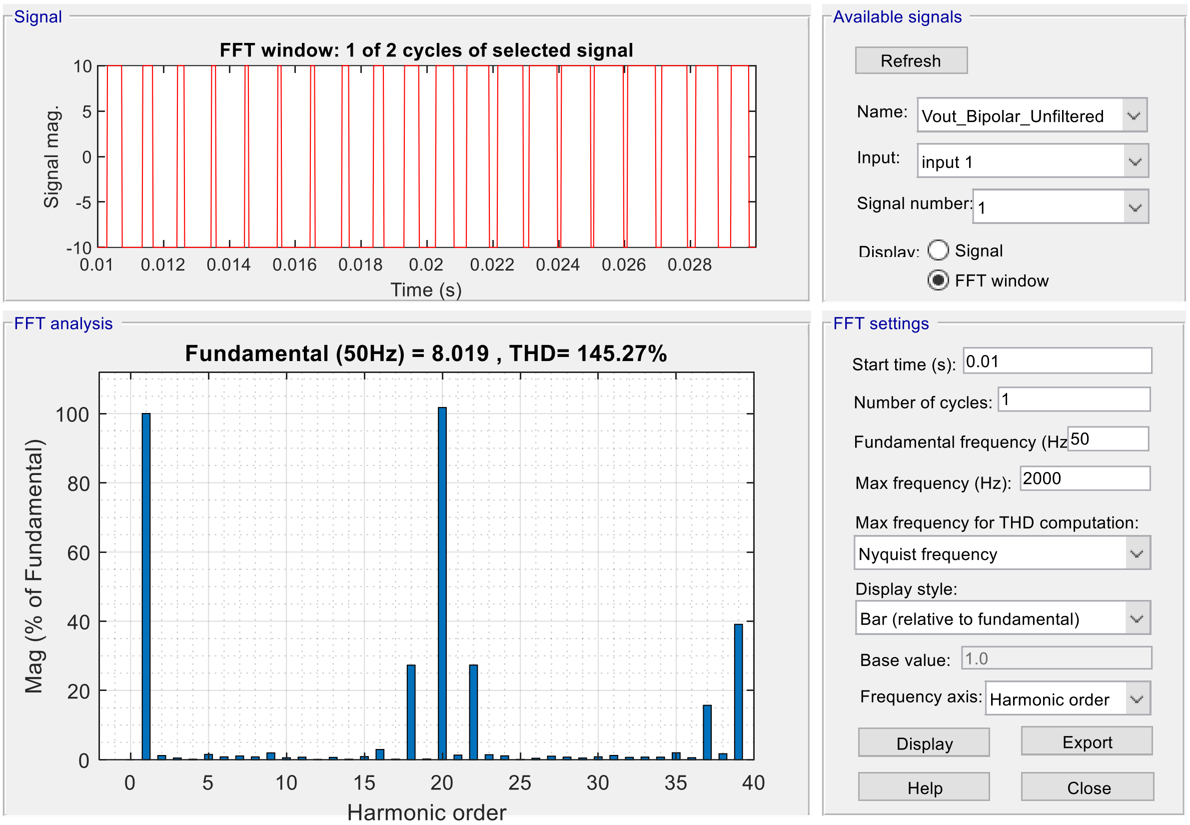


Figure 27. Harmonic spectrum of the bipolar inverter (without filter)

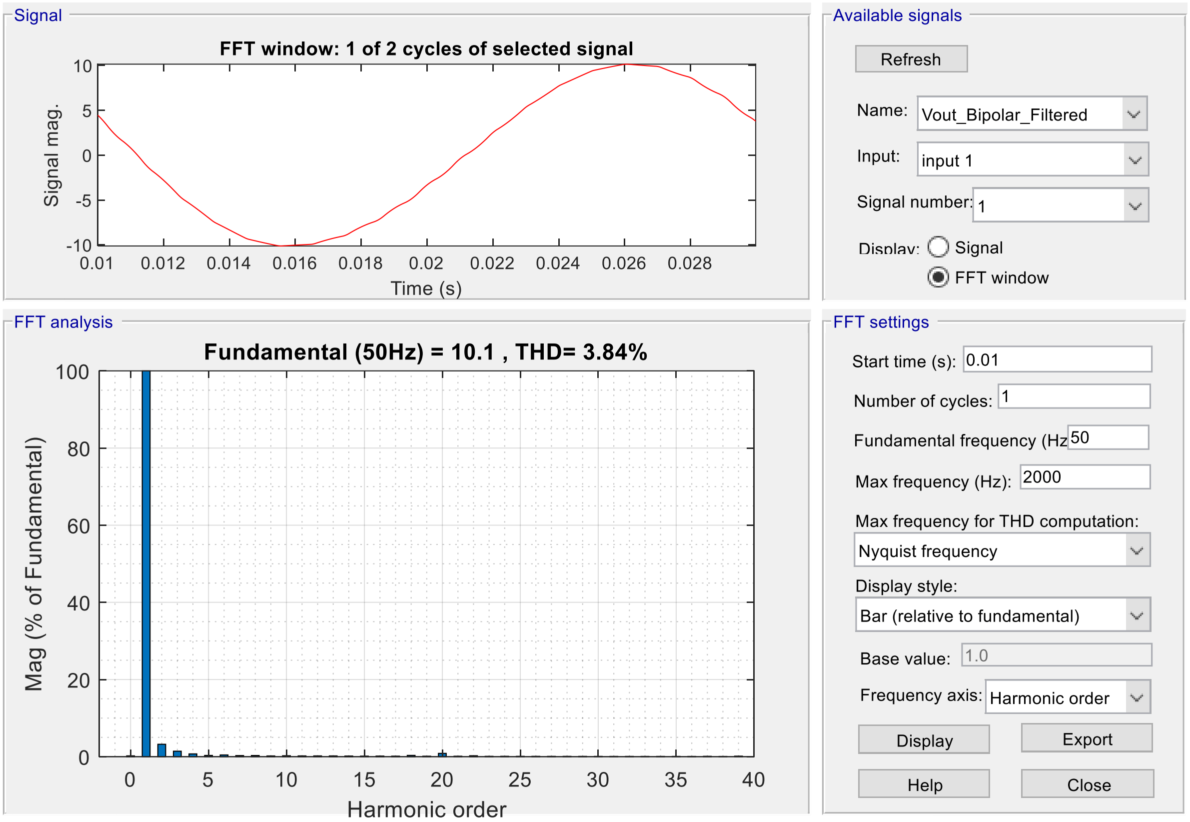


Figure 28. Harmonic spectrum of the bipolar inverter (with filter)

3.2.2. Unipolar Inverter

3.2.2.1. System Design

Figure 29 illustrates a simplified Simulink model of a unipolar inverter circuit. This model comprises the H-bridge and power supply used in the Simulink model of both square wave and bipolar inverters, two sine waves, a triangle generator, two relational operators, and two bitwise operators. The two reference signals are phase-shifted by 180°, with a frequency of 50 Hz and a peak amplitude of 0.8V each. Additionally, the carrier signal has a frequency of 1 kHz, a peak amplitude of 1V, and a phase shift of 180°. The parameters for these signals are illustrated in Figure 30.

In our design, each switch is individually controlled by a dedicated control signal, resulting in a unique configuration and additional control circuitry when compared to square wave and bipolar inverters. Control signals A, and B are obtained by comparing the two modulating signals with the triangular carrier using the two relational Operators. However, control signals C and D are obtained by inverting signals A, and B, respectively using the two bitwise operators. These control signals, namely A, B, C, and D, control switches S_{1H}, S_{2H}, S_{1L}, and S_{2L}, respectively, and they fulfill the following conditions:

S_{1H} is on when $V_{ref\,1} > V_{tri}$

S_{1L} is on when $V_{ref\,1} < V_{tri}$

S_{2H} is on when $V_{ref\,2} > V_{tri}$

S_{1H} is on when $V_{ref\,2} < V_{tri}$

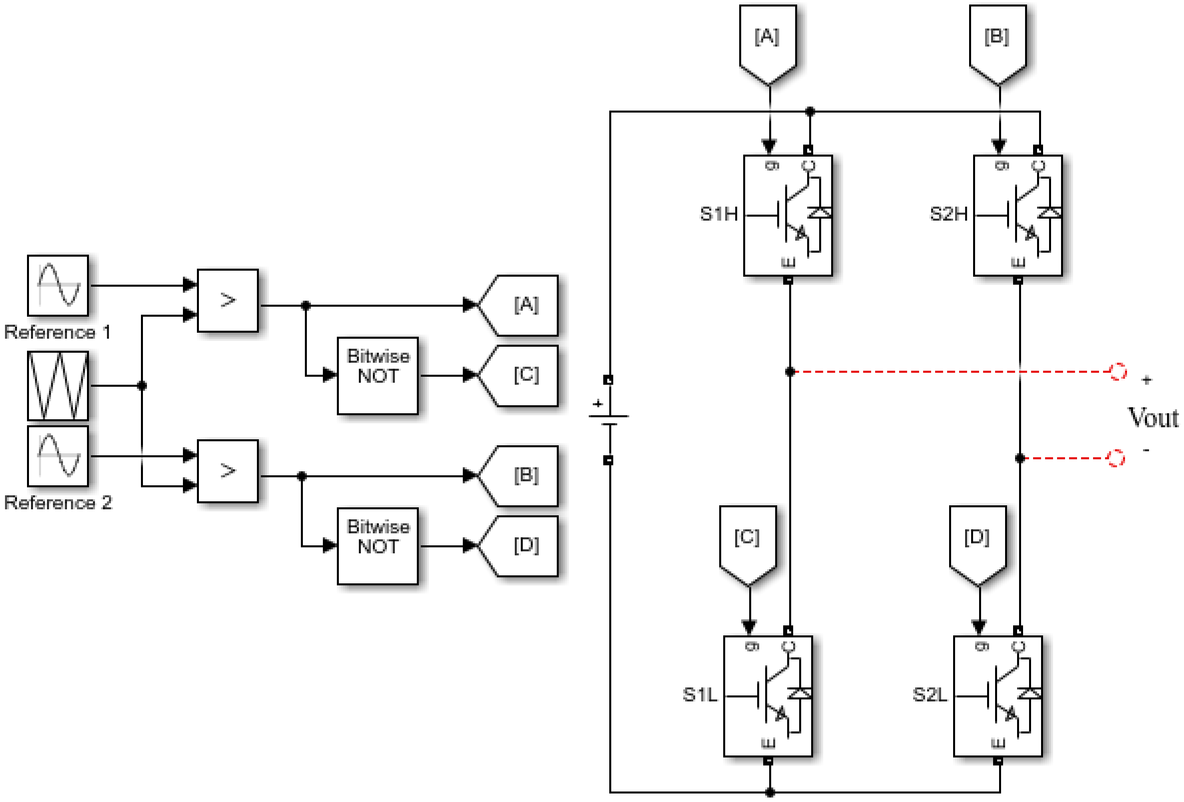
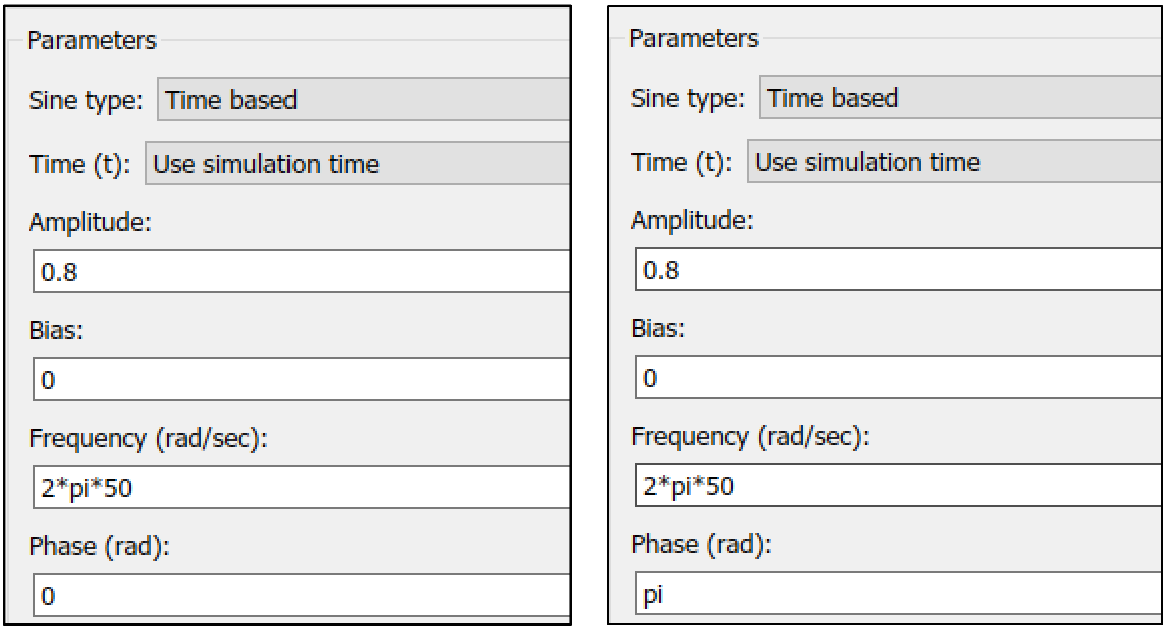


Figure 29. MATLAB\Simulink model of unipolar inverter



(a) (b)

Figure 30. (a)(b) Parameters of carrier and reference signals, respectively, for unipolar inverter

3.2.2.2. Simulation Results

The value of the DC source was selected to be +10 volts and the load was selected to be resistive with a value of 10 Ohms. The simulation results were focused on two cycles of the output frequency waveform.

The carrier and the two reference signals are multiplexed into a single trace on the scope, as shown in Figure 31.a. It can be seen from Figure 31. b and 31. c that the switching pattern of signal A in one half-cycle is similar to the switching pattern of signal B in the subsequent half-cycle, and vice versa. Furthermore, it fluctuates based on the subtraction of signal B from signal A, resulting in a frequency of 2 kHz, which is twice the frequency of the carrier. The unfiltered and filtered unipolar inverter outputs are combined into a single trace on the scope, as depicted in Figure 30.d. This figure demonstrates that the unfiltered output is unipolar, exhibiting voltage levels in a single polarity and fluctuates based on the subtraction of signal B from signal A, resulting in a frequency of 2 kHz, which is twice the frequency of the carrier. Furthermore, the filtered unipolar output appears as a sine wave with fewer distortions and a smoother waveform compared to the bipolar filtered output.

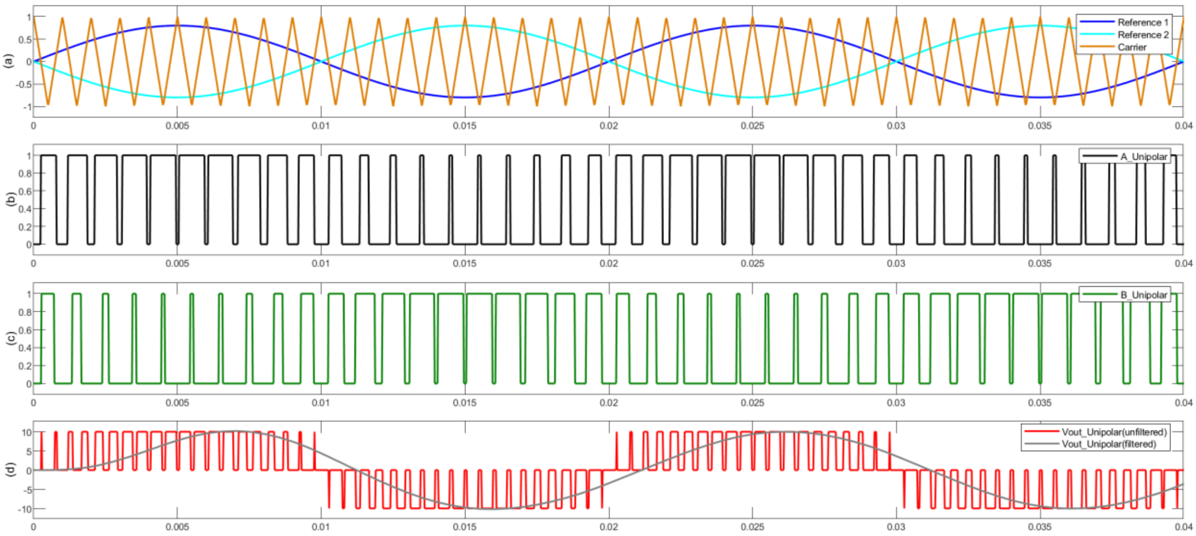


Figure 31. (a) Sine-triangle; (b) Control pulses for S_{1H}; (c) Control pulses for S_{2H}; (d) Unfiltered and filtered unipolar inverter outputs

Figure 32 depicts the harmonic spectrum of the unfiltered unipolar inverter output, revealing a reduced THD level of 76.12%, approximately half, in comparison to the bipolar unfiltered inverter output operating at the same carrier frequency of 1 kHz. Furthermore, the figure illustrates that the unipolar inverter effectively eliminates lower-order harmonic components. Moreover, by combining this inverter with the LC filter used in the bipolar inverter, an enhanced overall harmonic performance is achieved as shown in Figure 33. Overall, based on the provided THD values, the unipolar inverter offers superior harmonic performance compared to the square wave and bipolar inverter. This makes the unipolar inverter a more favorable choice in applications where low harmonic distortion is a priority.

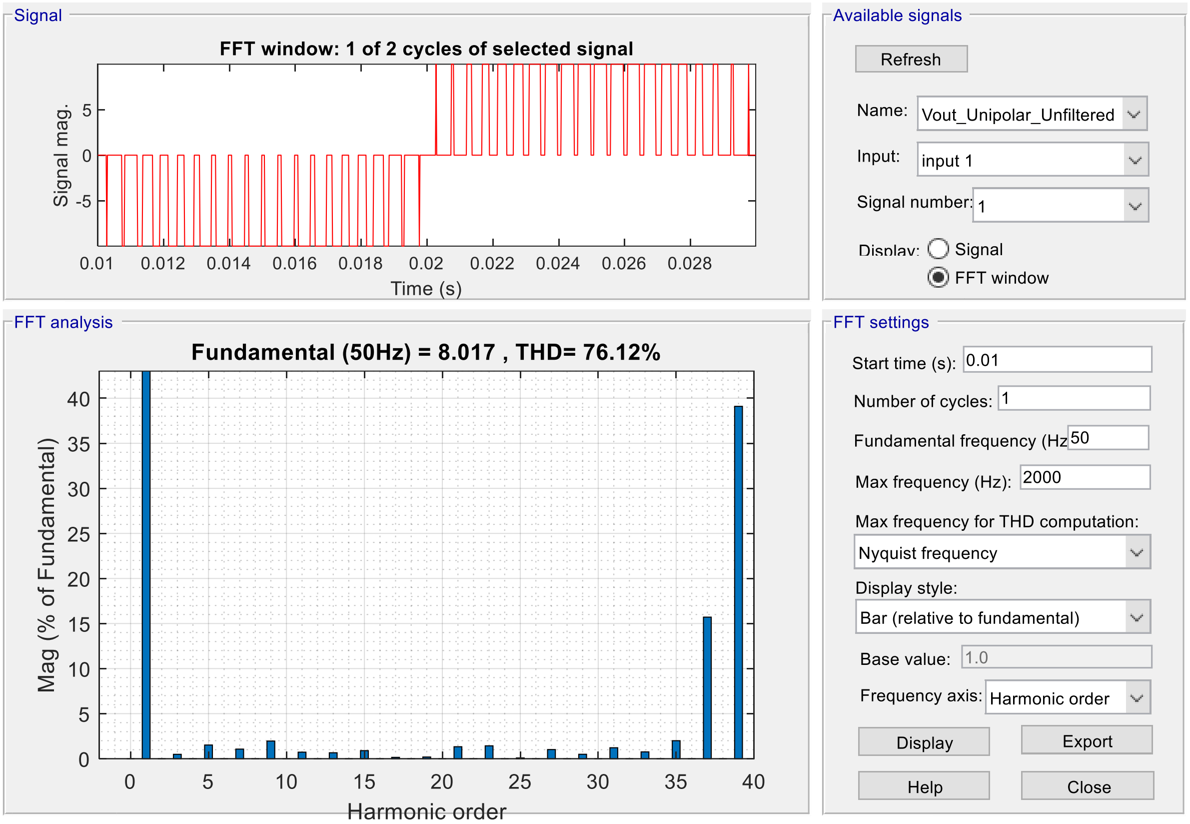


Figure 32. Harmonic spectrum of the unipolar inverter (without filter)

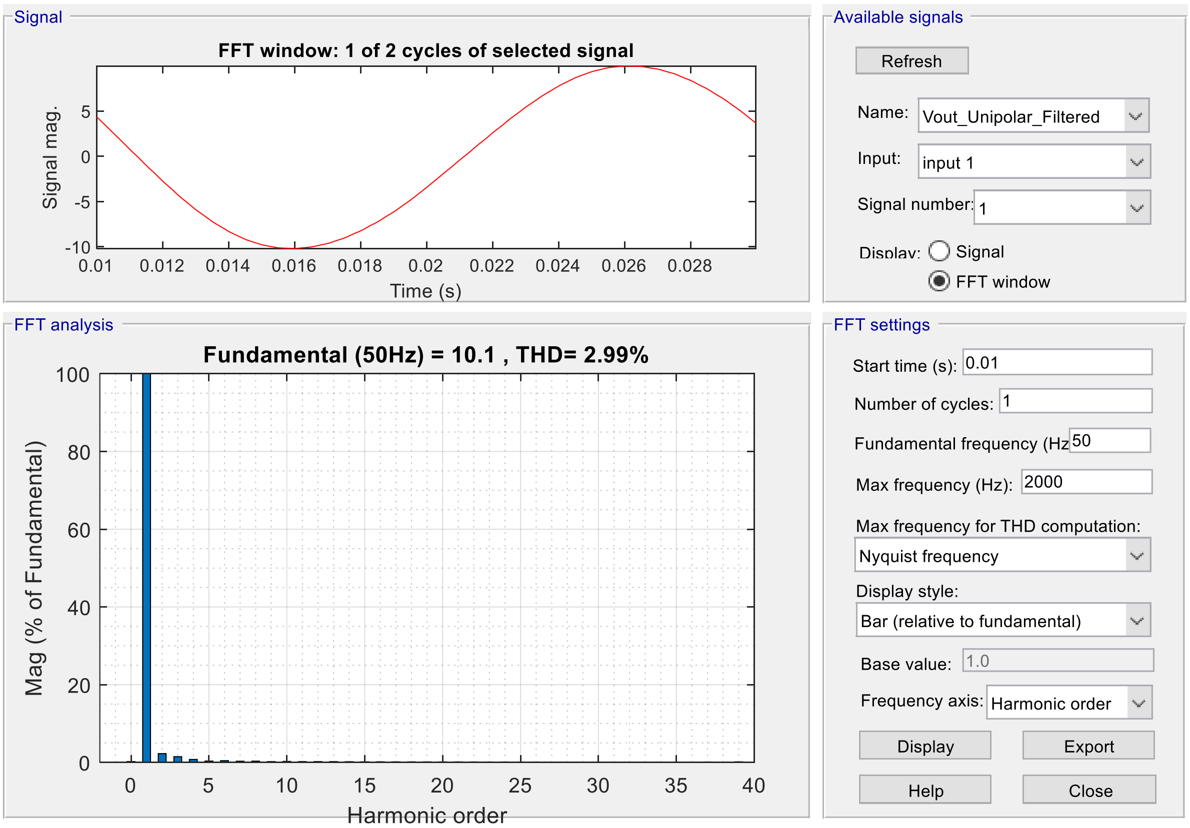


Figure 33. Harmonic spectrum of the unipolar inverter (with filter)

Chapter 4

Design and Implementation of Single-Phase Voltage Source Power Inverters Using FPGA

The main objective of this chapter is to demonstrate the capabilities of FPGA technology in implementing complex control algorithms for driving inverters effectively. Through the utilization of the Cyclone IV-E FPGA, we implemented three modes of single-phase voltage source power inverters. These specific modes, namely square wave, bipolar, and unipolar, were discussed in detail in Chapter 1 and 3. The hardware circuitry design for each mode is initially carried out using Proteus software. Once the design is validated, it is transferred to the prototype board for physical implementation. The switching process is initially designed using the VHDL and then simulated using Quartus II v9.1 software to verify the consistency of the on-off timing data with MATLAB\Simulink. Following the simulation, the design is downloaded to the DE2-board using a USB blaster cable. a Gwinstek two-channel digital oscilloscope GDS-1052U is used to measure and evaluate the output from both the Altera board and the power inverters.

4.1.Square Wave Inverter

4.1.1. System Design in Proteus

Figure 34 depicts the physical circuit schematic of the square wave inverter implemented using Proteus software. This circuit consists of three DC power supplies, an H-bridge with four power MOSFETs accompanied by antiparallel diodes, a resistive load, two limiting current resistors, two SN54LS240 buffers, two SN54LS04 hex inverters, and two H11D1M optocouplers.

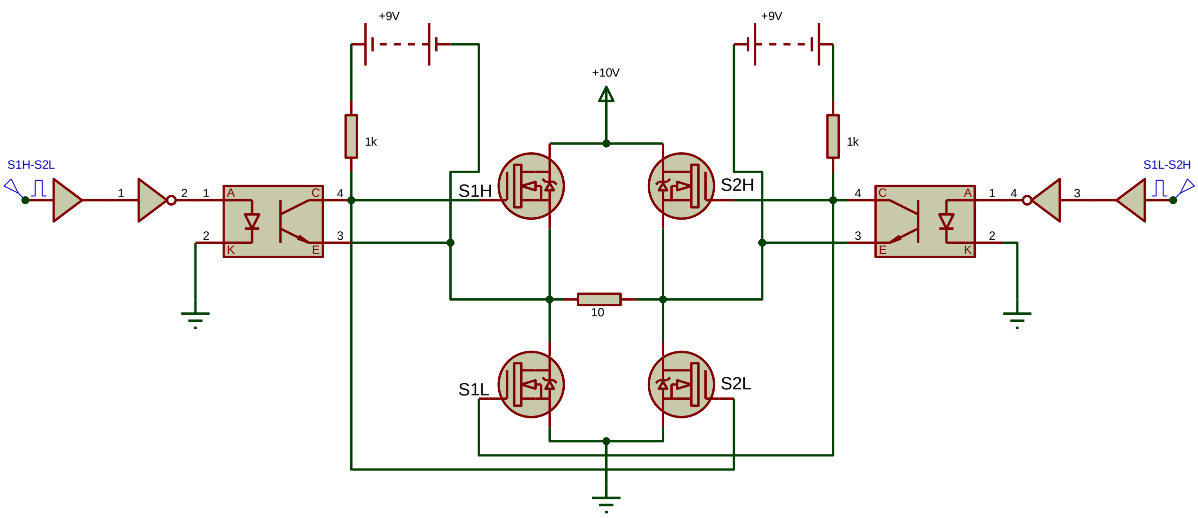


Figure 34. Circuit schematic of the square wave inverter designed in Proteus software

Given that we will work in a low-voltage application, the intentional selection of power MOSFETs over IGBTs aims to minimize power dissipation during the ON state. IGBTs generally have a higher saturation voltage (VCE (sat)) of around 2.05V, whereas power MOSFETs typically feature lower on-state resistance (RDS (on)). This lower RDS (on) results in reduced power losses for the same current value compared to IGBTs.

The optocouplers are utilized to perform voltage level shifting in the circuit. Specifically, they step up the voltage level outputted by the expansion header of the Altera DE2 board from 3.3V to 9V. This voltage level shift is necessary to meet the MOSFET gate threshold voltage requirement, ensuring proper triggering and operation of the MOSFETs.

The buffers are utilized to shape and maintain control signals' characteristics, such as rise time, fall time, and voltage levels during transmission within the electronic system.

The DC input source is set at +10V as a protective measure during the circuit implementation. It's worth noting that a higher voltage value, up to the maximum rating that the power MOSFET can withstand, could have been utilized. However, the decision to use a lower voltage level ensures an added layer of protection during the implementation process. The two remaining supplies are used to drive the two upper switches in a high-side configuration. A semiconductor switch placed in the upper circuit with respect to an external load is referred to as a high-side switch (power supply side), and when mounted in the lower circuit is called a low-side switch (ground side) [39], as illustrated in figure 35.

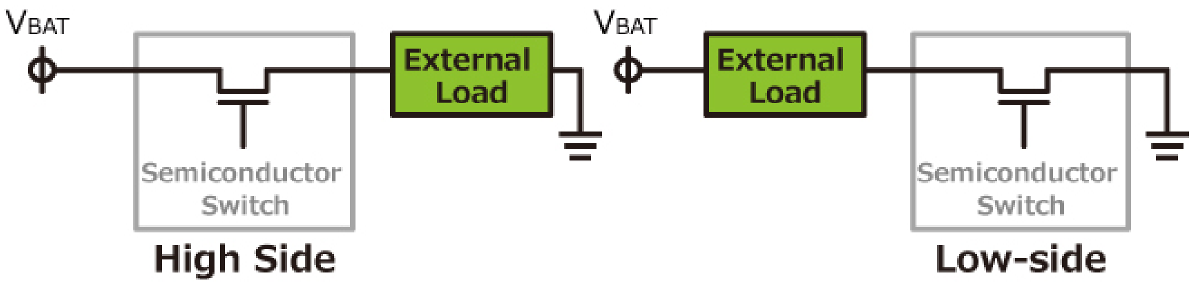


Figure 35 . High side switch/ Load side switch

Retrieved from: rohm.com [39]

4.1.2. System Design and Simulation in Quartus II

Figure 36 depicts the block diagram of the square wave inverter control signal generator. The first input signal, labeled "Clk," is directly connected to the default 50MHz clock of the FPGA through the Y2 pin. This connection indicates that the clock signal for the control signal generator is sourced from the FPGA's 50MHz clock. The second input signal, labeled "Rst," is an active low signal used to reset the system. It is connected to the "PUSH-BUTTON [0]" of the DE2 board through the M23 pin. Pressing this specific push button on the DE2 board triggers the reset functionality of the system. The two output control signals, namely "S1H_S2L" and "S2H_S2L." are used to control the two pairs of diagonal switches and are connected to the inputs of the hex inverters, as shown in the previous section, through the expansion header. The DE2-115 Board provides one 40-pin expansion header. The header connects directly to 36 pins of the Cyclone IV E FPGA and provides DC +5V, DC +3.3V, and two GND pins.

The symbol file labeled "SquareWave_Control" contrasts the hardware logic utilized in the controlling process. It comprises a clock divider block that utilizes a modulo n counter to divide the clock frequency by the value of n. This helps generate a control signal of a desired frequency. A dead time block employs a finite state machine (FSM) with six states to introduce the required delay between the on and off switching timings of switches on the same leg of the H-bridge, and a two-level cascaded counter to achieve a 50% duty cycle for both control signals.

In our design, the control signals are generated with a frequency of 50Hz and a dead time of 10us. The choice of 10us dead time is considered safe for our inverter system since the on-and-off timing of MOSFETs is typically in the nanosecond range.

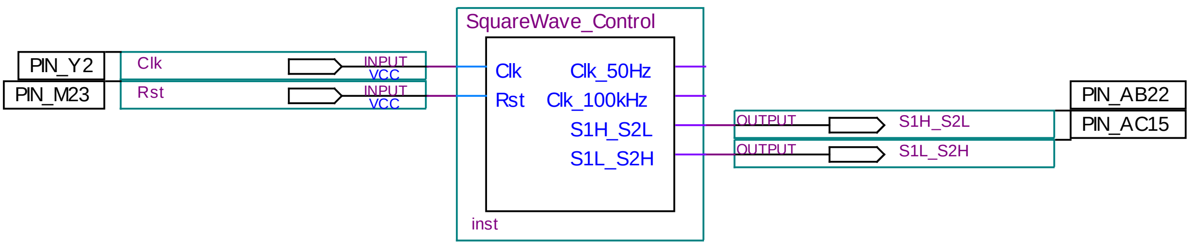


Figure 36. Block diagram of the control signals generator for the square wave inverter in Quartus II

To improve clarity, the simulation was extended to include two cycles of the inverter output waveform (i.e., 40ms).

As depicted in Figure 37, The “Clk” signal was parameterized with a clock value of 20ns period (i.e., 50 Hz frequency) and a 50% duty cycle. Whereas the” Rst “signal was disabled by forcing it high. It is not possible to observe the dead time within the output control signals. However, Figure 38 provides a zoomed-in view specifically focused on the dead time, allowing for a more detailed examination of this specific portion of the waveform.

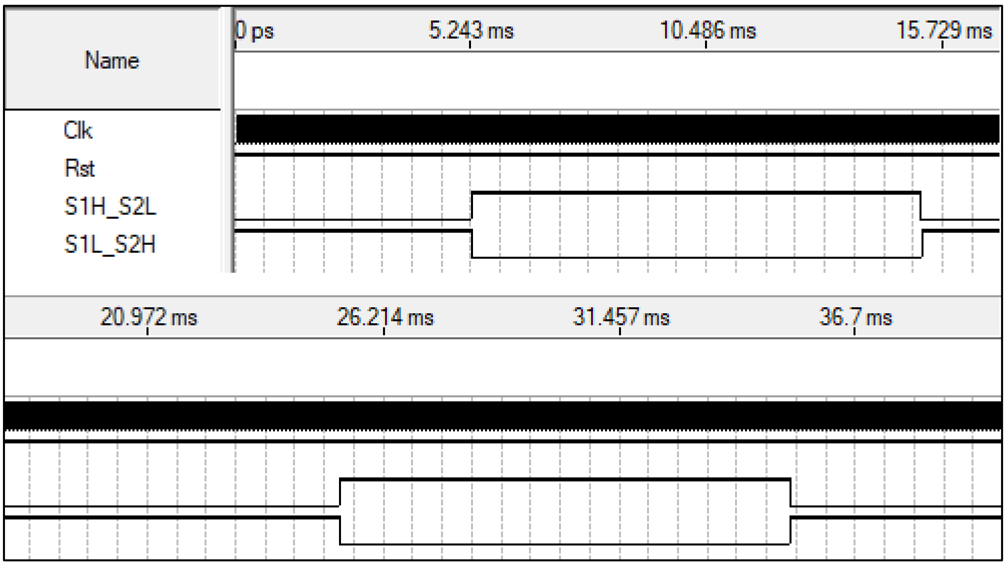


Figure 37. Control signals for the square wave inverter generated in Quartus II

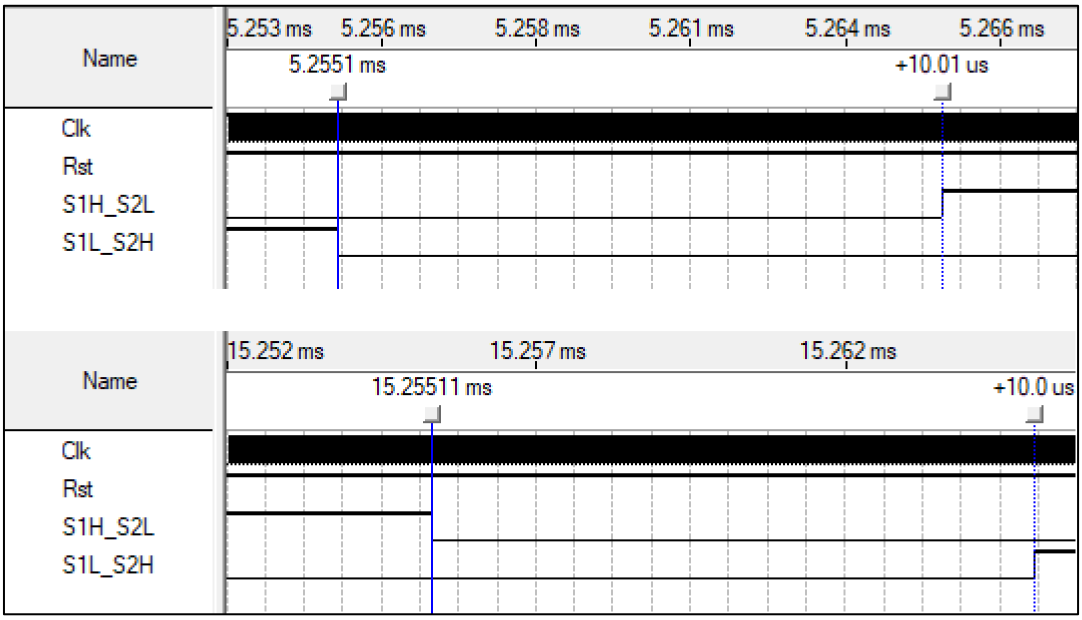


Figure 38. 10us dead time in a zoomed-in view in Quartus II

4.1.3. Experimental Results

Figure 39 depicts the control signals captured using a physical oscilloscope for the square wave inverter. These signals exhibit complementary waveform and maintain a 50% duty cycle, a voltage level of 3.36V, and a desired frequency of 50 Hz. Furthermore, Figure 40 shows a detailed emphasis on the dead time aspect associated with the signals. This figure demonstrates that the applied dead time is precisely 10 microseconds, as indicated in the X1X2 tab, which represents the difference between the cursor's positions.

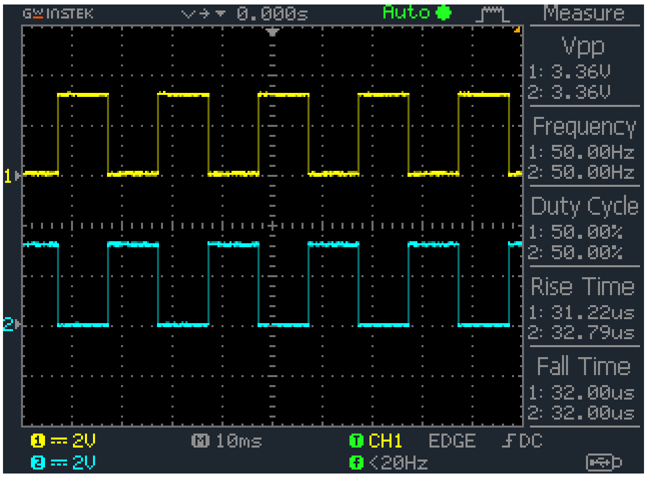


Figure 39. Control signals for the square wave inverter captured on an oscilloscope.

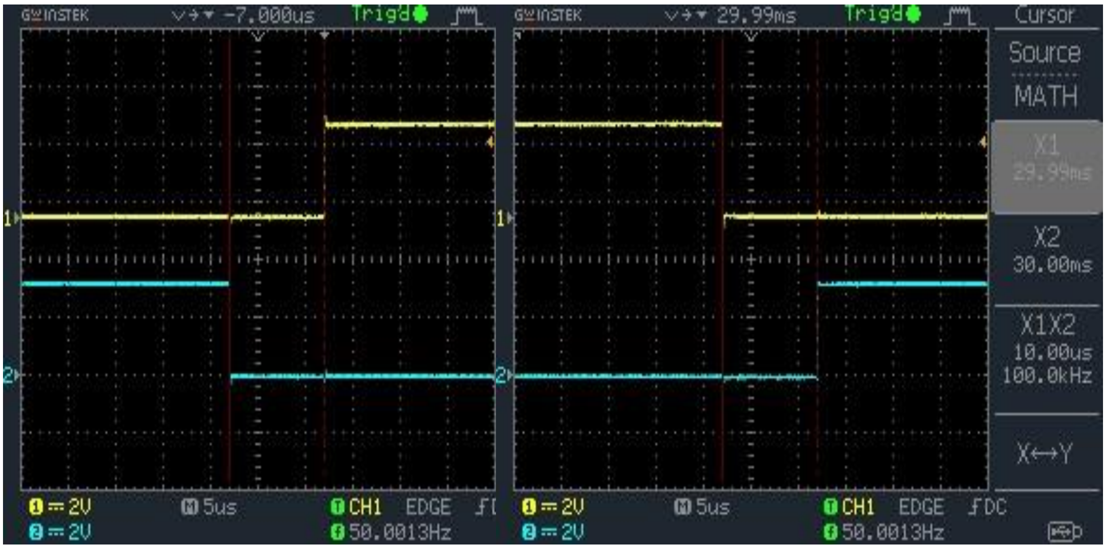


Figure 40. Zoomed-in view highlighting the 10us dead time in the control signals of the square wave inverter.

Figure 41 shows the output of the square wave inverter. The yellow and blue signals represent the voltages measured at the terminals of the load V_A and V_B, respectively. V_A corresponds to the voltage measured at the point between the emitter of the upper switch and the drain of the lower switch of the first leg, while V_B represents the voltage measured at the point between the emitter of the upper switch and the drain of the lower switch of the second leg. Both V_A and V_B have a peak-to-peak voltage of 10V each. The red signal represents the difference between the yellow and blue signals. It showcases the outcome of this inverter, exhibiting a peak-to-peak voltage of 20V and a frequency of 50Hz.

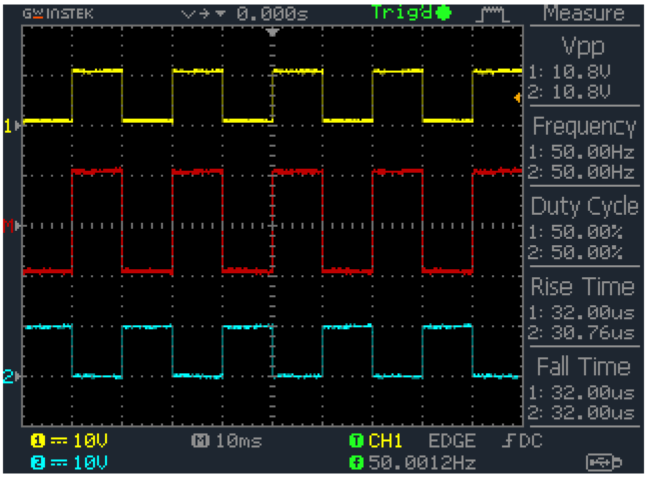


Figure 41. Output of the square wave inverter (red signal) with voltage measurements at load terminals V_A (yellow signal) and V_B (blue signal)

4.2. Bipolar Inverter

4.2.1. System Design in Proteus

The physical circuit schematic of the bipolar inverter is similar to the one of the square wave inverters discussed earlier. Nevertheless, this section has been shortened to allocate more attention and focus on the implementation of the bipolar switching scheme in the FPGA.

4.2.2. System Design and Simulation in Quartus II

Figure 42 shows the symbol file used for controlling the bipolar inverter. The Clk_PWM signal represents the switching clock set at 1kHz (i.e., one modulated pulse per 1 ms). The data1 signal refers to a ROM with 20 address locations. The ROM stores the various duty cycles of the switching pulses.

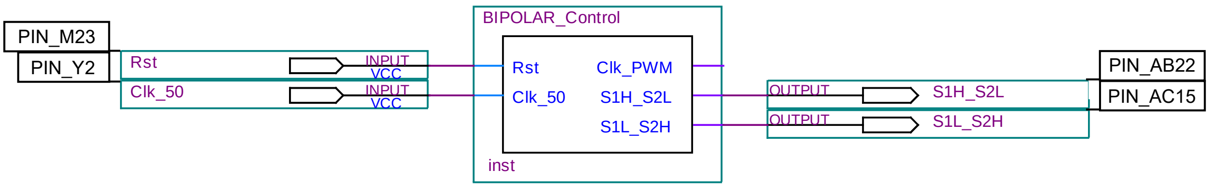


Figure 42. Block diagram of the control signals generator for the bipolar inverter in Quartus II

Since our design aims to achieve a frequency modulation index of 20 (i.e., 20 pulses per complete cycle) as discussed in Chapter 3, the deliberate decision to utilize a ROM with 20 address locations was made.

In an analog implementation, achieving a sinusoidal waveform is as simple as setting a sinusoidal control voltage. However, in digital implementation, a digital counter is used for the intersection of the duty cycle level with the value triggered by another counter instead of comparing a carrier signal with a reference signal using a comparator. Moreover, in digital the waveform needs to be sampled, and the duty cycle is adjusted at each sample, representing a PWM sinusoidal waveform. Furthermore, it is crucial to consider the resolution of the sine wave. In our design, an 8-bit resolution was chosen, which allows for duty cycles ranging from 0 to 255.

Figure 43 depicts the calculation of duty cycles for the first half cycle and the second half of the pulsated sine using C code programming. The variable 'n' represents the number of samples per half cycle. The inclusion of the value 128 in both duty cycles accounts for the initial pulse in each half cycle of the inverter output, which approximately starts with a 50% duty cycle. This behavior can be confirmed through the simulation of the bipolar inverter using MATLAB/Simulink, as discussed in Chapter 3.

Figure 44 illustrates complementary duty cycle values for pulses starting from each half cycle. The duty cycles add up to 256, representing a 100% duty cycle. The choice of using the float data type for the duty cycle values prevents the C compiler from rounding the values based solely on their decimal part, ensuring accurate representation. Subsequently, these values are stored into a ROM.

```c
#include <stdio.h>
#include <math.h>
int main() {
    int n=10;
    float dutyCycle1[10], dutyCycle2[10];
    int i=0;
    for(i=0;i<n;i++){
        dutyCycle1[i]=  (sin(3.14*i/(n-1))*128+128);
        dutyCycle2[i]= -(sin(3.14*i/(n-1))*128-128);
        printf("%f  %f\n", dutyCycle1[i],dutyCycle2[i]);
    }
    return 0;
}
```

Figure 43. Calculation of duty cycles for sinusoidal pulses in the digital implementation

```
128.000000  128.000000
171.757294  84.242706
210.242111  45.757896
238.817261  17.182741
254.039627  1.960372
254.075012  1.924990
238.919144  17.080858
210.398209  45.601788
171.948822  84.051186
128.203857  127.796143
```

Figure 44. C code output generating different duty cycles values for sinusoidal pulses in the digital implementation

The simulation in Quartus II of the bipolar inverter control signals generator is depicted in Figure 45. The control signals generate switching pulses with the same frequency and pulse width while exhibiting complementary logic levels. This complementary behavior ensures the efficient and proper operation of the bipolar inverter.

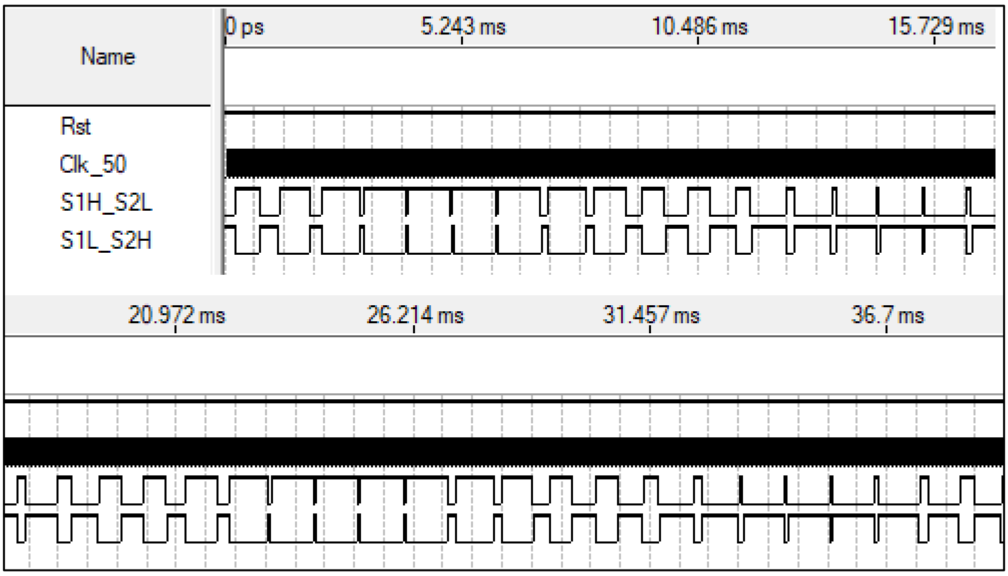


Figure 45. Control signals for the bipolar inverter generated in Quartus II

4.2.3. Experimental Results

Figure 46 shows the control signals for the bipolar inverter, as captured using an oscilloscope. On the other hand, Figure 47 illustrates the output voltage waveform of the inverter system. This voltage is represented in red and is generated by subtracting the blue and yellow signals at the terminals of the load V_A and V_B, respectively.

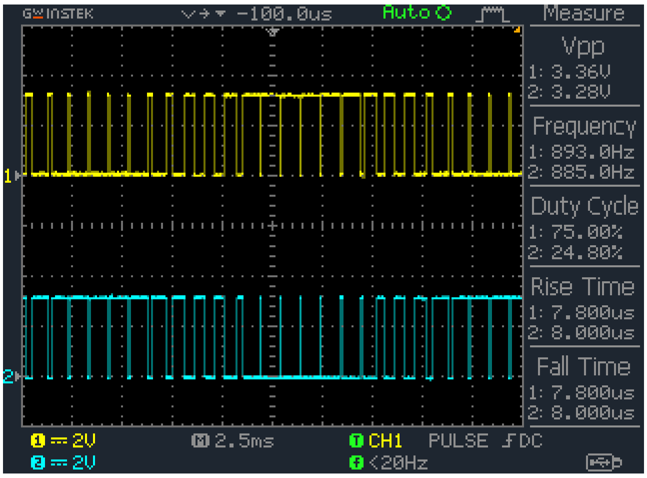


Figure 46. Control signals of the bipolar inverter

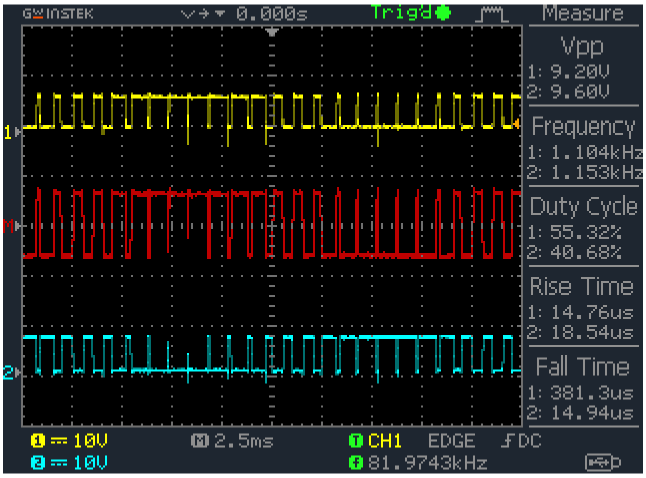


Figure 47. The output of the bipolar inverter (red signal) with voltage measurements at load terminals V_A (yellow signal) and V_B (blue signal)

4.3. Unipolar Inverter

4.3.1. System Design in Proteus

Figure 48 illustrates the circuit schematic of the unipolar inverter. This circuit shares similarities with both the square wave and bipolar inverters, including the H-bridge topology and switch arrangement. However, in the unipolar inverter, individual control of each power switch is required. The gates of lower switches are driven by the DC input power source of the system. This would be impossible if the DC input supply injected to the inverter was higher than 20V which corresponds to the maximum gate-source voltage the MOSFET can withstand.

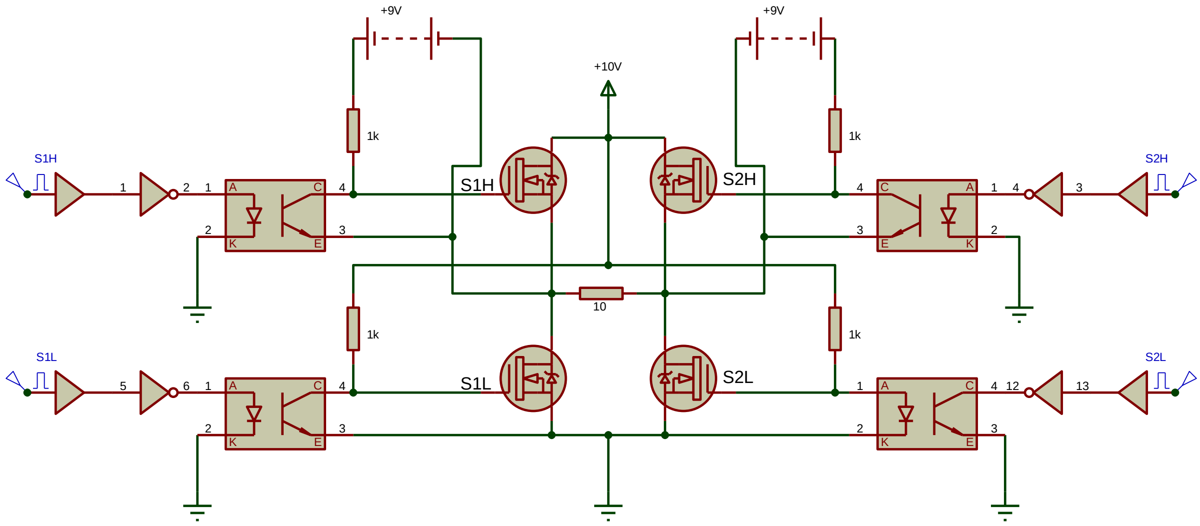


Figure 48. Circuit schematic of the unipolar inverter designed in Proteus software

4.3.2. System Design and Simulation in Quartus II

Figure 49 depicts the symbol file that presents the hardware logic utilized to generate the four control signals for the power switches. The design incorporates two ROMs responsible for storing the duty cycles of the control signals that drive the switches in the same leg. As illustrated in Figure 50, the control signals for the switches in the same leg are complementary, meaning that when one switch is activated, the other is deactivated. It is important to note that these signals operate at the same frequency, ensuring synchronized switching of the power switches.

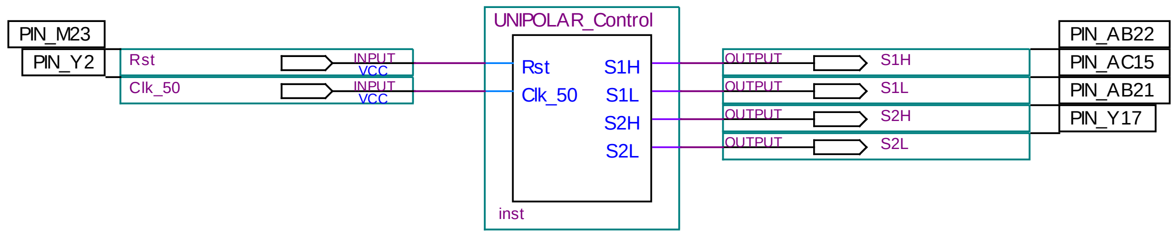


Figure 49. Block diagram of the control signals generator for the square wave inverter in Quartus II

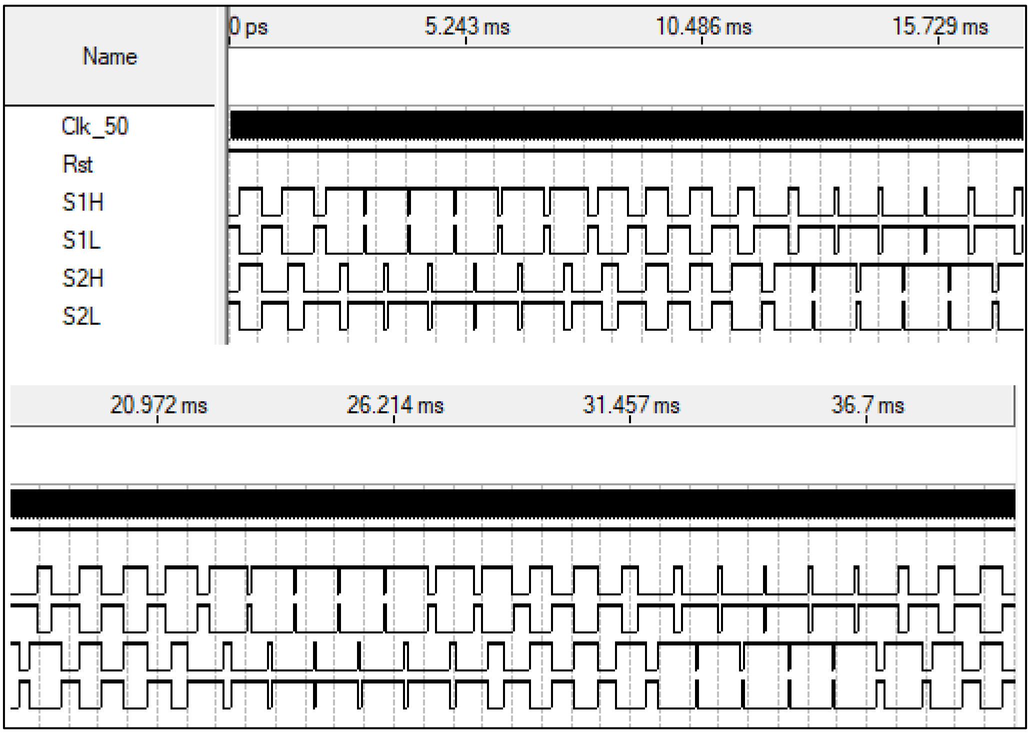


Figure 50. Control signals for the unipolar inverter generated in Quartus II

4.3.3. Experimental Results

Figure 51 depicts the control signals for the unipolar inverter, which were captured using an oscilloscope. In Figure 52, the output voltage waveform of the inverter system is presented. The red waveform represents the resulting output voltage, which is obtained by subtracting the voltage signals at the terminals of the load VA and VB (shown in blue and yellow, respectively). This configuration enables the generation of the desired AC output voltage from the DC input source.

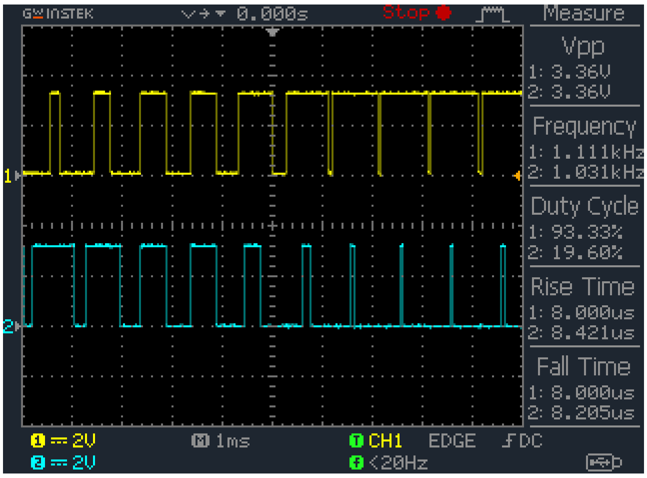


Figure 51. Upper switches control signals

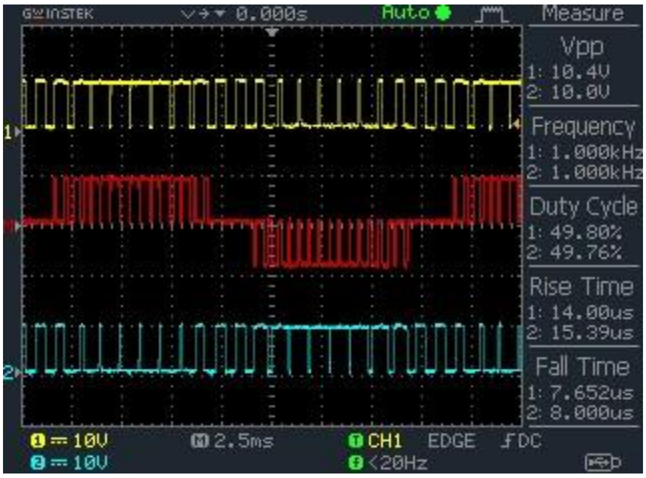


Figure 52. The output of the unipolar inverter (red signal) with voltage measurements at load terminals V_A (yellow signal) and V_B (blue signal)

Conclusion

This project successfully achieved the design, simulation, and implementation of a DC to AC single phase VSI using a full-bridge configuration and an FPGA-based control system. The full-bridge configuration demonstrated several advantages, including bidirectional current flow across the load and improved voltage conversion efficiency. The project also encompassed the exploration of different switching schemes, namely square wave, unipolar PWM, and bipolar PWM. Each technique offered distinct advantages and trade-offs in terms of inverter output waveform quality. The utilization of an FPGA-based control system provided flexibility and computational power for precise control over the inverter operation. Overall, this project highlights the importance of practical realization and underscores the significance of combining theoretical understanding with hands-on implementation to advance the field of power electronics.

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