National Institute of Electricity and Electronics
INELEC - BOUMERDES
DEPARTMENT OF RESEARCH

THESIS

Presented in partial fulfilment of the requirements of the

DEGREE OF MAGISTER

in Applied Electronics

by

Rachid BOUDERBALA

Charge-Extraction Technique for Studying the Surface-States in MOS Devices

Defended on November 14, 1992 before the jury:
President: Dr M. BENZOHRA, Professeur, USTO.
Members: Dr V. MITRA, Professeur, INELEC.
Dr A. OUADJAOUT, UDTS.
Dr K. HARICHE, INELEC.
Dr A. ABBABOU, USTHB.

Registration Number: 03/92

ACKNOWLEDGEMENTS

I would like to express my most sincere gratitude to my research adviser Dr. Ved Mitra for his untiring and continued interest and supervision throughout the project without which the present work could not be possible. The experience that I have gained under his able guidance is a valuable addition to my academic attainments.

I am especially grateful to Mr. Moufek, Director general of the institute for providing all the necessary research facilities and encouragement throughout this project. I am equally thankful to Dr. K. Harriche, head of research department for providing constant motivation and support. I must express my thankfulness to Dr. H. Bourdoucen for encouragement and useful suggestions from time to time. Thanks go to Mr. Y. Kribes for useful discussions and for providing us commercial devices. I must also acknowledge the cooperation and help by way of mutual discussions that I received from my collegue, A. Benfdila with whom much of this work was done in collaboration. Special thanks go to Dr. A. Amrouche (CDTA), for providing microscope prober and

devices used in this work. I am further indebted to H. Bentarzi whose presence as my collegue in the research group has been a source of inspiration and useful discussions. In addition, I would like to thank all the staff members who provided all support needed to achieve this work.
Finally, all this would have been impossible without the patience and continuous encouragements of my family.

PREFACE

The advancement in the fabrication technology of integration circuits and accordingly the reduction of feature size to micron and sub-micron range in VLSI using MOS technology has given rise to a new problem of hot electrons induced degradation of the device characteristics. Therefore the most current researches are directed towards the study of hot electrons and hot electrons induced effects in small channel MOS devices. An important aspect in such studies is the occurrence of traps at the $Si-SiO_2$ interface. Although a number of methods are now available to study the density and density distribution of these surface traps, but so far none of the methods is privileged to be called a universal method in the sense that it can be applied to all the MOS structures without any constraint. For example capacitance and conductance methods can be used in large area MOS capacitors. The charge pumping method can be used only in such MOSFET which satisfy certain geometrical condition according to which channel width to channel length ratio is quite larger than unity. Development of such a method, which could be equally applicable to MOS capacitors as well as to

MOSFETs without any geometric constraint, is yet to come out and in fact this was the motivation before our research adviser Dr. V. Mitra while assigning the present research project to us.

Obviously such a research project would be quite befitting to the need of the current technological and scientific development. However one more consideration, which had to be borne in mind and which laid a constraint on our research project, was the equipment facility available to us. The semiconductor research laboratory of INELEC, which was in use for the characterization of electronic devices before our admission, had two capital equipments of research standard, namely, a picoammeter (HP 4140B) and an HP 9836 computer besides some of other subsidiary measuring meters. All the above considerations and constraints then left before us almost a unique choice for our research project, that is, the study of surface states in MOS devices using charge pumping technique which requires mainly measurement of substrate current with precision.

However, the complete project had still many hurdles before it could be undertaken. Besides the need of a number of additional subsidiary measuring instruments and accessories having H.P. compatibility which were to be collected from various resources both inside and outside this institute, the main hurdle was how to procure MOS devices of known parameters. It was in fact a great challenge before us particularly in the period during which the sole fabrication

laboratory of this country, located at ENIE, SIDI-BELABBES, kept its fabrication work suspended due to certain reasons. We had no other option except to accept the challenge and struggle in search of a suitable source for the required devices outside our country.

After a long struggle we came in contact with certain researchers of Centre de Developement des Technologies Avancees (CDTA) Alger. This centre is engaged in the IC design by way of undertaking different design projects. The ICs so designed are then got fabricated by them in European Silicon Structures (ES2) France which is internationally reputed for IC fabrication. We utilized this opportunity and requested the concerned CDTA personnels to undertake a design project as per requirements of MOS devices needed by us. At last we succeeded in the procurement of MOS devices of our research requirements but not before initial six months of our research period. Some of these devices were in the chip form and needed a special microscope prober for their use which was also lent to us by CDTA. However we were not sure of eliminating all the external influences on the device during experimentation with this microscope prober inspite of covering it within a Faraday box designed and fabricated by ourselves in the metal shop of INELEC. Therefore we got a number of devices encapsulated by ES2 so that they could be safely used within the test fixture (HP 16055A) supplied by H.P. along with the picoammeter.

During the same period of our initial struggle we could

arrange other subsidiary H.P. compatible instruments and accessories enabling us to use the picoammeter, after necessary interfacing with the H.P. computer and other instruments, in its automated mode to yields necessary data for the implementation of charge pumping technique and the alternative technique which was eventually developed during the course of our research investigations.

In fact when we now look back on our initial struggle and extra efforts for arranging the equipment and devices for our research, we do not regret spending this period of six months on this part of our research project. We rather feel fully contented with our this additional training and experience that we have received from our research adviser and that has given us extra confidence for undertaking any large scale sophisticated research project. It is really a matter of great contentment and satisfaction for us to see that all work done and results obtained by us have made use of equipment and devices which satisfy full research sanctity and standard. We will feel furthermore contented if our efforts and labour could prove fruitful in achieving even a part of the expectations and motivation of our research adviser with which he assigned this research project to us.

On July, 22th 1992. R. BOUDERBALA

TABLE OF CONTENTS

CHAPTER 1 : INTRODUCTION.....1

CHAPTER 2 : MOS STRUCTURE.....8

2.1 Mos Structure: Qualitative Description.....8

2.2 Ideal Mos Structure.....8

2.3 Different Biasings of Ideal Mos Structure...10

2.4 C-V Characteristics of a Mos Capacitor.....13

2.5 Real Mos Structure.....24

CHAPTER 3 : OXIDE AND INTERFACE PROPERTIES

3.1 Silicon Dioxide in Mos Devices.....28

3.2 The Nature of Interface Trap and Oxide Charge.....31

3.2.1 Interface Trapped Charges.....31

3.2.2 Oxide Charge.....32

3.3 Influence of the Interface Trap charges on the Electrical Characteristics of Mos Devices.....34

3.3.1 Degradation.....34

3.3.2 Effect of Interface Traps on Electrical Characteristics.....36

3.3.3 Effect of Interface Traps on C-V Curves.....38

3.4 Control of Interface Trap Density.....39

CHAPTER 4 : MEASUREMENT TECHNIQUES OF INTERFACE TRAPPED CHARGES.....43

4.1 Introduction.....43

4.2 Interface Traps Density Extraction Methods..44

4.2.1 Determination of V_{FB}.....48

4.2.2 Accuracy and Limits of Interface Trap Density Extraction by C-V Methods.....51

4.3 Conductance Method.....54

4.3.1 General Principle.....55

4.4 Deep-Level Transient Spectroscopy.....60

4.5 Other Methods.....71

CHAPTER 5 : CHARGE PUMPING TECHNIQUE.....74

5.1 Introduction.....74

5.2 Basic Principle.....75

5.3 Methods of Measurements.....78

5.4 Groeseneken et al Model.....83

5.5 Limitations.....97

5.6 Other Developments in Charge Pumping Technique.....99

CHAPTER 6 : MEASUREMENTS AND EXPERIMENTAL RESULTS.....112

6.1 Introduction.....112

6.2 Measuring Equipment.....113

6.3 Experimental Devices.....117

6.4 Charge Pumping Experiments.....123

6.4.1 Experimental Set-Up.....123

6.4.2 Results and Discussion.....125

6.4.3 Conclusion.....145
6.5 An Alternative Experimental Approach.....145
CHAPTER 7 : CHARGE EXTRACTION TECHNIQUE FOR STUDYING THE INTERFACE TRAPS IN MOS DEVICES.....157
7.1 Introduction.....157
7.2 Theoretical Model.....158
7.3 Experimental Measurements.....173
7.4 Results and Discussion.....174
7.5 Conclusion.....186
CHAPTER 8 : CONCLUSION.....188

REFERENCES.....192

CHAPTER 1

INTRODUCTION

Surfaces of solids and interfaces between materials play an important role in a wide variety of phenomena. Because of the scientific importance and the economic impact of these phenomena, considerable efforts have been devoted to their study.

In 1935, Liandrat [1] proposed that the conductivity of a thin semiconductor layer could be modulated by an external field. The use of this field effect experiment provided a useful tool for the examination of some of the fundamental properties of semiconductor properties. The existence of a quantum states on a free semiconductor surface was demonstrated by Shockley and Pearson [2] in 1948 by a field effect experiment. The results of their experiment clearly demonstrated the importance of surface traps in determining

the degree of modulation that could be obtained in a surface field controlled device. Frosh and Derrick [3] found in 1957 that silicon dioxide acts as an effective barrier against commonly used impurities, thus preventing them from reaching the underlying silicon. This discovery is important because it forms the basis of present-day integrated circuit technology. Therefore, free surfaces are no more used, they have been replaced in 1960 by the solid-solid interface between the semiconductor and the grown oxide film of known composition and structure. This process is termed as oxide passivation. However the oxide layer so developed on the silicon surface is not free from different kinds of charge. The presence of these charges in the oxide alter the characteristics of the device developed underneath the protecting oxide layer by planar technology. In order to study the effect of the surface charge, it became important to know the structure of the surface, covering the devices fabricated by planar technology. The complete surface-structure is such in which a metal film is deposited over a SiO_2 layer protecting the silicon substrate. This metal-oxide-semiconductor briefly knwon as MOS structure is important in the study of various effects. Such studies eventually gave rise to the following three important devices which involve MOS structure.

1.Metal-oxide-semiconductor diode (MOS diode).

2.Metal-oxide-semiconductor field effect transistor (MOSFET).

3.Gate controlled P-N junction.

A detailed account of MOS structure will be presented in chapter 2.

Various types of charges, located in the silicon oxide layer and at the silicon-oxide interface have been found to cause instabilities and adversely affect the electrical characteristics of the devices. Their impact on the device performance and lifetime is becoming more pronounced as the device geometry is being reduced especially in short-channel MOSFET, while the power supply is not changed. In general, the origin of these charges has usually been linked with a disruption of the periodicity of the silicon lattice near the $Si-SiO_2$ interface. The level of these charges varies with different processing conditions depending on the oxidation rate, the crystal orientation, and oxide preparation. These charges within the MOS structure have been a subject of many investigations. The positive fixed charge, high electron trap density and large interface trap density act to decrease the carrier mobilities at the $Si-SiO_2$ interface by coulombic scattering. Reduced surface carrier mobilities are directly reflected in reduced MOS transistor transconductance [4]. The electron traps and interface traps are

also responsible for increased flicker noise measured in MOS transistors [5]. Subsequent techniques in controlling their density and their distribution in the energy band-gap have made possible the current widespread use of MOS devices in integrated circuit technology. Device characteristics affected by such charges include: threshold voltage, effective mobilities, current gain, junction leakage, frequency noise, and drain junction breakdown voltage all of which may affect the device performance and stability to some degree [4]. Such an influence is observed as a distortion and shift in the shape of the C-V curve. Most of the reliable results which have been obtained so far in thermally oxidized silicon, show that the doping type and concentration have a little effect on the variation of the density of the interface traps. However, a strong dependence on silicon orientation has been observed affecting the value of the trap density significantly in increasing order.

The understanding and characterization of $Si-SiO_2$ interface traps and their effect on MOS device performance is important in the present semiconductor technology. Thus, extensive research has been carried out on the nature, effect and the measurement of the interface trap properties. Various methods have been developed to determine the interface trap distribution. Of particular importance are the

conventional measurement techniques [6,7,8,9], the temperature method [10] and the DLTS technique [11]. However, some of these methods are unsatisfactory from the viewpoints of the sensitivity and/or the spectroscopic determination of the interface properties. Recently, a new method called charge pumping technique has been developed for studying the interface properties [12]. This technique [12] utilizes the dc substrate-current which is supposed to arise from charging and discharging of the interface traps at the $Si-SiO_2$ interface and appears to be quite promising for the extraction of the interface-trap density. However, the charge pumping technique is thought to suffer with certain limitations [13,14,15].

During the course of experimentation with the charge pumping technique, we observed a significant amount of substrate-current when the surface-region of the device is under the depletion regime. This substrate-current distinguishes itself from the oxide leakage-current arising from any of the commonly known processes [16]. There is a strong evidence that the resulting current is due to the non-steady state emission regime of carriers. These results led to the development of an alternative approach to the charge pumping technique for studying the interface traps in a MOSFET which is free from certain limitations. This new approach , which may be better called charge-extraction technique, can be

equally applied to MOS diodes without imposing any constraint on the device geometry.

The present thesis is devoted to give a comprehensive account of the charge pumping technique, scope and exploration of an alternative approach and accomplishment and development of a new technique called charge extraction technique for studying the interface properties of MOS devices. The whole thesis is presented in the form of 8 chapters. After introducing the subject in the present chapter, chapter 2 is devoted to the background study of the MOS structure itself covering all its essential features, characteristics and aspects which are relevant in the further development of the subject. In chapter 3, the properties of the $Si-SiO_2$ and, in particular, all those factors which contribute to the non-ideality of MOS structure are examined and their effect on the electrical characteristics are discussed. We end this chapter by examining briefly the impact that the fabrication technology may have on the generation and/ or on the reduction of these electrically active defects. Chapter 4 is centred around the capacitance methods. All those techniques, which are common in use such as the differentiation method [7], the integration method [17], the conductance method [9], and the DLTS technique [11], are presented in details whereas the others, which are more or less of historical interest only, are presented

briefly. Chapter 5 introduces the basic concepts needed to identify, understand, and analyse the phenomenon of charge pumping technique which is followed by a mathematical analysis and a few limitations of the technique. A brief account of the other developments on charge pumping technique is also presented. Chapter 6 covers the required instrumentation for the implementation and use of the charge pumping technique along with the details concerning the actual devices and the measuring set-up. The experimental results of the charge pumping technique are presented and discussed. Finally, the results obtained by the new technique are discussed and compared to those found by the charge pumping technique [12]. In Chapter 7, a theory of the new technique, called charge-extraction technique for studying the interface traps in MOS devices, is presented. Finally chapter 8 concludes with a discussion on the usefulness and future scope of the work presented in this thesis.

MOS STRUCTURE

2.1 MOS STRUCTURE: Qualitative Description

The MOS structure which is a particular form of the MIS structure, is one of the simplest heterostructure. It consists of an oxide layer usually thermally grown on a silicon substrate, an electrode called a gate made by vacuum deposition of a metal or by the deposition of polysilicon and an ohmic contact to the silicon substrate. Such a structure is shown on Fig. 2.1. The electrical properties of this structure will be discussed in relation with the application of the biasing voltage.

2.2 IDEAL MOS STRUCTURE

The ideal MOS structure is generally defined by the absence of any contact potential or work function difference between metal and semiconductor, and the absence of any

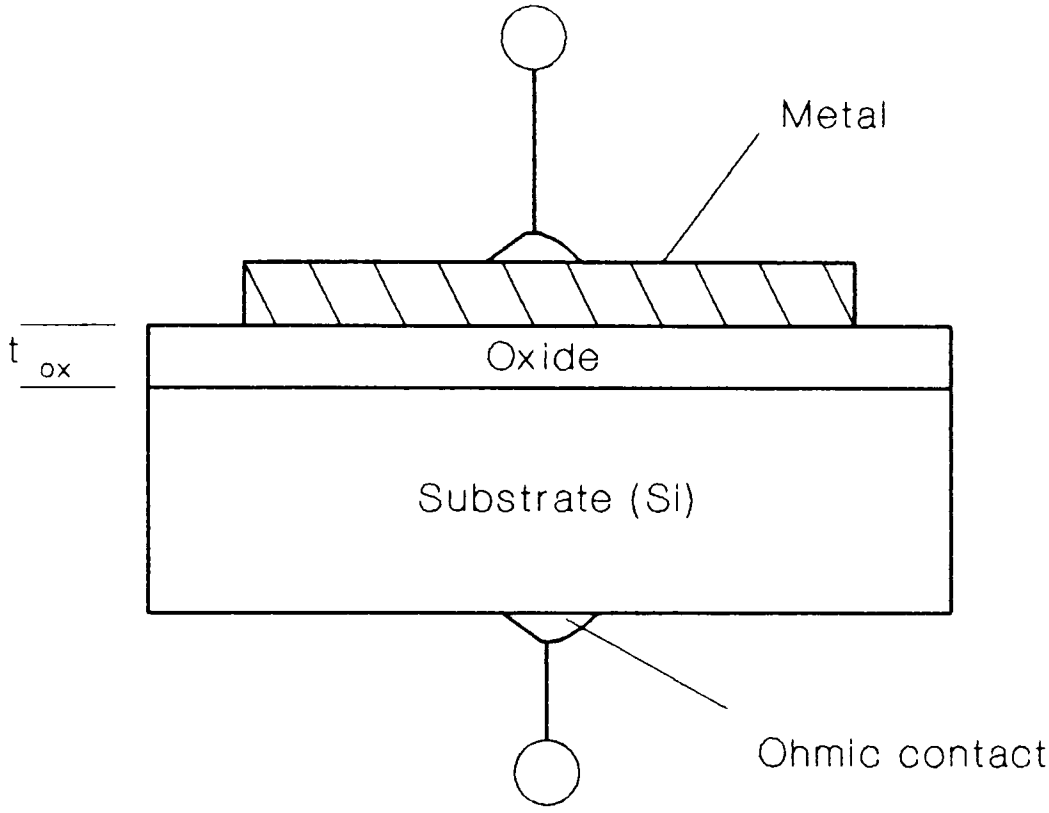


Fig. 2.1. Cross section of an MOS capacitor.

charge within the oxide or at the oxide-semiconductor interface.

At zero applied bias the bands are flat (Figure 2.2) and we have for both types of substrate (p- or n-type) the following condition:

$$\phi_{ms} = \phi_m - \left(\chi + \frac{E_g}{2q} \mp \psi_B \right) = 0 \qquad (2.1)$$

(the minus (-) and positive (+) signs inside the second term on the right hand side of the above equation stand for n-type and p-type respectively) where ϕ_m is the total work function; χ the semiconductor electron affinity; Ec the energy of the lower edge of the conduction band; Ev the energy of the upper edge of the valence band; E_g the band gap; q the electronic charge; and ψ_B the potential difference between the Fermi level and the intrinsic Fermi level E_i. Figure 2.2 illustrates the energy-band diagram of an ideal MOS structure. An applied voltage at the gate plate causes the bands to be bent downward or upward depending on the sign of this gate voltage. Figure 2.3 shows the energy-band diagram at the surface of a p-type semiconductor under the action of positive gate voltage producing a surface potential ψ_s.

2.3 DIFFERENT BIASINGS OF IDEAL MOS STRUCTURE

There are three regimes of interest when the MOS

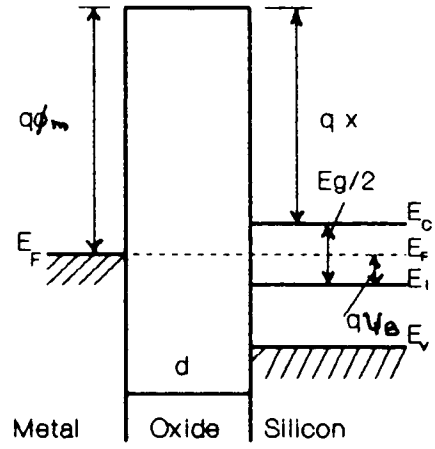


Fig.2.2 Energy-band diagram for ideal MOS structures at V = 0, n- type semiconductor.

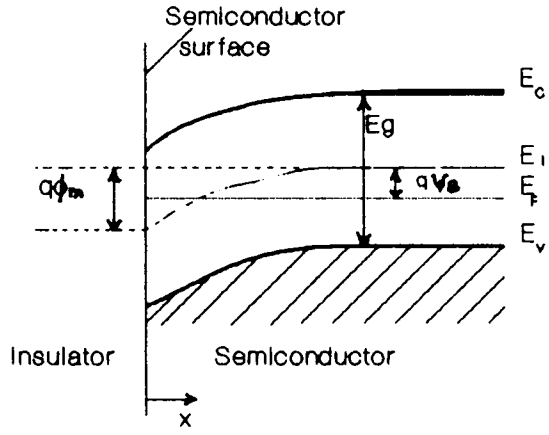


Fig.2.3 Energy-band diagram at the surface of of a p-type semiconductor.

capacitor is under biasing.

In the accumulation regime, the MOS capacitor is biased in such a way that the majority carriers are attracted towards the gate. For a p-type silicon, when a negative bias on the gate is applied, the negatives charges on the gate attract holes to the silicon surface to form an accumulation layer. The thickness of such layer depends on the bias and doping density, and is comparable to Debye length. Because of the increase in the concentration of holes, the Fermi level near the silicon surface will move to a position closer to the valence band edge.

When the gate bias is made positive with respect to flat-bands, holes are repelled from the silicon surface. As this process continues, the positive gate charges are balanced not by electrons, but by negative acceptor ions in the silicon surface depletion layer, so called because holes have been depleted from this surface region. As gate bias increases, the depletion layer widens to provide more acceptors ions to balance the gate charge. The Fermi level near the silicon surface will move to a position closer to the center of the forbidden region: This describes the depletion regime.

Finally, with increasingly positive applied voltage, the surface depletion region will continue to widen until electrons appear at the silicon surface in great numbers. The appearance of these electrons is a consequence of thermal

equilibrium. As holes are repelled from the silicon surface by the applied gate bias, electron density must increase and then form a thin inversion layer located very near the Si-SiO_2 interface depending on bias and doping density. Once inversion occurs, any further increase in positive gate charge is balanced almost entirely by the addition of electrons to the inversion layer, and the depletion layer no longer increases further in width. The Fermi level near the silicon surface will now lie closer to the conduction band edge. This describes the inversion regime. Figure 2.4 shows the energy-band diagram and the corresponding regimes for both n-type and p-type semiconductors.

2.4 C-V CHARACTERISTICS OF A MOS CAPACITOR

An MOS capacitor consists of a parallel plate capacitor with one electrode a metallic plate, called the gate and the other electrode, the silicon. The two electrodes are separated by a thin layer of SiO_2.

The MOS capacitor can be electrically modeled as an oxide, semiconductor, and interface state capacitance as shown in Fig. 2.5.

In the absence of any work-function difference, the applied gate voltage V_G will appear partly across the insulator and partly across the silicon. Thus,

$$V_G = V_{ox} + \psi_s \qquad (2.2)$$

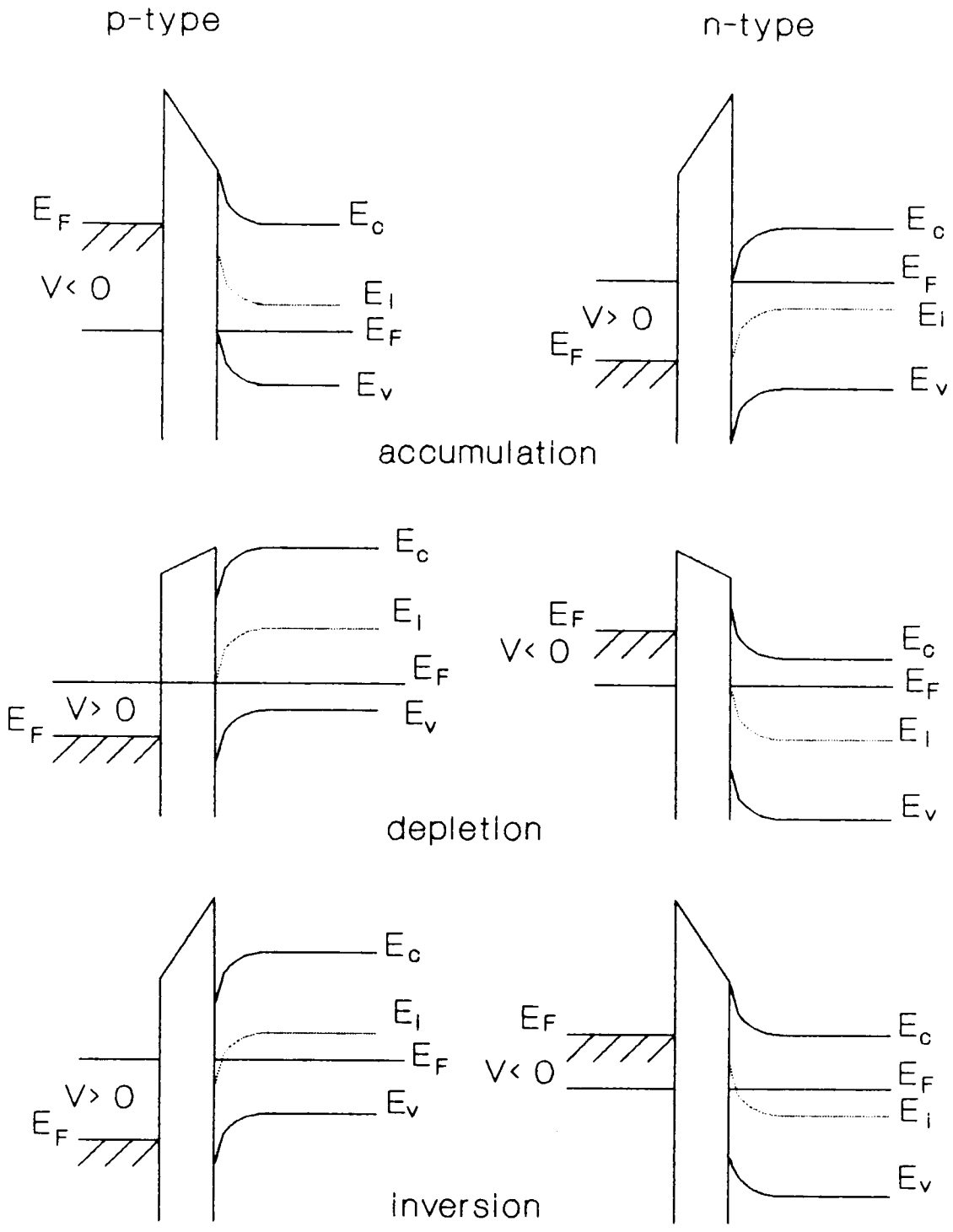


Fig. 2.4. Energy-band diagram for ideal MOS structure when V = 0 for both n-type and p-type semiconductors (after[16]).

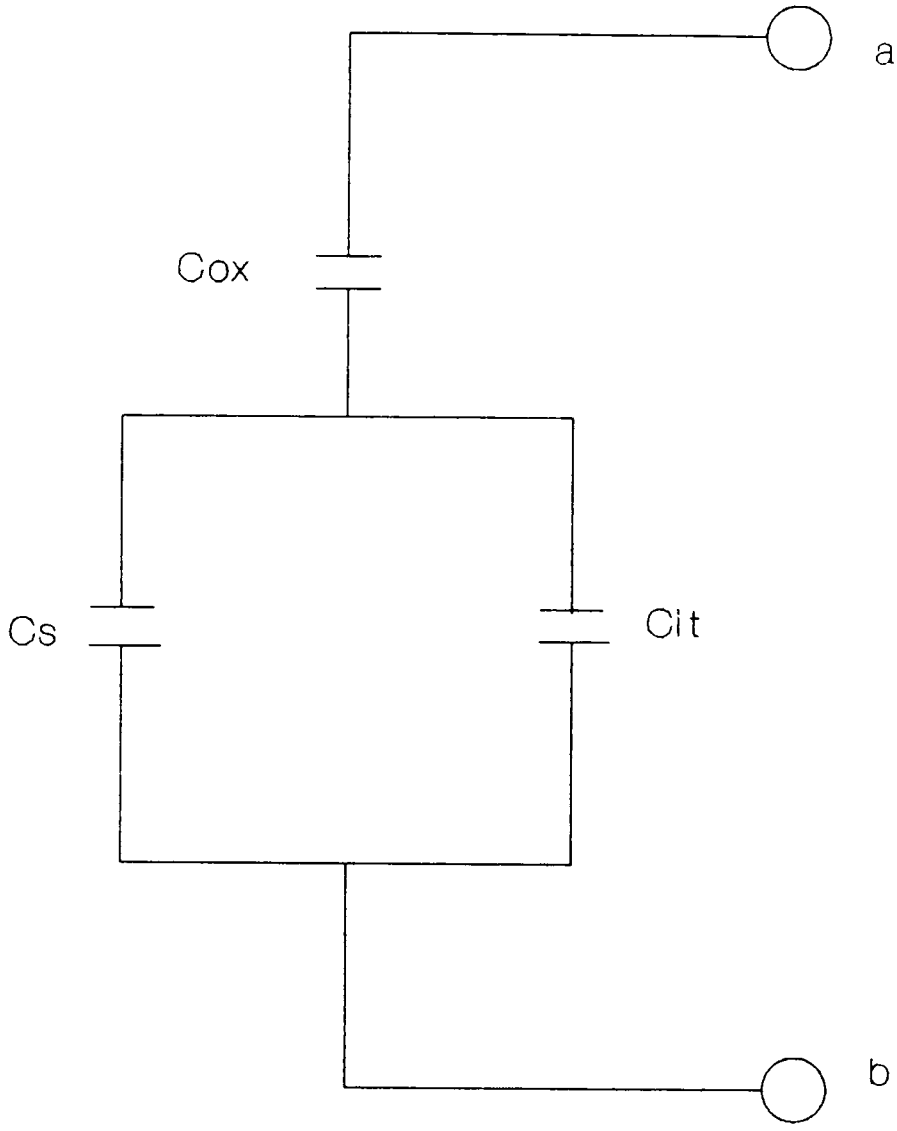


Fig. 2.5 Electrical model of MOS capacitor.

where V_{ox}, the potential difference across the insulator, is given by

$$V_{ox} = \frac{Q_s}{C_{ox}} \quad , \tag{2,3}$$

where Q_s is the surface charge and C_{ox} the oxide-capacitance.

For a given insulator thickness t_{ox}, the value of the oxide capacitance C_{ox} is a constant given by

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \quad , \tag{2.4}$$

where ϵ_{ox} is the dielectric constant. For a uniformly doped n-type substrate (N_d), Q_s can be found by solving Poisson's equation in a semiconductor and is given by [16]:

$$Q_s = \pm\sqrt{2q\epsilon_{si}\frac{kT}{q}\{N_d\{\exp\left(\frac{-q\psi_s}{kT}\right)+\frac{q\psi_s}{kT}-1\}+ \frac{n_i^2}{N_d}\left\{\exp\left(\frac{q\psi_s}{kT}\right)-\frac{q\psi_s}{kT}-1\right\}\}^{\frac{1}{2}}} \quad , \tag{2.5}$$

where ϵ_{si} is the dielectric constant of silicon, n_i the intrinsic carrier density of silicon, and kT/q the thermal voltage. The total capacitance C per unit area of the system

is given by

$$C = \frac{C_{ox} C_s}{C_{ox} + C_s} \tag{2.6}$$

where C_s the semiconductor capacitance, appearing in series to C_{ox}, is non-linear and much more difficult to be evaluated. This capacitance is a function of the total semiconductor space-charge Q_s and ψ_s and is given by

$$C_s = \partial \frac{Q_s}{\partial \psi_s} \tag{2.7}$$

Figure 2.6 shows the variation of the space-charge density Q_s as function of the surface-potential ψ_s. Combination of Eqs. (2.2), (2.3), (2.6), and (2.7) gives the complete description of the MOS device, and can be used to calculate low frequency C-V curves. Figure 2.7 shows a low frequency C-V curve calculated this way. The various regions, accumulation, depletion, weak inversion, and strong inversion and the surface band bending associated with each are shown. The low and high frequency C-V curves are practically identical in accumulation, depletion, and most of weak inversion because in these regions, minority carrier concentration in the depletion layer is negligibly small as compared to majority carrier concentration. The major difference between low and high frequency C-V curves occurs in weak to strong

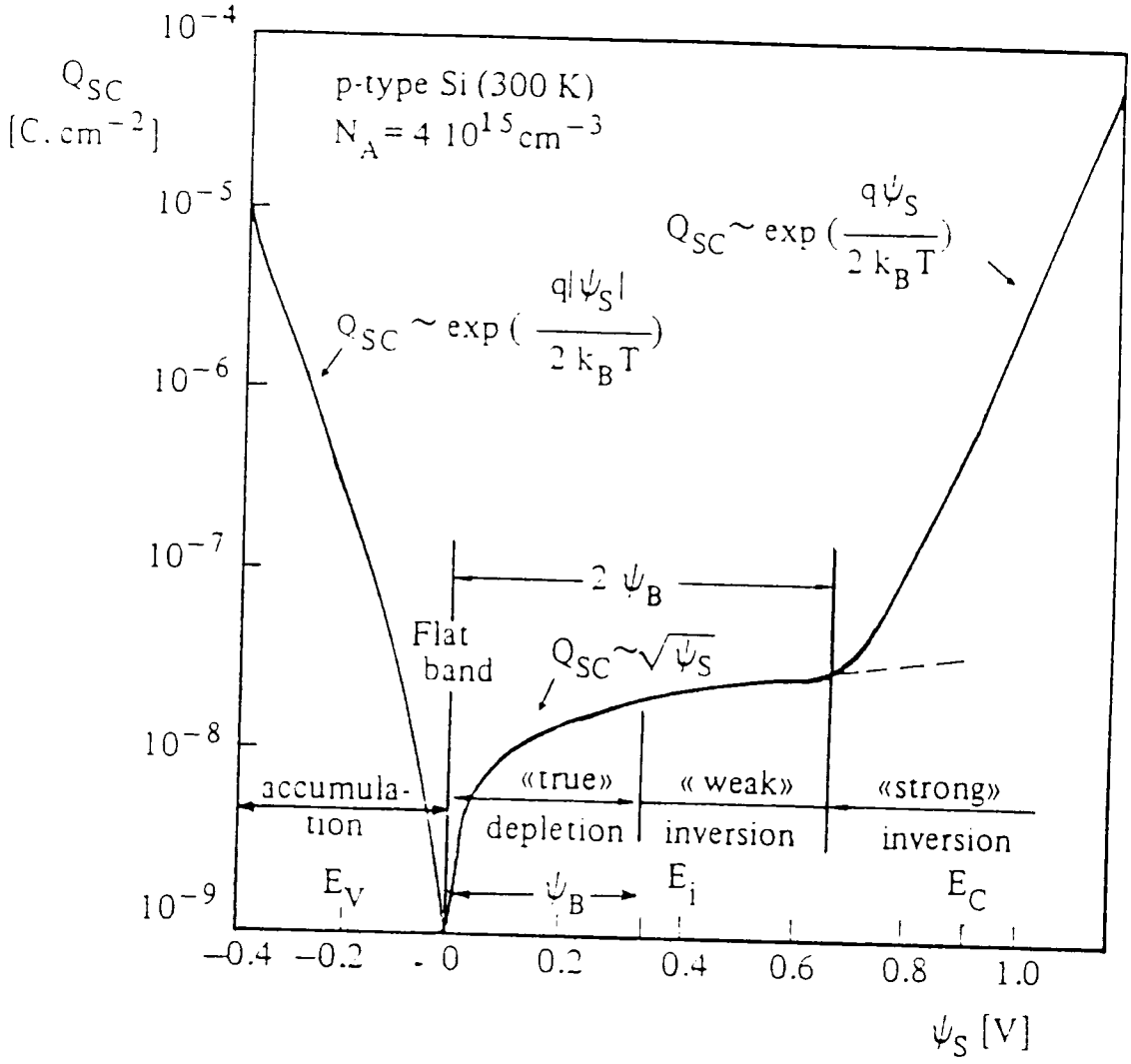


Fig.2.6 Space-charge density Qs in the semiconductor as a function of surface potential Us for p-type silicon, (After [16]).

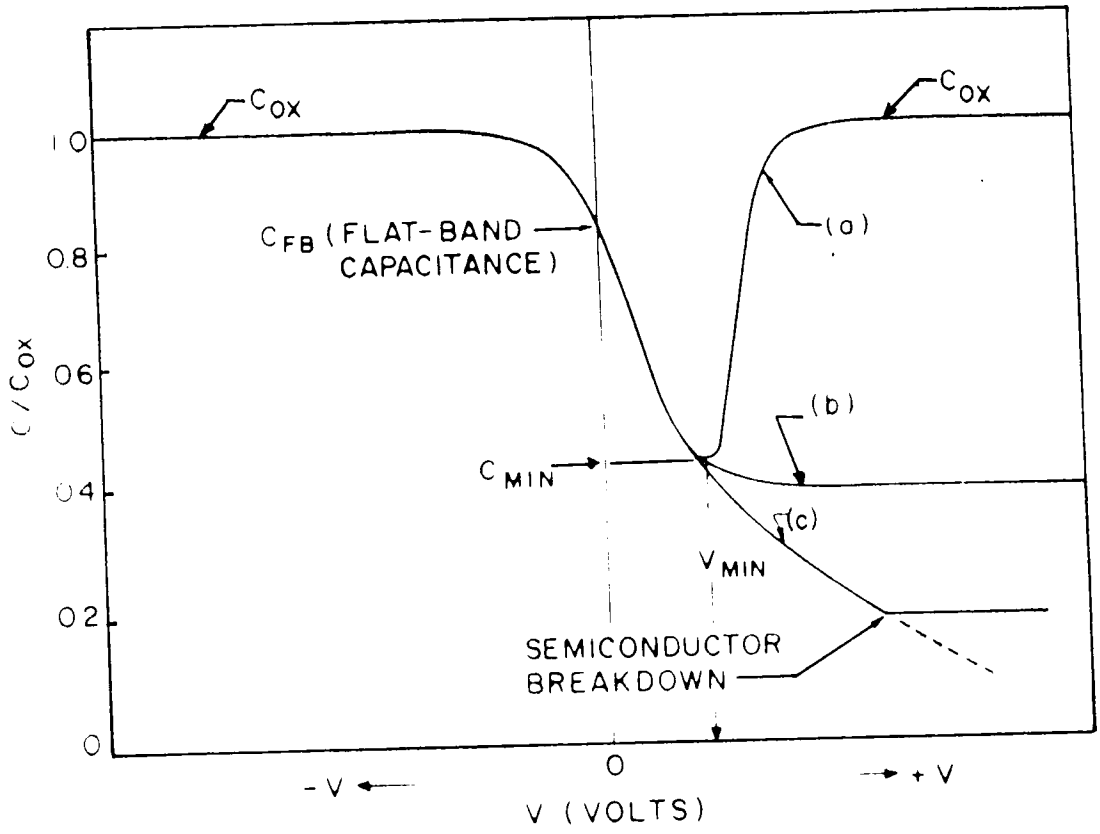


Fig.2.7 Normalized high and low frequency capacitance as a function of gate bias for an ideal p-type MOS structure (After [16]).

inversion where minority carrier concentration in the depletion layer becomes comparable to and exceeds majority carrier concentration. Minority carrier effect cannot be neglected in these regions.

For ($\psi_s = 0$), we have the flat-band condition, and Q_s is zero. In the case of an n-type substrate, the accumulation charge is negative when $\psi_s < 0$ and is given by

$$Q_{acc} \approx -Q_s \quad . \tag{2.8}$$

For $\psi_s > 0$, the semiconductor charge is positive and can be written as

$$Q_D + Q_{inv} \approx +Q_s \quad , \tag{2.9}$$

where Q_D is the depletion charge, and Q_{inv} is the inversion charge. In the depletion approximation $\left(\psi_s > \frac{3kT}{q}\right)$, the depletion charge, Q_D can be written as

$$Q_D \approx \sqrt{2q\epsilon_{si}N_a\psi_s} \quad . \tag{2.10}$$

and the C-V characteristic of the MOS capacitor takes the following form:

$$\frac{C}{C_{ox}} = \left(1 + \frac{2\epsilon_{ox}^2 \epsilon_o V_G}{q N_D \epsilon_{si} t_{ox}^2} \right)^{-\frac{1}{2}} , \qquad (2.11)$$

which is valid only for the depletion or weak inversion at the semiconductor surface.

For $\frac{3kT}{q} < \psi_s < \phi_B$, the inversion charge is negligible compared to the depletion charge. However, in the weak inversion, where $\phi_B < \psi_s < 2\phi_B$, the inversion charge increases rapidly, and $Q_{inv} \approx Q_D$ at the onset of strong inversion where $\psi_s = 2\phi_B$. In the strong inversion where $\psi_s > 2\phi_B$, the surface-potential remains essentially constant since Q_{inv} increases exponentially with ψ_s, and is given by

$$Q_{inv} \approx \sqrt{2q\epsilon_{si} \frac{kT}{q} \cdot \frac{n_i^2}{N_d} \exp\left(\frac{q\psi_s}{kT} \right)} \quad . \qquad (2.12)$$

Since the surface-potential is essentially pinned at $\sim 2\phi_B$ in strong inversion, the depletion charge is also fixed, and is given by

$$Q_D \approx \sqrt{2q\epsilon_{si} N_d (2\phi_B)} \quad . \qquad (2.13)$$

In the presence of interface charges at the Si-SO2 interface of the MOS capacitor, charge neutrality requires:

$$Q_G + Q_s + Q_{it} = 0 \quad , \qquad (2.14)$$

where Q_G and Q_s represent charges at the gate and in the semiconductor, respectively. Hence the capacitance is not the same but contains an additional interface trap capacitance, C_{it}. The interface trap capacitance, C_{it} is a function of the energy density of interface traps (D_{it}), measurement frequency (ω), and surface-potential (ψ_s).

The semiconductor and interface trap capacitances are functions of ψ_s. In addition, the interface traps and minority carriers in the inversion charge are controlled by frequency dependent Shockley Hall Read (SHR) generation-recombination processes. To prevent deep depletion of the substrate, all C-V measurements were started from the condition of strong inversion and swept to accumulation. At high frequency (say 100kHz), SHR generation-recombination processes are too slow to control the interface traps or inversion charge, and the contribution of D_{it} and Q_{inv} are negligible. Because the charges follow the slowly changing gate bias and mirrors some of the applied electric field, the effect of V_G on band bending is reduced. A larger swing is required to achieve the same band bending. Therefore, the capacitance measured at high frequency, C_{HF}, is simply given by

$$C_{HF} = \left[\frac{1}{C_{ox}} + \frac{1}{C_s(\omega)}\right]^{-1} \quad , \qquad (2.15)$$

where $C_s(\omega)$ is the effective semiconductor capacitance at

high frequency and is approximated by the capacitance due only to the accumulation charge for $\psi_s > 0$, and is given by

$$C_s(\omega)_{HF} \cong \frac{\partial Q_{acc}}{\partial \psi_s} \quad , \tag{2.16}$$

or due only to the depletion charge for $\psi_s < 0$, and is given by

$$C_s(\omega)_{HF} \cong \frac{\partial Q_D}{\partial \psi_s} \quad . \tag{2.17}$$

The quasi-static capacitance which is equivalent to the low frequency, C_{Qs}, is measured from the displacement current, I_d, due to a ramped bias voltage. The displacement current I_d flowing through the MOS capacitor in response to a time varying voltage V is related to the differential capacitance C_s by

$$I_d = C_{Qs} \frac{dV}{dt} \quad , \tag{2.18}$$

and can be written as

$$C_{LF} = C_{Qs} = \left(\frac{1}{C_{ox}} + \frac{1}{C_s + C_{it}} \right)^{-1} \quad , \tag{2.18}$$

which is simply the total capacitance due to all the compo-

nents.

2.5 REAL MOS STRUCTURE

The Fermi level plays an important role in formulating equilibrium conditions when two different systems of different energies are brought into contact. The combined system will be in thermal equilibrium only when E_F is the same in both parts. In general, the Fermi levels of different systems are different, then on contact there will be a flow of electrons from the system with higher initial E_F to the system with the lower initial E_F. This electron flow will continue until equality of the Fermi energies of the two systems is achieved. When no further net transfer of electrons occurs from one material to the other, the Fermi levels are equal. The bands are flat in the bulk semiconductor with the exception of the surface-region. The position of the Fermi level depends on the properties of the crystal and remains in its position despite band-bending. To bring the silicon surface to a flat-band condition or zero band-bending of such structure, it is necessary to apply an amount of gate voltage required to compensate for the difference in the work functions. This required voltage is called a flat-band voltage and is simply given by:

$$V_{FB} = \phi_{ms} \qquad (2.19)$$

There are a number of phenomena, so far neglected in the analysis of a metal-oxide semiconductor structure, such as the existence of metal-semiconductor work function difference, and various types of charges at the interface. For the ideal MOS diode, it was assumed that the work-function difference in Eq. (2.1) is zero. If the value of ϕ_{ms} is not zero, and if there exists an interface trap charge density Q_{it} at the Si-SiO2 interface, the external bias will be distributed across the oxide and the surface layer, such that

$$V_G = V_{ox} + \psi_s + \phi_{ms} \quad . \tag{2.20}$$

The effect of work-function difference ϕ_{ms} and of interface trap charge density Q_{it} can be cancelled by applying a gate potential equal to the flat-band voltage

$$V_{FB} = \phi_{ms} - \frac{Q_{it}}{C_{ox}} \quad . \tag{2.21}$$

Oxide charge is an important parameter in devices. The oxide charges can be mobile ions or fixed charges, which are spatially distributed in the oxide bulk with charge density $\rho(x)$ which varies with distance. Fixed oxide charge Q_f, is positive charge, primarly due to structural defects in the oxide depending on various processes such as oxidation ambient, temperature, cooling conditions, and on silicon crystal

orientation. This charge induces an image charge in the silicon surface. Therefore, the experimental capacitance-voltage curve will be displaced from the ideal theoretical curve by an amount

$$V_{FB} = \frac{Q_f t_{ox}}{\epsilon_o \epsilon_{ox}} \quad . \tag{2.22}$$

In electrical measurements Q_f can be regarded as a charge sheet located at the $Si-SiO_2$ interface. The mobile ionic charge Q_m, most commonly is caused by the presence of ionized alkali metal atoms such as sodium or potassium. This type of charge is located either at the metal-SiO_2 interface or at the $Si-SiO_2$ interface and can move from one edge to the other of the oxide layer under thermal-electrical stressing. Thus, the resulting movement causes a change in the electrical characteristics. In the case of one layer, the corresponding voltage that ensures flat-band voltage is given by [16]:

$$\partial V_{FB} = -\rho(x)\frac{x\,dx}{\epsilon_o \epsilon_{ox}} \quad . \tag{2.23}$$

The effects of all layers comprised between $x = 0$ and t_{ox} are added, and the gate voltage required to compensate this shift is given by [16]:

$$V_{FB} = -\int_0^{t_{ox}} \frac{\rho(x)x\,dx}{\epsilon_0 \epsilon_{ox}} \quad . \tag{2.24}$$

The total flat-band voltage, including the effect of work-function difference, interface trap charge and distributed oxide charge is then given by [16]:

$$V_{FB} = \phi_{ms} - \frac{Q_{it}}{C_{ox}} - \int_0^{t_{ox}} \frac{\rho(x)x\,dx}{\epsilon_0 \epsilon_{ox}} \quad . \tag{2.25}$$

CHAPTER 3

OXIDE AND INTERFACE PROPERTIES

3.1 SILICON DIOXIDE IN MOS DEVICES

Silicon MOS devices have achieved widespread acceptance and use throughout the microelectronics industry, which can be directly attributed to the many well-known advantages of silicon planar technology and, in particular, to the ease with which a silicon substrate can be thermally oxidized to form silicon dioxide, which can be used both as an insulating layer and a mask against the diffusion of impurities into the substrate itself.

The direct surface reaction of single-crystal silicon with oxygen to form thermal silicon dioxide (oxide) has several properties that are useful in the formation of Metal-Oxide-Semiconductor (MOS) devices. These properties have facilitated the manufacture of high performance MOS

transistors with high transconductance, high gate input resistance, good reproducibility, and fair stability [13,16,18]. In particular, the direct reaction of silicon with oxygen creates a sharp Si-SiO_2 interface with few dangling bonds. Since oxidation preserves the structure of the underlying silicon lattice, MOS devices have high surface carrier mobilities which are proportional to MOS transistor transconductance. Silicon dioxide has a large bandgap of approximately 8 eV that creates a 3.2 eV barrier to electrons and a 3.7 eV barrier to holes from silicon. Since oxide is an excellent insulator, MOS devices also have a large gate input resistance. Due to the strength of the Si-O bond, oxides are able to sustain large electric fields up to 12 Mv/cm. Finally, the kinetics of oxidation are well explained by the classical Deal and Grove model [19] and are easily controlled to give reproducible and uniform oxide thicknesses.

To achieve more complex and higher performance integrated circuits, the trend has been to scale down device geometries; especially, channel lengths and widths are decreased to increase circuit density, and gate dielectrics are thinned to maintain long channel characteristics. However, in order to maintain compatibility, the power supply voltage has remained constant resulting in high electric

fields and hot carriers that can damage MOS devices. In particular, exposing the MOS structure to ionizing radiation or to hot carriers has been shown to generate interface states and trapped charge in the gate oxide, which degrade device characteristics and eventually cause device failure [20]. This effect is especially troublesome in small geometry devices where large fields can accelerate carriers to high energies to overcome the $Si-SO_2$ interface potential barrier and getting trapped in the SiO_2 or generating interface traps. Although thick oxides are reasonable diffusion barriers to dopants, thin gate oxides are especially poor barriers to boron diffusion which complicates the use of p^+ doped polysilicon gates in MOS devices [21]. Recent interest has focussed on thin oxides (<200 A) for potential VLSI applications [22]. However, reducing oxide thicknesses introduces undesirable features while removing some of the disadvantages of using thicker oxides. Such problems have prompted more investigation in thin-gate oxide technology. Since mobile alkali ions can cause unpredictable flatband voltages shifts and dielectric stability, therefore special care is necessary to avoid alkali ion contamination during fabrication of MOS devices. Finally, the electrical strength of a silicon dioxide film is limited by the weakest region. In thin oxides, typical surface and interface irregularities can severely limit the electrical strength of the film

defects caused by radiation or similar bond-breaking process. They are located at $Si-SiO_2$ interface with energies falling, within the silicon bandgap. Interface trapped charge is in electrical communication with the underlying silicon and can thus be charged or discharged, depending on the surface potential and, consequently, will vary with the applied gate voltage. The total amount of interface trapped charge will also depend greatly on their distribution in energy throughout the bandgap and whether they are acceptor or donor types. Most of the interface trapped charge can be neutralized by low temperature (450°C) hydrogen annealing. Since Q_{it} is distributed through the energy bandgap another quantity the interface trap density D_{it} can be defined [16]:

$$D_{it} = \frac{1}{q}\left(\frac{dQ_{it}}{dE}\right) \quad . \qquad (2.1)$$

The density of interface traps can vary according to several factors such as silicon orientation [25].

3.2.2 Oxide Charges

There are three types of oxide charge Q_o, that are technologically important. The first type, oxide fixed charge Q_f is positive, and is primarly due to structural defect (ionized silicon) in the oxide layer less than 25 A from the

Si-SiO_2 interface. The density of this charge, whose origin is related to the oxidation process, depends on oxidation ambient temperature, cooling conditions, and on silicon orientation which affects the value of Q_f significantly, in an increasing order: (100)<(110)<(111) [26]. This density of fixed charge differs greatly from the interface trapped charge density in that its magnitude, for all practical purpose, is not a function of the applied gate voltage or surface potential in the silicon near the interface because the energy levels of the states associated with the fixed oxide charge density lie outside of the forbidden bandgap, so that their probability of occupancy will not be affected as the Fermi level sweeps across the forbidden band with variations in the applied gate voltage. Their ionized state gives rise to a positive charge which shifts the measured C-V curve by:

$$\Delta V = -\frac{Q_f}{C_{ox}} \qquad (2.2)$$

relative to a theoretical curve.

Unlike interface trapped charge, fixed oxide charge is not in electrical communication with the underlying silicon. Since fixed oxide charge density can not be determined in the presence of moderate densities of interface trap charge, it is only measured after a low temperature hydrogen treatment which minimizes interface trap density.

The second type, oxide trapped charge Q_{ot} may be positive or negative due to holes or electrons trapped in the bulk of the oxide. Trapping may result from ionizing radiation, avalanche injection, or other similar processes. Unlike fixed charge, oxide trapped charge is generally annealed out by low temperature (<500°C) treatment, although neutral traps may remain.

The third type, mobile ionic charge Q_m, most commonly is caused by the presence of ionized alkali metal atoms such as sodium or potassium. This type of charge is located either at the metal-SiO_2 interface, where it originally entered the oxide layer, or at the Si-SiO_2 interface, where it has drifted under an applied field. Drift can occur because such ions are mobile in SiO_2 at relatively low temperature and their number is limited by emission from the interface [13].

3.3 INFLUENCE OF THE INTERFACE TRAP CHARGES ON THE ELECTRICAL CHARACTERISTICS OF MOS DEVICES

3.3.1 Degradation

With the advancement of microelectronics technology, the study and use of MOS structure is becoming increasingly important. It is partly because MOSFETs have certain definite advantage over bipolar transistor on account of being unipolar and majority carrier devices. Partly it is due to additional advantage of MOS technology over the bipolar

technology which lies in the use of MOSFET as resistor also requiring much less space and low cost.

In CMOS technology the power dissipation can be tremendously reduced. However, with the reduction of feature-size in MOS technology especially in the submicron range, a serious problem is encountered due to degradation of device characteristics by hot-electrons. These degradations are many fold. The degradation may be in the substrate on the top of which the surface channel is produced, it may be in the oxide, or in the oxide-semiconductor interface. Among these three the most important is the degradation in the interface. This interface already carries some undesirable elements by way of defects, irregularity etc. due to mismatching of lattice in oxide formation over the semiconductor. These irregularities and defects on the interface give rise to surface states which lie within the bandgap. Its impact on the device performance and lifetime is becoming more pronounced as the device geometry is being reduced while the power supply is not changed. This results in electric fields in MOSFETs large enough to energize carriers flowing in the channel and to increase the generation of hot carriers. These hot carriers cause damage by way of creating interface states and trapping of the charge in the oxide. The combination of the two types of damage leads to a gradual degradations of electrical characteristics of MOSFETs

and eventual circuit failure. The hot carrier trapping mechanism includes bulk oxide trapping and interface trap generation involving both holes and hot electrons. It is believed that interface trap generation is the main cause of degradation.

3.3.2 Effect of Interface Traps on Electrical Characteristics

These interface traps can easily exchange charge with the silicon substrate and act as surface recombination centers; thereby causing a considerable increase in the leakage currents observed at the drain junction. These high drain junction leakage currents are undesirable because they decrease the sensitivity of a MOSFET to a weak signal and more power is consumed by the device than necessary for optimum performance. This leakage current is increased by an increase in D_{it}. Interface traps also act as scattering centers at the Si-SiO_2 interface; thereby reducing the effective carrier mobility in the channel and the field-effect mobility by immobilizing a portion of the carriers that would otherwise contribute to channel conductivity. Similarly, this effect can also contribute to a change in threshold voltage. The threshold voltage is increased in n-channel and decreased in p-channel devices. Interface traps can affect the drain junction breakdown voltage by

reducing the drain bias range over which the device can be operated. Besides they are responsible for the low-frequency (1/f) noise in MOS devices. This noise occurs because interface trap level occupancy fluctuates randomly. The resulting fluctuation in interface traps causes a corresponding fluctuation in channel charge density and thus channel conductance. This so-called flicker noise is dominated by interface traps for D_{it} above about $10^{11} cm^{-2} eV^{-1}$ and is determined by the volume of the channel for less than this value. Increasing channel volume decreases flicker noise power. The oxide fixed charge greatly affects the flat-band voltage and the threshold voltage of MOS capacitors and MOSFETs. Oxide fixed charge will tend to oppose the effect of interface traps in both n-channel and p-channel devices. It will not have any serious effects on most other important electrical characteristics. However, the effect of interface traps becomes increasingly important as degradation progresses. Therefore, the understanding and characterization of $Si-SiO_2$ interface traps and their effect in MOS device performance is important in the design of VLSI devices. One of the main reason why considerable disagreement still exists concerning the physical mechanisms of hot carrier degradation is believed to be the lack of a reliable technique to evaluate the damage at the interface caused by electrical stress or

radiation. Indeed, most of the studies have mainly based their conclusions about the nature of the degradation on the shift in current characteristics of the devices.

3.3.3 Effect of Interface Traps on C-V Curves

The influence of interface traps can be seen from the simplified equivalent circuit shown in Fig.3.1. The capacity of the semiconductor consists of two parallel parts, the space-charge capacity C_D and the interface trap capacity C_s which has the interface trap resistance R_s in series. The quantities C_D, C_s, and R_s are dependent on surface-potential and change when the surface field is changed. C_D can be calculated for each value of the surface-potential.

The interface trap parameters are unknown and have to be determined for each surface-potential by measuring the MOS capacitor, the MOS conductance or both. However, the impedance of the MOS capacitor is no longer similar to that of pure capacitance: a loss mechanism involved in carrier capture and remission gives rise to the occurence of a conductance in parallel to the MOS capacitance. In practice, the information contained in capacitance measurements is difficult to extract because the semiconductor capacitance C_D, affected by interface traps, occurs in series with the oxide capacitance, C_{ox}. It is known that only interface traps within a small energy range of the order of kT on either

side of the Fermi level contribute to the capacitance. For this to be confirmed, the change of surface-potential due to the applied ac voltage has to be less than kT/q. Since kT is about 26 meV at room temperature, compared to a width of the entire forbidden band equal to 1.1 eV, it is obvious that this technique can be used to probe the energy distribution of interface traps.

The influence of interface traps on the MOS curve is shown in Fig.3.2a. This influence is threefold: (a) The interface traps give an additional capacitance ΔC. (b) They cause a frequency dispersion of the curve. (c) They change the voltage axis by changing the dependence of ψ_s on voltage V.

The additional capacitance and the frequency dispersion is obvious from Fig. 3.2a. The influence on the voltage is explained in Fig.3.2b. When interface traps are present, the electric field E_{ox} in the oxide is higher than the field in the semiconductor surface. Therefore, more charges in the metal electrode are necessary to create a certain surface fields E_s in the silicon. Thus, the voltage that sets up this value of surface-potential ψ_s is higher by ΔV.

3.4 CONTROL OF INTERFACE TRAP DENSITY

The dominant parameters controlling the interface properties are the technological parameters for the oxide

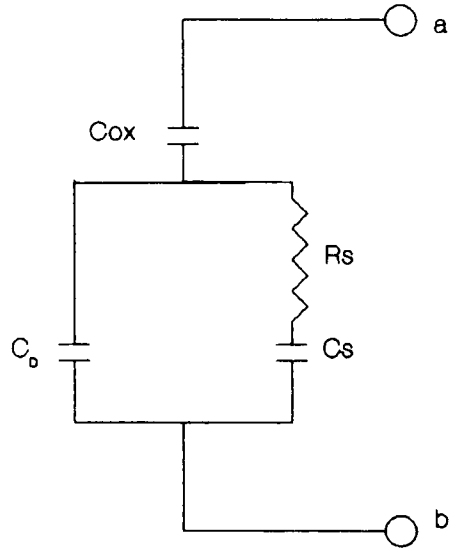


Fig. 3.1. Equivalent circuit of MOS structure with interface traps. Interface traps contribute Cs and Rs .

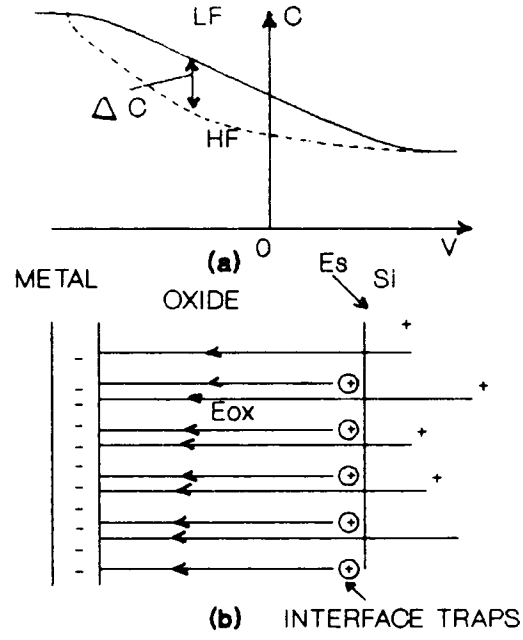


Fig.3.2 (a) Influence of interface traps on MOS curve (b) Electric field distribution in presence of interface traps.

growth. The oxide growth proceeds by three consecutive reactions, which are the transfer of oxygen into the oxide already formed, the diffusion of oxygen through the oxide, and the reaction of oxygen with silicon at the interface to form SiO_2.

Interface traps and oxide fixed charge characteristic of thermally grown SiO_2 can adversely affect device performance if their densities are not controlled. The influence is compounded by the fact that their densities can change with time during device life, thus posing a stability problem. To optimise device performance and stability, one must be able to control the oxide and interfacial properties during fabrication and keep these properties stable during device operation.

The interface trap level density can be controlled or minimized by using a high oxidation temperature and a (100) orientation, but it must be reduced further by annealing. There are two annealing methods effective for reducing D_{it} after thermal oxidation: the low temperature postmetallization anneal [25,27] and the high temperature postoxidation anneal [26]. Both of these methods are widely used. It was shown [26] that D_{it} and Q_f produced by thermal oxidation have the same silicon surface orientation dependence. The lowest values of Q_f and D_{it} are obtained for (100) orientation, and the higher values were consistently measured for

(111) silicon. The (100) orientation is the most widely used in integrated circuit technology.

It is also possible to reduce oxide trapping by making a suitable design for the geometry of the structure to avoid high fields due to hot carrier in short-channel. Therefore, many device structures have been proposed to improve MOSFET performance with higher response speed, lower power consumption, more reliable operation, and higher handling capability.

CHAPTER 4

MEASUREMENT TECHNIQUES OF INTERFACE TRAPPED CHARGES

4.1 INTRODUCTION

A number of techniques for the measurement of trapped charge on the Si-SiO_2 interface of MOS structures are available. Most of them employ the device in the form of a MOS capacitor and are based on the measurement of capacitance and conductance as a function of bias voltage, frequency, and temperature. In general these techniques, including all those which are better suited to MOS capacitors [6-9] as well as those which are solely based on MOS transistor function itself [28,29,30] are not only limitedly applicable because of a lack of sensitivity, incomplete information or inability to treat non-uniform spatial distribution. A very few techniques use measurement of substrate current [31,32]. Recently, it has been shown that the charge pumping

technique [12], which utilizes the substrate current in a MOSFET, for the determination of the interface properties, is capable of independently providing the amount of the charges that have been trapped in the $Si-SiO_2$. This technique will be described in chapter 5.

The discussion of experimental techniques in this chapter will be centered around the capacitance methods. All of these techniques, which are more common in use such as the differentiation method by Terman [7], the integration method by Berglund [17], the conductance method [9], and the DLTS technique [11], will be presented in details whereas the others which are more or less of historical interest will be presented only briefly in this chapter.

4.2 INTERFACE TRAPS DENSITY EXTRACTION METHODS

The interface trap density between flatband ($\psi_s = 0$) and the onset of the strong inversion ($\psi_s = 2\phi_B$) can be accurately extracted from C-V measurements by the following three methods:

1. The Terman method [7] is based on the comparison between the hypothetical high frequency C-V curve with interface traps to and an ideal C-V curve. The ideal curve is calculated for the same doping density and oxide thickness but without interface traps. This ideal C-V curve is calculated by the help of Eq.(2.15). However, the capacitance C_s in Eq.(2.15) is a known function of band bending ψ_s, and hence

can be calculated with the help of Eqs.(2.5) and (2.7). Therefore, a theoretical plot of C_{HF} versus ψ_s is made and compared with the measured plot of C_{HF} versus V_G. The amount of stretchout, as measured by ΔV between the ideal and the measured high frequency C-V curves at a particular surface-potential, determines the interface trap density D_{it}. The additional charge, ΔQ_{it}, generated by interface traps is given by [7]:

$$\Delta Q_{it} = C_{ox} \Delta V \quad , \tag{4.1}$$

where C_{ox} is the capacitance per unit area of oxide-layer. The interface traps density per unit surface potential ($\Delta \psi_s = 1eV$) is given by [7]:

$$D_{it} = \frac{1}{q} \frac{dQ_{it}}{d\psi_s} \quad , \tag{4.2}$$

where q is the electron charge.

2. The low frequency method proposed by Berglund [17], makes it possible to determine the conductor surface-potential ψ_s as a function of the applied voltage V_G directly from low-frequency differential capacitance measurement, and no differentiation is required to determine the density of interface traps, D_{it}. In the low-frequency, the surface

potential corresponding to the bias voltage can be determined without assuming a doping profile. Since an incremental increase in V_G causes an incremental increase in ψ_s through a capacitive voltage divider (see Fig.2.5) one can write

$$\partial \psi_s = \frac{C_{ox}}{C_{ox} + C_s + C_{it}} \partial V_G \quad . \qquad (4.3)$$

Rearranging Eq.(4.3) in terms of C_{LF} given by Eq.(2.18) and integrating under the condition that $\psi_s = 0$ at $V_G = V_{FB}$ yields

$$\psi_s = \int_{V_{FB}}^{V_G} \left(1 - \frac{C_{LF}}{C_{ox}} \right) dV_G \quad . \qquad (4.4)$$

Equation (4.4) indicates that the surface potential at any applied voltage can be determined by integrating a curve of $\left(1 - \frac{C_{LF}}{C_{ox}}\right)$. It is important to notice that Eq.(4.4) is valid only when the interface traps are in equilibrium at all times during the measurement of C(V). The energy density of interface traps, D_{it} (states/$cm^2 eV$), can be expressed in terms of the capacitance C_{it} of the interface traps as

$$D_{it}(\psi_s) = \frac{C_{it}(\psi_s)}{q} \quad . \qquad (4.5)$$

Solving Eq.(2.18) for C_{it} and replacing in Eq.(4.5) gives

$$D_{it}(\psi_s) = \frac{1}{q} \cdot \{(\frac{1}{C_{LF}} - \frac{1}{C_{ox}})^{-1} - C_s(\psi_s)\} \quad , \qquad (4.6)$$

where $C_s(\psi_s)$ is the semiconductor capacitance.

Determination of $D_{it}(\psi_s)$ from Eq.(4.6) needs C_{ox}, C_{LF} and $C_s(\psi_s)$. Whereas C_{ox} can be obtained from the oxide-data and C_{LF} from the experimental C-V curve, the quantity $C_s(\psi_s)$ needs certain manipulation. This quantity $C_s(\psi_s)$ can be obtained with the help of Eqs.(2.5) and (2.7) if the surface-potential ψ_s is known. The determination of C_{LF} from low-frequency C-V curves also needs the value of ψ_s. The value of ψ_s is obtained with the help of Eq.(4.4) provided the flatband voltage V_{FB}, which form the lower limit of the integral of Eq.(4.4) is known. Therefore main quantity of interest which remains to be worked out in the determination of D_{it} is V_{FB}. The determination of V_{FB} will be described later in this section.

3. The energy density of interface traps also can be calculated by using both high and low frequency CV curves. Assuming that no traps contribute any capacitance at high frequency, from Eq.(2.15) we can obtain a measured value of C_s given by

$$C_s(V_G) = \left\{ \frac{1}{C_{HF}(V_G)} - \frac{1}{C_{ox}} \right\}^{-1} \quad . \qquad (4.7)$$

Therefore, by substituting for $C_s(V_G)$ in Eq.(4.6), D_{it} becomes

$$D_{it} = \frac{1}{q} \left\{ \left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}} \right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}} \right)^{-1} \right\} \quad . \qquad (4.8)$$

The distribution of interface traps in the bandgap is determined by calculating the surface potential ψ_s at which C_{LF} and C_{HF} are measured and as stated earlier ψ_s can be obtained with the help of Eq.(4.4) provided the flatband voltage V_{FB} is known.

4.2.1 Determination of V_{FB}

The LFCV and HFCV measurements are used to extract the flat-band voltage, V_{FB}, as needed in Eq.(4.4) for the determination of ψ_s and hence the density of interface traps D_{it}. However, before V_{FB} can be determined, it needs knowledge of another quantity the flat-band capacitance C_{FB} which itself is a function of the substrate doping concentration N_a. The semiconductor capacitance acquires a minimum value $(C_s)_{min}$ when the depletion layer acquires the maximum width W_{max} so that

$$(C_s)_{min} = \frac{\epsilon_s A}{W_{max}} \quad , \tag{4.9}$$

and

$$W_{max} = \left[\frac{4\epsilon_s |\phi_B|}{q N_s} \right]^{\frac{1}{2}} \quad , \tag{4.10}$$

where ϵ_s is the silicon dielectric constant and A the device area. The bulk potential $|\phi_B|$ can be represented in terms of the substrate doping concentration N_a and intrinsic concentration n_i as

$$|\phi_B| = \frac{kT}{q} \ln\left(\frac{N_s}{n_i}\right) \quad , \tag{4.11}$$

where k is the Boltzmann constant and T the temperature in Kelvin. Using Eq.(2.15), the minimum capacitance in a HFCV curve can be written as:

$$(C_{HF})_{min} = \left[\frac{1}{C_{ox}} + \frac{1}{(C_s)_{min}} \right]^{-1} \quad . \tag{4.12}$$

Substituting and eliminating ϕ_B, W_{max}, and C_a give the following relationship for N_a:

$$N_s = \frac{4kT}{q^2 \epsilon_s A^2} \left(\frac{C_{ox}(C_{HF})_{min}}{C_{ox} - (C_{HF})_{min}} \right)^2 \ln \frac{N_s}{n_i} \quad . \qquad (4.13)$$

The capacitance of the MOS device at $\psi_s = 0$, which is called the flatband capacitance C_{FB}, is built up of two capacitors. These two capacitors, one of which is the oxide capacitance C_{ox} and another the flatband capacitance of semiconductor C_{FBS}, are connected in parallel and so

$$C_{FB} = \frac{C_{ox} C_{FBS}}{C_{ox} + C_{FBS}} \quad . \qquad (4.14)$$

In fact the flatband capacitance of the semiconductor is the capacitance of the surface layer of the substrate within a distance equal to the Debye length L_D from the interface so that

$$C_{FBS} = \frac{\epsilon_s A}{L_D} \quad , \qquad (4.15)$$

where L_D is given by

$$L_D = \left(\frac{kT \epsilon_s}{q^2 N_s} \right)^{\frac{1}{2}} \quad . \qquad (4.16)$$

The nearest gate voltage corresponding to the capacitance CFB on the HFCV curve is the required value of the flatband voltage V_{FB}. The value of V_{FB} so obtained can be used in Eq.(4.4) to obtain a relation between ψ_s and V_G which in turn can be utilized to obtain the value of C_{HF} and C_{LF} from their respective experimentally measured HFCV and LFCV curves. Finally after knowing C_{HF} and C_{LF} at any desired value of ψ_s, the corresponding value of D_{it} can be obtained using either of the relations (4.6) or (4.8).

As the determination of D_{it} involves the use of several relations, of which some are in closed form and others are not such as Eq.(4.13), the whole analysis needs a certain program to be developed which after using the stored data can yield automatically the values of D_{it} at different values of ψ_s.

4.2.2 Accuracy and Limits of Interface Trap Density Extraction by C-V Methods

The extraction of interface density from the capacitance methods has several limitations in accuracy. In Terman method [7], one source of error is the need of a theoretical C-V curve which makes use of a certain assumed doping profile. Spatial nonuniformities at the charge distribution in the oxide along the interfacial plane also can cause an error in the calculated $C_s(\psi_s)$. Another error is failure to measure a true high frequency C-V curve, particularly a

problem near flatband or in accumulation. As flatband is approached, majority carrier density increases, making capture more rapid and interface trap time constant shorter. The determination of C_{ox} also causes a problem, since in the case of an oxide, generally we consider the highest value of the measured capacitance at the lowest frequency. However, its main advantage lies in the rapidity and the great simplicity. It becomes quite inaccurate and unreliable for low interface trap density (less than $10^{11} cm^{-2} eV^{-1}$), because the shifting between the theoretical and experimental C-V curves is very small to be exploited.

Like the high frequency capacitance method, the Berglund method [17] needs a theoretical estimate of semiconductor capacitance C_s, which is most easily done when assuming doping profile. Usually this profile is nonuniform due to impurity redistribution during oxidation process. Such doping nonuniformity leads to an underestimate of D_{it} (error in extracting D_{it}). A more serious error occurs when the theoretical C_s is subtracted from the measured ($C_s + C_{it}$). Therefore, an error in ψ_s leads to the use of a value of C_s corresponding to the wrong band bending. This error will be most serious where (C_{it}/C_s) is small or where C_s is a rapid function of band bending. Another serious error is due to the wrong calculation of V_{FB} at the matching point where $\psi_s = 0$, which can produce erratic D_{it} values, especially around flatband and accumulation regions, and occasionally

near strong inversion. However, both methods suffer from the inaccuracy introduced by an assumed doping profile.

The combined high-low frequency method [8] is able to extract C_{it} as a difference in measured capacitance without assuming any particular doping profile and the need for a theoretical computation of C_s is eliminated. Since the interface trap density is calculated from the difference in HFCV and QSCV (or LFCV), the method erroneously counts inversion charge (Q_{inv}) as interface traps. As inversion is approached, the HFCV does not include capacitance due to the inversion layer, since minority carriers do not respond. However, the LFCV curve does contain this inversion layer capacitance C_I; thereby counting C_I as interface trap capacitance. The difference taken between LFCV and HFCV curve therefore includes this term ($C_{it} + C_I$). The value of the interface traps density D_{it} extracted from this capacitance will be in error unless C_I is negligible compared to C_{it}. This error becomes intolerable and places a limit on the surface potential at the onset of strong inversion. Towards accumulation, both HFCV and LFCV increase as C_s increases. Therefore, C_{it} is difficult to extract as a small difference between two large numbers. This places a limit on the surface potential at flatband. The most reliable measurement of interface trap density is at midgap where $\psi_s = \phi_s$ (in the range extending from mid-depletion to weak inversion). This method is effective only with a large

gate area. Its main advantage is that C_s is determined experimentally from a high frequency C-V measurement for the same gate bias at which ($C_s + C_{it}$) is measured using a LFCV measurement. Therefore, the subtracted C_s automatically corresponds to the correct band bending.

4.3 CONDUCTANCE METHOD

This method has been proposed by E.H. Nicollian and Goetzberger [9]. It is based on the steady state loss due to the capture and emission of carriers by interface traps. This energy loss is measured as an equivalent parallel conductance G_p. This conductance related to the loss is proportional to the capacitance C_s (associated to the interface traps) and inversely proportional to the characteristic time τ. This technique provides more and accurate information about interface traps, particularly when the density is low such as in thermally oxidized Si-SiO_2 system. A fundamental property of this advanced technique is not only the capacitance, but also the conductance or the phase. Both are related by the Kramers-Kronig relation. Interface trap density and capture cross section are obtained from measurements of the MOS admittance as a function of voltage and frequency of the gate bias. However, a large number of measurements are required to achieve such detailed results,

and only that portion of the energy gap which lies between mid-gap and the Fermi level can be conveniently probed with this technique.

4.3.1 General Principle

The principle of the MOS conductance technique can be easily understood by the simplified equivalent circuit shown in Fig.3.1. It consists of measuring the admittance of the MOS structure at different frequencies while keeping the bias voltage and temperature constants, and to extract the equivalent parallel conductance G_p. The measured admittance Y_m of the MOS capacitor is given by

$$Y_m = G_m + j\omega C_m \quad , \tag{4.17}$$

where G_m is the measured equivalent parallel conductance, C_m the measured capacitance, and ω the angular frequency of the applied gate voltage signal. Converting this admittance to an impedance, subtracting out of it the reactance of the oxide capacitance, and converting back to an admittance yields the required equivalent parallel conductance G_p as its real part. Thus

$$\frac{G_p}{\omega} = \frac{\omega C_{ox}^2 G_m}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \quad , \tag{4.18}$$

where C_{ox} is the oxide capacitance measured in strong accumulation at low frequencies. Therefore, the variation of G_p/ω with bias or frequency can be easily plotted. It can be easily shown [9] that the equivalent parallel capacitance C of a single-level interface-state near the conduction band is

$$C = \frac{C_s}{1+\omega^2\tau^2} \quad , \tag{4.19}$$

and the equivalent parallel conductance G_p is

$$G_p = \frac{C_s\omega^2\tau}{1+\omega^2\tau^2} \quad , \tag{4.20a}$$

so that

$$\frac{G_p}{\omega} = \frac{C_s\omega\tau}{1+\omega^2\tau^2} \quad , \tag{4.20b}$$

where τ is the interface-trap life time whose value is R_sC_s; C_s and R_s being the capacitance and resistance associated with the interface traps which are functions of surface potential.

This interface-state RC network appears in parallel with the semiconductor depletion-layer capacitance C_D, as shown in Fig.3.1. G_p is divided by ω to make Eq.(4.20b) symmetrical

in $\omega\tau$.

Using the simplified circuit shown in Fig.3.1, the equivalent parallel capacitance is

$$C_p = C_D + \frac{C_s}{1+\omega^2\tau^2} \quad . \qquad (4.21)$$

where C_D is the semiconductor depletion-layer capacitance. Equation (4.21) describes the capacitance dispersion and is the basis of Terman's method. To extract C_s and τ from C_p using Eq.(4.21), C_D must be known and can be calculated using an estimated doping density. On the other hand, Eq.(4.20b) does not contain C_D and depends only on the interface trap branch of the equivalent circuit. At a given bias, G_p/ω can be measured as a function of frequency. A plot of G_p/ω versus $\omega\tau$ will go through a maximum when $\omega\tau = 1$ which gives directly τ. The value of G_p/ω at the maximum is $C_s/2$. Thus, the equivalent parallel conductance corrected for C_{ox} gives C_s and $\tau = R_s C_s$ directly from the measured conductance. Once C_s is known, the interface trap density is obtained by using the following relation given by

$$D_{it} = \frac{C_s}{qA} \quad , \qquad (4.22)$$

where A is the area of the device.

However, in practice the interface traps are observed to

be comprised of many levels so closely spaced in energy that they cannot be distinguished as separate levels. Thus, they appear as a continuum over the band gap of the silicon. For the continuum of traps or states, the real part of the admittance is given by [9]:

$$\frac{G_p}{\omega} = \frac{q D_{it}}{2\omega\tau_m} \ln(1+\omega^2\tau_m^2) \quad . \qquad (4.23)$$

G_p is directly related to D_{it}. The maximum value $(G_p/\omega)_{max}$ of G_p/ω is approximately $0.4qD_{it}$ at $\tau = \tau_m$ such that $\omega\tau_m = 1.98$. Therefore, the value of D_{it} is obtained from

$$D_{it} = \frac{1}{0.4q}\left(\frac{G_p}{\omega}\right)_{max} \quad . \qquad (4.24)$$

These relations, however, are only approximately true because they are derived from a single-level equivalent circuit. For more precise results, the statistical model equations have to be used [9]. Figure 4.1 shows the expected

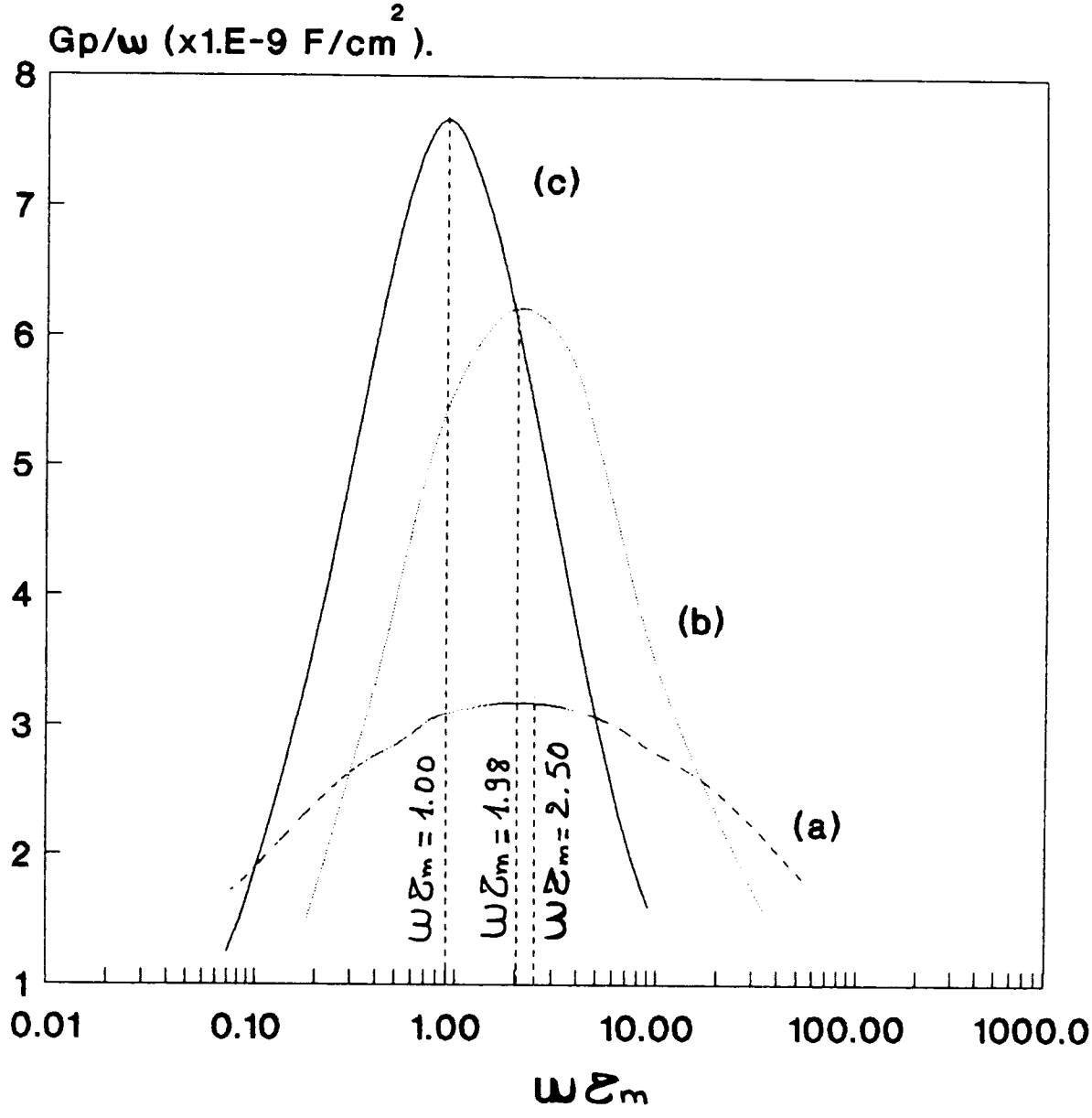


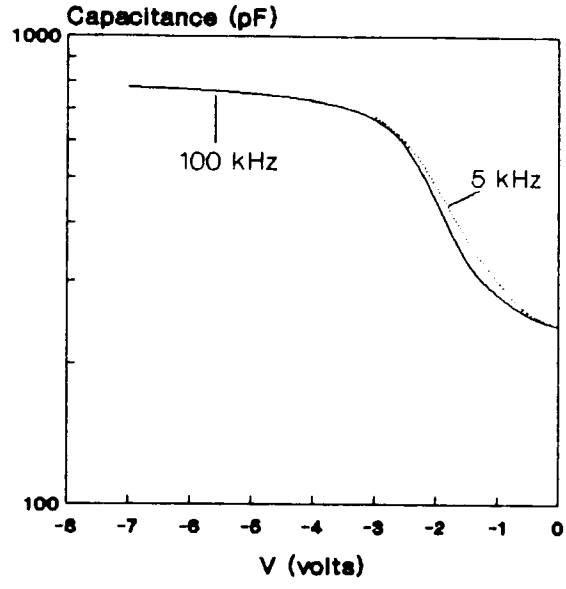
Fig.4.1 (a) Plot of Gp/ω versus log$\omega\tau_m$ illustrating the observed interface trap time constant. Curve (b) for a continuum interface trap. Curve (c) for a single-level interface trap (after [9]).

G_p/ω for a single level, continuum, and the statistical model. From Fig.4.1, it is seen that the peak of the G_p/ω curves is lower than is expected from the simple formula and occurs when $\omega\tau_{max} = 2.5$. This condition $\omega\tau_{max} = 2.5$ is used to find τ_{max} from the frequency at which the measured G_p/ω versus frequency curve goes through a maximum at each bias.

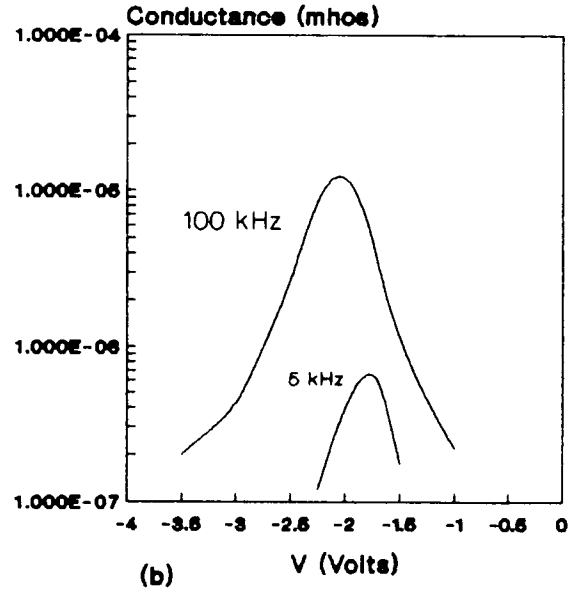
The conductance method is more sensitive than the capacitance methods because C_s is measured directly, not as a difference between C_p and C_D. This is illustrated in Fig.4.2, which shows the measured capacitance and conductance. Taking difference in capacitances leads to round-off error in computing C_s. Moreover, because C_D is larger near flatband than near midgap, this error will be more severe near flatband and puts a limit on how close in energy to the majority band edge D_{it} can be extracted. The relative error of the conductance method depends on the relative error of measuring C_{ox}, C_m, G_m, and ω.

4.4 DEEP-LEVEL TRANSIENT SPECTROSCOPY

The Deep-Level Transient Spectroscopy (DLTS) which was initially developed for MOS capacitors has also been extended for MOS transistors [29]. The DLTS developed by D.V lang [11] is based on the physics of the high-frequency capacitance transients method [33]. This technique is used to obtain information about an impurity level in the depletion region of a Shottky barrier or a p-n junction by



(a)



(b)

Fig.4.2 Comparison of MOS capacitance (a), and (b) conductance measurement at two frequencies (after [9]).

observing the capacitance transient associated with the return to thermal equilibrium of the occupation of the level following an initial non-equilibrium condition. The principle is simple; after an appropriate variation of the reverse bias of the junction from V_0 to V_1 with $|V_1| < |V_0|$ during a time t_p, one obtains a transient capacitance associated to the carrier emission of the defect filled during the t_p as shown in Fig.4.3a. The electron emission is mirrored in the capacitance change, consequently all information about the concentrations, energy levels, and capture cross sections of these traps results from the capacitance changes.

By applying a large reverse-bias (quiescent state) to the sample, a wide space charge region is created where majority carrier traps are emptied. When a zero or small negative bias pulse is applied, the traps are filled with majority carriers from the bulk population. When the filling pulse is removed, the traps emit carriers to their respective band edge. Since the electronic transitions in the space charge region are essentially due to emission process (depleted of free carriers), the time constant for this emission process is controlled via a change of junction capacitance ΔC. These filled energy states return to their initial condition if a thermal stimulation is provided. The trap occupancy will change as a result of a change in the equilibrium conditions. In general this change will be a time dependent

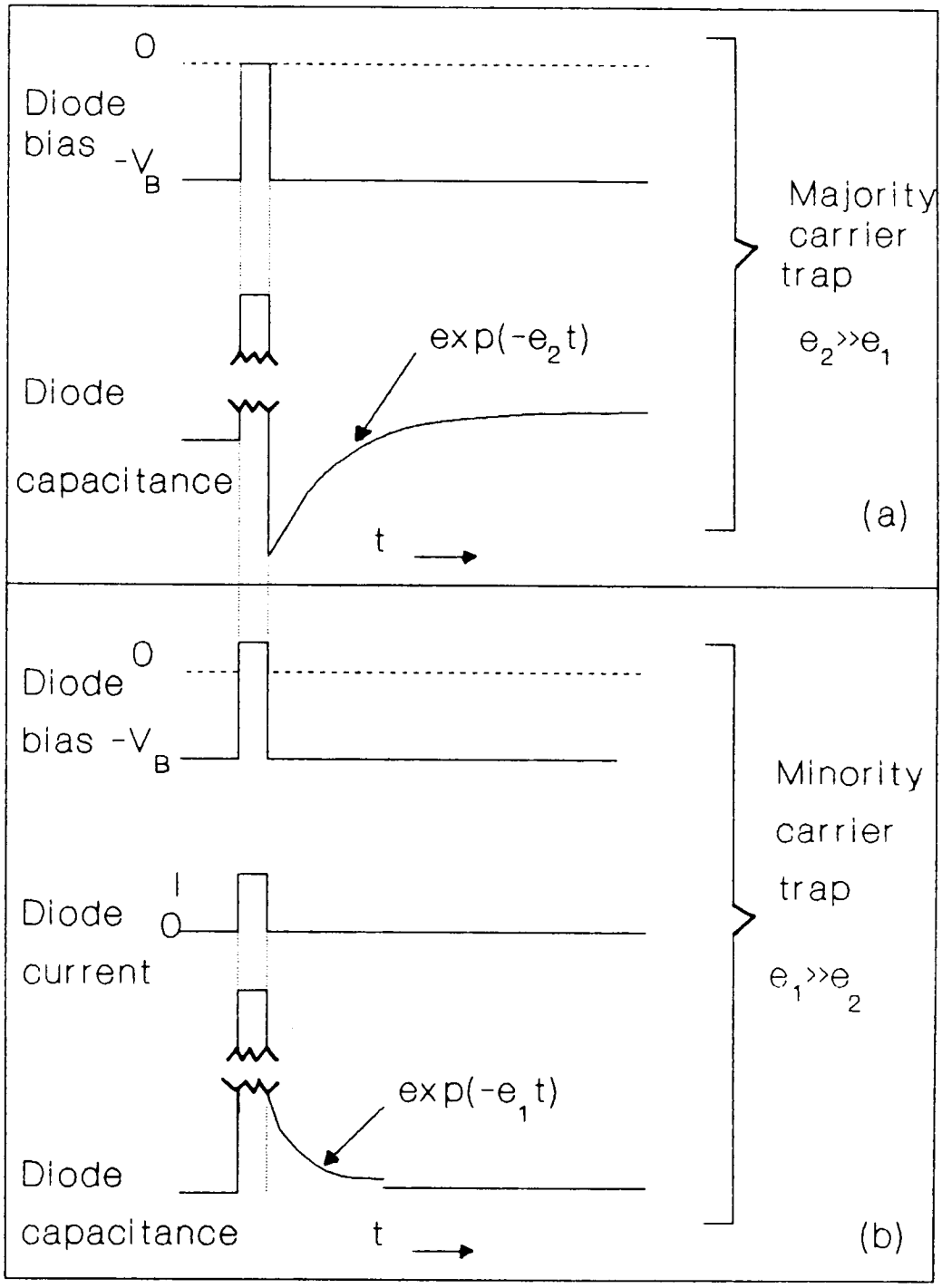


Fig.4.3 Typical time dependence involved in pulsed bias capacitance transients for (a) majority- and (b) minority carrier traps.

exponential function.

To detect minority carrier traps, an injection pulse (forward filling pulse) is used in a p-n junction to fill the minority carrier traps with minority carriers as shown in Fig.4.3b.

The method is based upon the production of a rate window which was originally implemented by a double boxcar integrator [34]. The use of a double boxcar to select the rate window is illustrated in Fig.4.4. The transient signals are fed into this device with gates at preassigned time t_1, and t_2 and produce an output proportional to their average difference. The change in capacitance between t_1 and t_2 is called the DLTS signal, and is given by [11]:

$$\Delta C = C(t_1) - C(t_2) \quad , \tag{4.25}$$

and the normalized DLTS signal S(T) is defined as follows :

$$S(T) = \frac{C(t_1) - C(t_2)}{\Delta C(0)} \quad , \tag{4.26}$$

where $\Delta C(0)$ is the capacitance change at t = 0 due to a saturating injection pulse and is given by

$$\Delta C(0) = C(\infty) - C(0) \tag{4.27}$$

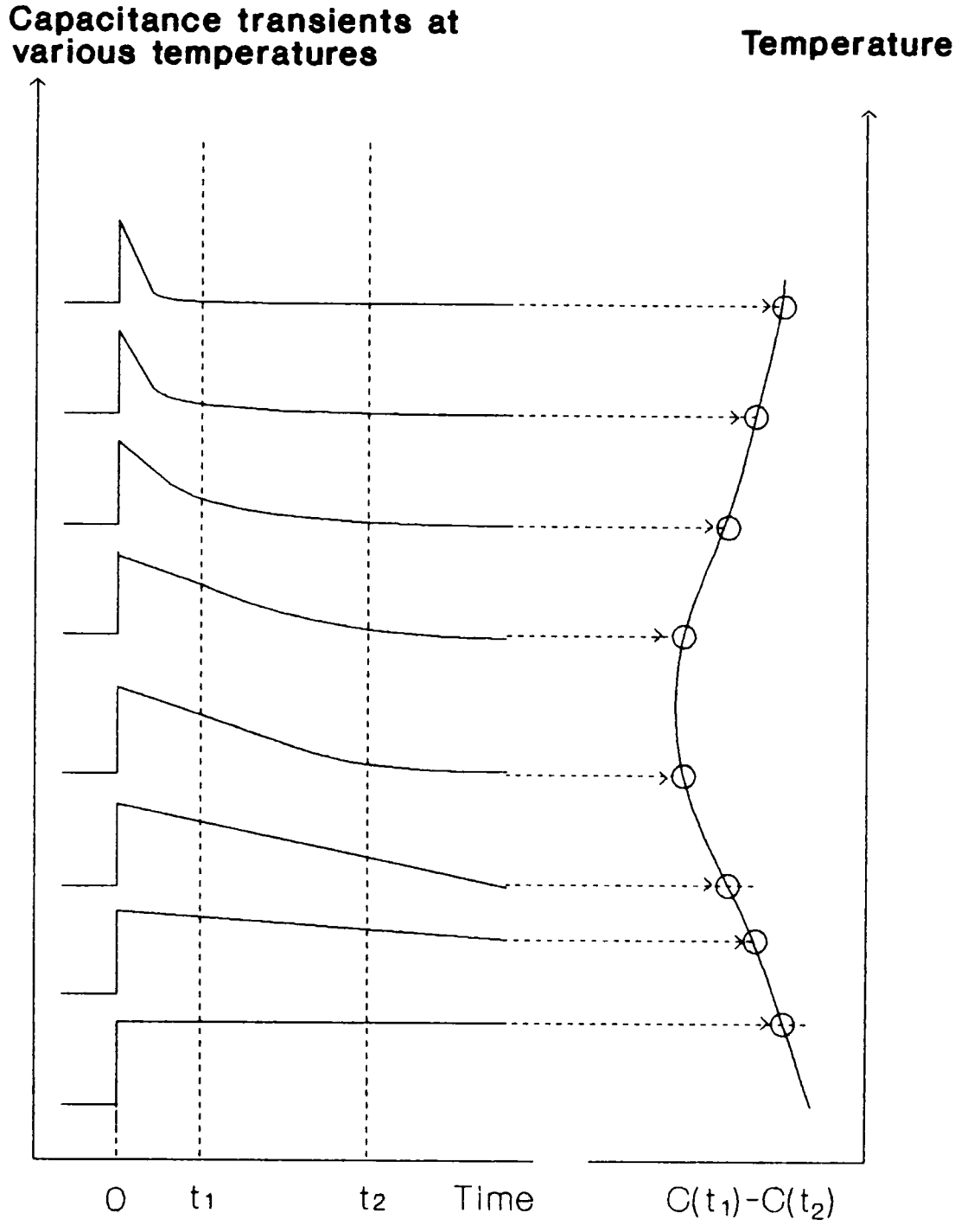


Fig.4.4 Illustration of how a double boxcar is used to define the rate window.

where $C(\infty)$ and C(0) are given respectively by [35]:

$$C(\infty)=\sqrt{\frac{N_D q\epsilon A^2}{2(V_i-V)}} \quad , \tag{4.28}$$

and

$$C(0)=C(\infty)\left[1-\frac{N_T}{2N_D}\right] \quad , \tag{4.29}$$

where A is the area of the junction, ϵ the permitivity of the dielectric constant of the depleted material, V_i the built-in bias voltage of the junction, V the externally applied voltage, q the charge of the electron, N_D the density of ionized doping centers, and N_T the trap concentration. If the capacitance is assumed to be exponential with time constant τ then

$$S(T)=\exp\left(-\frac{t_1}{\tau}\right)-\exp\left(-\frac{t_2}{\tau}\right) \quad , \tag{4.30}$$

where the temperature dependence of τ is given by the emission probability or thermal emission rate. The emission rates for an electron and a hole at equilibrium are given respectively by [36,37]:

$$e_n = \upsilon_{th}\sigma_n n_i \exp\left(\frac{E_T - E_i}{kT}\right) \quad , \qquad (4.31)$$

and

$$e_p = \upsilon_{th}\sigma_p n_i \exp\left(\frac{E_i - E_T}{kT}\right) \quad , \qquad (4.32)$$

where v_{th} is the thermal velocity of the carriers, n_i the intrinsic carrier concentration, E_T the energy level of the center, $\sigma_n(\sigma_p)$ the capture cross section , which describes the effectiveness of the center to capture an electron (hole), k the Boltzmann constant, and T the absolute temperature. Equation (4.30) can also be written as:

$$S(T) = \exp(-\frac{t_1}{\tau})\left(1 - \exp\left(-\frac{\Delta t}{\tau}\right)\right) \quad , \qquad (4.33)$$

where $\Delta t = t_2 - t_1$. The relation between the time constant at the peak in the DLTS and the sampling times t_1 and t_2 are determined by differentiating S(T) with respect to τ and setting the result equal to zero. The derived equation is then:

$$\tau_{max} = \frac{t_1 - t_2}{\ln\left(\frac{t_1}{t_2}\right)} \quad , \qquad (4.34)$$

which corresponds to a temperature T_m of the peak.

Thus, the values of t_1 and t_2 determine the rate window for a DLTS thermal scan as shown in Fig.4.4. The rate window defined by Eq.(4.34) may be set such that the measurement instrument only responds when it sees a transient with a rate within the rate window. If the emission rate of a trap is changed by varying the sample's temperature, the instrument will show a response peak at the temperature when the trap emission rate is within the window. In other words, as the temperature increases, the shape of the transient changes in a manner characteristic of a particular trap. ΔC will be small at high temperatures since all the traps are readily ionized, and small at low temperatures since only a few will be ionized. Hence, between these two extremes the DLTS signal goes through a maximum and the peak occurs when the emission rate from the deep level coincides with the rate window defined as [11]:

$$\frac{1}{e_n} = \tau_{max} = \frac{t_1 - t_2}{\ln\left(\frac{t_1}{t_2}\right)} \quad . \tag{4.35}$$

If the temperature scan is repeated with a new rate window, the peak will occur at another temperature.

The concentration of a trap can be obtained directly from the capacitance change corresponding to completely filling

the trap with a saturating injection pulse (in the case of minority carrier trap) or the largest majority carrier pulse (in the case of majority carrier trap). This concentration N_T, is determined from the height of the transient $\Delta C(0)$ and is given by the simple expression [11]:

$$N_T = \frac{2\Delta C(0) N_D}{C(\infty)} \quad , \qquad (4.36)$$

where all the symbols have their usual meaning. The magnitude of the peak maximum gives [$C(t_1) - C(t_2)$] for a given rate window as determined by t_1 and t_2. The value of the $(\tau)_{max}$ corresponding to peak can be known with the help of Eq.(4.35). Using this value of $(\tau)_{max}$ and t_1 and t_2, the value of S(T) can be known from Eq.(4.33). Using this value of S(T) and measured peak magnitude [$C(t_1) - C(t_2)$] in Eq.(4.26), $\Delta C(0)$ can be obtained.

In addition, one can determine the activation energy, which is a characteristic of each trap, from the temperature shift of the DLTS peak with different rate windows. Thus, by measuring the temperature at which the peaks occur, for known t_1 and t_2 the trap emission rate can be obtained from Eq.(4.34). If this procedure is repeated for different rate windows, the variation of emission rate with temperature may

be ascertained. However, Eq.(4.31) when expressed in terms of the effective density of state in the conduction band may be written as follows [11]:

$$e_n = \sigma_n g v_{th} N_c \exp\left(-\frac{\Delta E_a}{kT}\right) , \qquad (4.37)$$

where $\Delta E_a = E_c - E_T$, g is the degeneracy factor of the deep level, N_c the effective density of states in the conduction band, E_c the energy of the conduction band and the other symbols have their usual meaning. Similarly, the hole emission coefficient e_p may be written as follows [11]:

$$e_p = \sigma_p g v_{th} N_V \exp\left(-\frac{\Delta E_a}{kT}\right) , \qquad (4.38)$$

where $\Delta E_a = E_T - E_V$, Nv is the effective density of states in the valence band, Ev the energy of the valence band, and the other symbols have their usual meaning. Since these quantities are, in general, temperature dependent one must use more care to obtain an accurate value of ΔE. As Nc is proportional to $T^{\frac{3}{2}}$ and v_{th} is proportional to $T^{\frac{1}{2}}$, the rate window (or emission rate) value is divided by T^2 in order to remove the temperature dependence from the emission rate leaving only the desired energy contribution from the emission rates as given by Eqs.(4.31) and (4.32).

In conclusion, it is possible to fully characterize the deep levels in a semiconductor using DLTS. Indeed, the technique is extremely sensitive, rapid and straightforward in analysing the concentrations, energy levels and capture rate of these deep levels. The DLTS technique may be viewed as an improved version of the thermally stimulated capacitance (TSCAP) survey method [38] because of its spectroscopic nature which enables different traps to be reproducible when plotted against a single variable. In addition, the technique permits the determination of trap concentration profiles either by filling the traps with a majority carrier pulse with a sequence of reverse bias, or maintaining the reverse bias constant and altering the filling pulse.

One drawback of DLTS is that it might miss minority-carrier traps that cannot be saturated at practical levels of forward current. Besides, this setup requires a high-quality averager to detect the small capacitance transients, and the analysis is rather complex.

4.5 OTHER METHODS

There are several other methods [10,28,29,30,38] used to study the interface properties in MOS devices but they are of less importance.

The temperature method, proposed by Gray and Brown [10], complements the others because it permits measurement of interface-trap density close to the band edges, while the

previous techniques are more effective in the region around midgap. Especially, this method is related to the previous method of Terman [7]. It uses temperature variation at a fixed surface-potential to vary the charge due to interface traps.

The first method to determine interface traps on MOS transistors was suggested by Van Overstraeten et al [28]. Information on interface-traps can be obtained by their effect on the source-drain in IGFETs in weak inversion. Although satisfactory results are obtained using this technique it is only applicable for long-channel devices (> 20 μm) and at low drain voltages. However, high accuracy can not be obtained, because the results are very sensitive to oxide charge fluctuations. The fluctuation parameter must be determined by other method. If charge fluctuations are included in the analysis, the evaluation becomes very elaborate. Since this method determines interface-trap densities in a practical device, it is still of importance and is occasionally applied.

The deep-level transient-spectroscopy technique (DLTS) which was developed for MOS capacitors can also be performed on MOS transistors [29]. This technique yields information on interface-trap densities and capture cross sections from the measurement of capacitance transients resulting from electron and hole emission from the traps to the conduction band and the valence band. However, this setup requires a

high-quality averager to detect the small capacitance transients, and the analysis is rather complex.

Finally, the method based on the relation between $1/f$ noise and interface-trap density [30,39] has been used in some cases to determine this interface trap density. Although many investigations have been performed for $1/f$ noise in MOS transistors, no definite theory has been set forth to explain different results obtained from different sources. However, in view of the lack of agreement among the different theories on $1/f$ noise such a determination is only qualitative.

CHAPTER 5

CHARGE PUMPING TECHNIQUE

5.1 INTRODUCTION

Since the existence of interface traps at the Si-SiO_2 interface was demonstrated, different techniques have been proposed for the determination of the density of these traps and of their energy distribution [6-9]. All of them are based on the C-V measurement and so they are applicable to MOS capacitors and not to small size MOS transistors. Therefore there is a need for a reliable technique which allows the determination of interface trap density and their distribution directly on MOS transistors.

Recently a new method based on the charge-pumping phenomena in transistors has been developed which in its simplest form determines the average interface-trap density and in more complex form determines their energy distribution. This technique was first mentioned by Brugler and

Jespers [31] as a possible technique for measuring the interface-trap density. But it could not be utilized until its theory and use was presented by Groeseneken et al [12]. This technique is based on a recombination process at the $Si-SiO_2$ interface involving the interface traps.

Quite recently, many improvements have been done. The spatial variation of surface potential and the modulation of the effective gate area by source have been thoroughly studied. A model [14] has been proposed to remove those limitations. In addition, the interface-trap density over most of the bandgap has been treated [40], and the limited midgap penetrability and the inaccuracy of the capture cross-section have been removed [15].

5.2 BASIC PRINCIPLE

The charge pumping current was observed by Brugler and Jespers [31] in the form of a net dc current at the substrate during measurements of capacitance on enhancement-type MOS transistors. They showed that this current consists of two components; one component called surface state or interface trap component involves coupling of pumped charge (from the drain and source) with interface traps at the $Si-SiO_2$ interface, and a second component called geometric component involves recombination of free charge of the inversion layer with the majority carriers of the substrate.

It has been shown [31] that under the condition when the width (W) to length (L) ratio of the channel of MOS transistor is greater than unity (W/L>>1), the geometric component is negligible and pumping current mainly comprises of interface trap component. It is under this condition W/L>>1 that pumping current can be used for the determination of surface state density and their distribution. It may be noted that this pumping current is in a direction opposite to that of the reverse current between drain/source and substrate. As the dc meter, connected between the substrate and the ground, cannot respond to ac pulse, the dc current detected by it stands for a new phenomenon.

The basic experimental set-up as introduced by Brugler and Jespers [31] is shown in Fig.6.3 in the case of an n-channel transistor. The gate of a MOS transistor is connected to a pulse generator, and a reverse bias Vr is applied to the source and the drain. When the transistor is pulsed between inversion and accumulation, it gives rise to a net flow of negative charge into the substrate. Indeed, electrons (coming from source/drain) fill the surface states during the inversion period of the gate pulse. When holes (coming from substrate) reach the interface traps during accumulation, they recombine with these trapped electrons, giving rise to a net current flowing from the substrate, via the interface traps, to the source and drain.

The net charge Q_{it} pumped from the drain/source that undergoes recombination with the interface traps is given by [12]:

$$Q_{it} = A_g q \int D_{it}(E) dE \qquad (5.1)$$

Equation (5.1), when expressed in terms of the surface potential sweep, becomes

$$Q_{it} = A_g q^2 \overline{Dit} \Delta\psi_s \qquad (5.2)$$

where $\overline{Dit}$ ($cm^{-2}eV^{-1}$) is the mean surface state density averaged over the energy levels swept by the Fermi level, Ag (cm^2) the channel-area of the transistor, q(C) the electron charge and $\Delta\psi_s$ (V) the total sweep of the surface potential. By applying a repetitive pulses to the gate with frequency f, this charge Q_{it} will give rise to a current in the substrate given by [12]:

$$I_{cp} = f Q_{it} = f A_g q^2 \overline{D_{it}} \Delta\psi_s \qquad (5.3)$$

Therefore, this substrate current is caused by a recombina-

tion at the interface traps and is directly proportional to the interface trap density in the channel, the frequency of the gate pulse, and the transistor area. Its magnitude increases linearly with gate pulse frequency over the limits of the measuring equipment [31] when the leakage effects were swamped. From the measurement of this substrate current, an estimate of the mean value of the interface trap density $\overline{D_{it}}$ over the energy range swept by the gate pulse can be obtained.

5.3 METHODS OF MEASUREMENTS

In general three methods have been employed to measure the pumping current:

Method A : By keeping the pulse base level in accumulation and pulsing the surface into inversion with increasing amplitudes [31];

Method B : By varying the pulse base level from inversion to accumulation while keeping the amplitude of the pulse constant [32]. This method was used by Elliot and will be referred as Elliot method.

Method C : By keeping the pulse base level in inversion and pulsing the surface into accumulation [41].

In order to obtain the interface-trap density distribution near the conduction band, Brugler and Jespers [31] suggested to keep the pulse base level in accumulation and pulsing the

surface into inversion with increasing amplitude of the gate pulse. In the same way, the interface-trap density distribution near the valence band can be obtained by using method C [41]. In these two cases, the dependence of the energy distribution of the interface traps is given by :

$$q^2\overline{D_{it}}\psi_s = \frac{dQ_{it}}{dV_g}\frac{dV_g}{d\psi_s} \qquad (5.4)$$

where :

$$Q_{it} = \frac{I_{cp}}{A_g f} \quad . \qquad (5.5)$$

The determination of $dV_g/d\psi_s$ is, then, necessary to know the interface-trap density distribution near the two bands (conduction band and valence band). In fact these two methods A and C are reciprocal to each other and do not reveal any basic difference in the characteristics [12]. The current shows a saturation level when the top of the pulse exceeds the threshold voltage of the MOS transistor. However, in practice the saturation does not occur in the case when the reverse bias voltage V_r=0 and this is attributed to a geometric component still playing a role. Since during the rising edge of this characteristic the potential barrier between source/drain and the substrate prevents the carriers

from flowing into the channel to fill the empty traps, Elliot [32] suggested to keep the amplitude of the pulse constant and varying the pulse base level from inversion to accumulation. This procedure also needs the dependence of surface potential on the gate voltage, which can be obtained by QSCV technique of the MOS structure. One of the drawbacks of these methods [31,32,41] is the requirement to know the dependence of the surface potential on gate voltage, which is to be obtained by quasi-static C-V measurements on the MOS transistor under test. In this way the advantage of the simplicity of the charge pumping method is lost.

This simplified model as described above could not provide more information about the other properties of the interface traps such as their nature and the energy distribution in the midgap. As, this model does not take into account certain important phenomena such as the emission process described by Simmons and Wei [42,43] in its mathematical modelling. its results are not supposed to give correct estimate of the interface traps and other related quantities. Indeed, one part of the trapped charge (electrons in the case of n-channel MOSFET) will not recombine with the majority carriers (holes) coming from the substrate when the surface is pulsed from inversion to accumulation. These electrons are emitted towards the conduction band and collected by the source/drain as mobile carriers. On the

other hand, when the surface is pulsed from accumulation to inversion, one part of the interface traps is filled by the emission of holes. In other words the interface traps are filled by the electrons from the valence band (supplied by the substrate) and not by the capture of electrons from the conduction band supplied by the two junctions (source and drain).

Recently, Groeseneken et al [12] proposed another model for charge pumping current by taking into account this emission process. They showed how the idea of electron and hole emission can be utilized to extract information about the interface trap distribution in the forbidden energy gap, without requiring the knowledge of the surface potential dependence on gate voltage.

Before describing this model and the mechanisms of emission and capture of the interface traps, two important points are discussed:

(a) In the case of large signals, sweeping an important range of the surface potential with rising and falling times relatively small, most of the interface traps, especially, those located at the midgap are not in dynamic equilibrium during the rising and falling steps of the voltage sweep. For this reason, the top level of the applied signal should exceed the threshold voltage so that the device may remain in the inversion mode for sufficient time needed to allow

complete filling of the interface traps. In strong inversion, this filling time becomes very small since it is inversely proportional to the carrier density [31]. Similarly, the bottom level of the signal should be less than the flat-band voltage such that the interface traps will be emptied during this accumulation mode where the hole density is very large.

(b) The minority carrier response time forming the inversion layer depends greatly on the surface potential and on the channel length; the forming time of the inversion layer is, indeed inversely proportional to the square of the channel length. Therefore, it is evident that for long channel the inversion layer charge cannot follow the signal and cannot be in dynamic equilibrium with the variation of the potential. Besides, the time during which the channel is in inversion should be longer than the response time of the inversion layer. This is another reason for which the top level should exceed the threshold voltage, because the minority carrier response time in strong inversion is too small compared to the one in weak inversion.

5.4 GROESENEKEN ET AL MODEL

Groeseneken et al [12] considered a waveform as shown in Fig.5.1, which is applied to the gate of the transistor. The signal has a rise time t_r and a fall time t_f, a period T, and an amplitude $\Delta V_g = V_{gh} - V_{gl}$, where V_{gh} and V_{gl} are respectively the high and low levels of the signal. When the surface is in accumulation ($V_g = V_{gl}$), all the interface traps below the quasi Fermi level of the minority carries are filled with electrons, while those above it are empty. The states or traps are thus in equilibrium with the energy bands. According to Groeseneken et al [12] model of the charge pumping technique in MOSFET's, the charging and discharging of the surface-traps during a certain surface-potential sweep is supposed to take place under two regimes. The first regime is governed by the steady-state recombination of the interface traps with the charge carriers which are available in the surface-region and this happens only when the surface-region enters either into accumulation or into deep inversion. The second regime is governed by the non-steady-state emission from the interface traps which occurs when the surface-region is under depletion condition. It may be noted that the depletion condition is supposed to prevail in the energy-region enclosed between the energy levels E_B and E_T which correspond to flat-band voltage V_{FB}

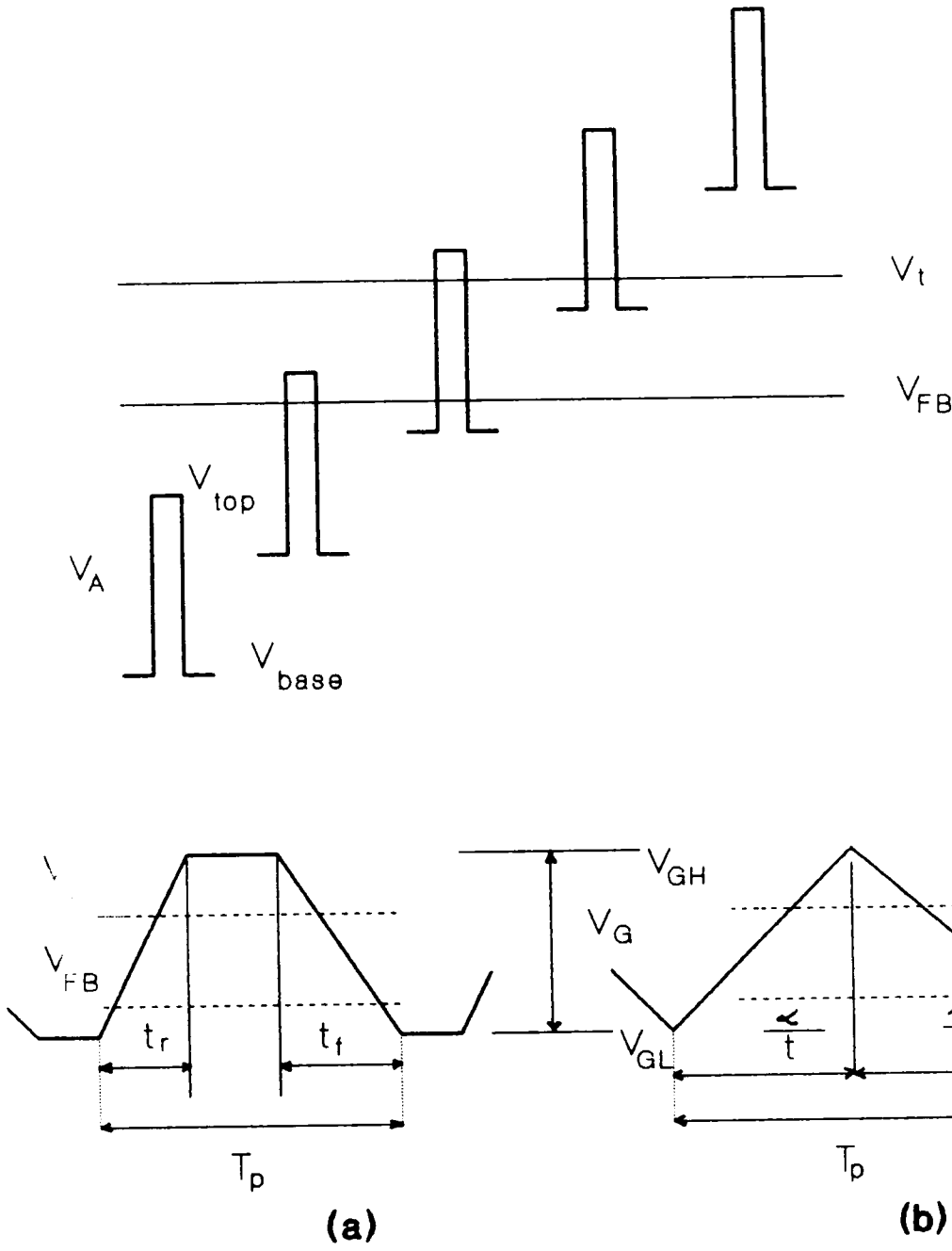


Fig.5.1 Waveforms applied at the gate when performing charge pumping. The different paramaters are indicated.

and threshold voltage V_T respectively. However, due to hysteresis these energy-levels are likely to be changed to E'_B and E'_T [Fig.(5 2)] respectively. Therefore, the non-steady-state emission commences from E'_B while going from accumulation to inversion and at E'_T while going from inversion to accumulation. The device passes through several regions of the energy diagram when the pulse sweeps from deep accumulation to deep inversion and back.

During the rising part of the gate signal (positive sweep), the surface potential is changing at a certain rate and the following three successive processes may be identified:

(a) During the transition from deep accumulation to V'_{FB} the quasi-Fermi level at the interface will rise and interface traps will begin to fill with electrons (coming from the substrate) by the process of hole emission. This part is described to correspond to steady-state in which the interface traps acquire equilibrium with carriers (holes). Therefore, holes that have to be emitted from the interface traps towards the valence band will flow back to the substrate to maintain equilibrium.

(b) After crossing V'_{FB} , this process will continue until the gate potential reaches the threshold voltage V_T. However, as soon as this rate of trapped charge imposed by the emission process becomes smaller than the one required by

the voltage sweep at the gate, the channel is in the non-steady state regime and the emptying of the traps is controlled completely by the emission process, as described in detail by Simmons and Wei [42,43]. This part is described to correspond to non-steady-state since enough carriers (holes) are not available for recombination in the depletion layer. These holes will flow back to substrate indirectly by combining with valence electrons and releasing holes in the substrate. In fact this is the only way how interface traps while going from V'_{FB} to V'_T release holes. The other possibility by accepting electrons from drain/source is ruled out since the drain/source are at reverse bias with respect to the substrate. This is a non-steady-state process and continues until the gate voltage exceeds the threshold voltage V'_T.

(c) When the gate voltage is close to the threshold voltage V'_T, the trapping time constant becomes gradually smaller and consequently electrons will be trapped in the interface traps not yet emptied (of holes). This process will become important when the gate voltage is almost equal to the V'_T. After V'_T the device enters into inversion and plenty of electrons are available, therefore, the remaining traps will be filled by electrons coming from the source and drain junctions. Therefore, the electron capture process will dominate over the hole emission process in filling the

interface traps wit electrons, and the channel is back in equilibrium with t e energy bands. This time constant is given by [31]:

$$\tau_n = \frac{1}{v_{th} n_s \sigma_n} \quad , \tag{5.6}$$

where n_s is the surface concentration of minority carriers, v_{th} the thermal velocity of the carriers, and σ_n the capture cross section of electrons.

During the falling p rt of the gate signal (negative sweep), similar mechani ms take place. First, electrons are emitted from the interface traps towards the conduction band and flow back to the source and drain in a steady state regime, until approximately threshold voltage (V'_T) is reached. It may be noted that surface potential at V'_T is higher than at V_T due to the hysteresis [42] because, while coming from deep inversion, the electrons are not promptly emitted by the interface traps and they remain filled upto more extent at V_T' than at V_T. Thereafter, a non-steady-state emission of electrons from the interface traps to the conduction band occurs followed by their removal through source and drain until the absolute value of the gate voltage crosses V'_{FB}. Finally, when the gate voltage crosses V'_{FB}, the trapping time constant of holes becomes important since plenty of holes are again available, and holes (coming

from the substrate) will fill the remaining occupied (with electrons) traps. Similarly, this time constant is given by [31]:

$$\tau_p = \frac{1}{v_{th} \cdot p_s \cdot \sigma_p} \quad , \qquad (5.7)$$

where p_s is the surface concentration of holes, and σ_p the capture cross section of holes. Different regions of the steady-state recombination and non-steady-state emission of the interface traps are shown on the energy-band diagram of silicon in Fig.5.2. The same regions are briefly described in table 5.1.

Therefore, four different currents are associated with these regimes [12]:

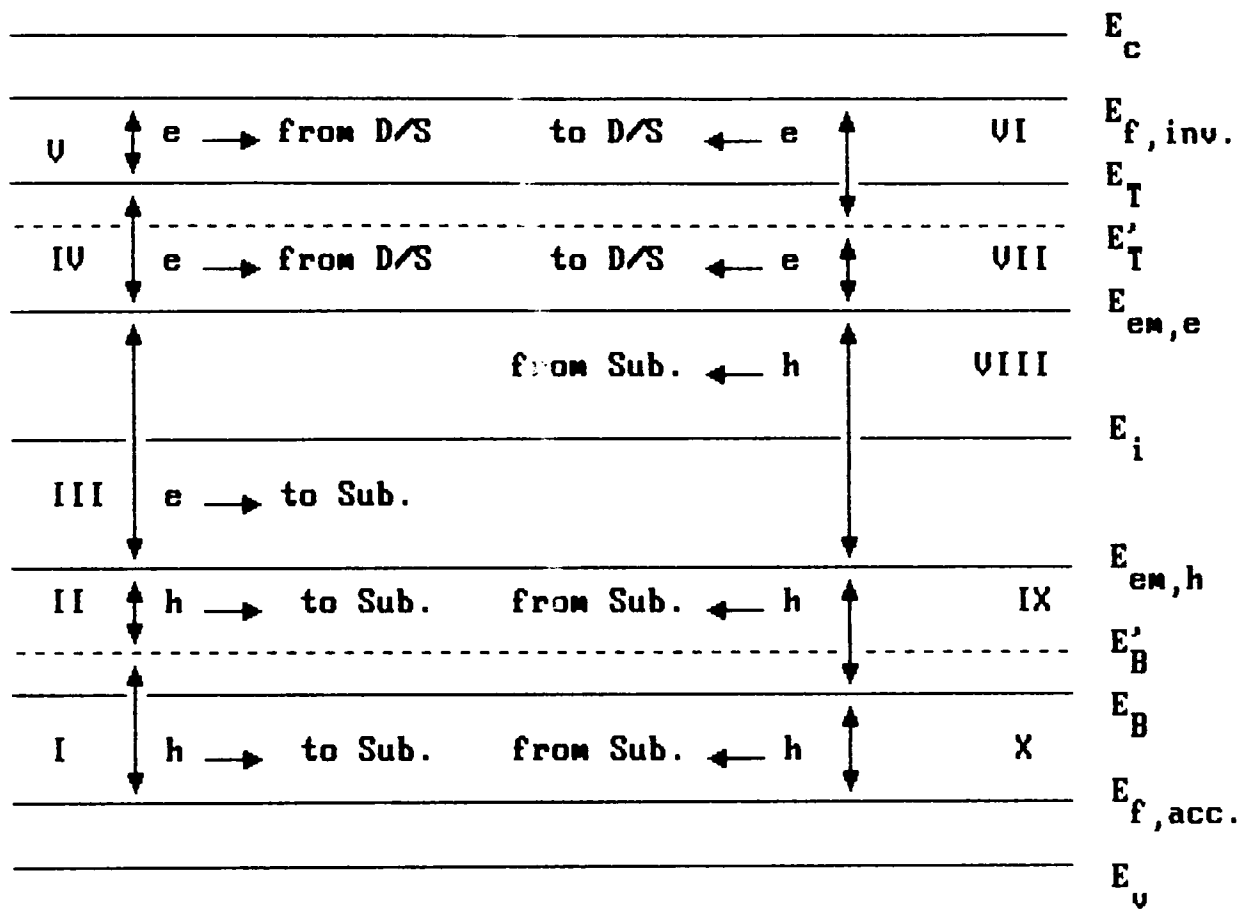
$$I_1 = -q^2 \overline{Dit} \Delta\psi_e f A_g \qquad (5.8a)$$

$$I_2 = q^2 \overline{Dit} \Delta\psi_{ee} f A_g \qquad (5.8b)$$

$$I_3 = -q^2 \overline{Dit} \Delta\psi_h f A_g \qquad (5.8c)$$

$$I_4 = q^2 \overline{Dit} \Delta\psi_{he} f A_g \qquad (5.8d)$$

where $\Delta\psi_e = E_{Fins} - E_{em,h}$, $\Delta\psi_{he} = E_{em,h} - E_{Facc}$, $\Delta\psi_{ee} = E_{Fins} - E_{em,e}$, and $\Delta\psi_h = E_{em,e} - E_{Facc}$.



D/S : Drain / Source.
E_c : bottom of conduction band.
E_i : Intrinsic level.
E_B : Energy corresponding to flat band voltage.
E'_B : Modified E_B due to hysteresis.
$E_{f,inv.}$: Deep inversion level.
$E_{f,acc.}$: Deep accumulation level.
Sub. : Substrate.
E_v : Top of valence band.
E_T : Energy corresponding to threshold voltage.
E'_T : Modified E_T due to hysteresis.
$E_{em,h}$: Hole emission level.
$E_{em,e}$: Electron emission level
h : Hole, e : Electron.

Fig.5.2 Energy-band diagram illustrating different regions of the steady-state recombination and non-steady-state of the interface traps.

Table 5.1. Details of the different surface-potential regions of the steady-state recombination and non-steady-state emission of the surface-states.

Regions	Surface Potential Sweep	Surface-Process	Carrier-Process	Current-Direction w.r.t GND
I	$E_{f,acc.}$ to E_B'	s.s.h. emission.	h. trans. to sub.	Positive
II	E_B' to $E_{em,h}$	N.s.s.h. emission.	h. trans. to sub.	Positive
III	$E_{em,h}$ to $E_{em,e}$	s.s.e. trapping.	e. supp. from D/S.	Negative
IV	$E_{em,e}$ to E_T	s.s.e. trapping.	e. supp. from D/S.	Negative
V	E_T t $E_{f,inv.}$	s.s.e. trapping.	e. supp. from D/S.	Negative
VI	$E_{f,inv.}$ to E_T'	s.s.e. emission.	e. trans. to D/S.	Positive
VII	E_T' to $E_{em,e}$	N.s.s.e. emission.	e. trans. to D/S.	Positive
VIII	$E_{em,e}$ to $E_{em,h}$	s.s.h. trapping.	h. trans. from sub.	Negative
IX	$E_{em,e}$ to E_B	s.s.h. trapping.	h. trans. from sub.	Negative
X	E_B to $E_{f,acc.}$	s.s.h. trapping.	h. trans. from sub.	Negative

s.s. : Steady-state
N.s.s.: non-steady-state
Sub. : Substrate
trans. : transported
Supp. : supplied
D/S : drain/source
h : holes
e : electrons

E_{Finv} represents the Fermi-level position when the gate voltage is at its highest value (inversion) while E_{Facc} represents the Fermi-level position when the gate voltage is at its lowest value (accumulation). Direction of currents due to the charging and discharging of the interface traps in different regions (I to V during gate-voltage sweep for the energy-interval from $E_{f,acc}$ to $E_{f,inv}$ and V to X during gate-voltage sweep from the energy-interval from $E_{f,inv}$ to $E_{f,acc}$) which have been considered are given in Fig.5.2 and table 5.1. An inspection of Fig.5.2 reveals that the net substrate-current I_{cp}, called charge-pumping current during one cycle of the voltage pulse comes out to be negative and arises due charging and discharging of the interface traps within the surface-potential interval $\Delta\psi=(E_{em,e}-E_{em,h})$ only, whereas currents due to other regions are cancelled out mutually during the forward and the reverse voltage sweeps, and I_{cp} is given by [12]:

$$I_{cp}=I_3 \quad I_{} = q^2\overline{Dit}(\Delta\psi_{he}-\Delta\psi_h)f A_g \quad . \qquad (5.9)$$

It may be pointed out that Groeseneken et al [12] have implicitly supposed a uniform distribution of the interface traps in the forbidcen band-gap in writing the Eq.(5.8).

It is shown that during the voltage sweep from accumulation to inversion (or vice-versa) a steady state emission

process is followed by a non-steady state emission. Crucial in the derivation is the knowledge of the non-steady state emission levels $E_{em,h}$ and $E_{em,e}$ as a function of the rise and fall times of the gate pulses respectively, which are given by [42] :

$$E_{em,h} = E_i + \frac{kT}{q} \ln(v_{th} \sigma_p n_i t_{em,h}) \qquad (5.10a)$$

$$E_{em,e} = E_i - \frac{kT}{q} \ln(v_{th} \sigma_{n_i} t_{em,e}) \quad , \qquad (5.10b)$$

where $t_{em,e}$ and $t_{em,h}$ are the times of non-steady state emission for electrons and holes, respectively, and are given by [12]:

$$t_{em,e} = \frac{|V_{fb} - V_{th}|}{|\Delta V_g|} t_f \qquad (5.11a)$$

$$t_{em,h} = \frac{|V_{fb} - V_{th}|}{|\Delta V_g|} t_r \quad , \qquad (5.11b)$$

where V_{fb} is the flat-band voltage, V_{th} the threshold voltage, t_r and t_f are respectively the rise and fall times of

the applied signal. For triangular signals $t_{em,e}$ and $t_{em,h}$ are given just by replacing in Eqs.(5.11) t_f and t_r respectively by α/f and $(1-\alpha)/f$; where f is the frequency and α is defined as the fraction of the period during which the gate voltage is rising. The electron-emission level $E_{em,e}$, upto which the non-steady-state emission actually occurs, depends upon the available emission-time $t_{em,e}$. If sufficient emission-time is available that is at low frequency, the non-steady-state emission of electron can continue upto the lowest possible trap-level which has been considered [12] at E_i. At higher frequencies in the range of a few kilohertz, the electron-emission level $E_{em,e}$ lies closer to E'_T and only a small surface-potential interval (E'_T - $E_{em,e}$) undergoes electron-emission. Similar arguments apply to the case of hole-emission while going from E'_B to the extreme trap-level E_i in which the hole-emission level ($E_{em,h}$) lies between E'_B and E_i.

The charge pumping current I_{cp} is then obtained by combining Eqs.(5.9) to (5.11) which comes out in the case of square pulses as

$$I_{cp} = 2q\overline{D_{it}} f A_g kT\left[\ln\left(\upsilon_{th} n_i \sqrt{\sigma_n \sigma_p}\right) + \ln\left(\frac{|V_{fb} - V_{th}|}{|\Delta V_g|}\sqrt{t_r t_f}\right)\right] \qquad (5.12)$$

and for triangular pulses

$$I_{cp} = 2q\overline{D_{it}} f A_g kT[\ln(v_{th} n_i \sqrt{\sigma_n \sigma_p}) + \ln\left(\frac{|V_{fb} - V_{th}|}{|\Delta V_g|}\frac{1}{f}\sqrt{\alpha(1-\alpha)}\right)] \quad . \qquad (5.13)$$

The total charge of the interface traps which recombines during each cycle is given by

$$Q_{it} = \frac{I_{cp}}{f} \quad . \qquad (5.14)$$

By plotting Q_{it} as a function of the frequency on a semilogarithmic plot, one obtains a straight line as shown in Fig. 5.3 when using triangular pulses. The extrapolation of this curve to zero charge results in

$$f_o = \sqrt{\sigma_p \sigma_n} v_{th} n_i \frac{|V_{fb} - V_{th}|}{|\Delta V_g|}\sqrt{\alpha(1-\alpha)} \quad . \qquad (5.15)$$

The geometrical mean value of the capture cross sections can be determined with the help of Eq.(5.15). The slope of the curve is given by

$$\frac{dQ_{it}}{d\log f} = 2qkT\frac{\overline{D_{it}}}{\log e} A_g \quad , \qquad (5.16)$$

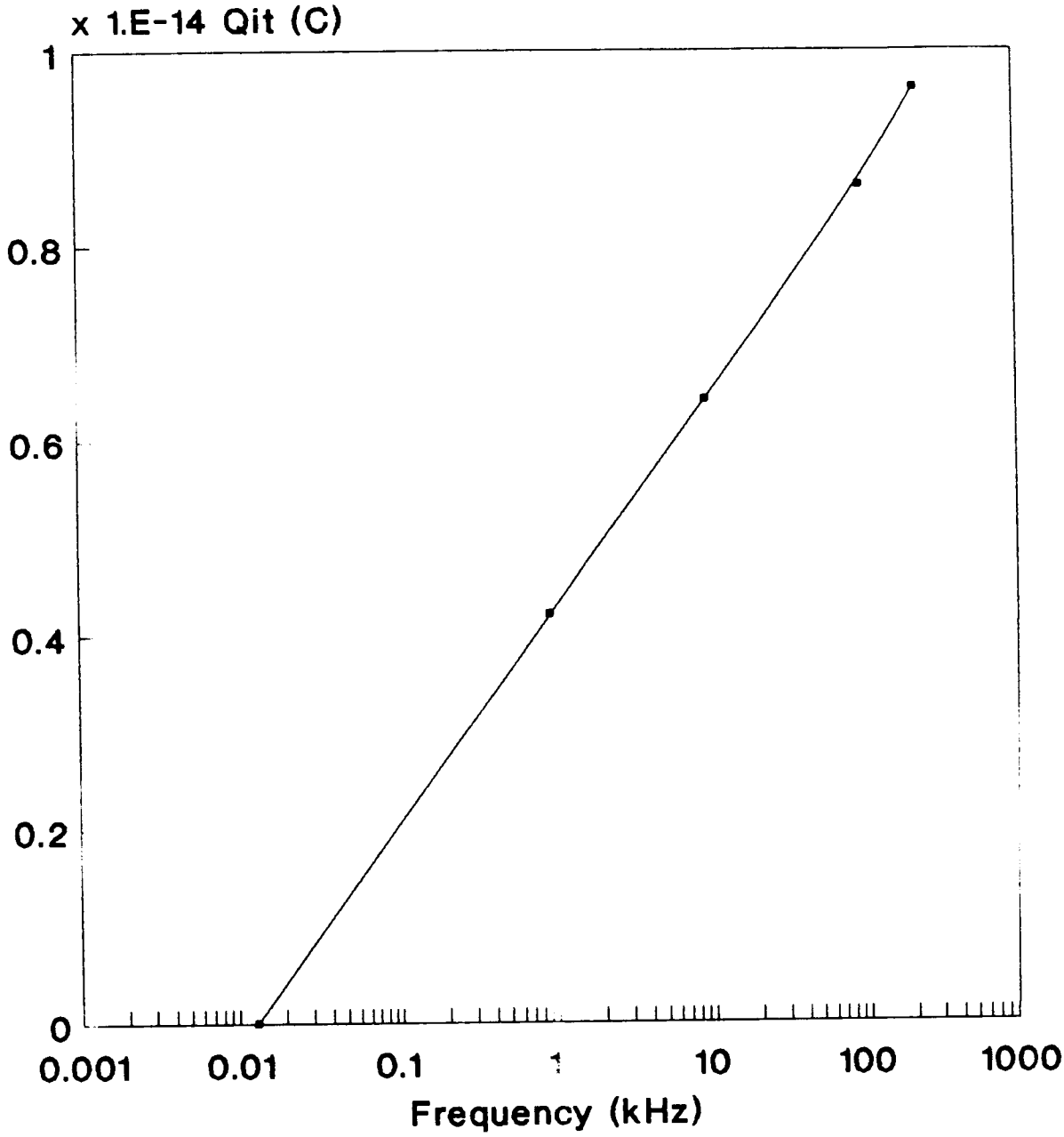


Fig.5.3 Qss versus frequency used to determine the mean capture cross section and average interface-trap density (After [12]).

and allow the determination of the mean value of the interface trap density.

The energy distribution of interface traps over a large part of the forbidden energy gap can be obtained by varying the rising and falling times of the applied square pulses. The total charge of the interface traps that recombine per cycle is given by

$$Q_{it} = q A_g \int_{E_1}^{E_2} Dit(E) dE \quad , \qquad (5.17)$$

where $E_1 = E_{em,h}$ and $E_2 = E_{em,e}$ are the boundaries of the energy range which is scanned and $D_{it}(E)$ is the interface trap density at energy E. From Eq.(5.17), it can be easily proved that $D_{it}(E)$ is given by [12]:

$$D_{it}(E_{12}) = -\frac{t_{r,f}}{q A_g kT f} \frac{dI_{cp}}{dt_{r,f}} \quad . \qquad (5.18)$$

Nevertheless, the energy distribution as given by Eq.(5.18) does not strictly remain valid over all the energy band-gap, since the capture cross sections for electrons and holes do not remain constant throughout the bandgap but decrease exponentially in the vicinity of the band-edges [12]. Besides, Groeseneken et al [12] assumed σ_n and σ_p to be

equal because their model cannot determine them separately. However from the literature it is known that σ_n/σ_p is not equal to 1 but can be as high as 1000 [44].

5.5 LIMITATIONS

A few limitations and uncertainties may be pointed out here which seem to be inherent in the above approach of charge-pumping method. The expressions of the emission-time of the electrons and holes $t_{em,e}$ and $t_{em,h}$, which are used [12] for obtaining the surface-potential interval $\Delta\Psi$, make use of the flat-band voltage V_{FB} and threshold voltage V_T. This may introduce an error as V_{FB} and V_T are effectively changed to V'_{FB} and V'_T respectively. Using a triangular pulse, a linear relationship between the recombined charge per cycle $Q_{ss} = \frac{I_{cp}}{f}$ and the frequency f has been considered [12] which is an over-simplifying assumption. If at all this assumption holds good, it is only for very small values of the fraction α of the pulse-period during which the voltage pulse rises. In fact this assumption can introduce a large amount of uncertainty in the value of $\sqrt{\sigma_e\sigma_h}$ (σ_e and σ_h are the electron and hole capture cross-sections) and hence in the value of $\overline{D_{it}}$ (the average density of surface-states). Alternatively, the correctness of the charge-pumping method will depend upon the correct use of σ_e and σ_h, different estimates of which in the literature differ so much that no

unique value of $\sqrt{\sigma_n \sigma_h}$ can be fixed. Yet another source of uncertainty may be pointed out which lies in the supposition of positive direction of the currents for the energy-regions of non-steady-state emissions II and VII. These currents have been considered [12] to contribute nothing to the net substrate-current on the argument that these currents are nullified by their counterparts during the sweep of the energy-regions IX and IV. The carriers emitted under the non-steady-state regions II and VII, find the drain/source-substrate circuit as an additional path to flow out giving rise to positive substrate-current but still at least some fraction of them may follow the gate-substrate path contributing to the negative substrate or charge-pumping current. In fact at certain frequencies, an appreciable gate-current has been observed apart from the usual charge-pumping current even in the case of charge-pumping method during the present study. Besides the above uncertainties, the charge-pumping technique is limited to the use of MOSFETs only and that too for those which satisfy the geometrical requirement $\frac{W}{L} \gg 1$ where W and L are the width and length of the channel respectively.

5.6 OTHER DEVELOPMENTS IN CHARGE PUMPING TECHNIQUE

The phenomenon was first identified by Brugler and Jespers [31]. The description of the possible mechanisms occuring in a charge pumping [45,46] and its recent extension by Geoeseneken et al [12] have led to the development of several methods. All of the common methods based on charge pumping phenomenon require the application of Shockley-Read-Hall modeling theory [47,48] to model the trapping and detrapping behaviour of the interface traps. The goal in these methods is to determine simultaneously both a capture cross-section as well as a density of interface traps and their distribution as function of energy position. Most of these techniques [12,31,32,49] are based on the Simmons and wei analysis of charge emission from interface traps in MOS capacitors [42,43], and have provided a detailed model which adequately describes the effect for the case involving low frequencies and hence slow rates of transition between strong inversion and strong accumulation. These restrictions are due to the fact that the model assumes emission-controlled operation only, and omits the surface-potential controlled operation as well as the effect of non-steady-state capture processes. These omissions have, practically, no adverse effect on the quality of the model if it is used as technique for interface trap in an IC device since the pump

is generally operated in the emission-controlled mode. However, the pump may also operate in the surface-potential-controlled mode, and steady-state may not be reached in capture processes as a result of high repetitious frequencies or weak/accumulation conditions. Based on these considerations, a model has been developed by Cilingiroglu [14]. This model [14] which originates from the Shockley-Read-Hall theory of trapping [47,48] describes interface-trap charge pumping for any trapezoidal gate signal and any reverse biasing source voltage. However, the model [14] has omitted the effect of the geometrical charge pumping current which is regarded as a parasitic current and suppressed to a negligible level.

The model of Cilingiroglu [14] incorporates the three basic effects that govern the phenomenon: the non-steady-state electron and hole capture processes, the limited excursion of the surface potential, and the electron and hole emission processes. In the previous models, only the latter has been taken into account which limits the validity of these models to the case of low-frequency gate excitation that sweeps the surface between strong inversion and strong accumulation at slow transition rates. The model of Cilingiroglu [14] removes certain limitations due to several mechanisms which may have an important effect on the charge pumping current such as: surface potential fluctuations due

to spatially nonuniformly distributed charges [13], the modulation of the effective gate area by the gate voltage, the lateral current resulting from charge transport between source and channel.

The spatial variation of surface potential and the modulation of gate area by source voltage appeared to be the most important of all. Spatial variation of the surface potential is generally attributed to interfacial charge nonuniformities and has the effect of dispersing any MOS variable that is a function of surface potential (stretch-out of C-V characteristics and the trap time-constant dispersion observed in MOS capacitors [13]). The most pronounced effect of surface-potential variation on the charge-pumping current is observed when I_{cp} is limited by non-steady-state capture processes; in this mode, I_{cp} is exponentially dependent on trap time constants, whose dependence on surface-potential is also exponential. Lateral currents resulting from charge transport between source and channel may strongly influence the charge-pumping current. An important conclusion of this author [14] is that there is no good correlation between the experimentally observed and the calculated edges as suggested by Groeseneken et al [12]. The conclusions drawn [14] about the difference between theory and calculations are confirmed by the same authors [50]. In the majority of previous workers, the width of the modulation of gate area

which is a dead zone has been assumed equal to the classical depletion width of a step p-n junction [12,32]. This approximation is valid only for the condition of flatband, because in accumulation the width shrinks considerably with the increasing gate bias [51]. The effect of gate bias is further evidenced by the measured 1 MHz C-V plots belonging to the test pump. The capacitance decreases with the increasing reverse bias, apparently due to the modulation of gate area. The effect is more pronounced for $V_G = V_{FB}$ resulting in a capacitance variation as the reverse biasing is varied. This effect can be characterized directly from the measured I_{cp} data.

According to this model [14], the energy distribution is determined by the following equations for the trap potential at $v_t < 0$:

$$N_{it}(-v_{cf}) \cong \frac{1}{Aktf}\left(1+\frac{d\ln\sigma}{dv_{cf}}\right)\frac{dI_p}{d\ln\alpha_f} \quad . \qquad (5.19)$$

A similar equation can be obtained for the traps located at $v_t > 0$:

$$N_{it}(v_{cr}) \cong \frac{1}{Aktf}\left(1+\frac{d\ln\sigma}{dv_{cr}}\right)\frac{dI_p}{d\ln\alpha_r} \quad , \qquad (5.20)$$

where v_{cf} and v_{cr} are the most and least energetic char-

ge-pumping traps in emission-controlled mode, α_f and α_r are respectively the falling and the rising edge transition rate of gate waveform ($V.S^{-1}$), and the other symbols have their usual meaning.

In the determination of the energy distribution, a priori knowledge of $\sigma(v_t)$ is necessary [14] whereas the values of σ is assumed constant in [12]. The gate voltage interval for surface depletion in Eq.(5.10a) is limited by the flatband and threshold voltages. This is true only for a zero reverse bias voltage (V_r = 0). The model [14] reduces to a simpler form for the case of steady-state capture processes and identical rise and fall times. This simple model can be easily applied provided that the energy distribution of the interface-trap density and the mean capture cross-section are known. The former has been extracted with the aid of the measured dc generation current and the latter by the method proposed by Groeseneken et al [12]. Therefore, the most significant limitation encountered in this model [14] is the determination of the mean capture cross-section which requires the use of the Groeseneken et al model [12]. However, the value of σ found by Groeseneken et al [12] is based on some assumptions already discussed in section 5.5. Although the technique [12] has several limitations, its inability to penetrate midgap and the inaccuracy of the capture cross-section measurement are quite important.

A new technique [15] based on charge pumping and pulsed interface probing has been developed for the spectroscopic characterization of interface traps in MOS devices. This technique is based on the combination of the conventional charge-pumping [12] and the pulsed interface probing (PIP) technique [52]. The latter is performed by periodically driving the interface from depletion into inversion by using narrow pulses as shown in Fig.5.4a. The modified charge-pumping technique is based on the same experimental procedure as PIP with the only exception that an accumulation pulse is added to each cycle. The resulting bipolar gate waveform, shown in Fig.5.4b, creates recombination at the interface just like the trapezoidal waveform of the original charge-pumping technique. The only difference between these two waveforms is the absence of inverting pulses in the latter. It consists of measuring the source currents by using, alternatively, the bipolar waveform and the unipolar waveform. Since these narrow inverting pulses have negligible effect on the leakage current, particularly for the long emission times involved in midgap scanning, the source current measured with the unipolar waveform is equal to the leakage component of the source current measured with the bipolar waveform. The difference between the source current values measured with the two waveforms is independent of

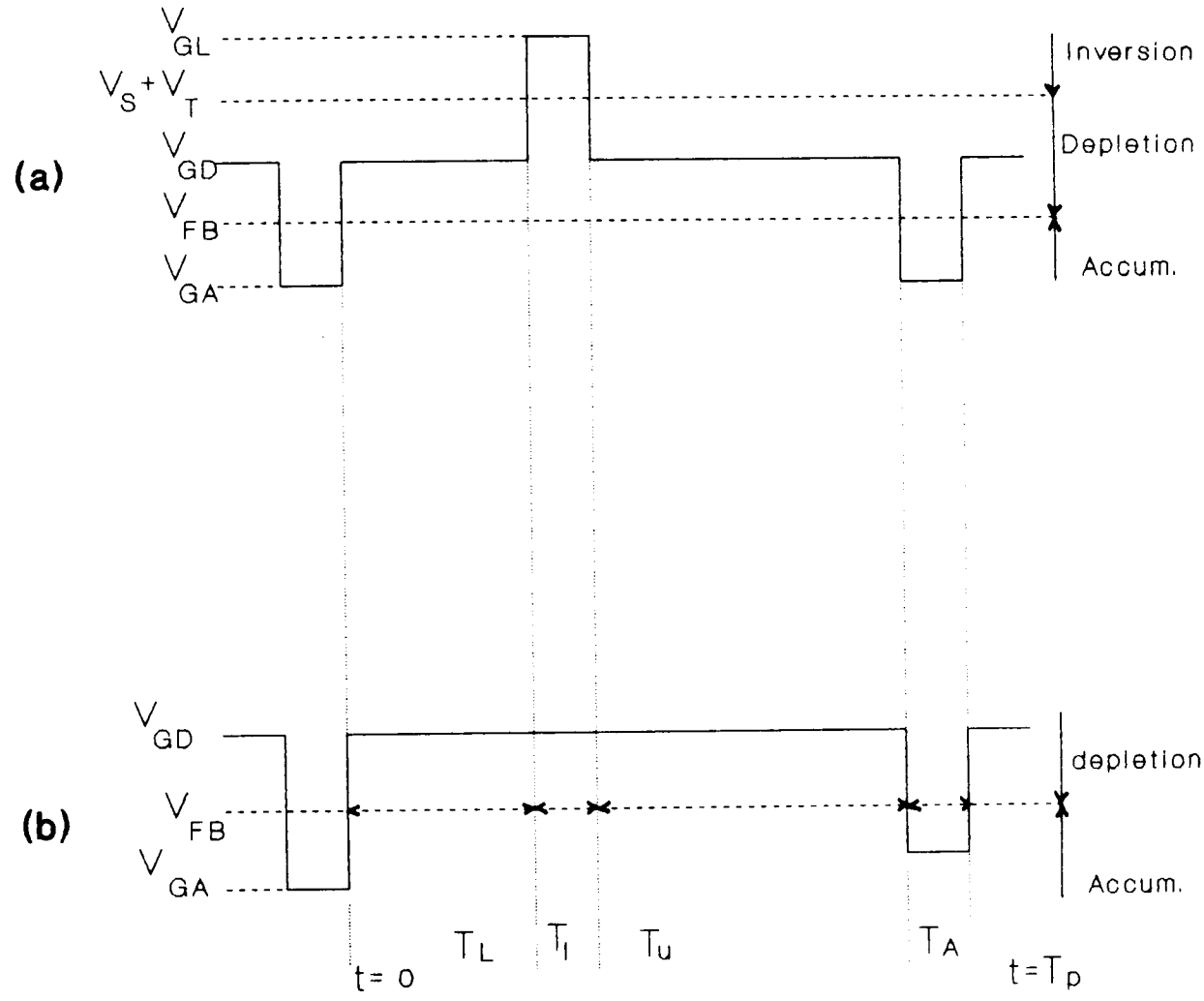


Fig.5.4 Two gate waveforms used in the modified charge-pumping technique, (a) Bipolar, (b) Unipolar.

noninterface currents and, therefore, is used for the determination of interface-trap density and capture cross-section. The measured difference can be expressed as

$$\Delta I_s = I_{it2} - I_{it1} \quad , \qquad (5.21)$$

where I_{it2} and I_{it1} denote the interface current for the bipolar and unipolar waveforms, respectively. This technique [15] removes the above mentioned limitations and eliminates some potentially distorting effects associated with the original charge-pumping technique such as the dependence of emission times on the flat-band and threshold voltages of the device under test and on source voltage, and on device parameters and terminal voltages. Another significant aspect of this technique [15] is that it specifies the upper and lower limits of the energy range and shows how the scannable range is reduced.

Another technique of measuring the density of interface traps at the Si-SiO_2 has been developed by Tseng [40]. This method is based on a charge-pumping phenomenon without the need for Shockley-Hall-Read (SHR) theory. The technique resembles low-frequency C-V in that it attempts to measure a change in stored charge in a device between equilibrium states of the device. The technique depends strongly on the applied gate signal which is a complex form shown in

Fig.5.5. This waveform allows the separation by energy position, that is, which states will behave as traps and which as recombination centers. The latter will effectively contribute to a measured dc current flowing across the source/drain substrate junction. The resulting measured current is given by [40]:

$$I_{cp} = -qAf \int_{\phi_{F-step}}^{\phi_{FH}} D_{it}(\phi) d\phi - f Q_{rit}^{s/d} \quad , \qquad (5.22)$$

where $Q_{rit}^{s/d}$ is the charge supplied to unfilled interface traps from the source/drain region via electron transport along the conduction band and subsequent electron capture, ϕ_{FH} and ϕ_{F-step} are the surface potential values equal to E_{FH}/q and E_{F-step}/q, respectively, and the other symbols have their usual meaning. E_{FH} is the Fermi level energy at the interface associated with the highest gate voltage V_H, and E_{F-step} the Fermi-level energy established at the interface during the time t_{step}. Taking the derivative of Eq.(5.22) with respect to ϕ_{F-step} yields

$$\frac{dI_{cp}}{d\phi_{F-step}} = qAf D_{it}(\phi_{F-step}) \quad , \qquad (5.23)$$

and expressing the derivative of I_{cp} as a partial derivative

with respect to the gate potential and solving for $D_{it}(\phi_{F-step})$,

$$D_{it}(\phi_{F-step}) = \frac{1}{qAf}\frac{dI_{cp}}{dV_{step}}\frac{dV_{step}}{d\phi_{F-step}} \quad . \qquad (5.24)$$

The determination of the energy density of interface traps from Eq.(5.24) requires the knowledge of the gate voltage-surface potential relation. Equation (5.24) is derived by making some assumptions concerning the timing features t_{H-step}, t_{step}, and t_{step-L} of the gate waveform. For Eq.(5.24) to be valid at a particular E_{F-step}, the timings t_{step} and t_{step-L} should satisfy the following condition:

$$t_{step-L} < \tau_n < t_{step} \quad , \qquad (5.25)$$

where τ_n is the electron emission time constant. Furthermore, t_{H-step} should be large enough to prevent the occurrence of transient accumulation phenomenon during the transition from the high to step voltage levels at the gate. In order to find the voltage range of V_{step}, which corresponds to the location of the Fermi level in a range of energy traps whose constant fall within the window is given by Eq.(5.24), V_{step} is swept from V_T to V_{FB}. Figure 5.6 shows a theoretical charge pumping current as a function of a step voltage. The slope of region II of the I_{cp}-V_{step} curve is directly proportional to D_{it}, as analytically given

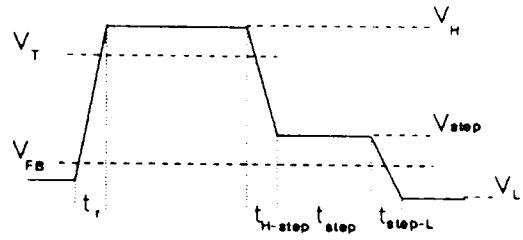


Fig.5.5 Gate waveform used in new charge pumping method.

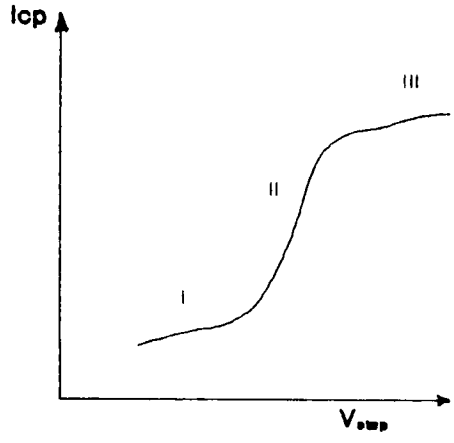


Fig.5.6 Theoretical charge pumping current Icp as function of gate step voltage V_{step}.

by Eq.(5.24). However, Eq.(5.24) is not applicable in either region I or III because the Fermi level no longer ensures those traps, lying above E_{F-step}, and detraped by electron emission to the conduction band and traps, lying below E_{F-step}, and detraped by hole capture from the valence band.

This method [40] distinguishes itself most from the previously proposed charge-pumping methods, such as those found in [12,45], in that it can provide a quasi-static type method by establishing a quasi-Fermi level at the location in the bandgap where D_{it} is to be determined. However, a few limitations and uncertainties may be pointed out here which seem inherent in this approach of charge-pumping technique [40]. The timing features t_{H-step}, t_{step}, and t_{step-L} of the gate waveform must satisfy the restrictions discussed above to make Eq.(5.24) valid in both inversion and depletion and hence the determination of D_{it} as indicated by Eq.(5.24). The determination of D_{it} requires the dependence of surface potential on gate voltage, which can be obtained by QSCV technique of the MOS structure. As pointed out in section 4.1.2, the QSCV itself presents some limitations in determining the gate voltage-surface potential relationship which is used to determine D_{it}. In addition , to locate the Fermi level in a range of energy traps whose time constants fall within the window given by Eq.(5.24), V_{step} must be swept from V_T to V_{FB}. The use of V_{FB} and V_T may introduce an error

in D_{it} since there is no accurate method for the determination of flat-band voltage. Finally, the last drawback encountered in this technique is the procedure used to determine the transition times needed to eliminate the transient accumulation phenomenon or so-called geometric component for different device geometry.

CHAPTER 6

MEASUREMENTS AND EXPERIMENTAL RESULTS

6.1 INTRODUCTION

The present project was undertaken to develop the charge-pumping technique for studying the properties of interface traps in the laboratory using Groeseneken et al model [12] with the aim of verifying the results of previous workers and to explore if any more useful variation or modification in the existing techniques could be achieved. During the course of the proposed experimentation with the charge-pumping technique we have observed a considerable amount of dc substrate-current when the surface-region of the MOSFET is periodically cycled between the flatband and threshold voltage. Arguments show that this current arises due to the non-steady-state emission of carriers. This led to the development of a new technique and experimentation

which will be presented in the next chapter. All the experimental results on the measurement of charge-pumping current revealing its different characteristics as regards to its suitability or limitations in the study of interface trap charges in MOS devices are given in this chapter.

6.2 MEASURING EQUIPMENT

All the measuring instruments of the present experimentation used in this work have been chosen with H.P. competivitity so that they may be made to function in the automated mode in conjunction with a H.P. Computer. A description of each instrument is given in the following.

a) The HP Computer:

The HP 9836 desktop computer is a top-quality computer and powerful instrument controller. Its integrated design, easy programming language, and many features make it simple to program and to operate. The HP computer is programmed to control the compatible instrumentation acquiring the data and to process it to yield the desired results. A software is developed to control measuring instruments and to record and analyse data. Different I-V and I-F characteristics have been plotted on the HP 2631G printer.

b) The Picoammeter:

The HP 4140B picoammeter and dc programmable voltage

source was used to measure the substrate current. It is also used to measure I-V characteristics and a low C-V curve (or quasi-static capacitance). It has a built-in ramp generator (100 mV/sec), a zero offset control to cancel displacement current through test leads or test fixtures, and gives capacitance versus voltage or normalized capacitance versus voltage measurements. It has digital readout and can be interfaced with an HP computer. It comprises a high stability pA meter with 10^{-15}A resolution and has an accuracy of 5% for long integration times (1-2 sec) at current levels of 10 pA. It is provided with two programmable voltage sources. One of the two voltage sources (V_A) can operate not only as a programmable dc voltage source, but also as a unique staircase and accurate ramp generator with an output range from -20 to 20 volts. The other one (V_B) which is a dc voltage source has an output range from -100 to 100 volts.

c) The Digital Multimeter:

The HP 3478A digital multimeter is a very powerful instrument and fully programmable HP-IB. It is used to measure the amplitude of the gate signal applied to the device. The HP 3478A offers dc voltage performance from 100 nanovolt sensitivity up to 300 volts (full scale), true RMS capability up to 300 kHz, and resistance measurements from 100 microohm sensitivity to 30 Megaohm (full scale). Its dc

and true RMS ac current measuring capability is from 1 μA to 3A. This instrument can be readily interfaced with a computer model.

d) The Frequency Meter:

The HP 5325A frequency counter is a high performance instrument for measuring the frequency as well as the period of the applied signal voltage. It has a high sensitivity and accuracy. The sensitivity for frequencies is 1 μHz and for period 1 nanosecond. This instrument is an HP-IB compatible.

e) The Function Generator:

Three function generators and one pulse generator have been used either individually or in combination to provide the desired signal.

The Tektronix RG.504 generator provides low distortion sine, square, triangle, and pulse waveforms over the frequencies from 0.001 Hz to 40 MHz in ten decades. The output amplitude is 10 mV to 30 volts peak-to-peak into an open circuit and 5 mV to 15 volts into a 50 ohm load. It has a voltage-controlled frequency (VCF) input that controls the output frequency from an external voltage source.

The Tektronix RG.501 is a pulse generator which generates a sawtooth waveform of different period and fall and rise time.

The HP 3311A is a versatile function generator having sine,

triangle, square and pulse outputs with a maximum output of 10 volts peak open circuit or 5 volts peak into 600 ohm. The signal may be offset by ±10 V dc or ±5 V respectively. The pulse output has a duty cycle of 10 to 20% of the total period. Its frequency range is 0.1 Hz to 1 MHz. The frequency may be externally controlled by an application of an external voltage to the VCO terminals. It has the floating ground feature, and is suitable to be used in series with either of the generator to provide a desired output.
The Wavetek 180 model function generator was used to supply a signal of constant amplitude and variable frequency for precise purpose. It provides sine, square and triangle waveforms over the frequencies from 0.002 to 2 MHz. It is characterized by its output fine adjustment and the VCO (voltage controlled oscillator) input.

f) The Oscilloscope:

The Tektronix 7603 oscilloscope is a dual input channel with a sensitivity of 1 millivolt and 0.1 μs. It was used to display the shape of the applied signal and eventually for adjustment in the amplitude.

g) The Microscope-Prober:

This probe station is suited for measuring MOSFETs and MOS capacitors made in array on a silicon wafer or incorporated in a test pattern in a wafer containing an array of

integrated circuits. All electrical connections to external instruments were coaxially shielded up to the micromanipulators. The microscope-prober used was the Karl-Sauss MP5 prober. It has 100 probe fix points and a microscope with a variable magnification scale. It is HP-IB compatible and interface readily with a computer model.

h) The Test-Fixture Box:

The HP 16055A test-fixture box with its corresponding accessories was used for connecting general devices. The electrostatic/light-shielding cover allows stable and accurate measurements at extremely low current levels.

6.3 EXPERIMENTAL DEVICES

The experimental devices used in this study came from different suppliers with different technology.
One set of devices consists of a few commercial devices such as MOS transistor 3N170 manufactured by National Semiconductors company U.S.A. These MOS transistors are four terminal devices having isolated substrate, gate, drain and source. Among the device parameters, only the threshold voltage is known.

Another set consists of a number of devices in the form of wafers, fabricated by ES2 (European silicon structures,

France) laboratory, which were made available for the present experimentation by courtesy of CDTA (centre de development des technologies avancees) research center. Figures 6.1 and 6.2 show different sets of devices fabricated by ES2 laboratory. The wafers consist of MOS transistors and MOS diodes with different gate-areas. All the devices from ES2 laboratory have a common doping concentration of the substrate and oxide thickness. Figure 6.1 shows wafers fabricated by ES2 using the 1.2μm CMOS technology. They consist of sets of transistors having the source, the gate and the substrate common. One series is an n-type and the other is a p-type substrate. The device parameters of two series are summarized in table 6.1. Figure 6.2 shows another set of wafers fabricated by ES2 laboratory using the 2 μm CMOS technology. All transistors are n-channel with independent substrate and source. Each transistor is built on a specific well and their terminals (gate, source, drain, and substrate) are independently accessible. In addition there are some MOS capacitors which are built in the n-substrate. The doping concentration of p-well is $7.6x10^{15}cm^{-3}$ in the transistors and that of the n-substrate is $2.7x10^{16}cm^{-3}$ in MOS diodes. Dry nitrogen annealed oxide of thickness 400 A is used underneath the aluminium gate in all the devices. Some of these wafers are encapsulated in 64 pin PGA package. The

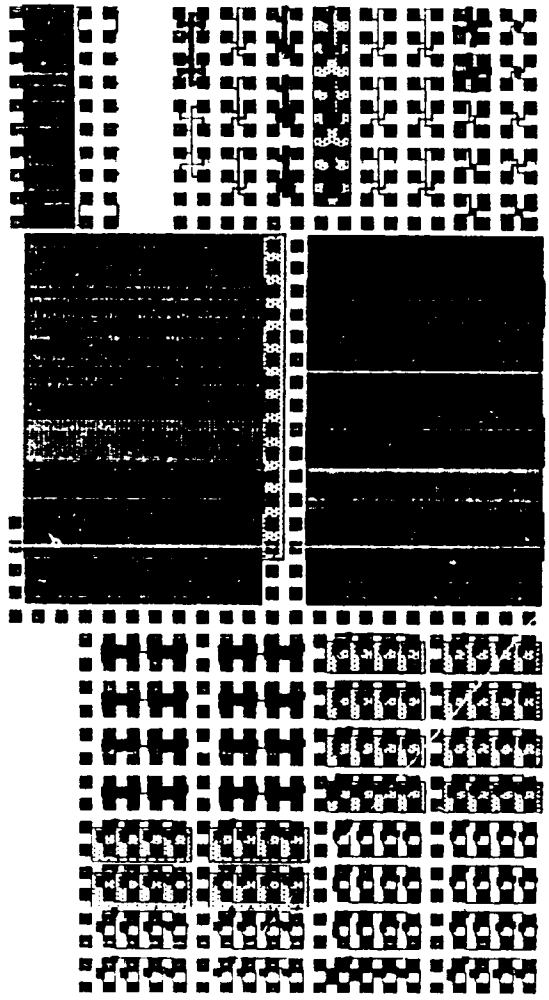


Fig.6.1a General view of a wafer fabricated by ES2 laboratory using 1.2 um process.

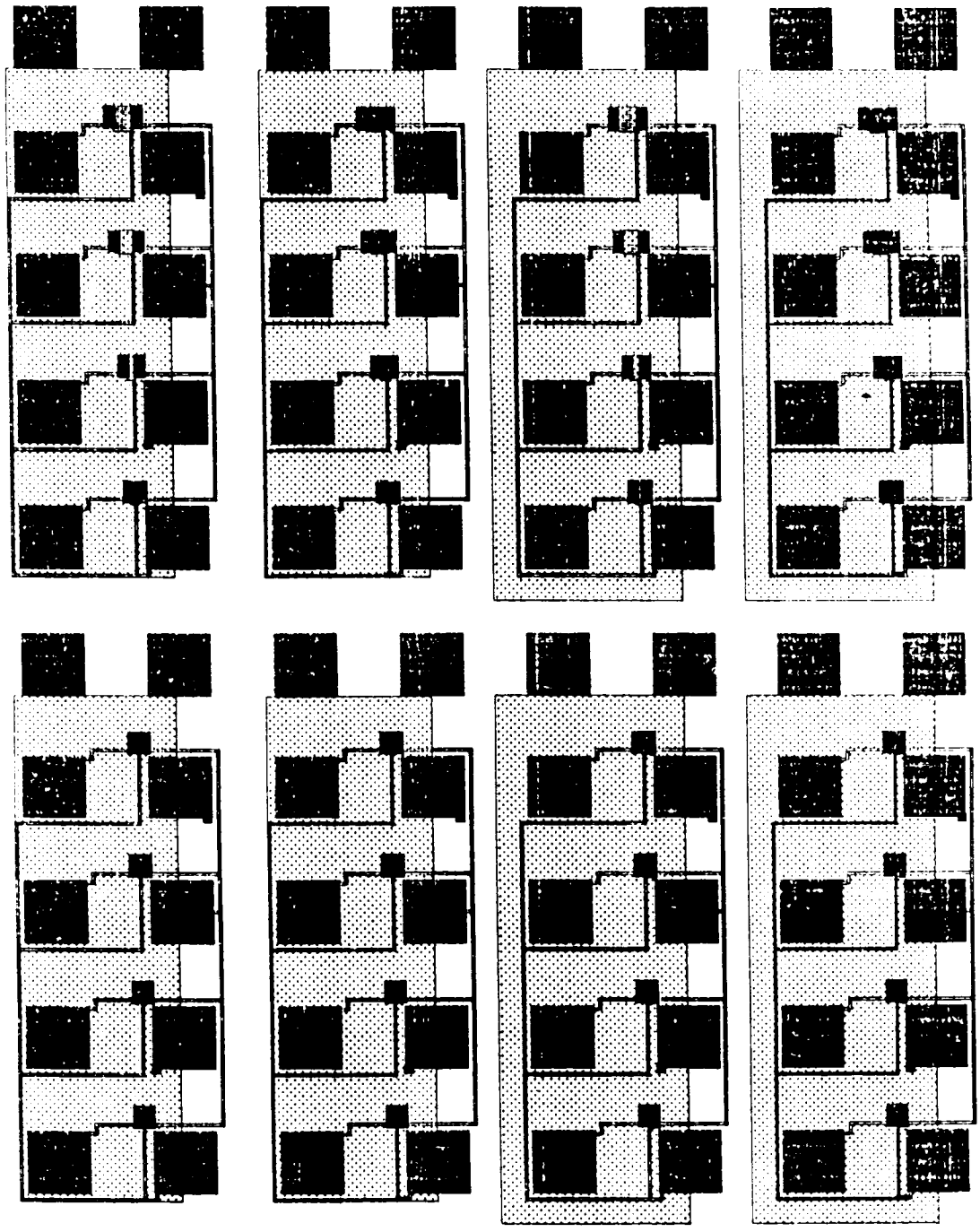


Fig.6.1b View of a MOSFET included in a wafer fabricated by ES2 laboratory using 2 um process.

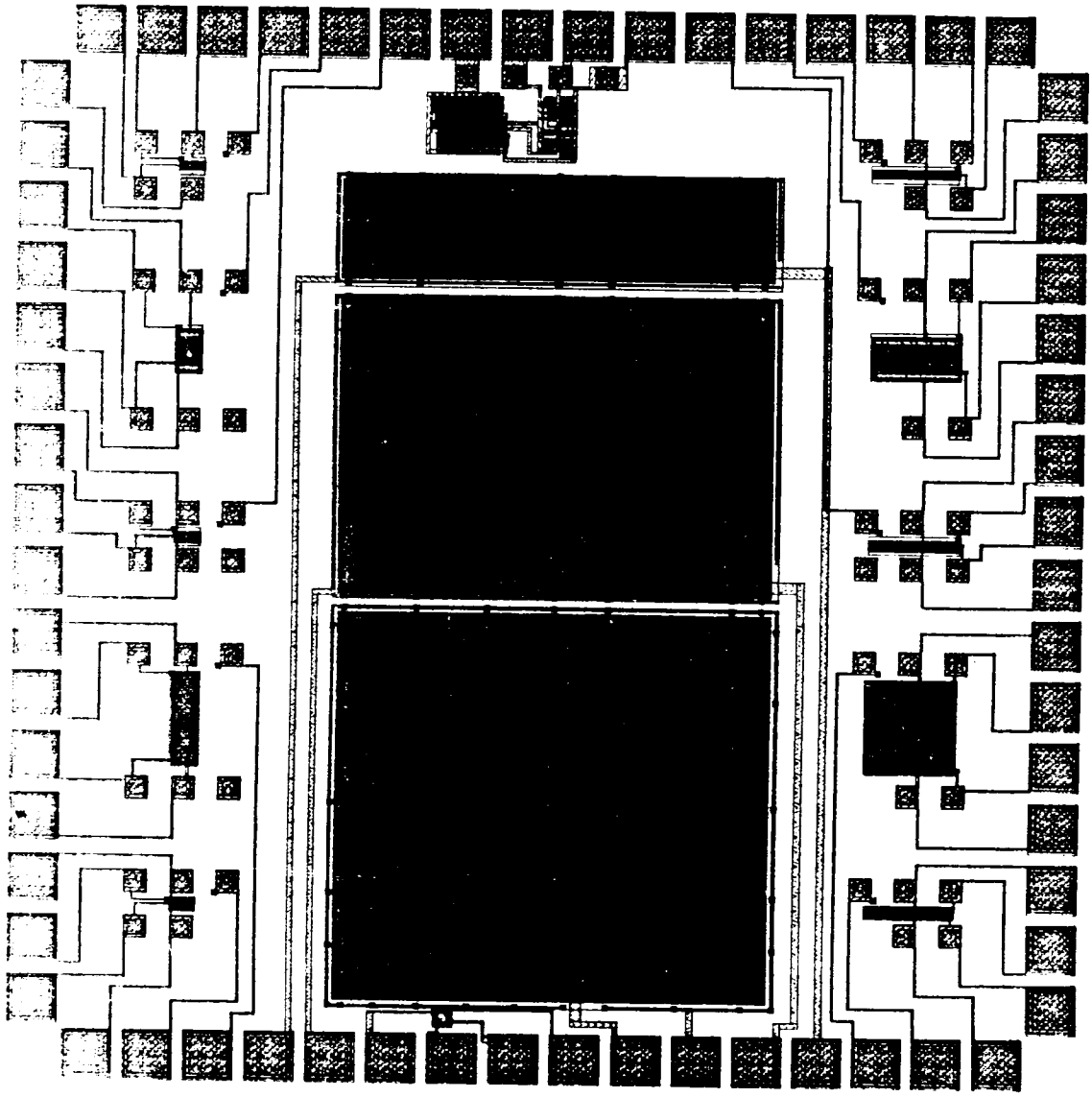


Fig.6.2 General view of a wafer fabricated by ES2 laboratory using 2 um process.

TABLE 6.1 Device parameters of wafers shown in Fig.6.2.

MOS device	Area WxL (μm^2)	Type	N_a (cm^{-3})	tox (nm)
TR: 1	80x2	n-channel	$7.6x10^{15}$	40
TR: 2	80x8	"	"	"
TR: 3	80x20	"	"	"
TR: 4	80x80	"	"	"
TR: 5	80x300	"	"	"
TR: 6	300x2	"	"	"
TR: 7	300x8	"	"	"
TR: 8	300x20	"	"	"
TR: 9	300x80	"	"	"
TR: 10	300x300	"	"	"
Capacitor or Diode	**Area (mm^2)**	**Type**	**N_a (cm^{-3})**	**tox (nm)**
1	0.5	p-channel	$2.6x10^{16}$	40
2	1.5	"	"	"
3	2.0	"	"	"

gate-area of p-well MOSFETs ranges from 300x300 to 300x8 μm^2 in one series, and from 80x80 to 80x8 μm^2 in the other. Gate area of n substrate diodes has values 0.5, 1.0 and 1.5 mm^2.

6.4 CHARGE-PUMPING EXPERIMENTS

6.4.1 Experimental Set-Up:

The charge pumping measurements were undertaken using the general set-up as shown in Fig. 6.3. The devices used in this study are n-channel MOS transistors, fabricated on p-well. The substrate-current was measured, using the HP 4140B picoammeter, whose output was smoothed internally by a low-pass filter. The HP 4140B is also used to supply a variable output voltage through the programmable source (V_A). This voltage source is used in series with the HP 3311A generator to generate an oscillating signal of variable base level. This signal can sweep the surface-region of the MOS transistor from deep accumulation to deep inversion while the drain D and source S are together connected to the reverse source biasing (V_B) of the HP 4140B. The shape of the applied signal and its position are displayed on the Tek. 7603 oscilloscope. The RG. 501 sawtooth generator is combined with the HP 3311A to provide a desirable sawtooth signal used to determine the density of interface traps [12]. The signal frequency is read on the HP 5874A and its amplitude is read on the HP 3478A multimeter.

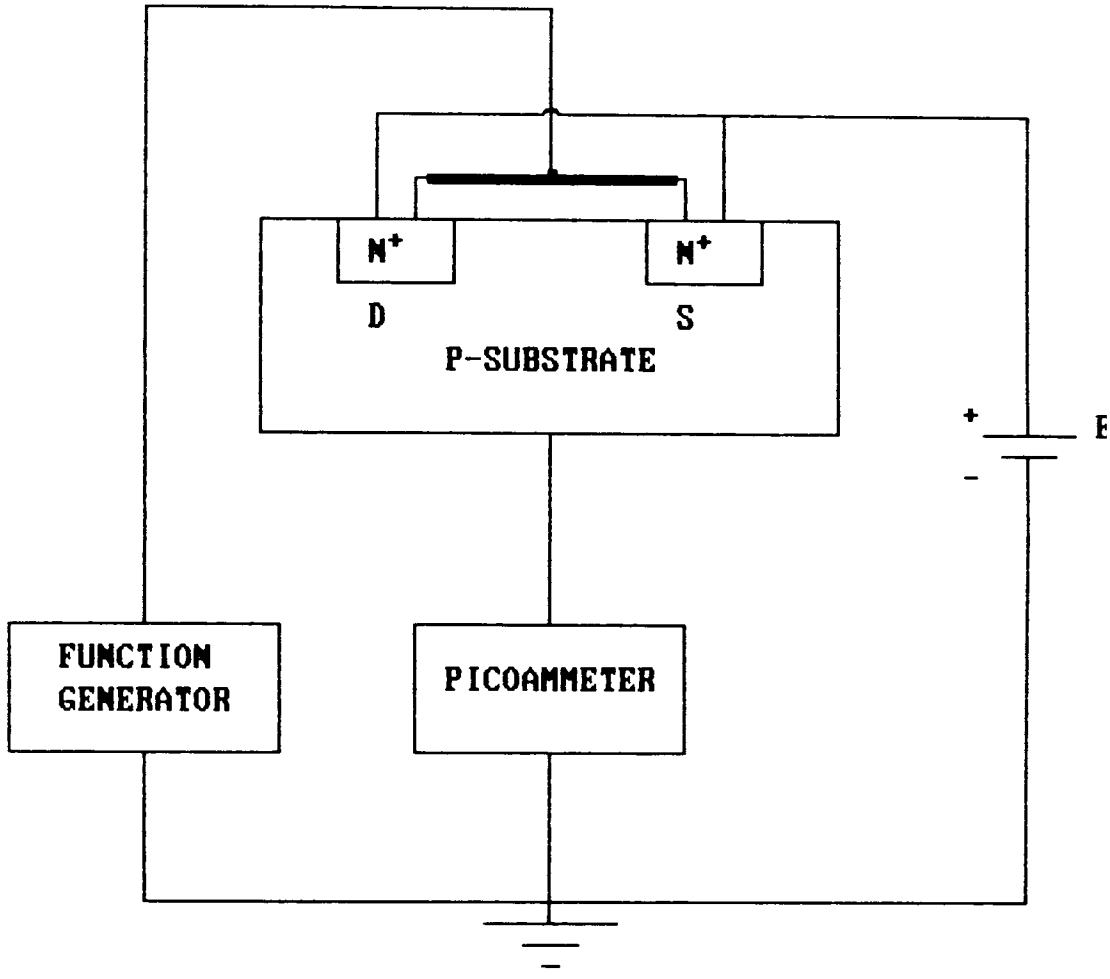


Fig.6.3 General setup illustrating the principle of the charge pumping technique.

6.4.2 Results and Discussion

In this section, we will present our experimental results on the measurements of charge pumping current which we have carried out in order to reproduce and verify the findings of previous workers such as dependence of charge pumping current on the gate voltage amplitude, the frequency, the reverse bias on the source, and the pulse shape. With the aid of the experimental setup shown in Fig.6.3, measurements were done on a number of MOSFETs. A sample was mounted in the 16055A Test Fixture. An HP 3311A Function Generator with a rectangular pulse was used. The amplitude of the pulse was accurately measured by using the HP 3478A digital multimeter, the frequency was measured by the HP 5384A and monitored with the TEK. 7603 oscilloscope. The substrate-current was measured, using the HP 4140B picoammeter. Figure 6.4a shows that the magnitude of the substrate current is increased with gate pulse frequency, becoming linear when leakage effects are swamped. This linearity is clearly indicative of a charge pumping action whereby a fixed charge is measured at each gate pulse. The most commonly used charge-pumping version [32] referred as method B or Elliot method in chapter 5, uses gate pulses with constant amplitude ΔV_A and constant rise and fall times (t_r and t_f), and monitors the charge-pumping currents as a function of the varying base level of the pulses. A typical example of the characteristics that are obtained by Elliot method is

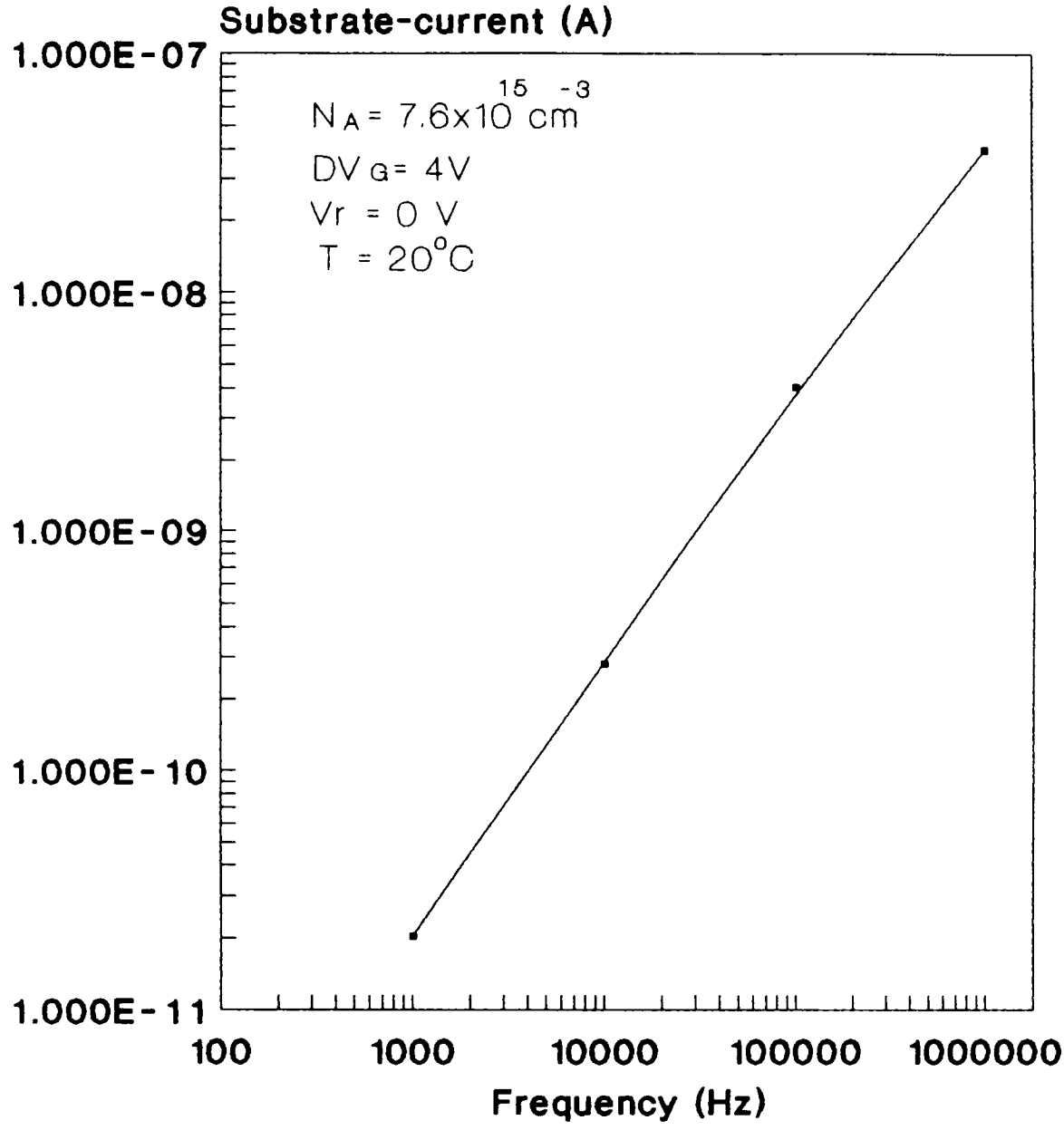


Fig.6.4a Dc substrate current versus gate pulse frequency for an n-channel MOSFET with L = 20 um, W = 300 um, tox = 300 A.

shown on Fig.6.4b (logarithmic scale) and Fig.6.4c (linear scale). Figures 6.5a,b show experimental curves for a commercial device MOSFET transistor 3N 170 and a MOSFET of area 300x8 μm^2 by using Elliot method.

Figure 6.6 shows a comparison of the experimental charge-pumping currents when using method A [31] and method C [41] on one of our devices. The curve (a) on this figure is obtained when using method A; the pulse base level in accumulation was kept at -3 V and pulsed into inversion by increasing the amplitude in steps of 0.5 V. The pulse frequency was 10 kHz and the reverse voltage was equal to 0.2 V. A saturation level for the charge-pumping current is expected when the top of the gate pulse exceeds the threshold voltage of the MOS transistor. The curve (b) is obtained when using method C; the pulse base level in inversion is kept at 3 V and pulsed into accumulation by increasing the amplitude in steps of 0.5 V. The pulse base level is kept constant in inversion to avoid the so-called geometric component of the current , or at least to keep it constant. The charge-pumping conditions are the same as in the previous case. These two methods are reciprocal to each other and do not reveal any basic difference in the characteristics, and in neither case the expected saturation could be obtained.

Figure 6.7 shows the effect of the pulse shape on the charge-pumping current. This effect is illustrated by using Elliot method [32] on one of the devices. The first curve on

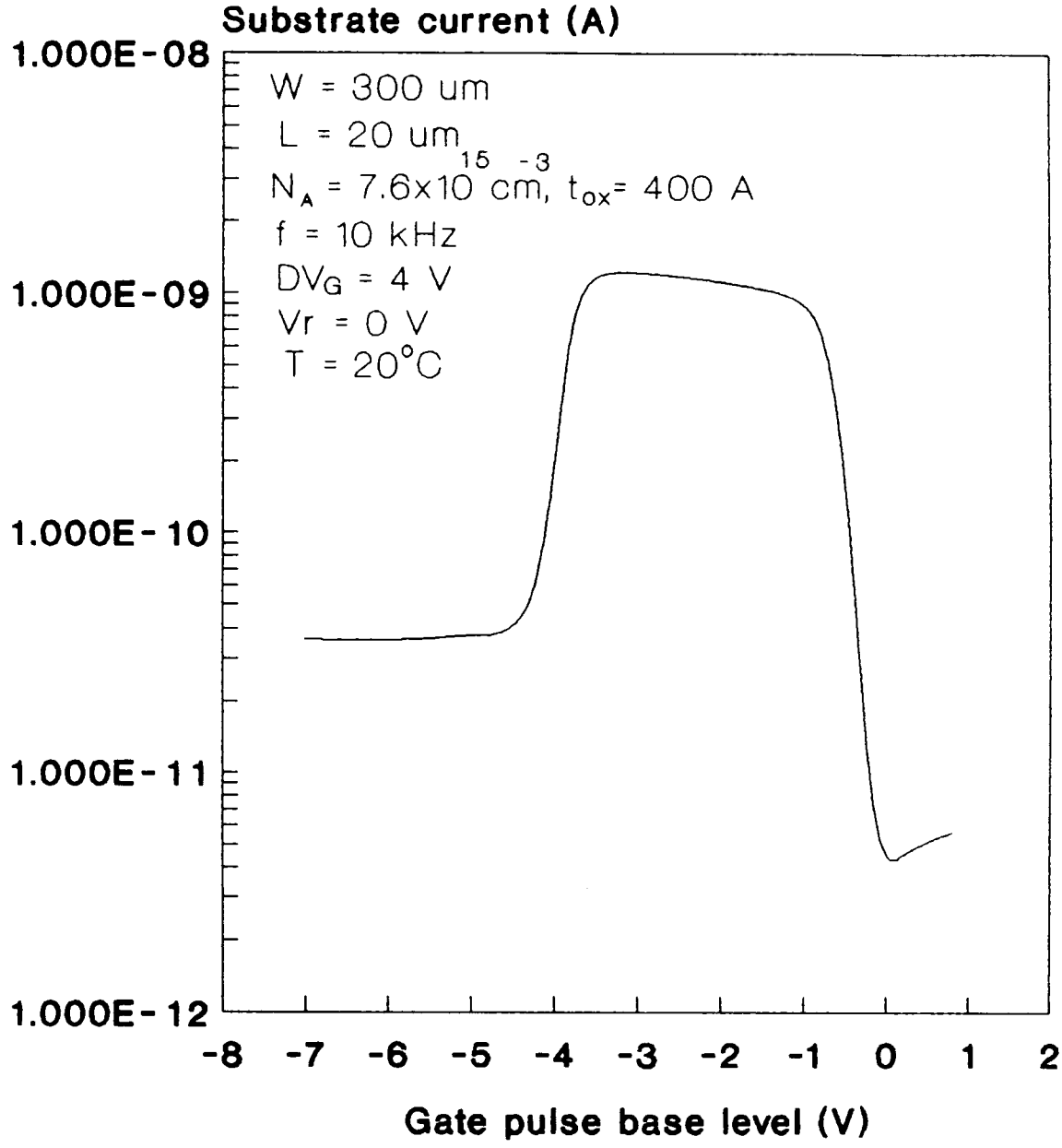


Fig.6.4b Charge pumping current as a function of base level of the gate voltage pulse using Elliot method for MOSFET (Logarithmic scale).

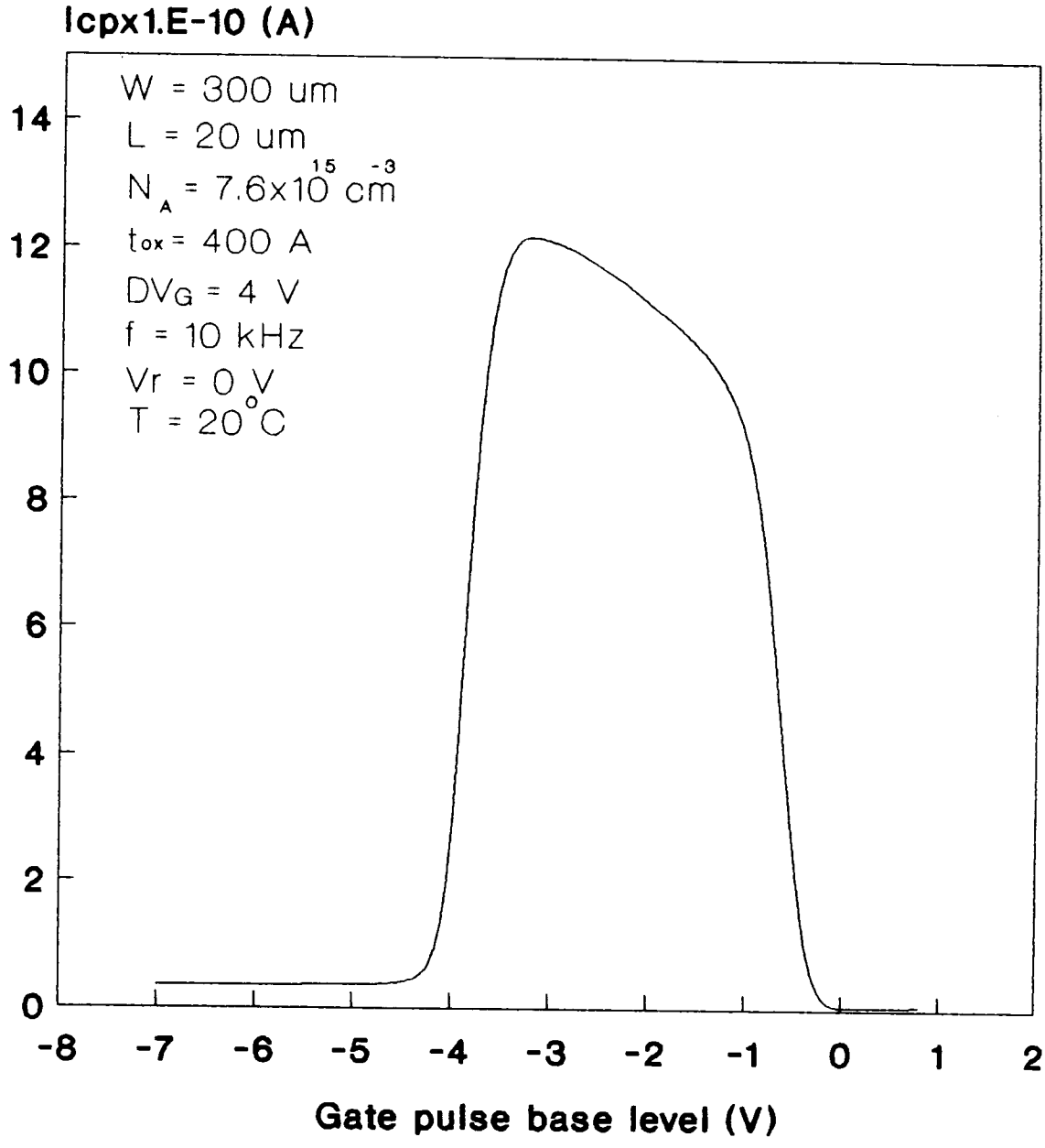


Fig.6.4c Charge pumping current as a function of base level of the gate voltage pulse using Elliot method for MOSFET (Linear scale).

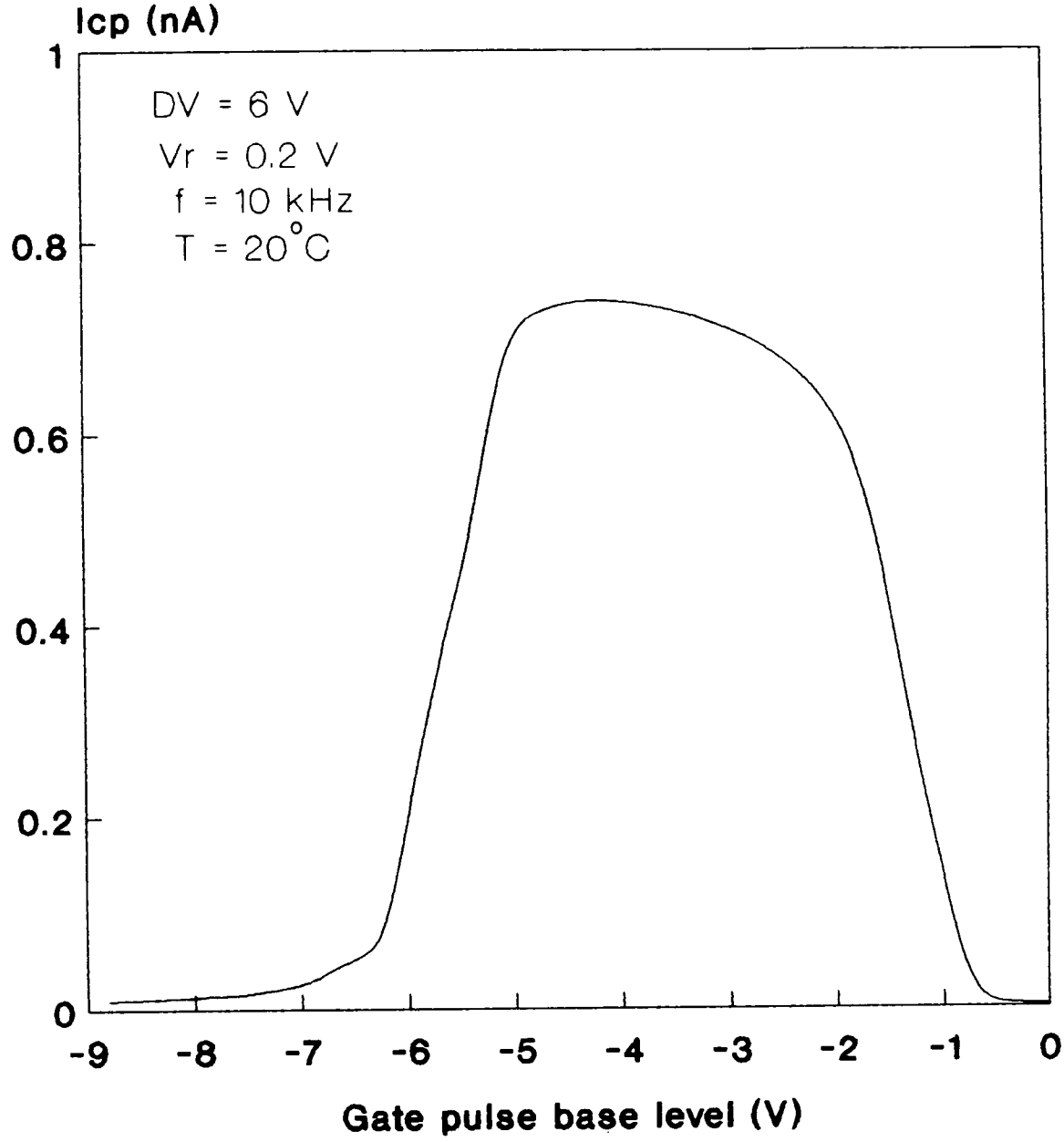


Fig.6.5a Experimental CP curve for an n-channel MOSFET 3N 170 using Elliot method.

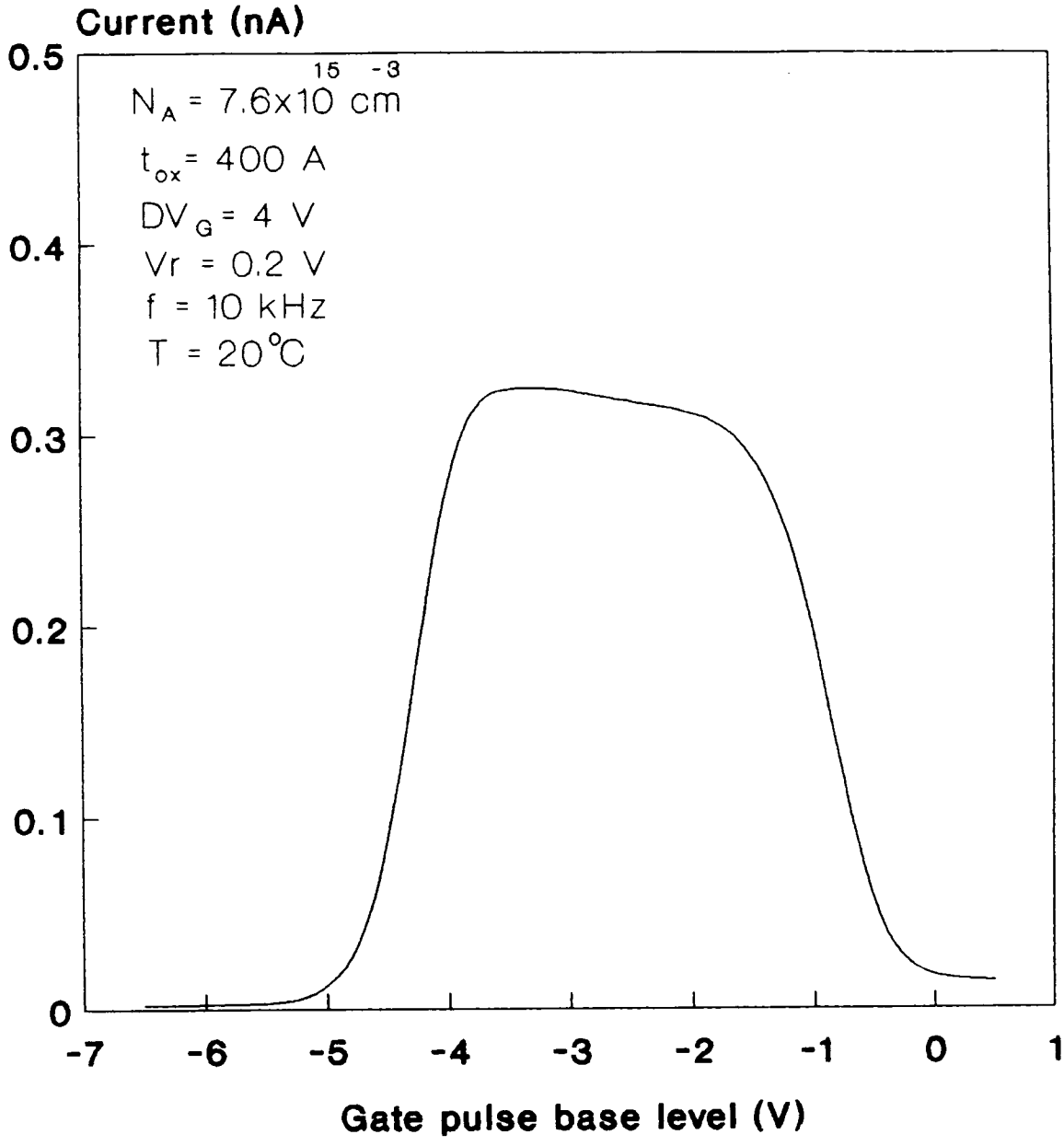


Fig.6.5b Experimental CP curves for an n-channel MOS transistor of area 300x8 um^2 using Elliot method.

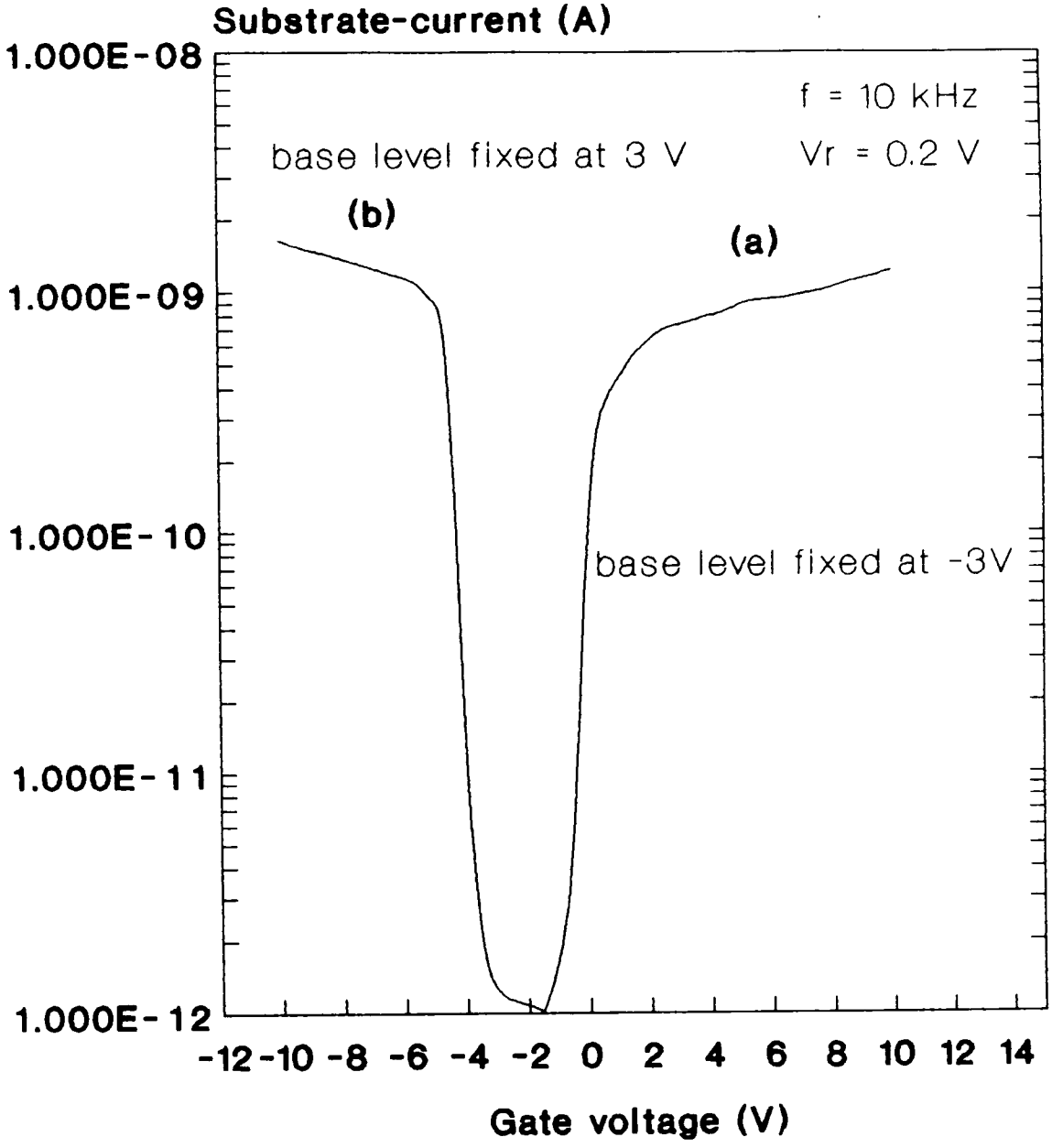


Fig.6.6 Current increase with (a) top level and (b) base level of the gate pulse for MOSFET 3N 170.

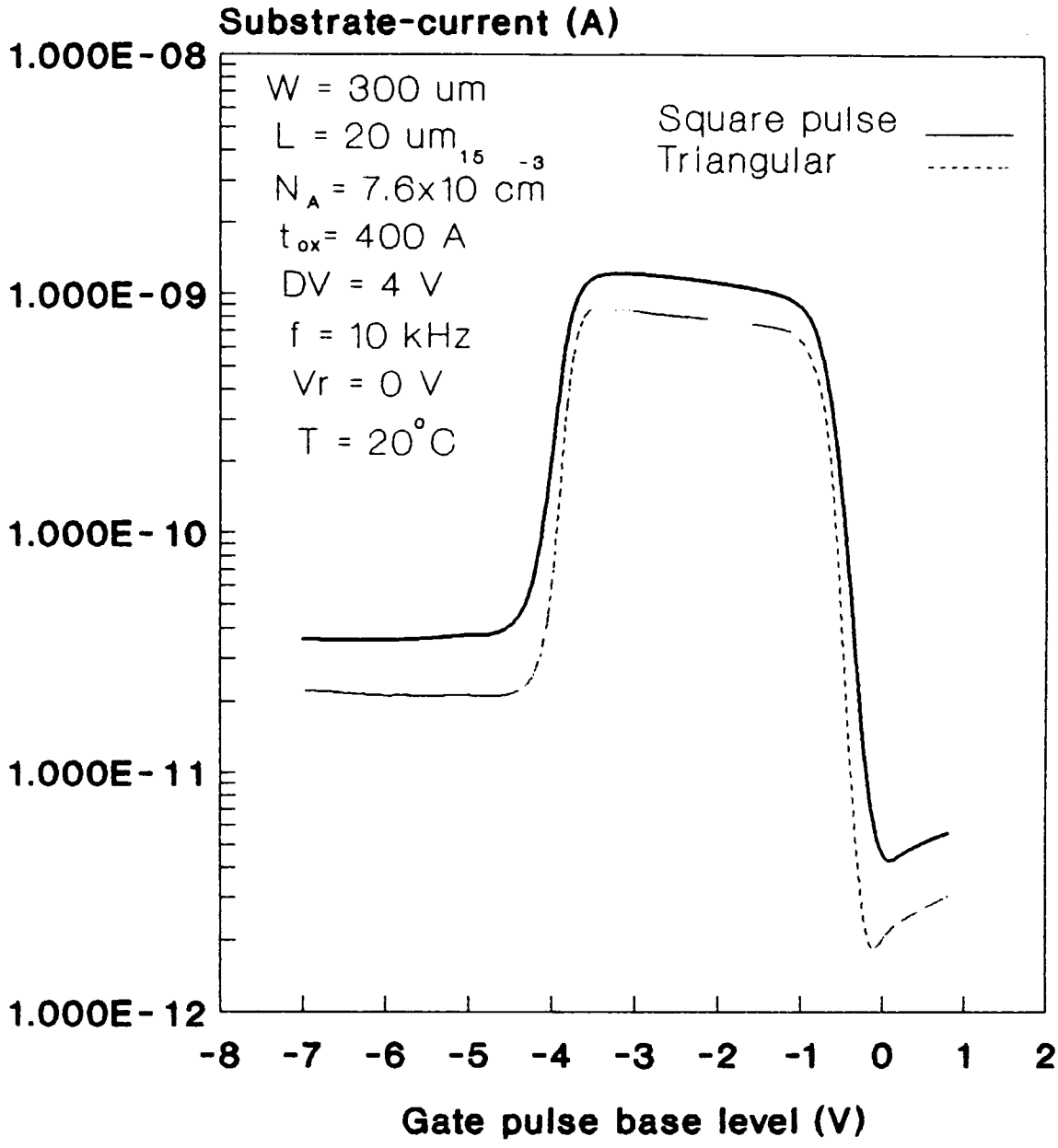


Fig.6.7 Effect of the pulse shape on the Charge pumping current (Logarithmic scale).

this figure is obtained when using square pulses, the second when using sawtooth or triangular pulses. The charge-pumping current for square pulses comes out to be much more than for triangular pulses. This difference is explained by attributing it to a geometric component [31] which is still playing a role. In using sawtooth or triangular pulses, it was believed that this component vanishes because of the longer time available for the mobile carriers to reach source and drain when driving the surface region back towards accumulation.

In order to illustrate the influence of a geometric component, Fig.6.8 shows the curves for one of the devices using Elliot method [32] with W/L = 1, which is not a very favourable geometry. When using square pulses, we observe a very steep current increase with a well defined maximum. When using triangular pulses, the phenomenon vanishes and the current saturates as expected.

In Fig.6.9, the measured frequency dependence of the charge-pumping is shown, for both square and triangular pulses with duty cycle α = 0.5 V. The gate-voltage was switched between -2 and +2 V while a reverse voltage of 0.2 V was applied to source and drain. It can be seen that a linear frequency dependence is obtained for the square pulses and even for the triangular pulses. The charge-pumping current comes out to be more in the case of square pulses than that of triangular pulses because of the larger rise and fall

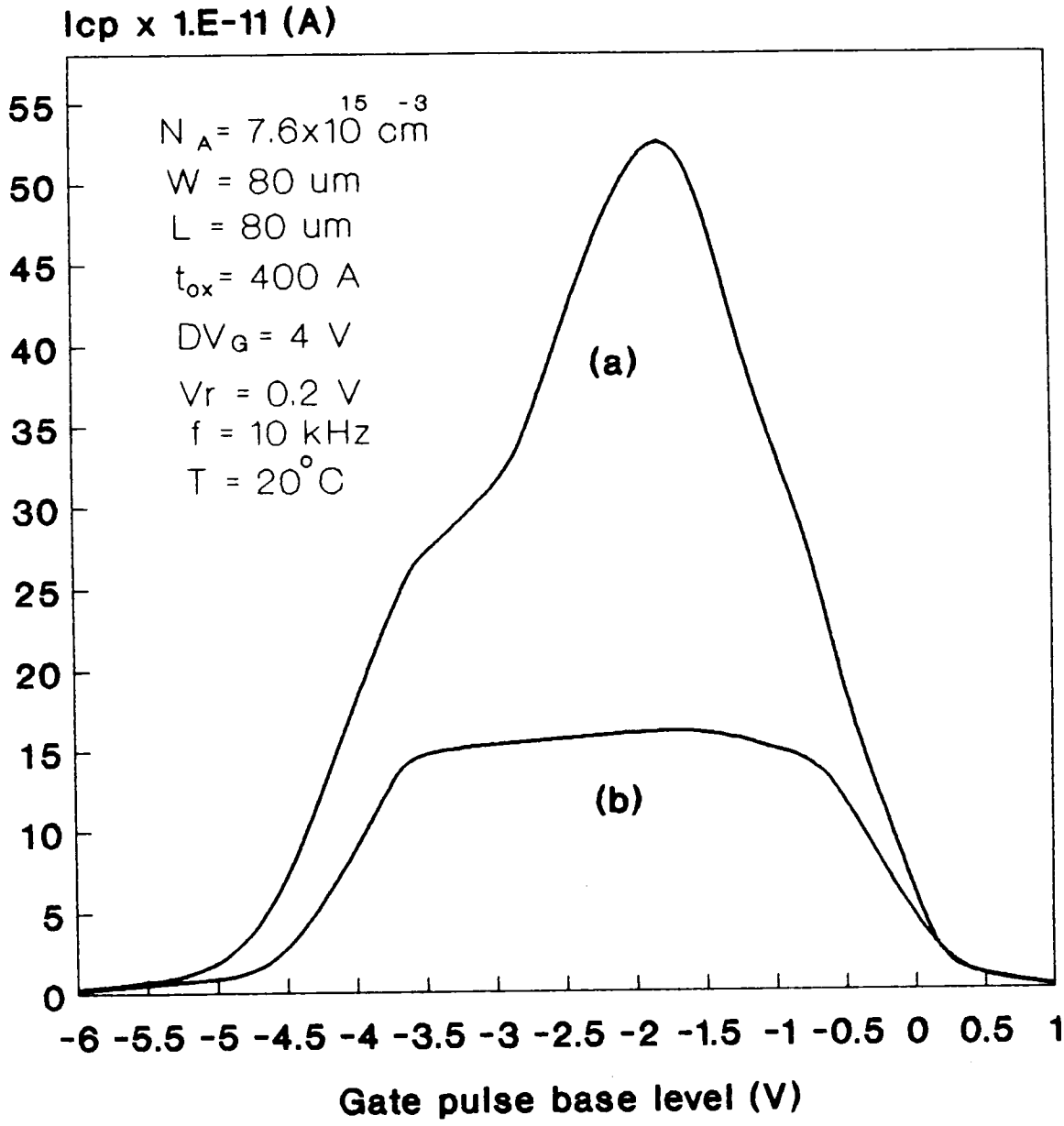


Fig.6.8 Elliot curves for (a) square and (b) triangular gate pulses in a square geometry MOSFET (W/L=1).

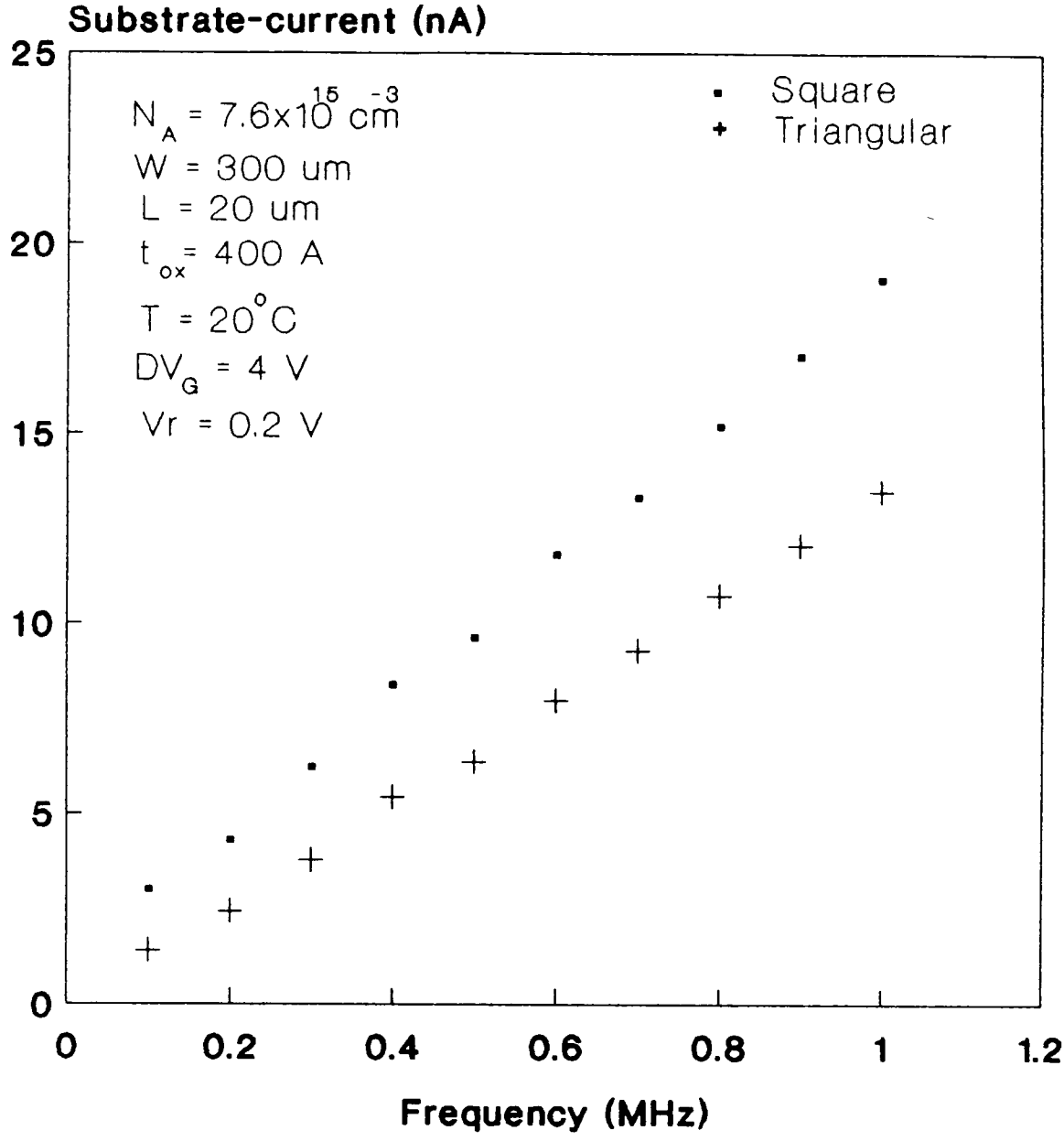


Fig.6.9 Frequency dependence of the charge-pumping current for square pulses and triangular pulses (α = 0.5). The symbols are experimental points.

times for the triangular waveforms as compared to the square waveforms. However, it has been observed that, at frequencies above 1 MHz the current starts decreasing for triangular pulses [12]. It has been found in the present experiment that the above statement was not verified since we did not see any nonlinearity of I_{cp} even for very high frequencies as shown in Fig.6.10. This is supported by the work of Ouisse et al [53].

Figure 6.11 shows the measured charge-pumping current and its dependence on the amplitude of the gate-voltage. By increasing the amplitude of the applied gate-voltage, one can observe an increase of the charge-pumping current as predicted by the emission phenomenon when considering Eq.(5.1a,b). Indeed, by increasing the amplitude of the gate-voltage, one obviously decreases the time that the transistor spends in the depletion, and consequently the time which is available for emission. Therefore, there will be less emission and more recombination, and so the current will increase.

The dependence of charge-pumping current on the reverse voltage is illustrated in Fig.6.12. An increase of V_r is accompanied by an increase of $|V_{FB}-V_T|$ and therefore as predicted by Eq.(5.1a,b) the charge-pumping current is decreased.

Figure 6.13 shows the experimental charge-pumping curves for an n-channel MOSFET at different frequencies when using

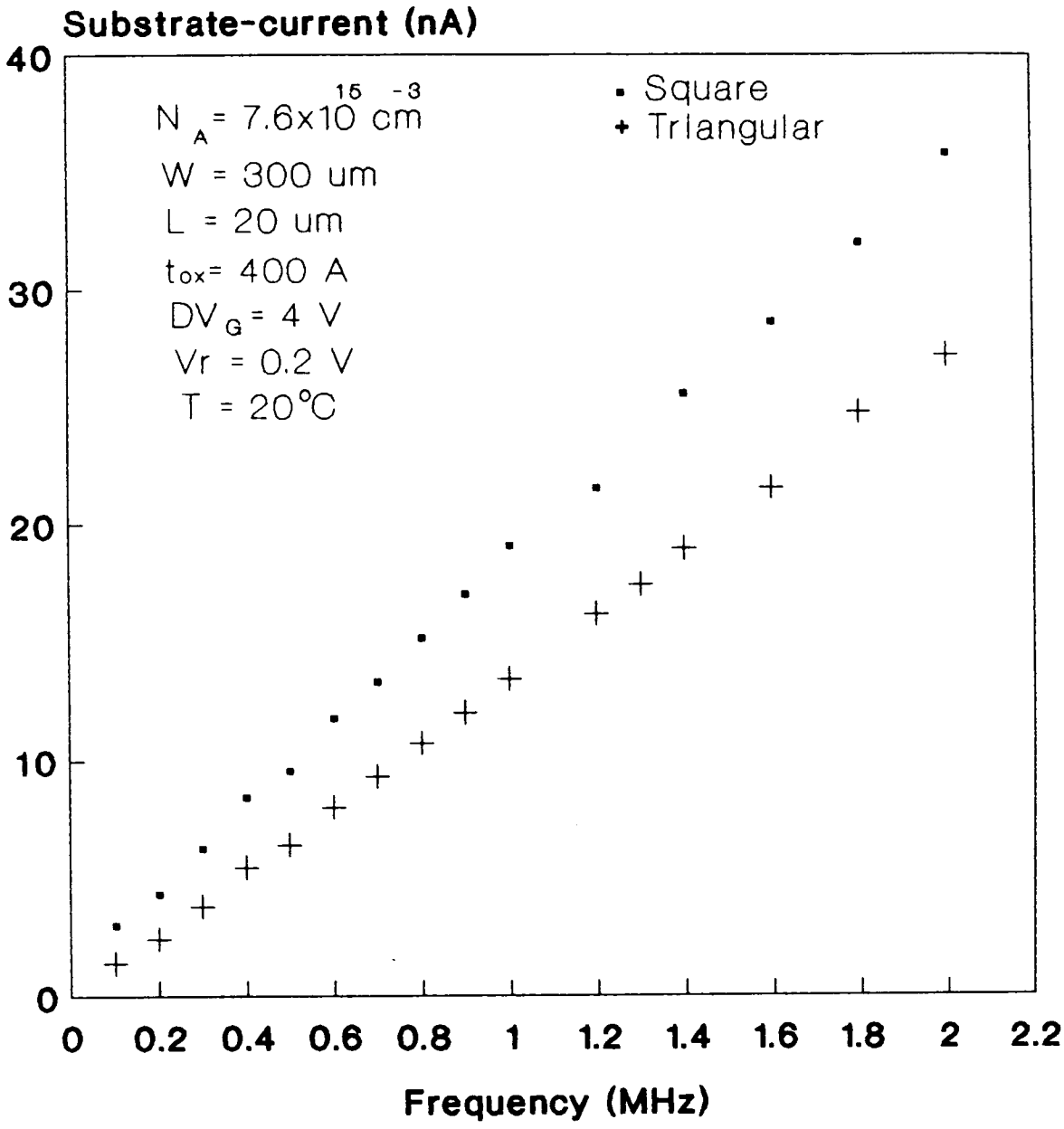


Fig.6.10 Frequency dependence of the charge-pumping current for square pulses and triangular pulses (α=0.5). The symbols are experimental points.

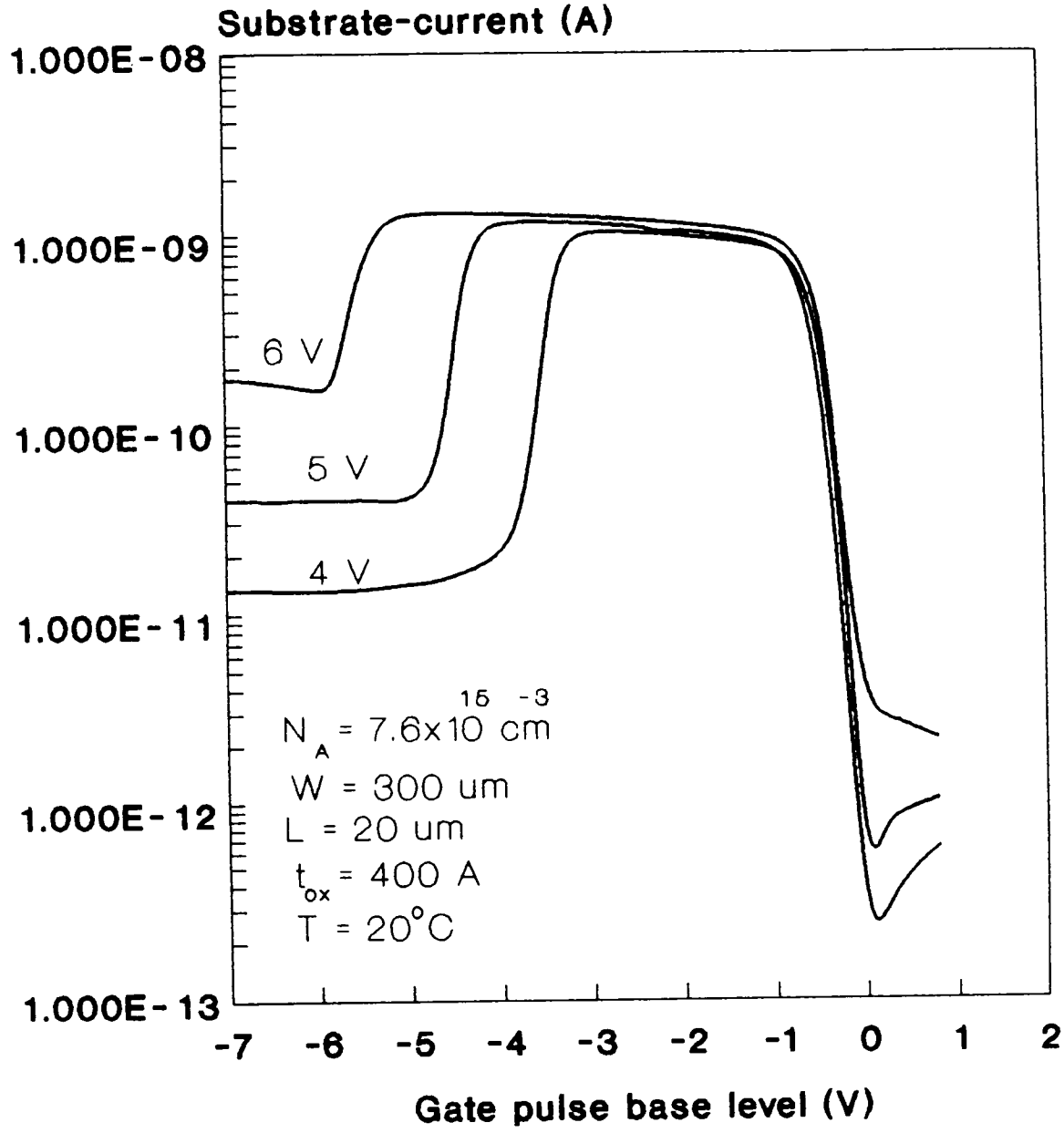


Fig.6.11 Effect of the amplitude of the gate voltage signal on the Elliot curves between Icp and base level. Charge pumping conditions: Vr = 0.2 V, f = 10 kHz.

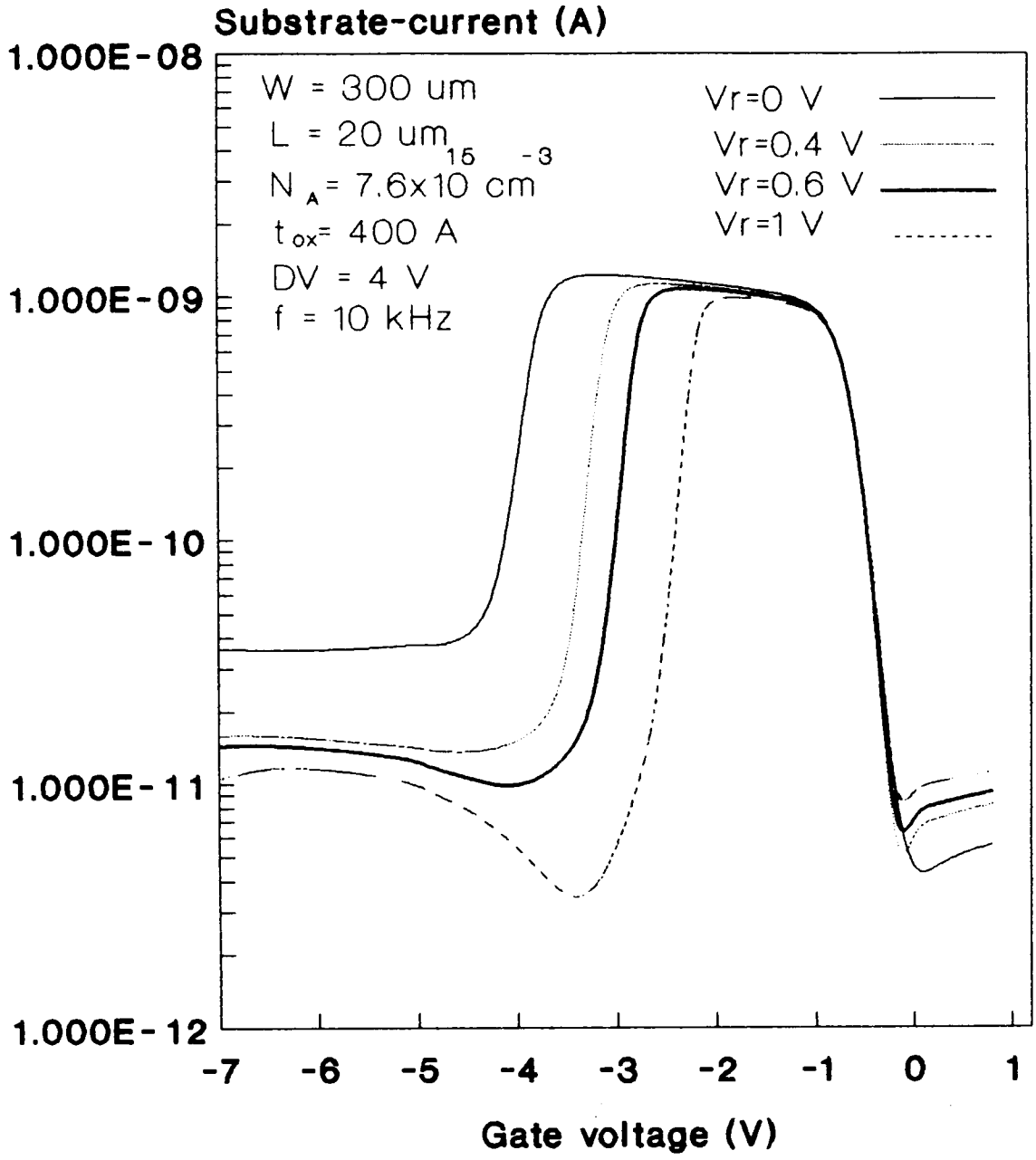


Fig.6.12 Effect of the reverse bias Vr of drain/source on charge pumping current.

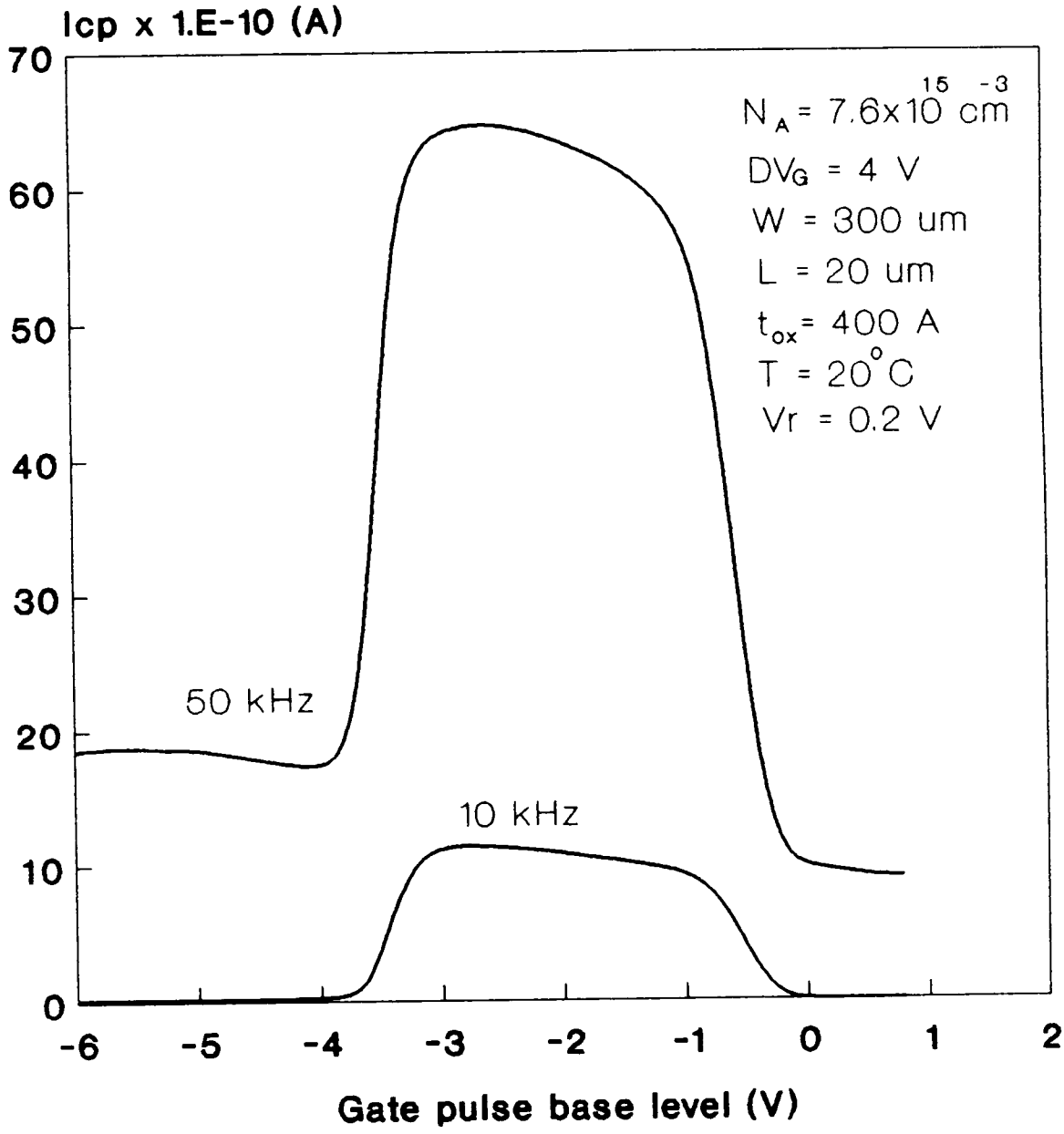


Fig.6.13 Effect of frequency of the gate voltage signal on the Elliot curves between Icp and base level.

Elliot method [32]. The amplitude of the gate signal was 4 V, the reverse voltage was equal to 0.2 V. One can observe an increase of the charge-pumping current when the frequency is increased.

In chapter 5 the total traps-charge Q_{it}, that recombines in one cycle of the applied gate voltage signal, is shown to have a value I_{cp}/f and according to Groeseneken et al [12] Q_{it} versus f curve is supposed to come out a straight line. The intercept f_o of this straight line on the frequency axis is shown to be related to the average capture cross-section $\sqrt{\sigma_e \sigma_h}$ by Eq.(5.15) and the slope of the straight line is shown to be related to the average density of the surface traps $\overline{D_{it}}$ by Eq.(5.16). Figure 6.14a shows Q_{it} versus frequency used to determine the geometrical mean value of the capture cross sections and the mean value of the interface-traps density for an n-channel MOSFET with a channel length of 20 μm, a channel width of 300 μm, and an oxide-thickness of 400 A. The gate pulse amplitude for the triangular waveform (α = 0.5 V) was 6 V while a reverse voltage of 0.5 V was applied to the source and drain. From the extrapolation of this experimental curve to zero charge, the obtained frequency f_o gives a value for a mean capture cross-section of about $4.5x10^{-15}cm^2$, and the slope of this curve gives an average interface-traps density of $2.27x10^{10}cm^{-2}eV^{-1}$. Similarly, Fig.6.14b shows Q_{it} versus frequency for a MOSFET of area 300x8 μm^2. It may be noted that

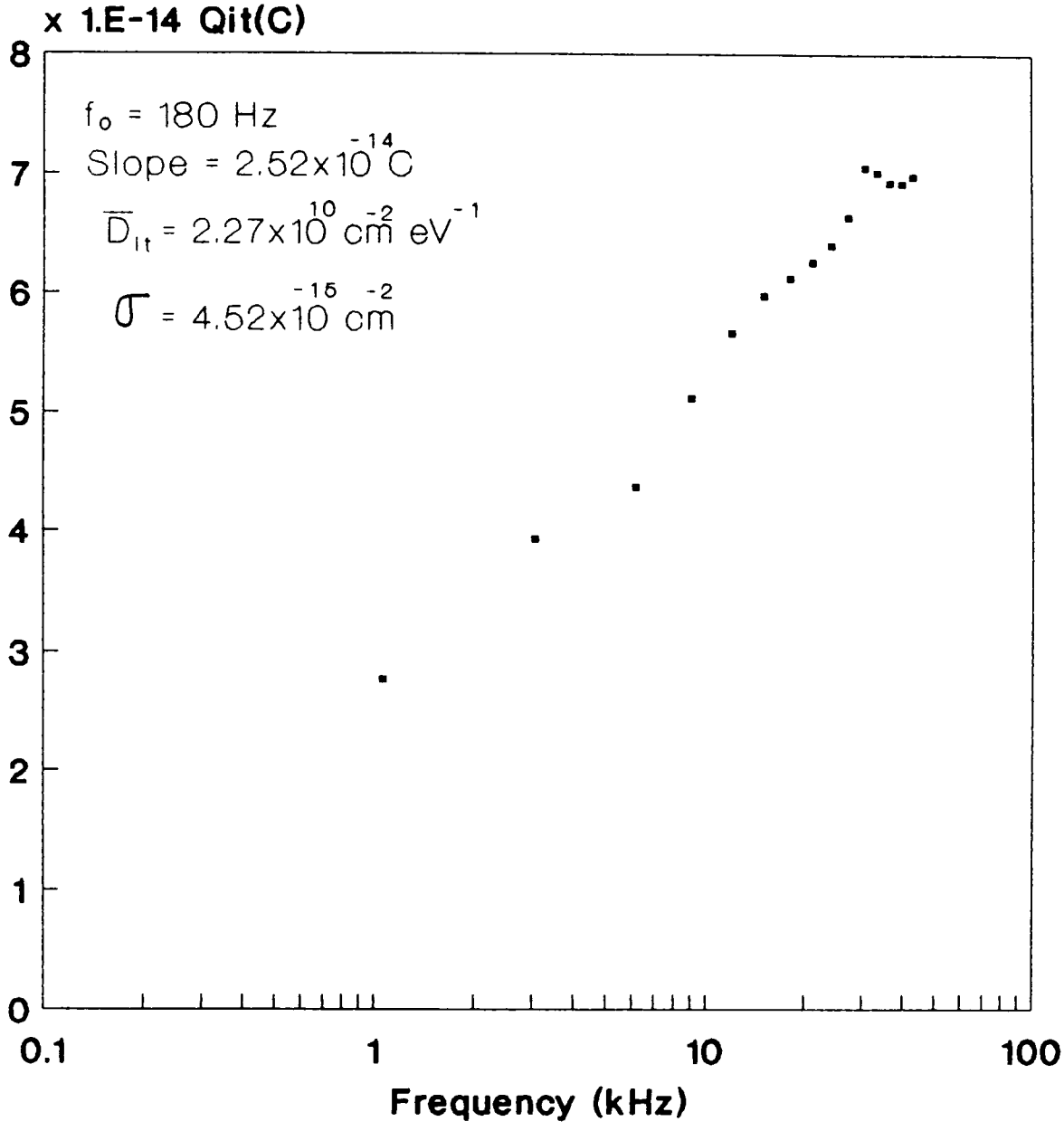


Fig.6.14a Qit versus frequency used to determine the mean capture cross section and the average interface-trap density. Using Groeseneken et al method [12].

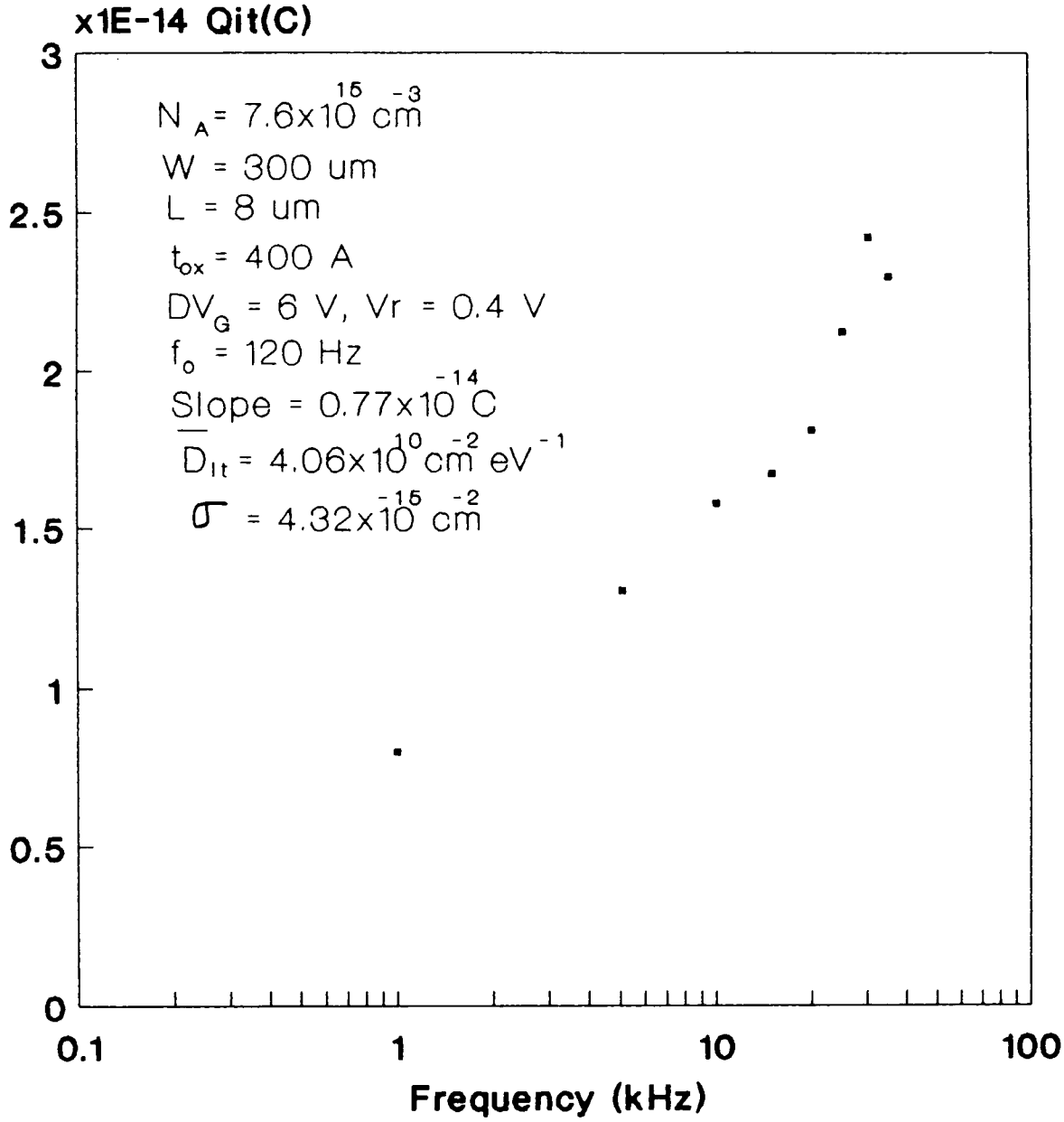


Fig.6.14b Qit versus frequency used to determine the geometrical mean value of the capture cross sections and the average interface-trap density. Using Groeseneken et al method [12].

the flatband and threshold voltages used in the expression (5.13) to determine the mean capture cross section can be obtained using the charge pumping technique [50,53].

6.4.3 Conclusion.

The most attractive features of the charge-pumping technique lie in its quick and simple experimental and analytical procedure. It resolves interface traps density with fairly good accuracy in sizable portions of the upper and lower halves of bandgap and also provides an extrapolated estimate for the mean capture cross-section [12]. However, this technique has several limitations. Its inability to probe midgap and uncertainty in the determination of the capture cross-section measurement are the two major drawbacks.

6.5 AN ALTERNATIVE EXPERIMENTAL APPROACH

The charging and discharging of the interface traps at the Si-SiO_2 interface of a MOS structure can occur under two regimes. The first regime is of steady state recombination which applies when the surface region enters either into deep accumulation or into deep inversion. The second regime is of non-steady-state emission which applies when the surface region is under depletion condition. In the theory of charge pumping current, charging and discharging of the interface traps under the first regime only is supposed to

contribute certain net current, which is identified as charge pumping current, whereas the second the regime is supposed to contribute a net zero current as discussed earlier in section 5.5. Referring Fig.5.2, the direction of the currents corresponding to the energy regions II and VII of non-steady-state emission has been considered positive that is flowing from the substrate to the ground. These currents are considered to be nullified by their counterparts during the sweep of the energy regions IX and IV.

This assumption forms an important basis of the charge pumping technique and needs verification. In order to verify the validity of this assumption we measured the gate current during the measurement of the charge pumping current using Elliot method. A significant amount of gate current is observed at least at certain specific frequencies. A comparison of the magnitude of the gate and substrate currents during the measurement of the charge pumping current by Elliot method is shown in Fig.6.15. This gate current has been completely ignored in all the charge pumping techniques whereas Fig.6.15 shows that it is quite important at least at certain frequencies. Existence of this gate current forms another important limitation and uncertainty of the charge pumping technique apart from others as discussed earlier.

To further confirm the existence of this gate current, we carried out the Elliot version of the experiment with open drain and source because this will eliminate the occurrence

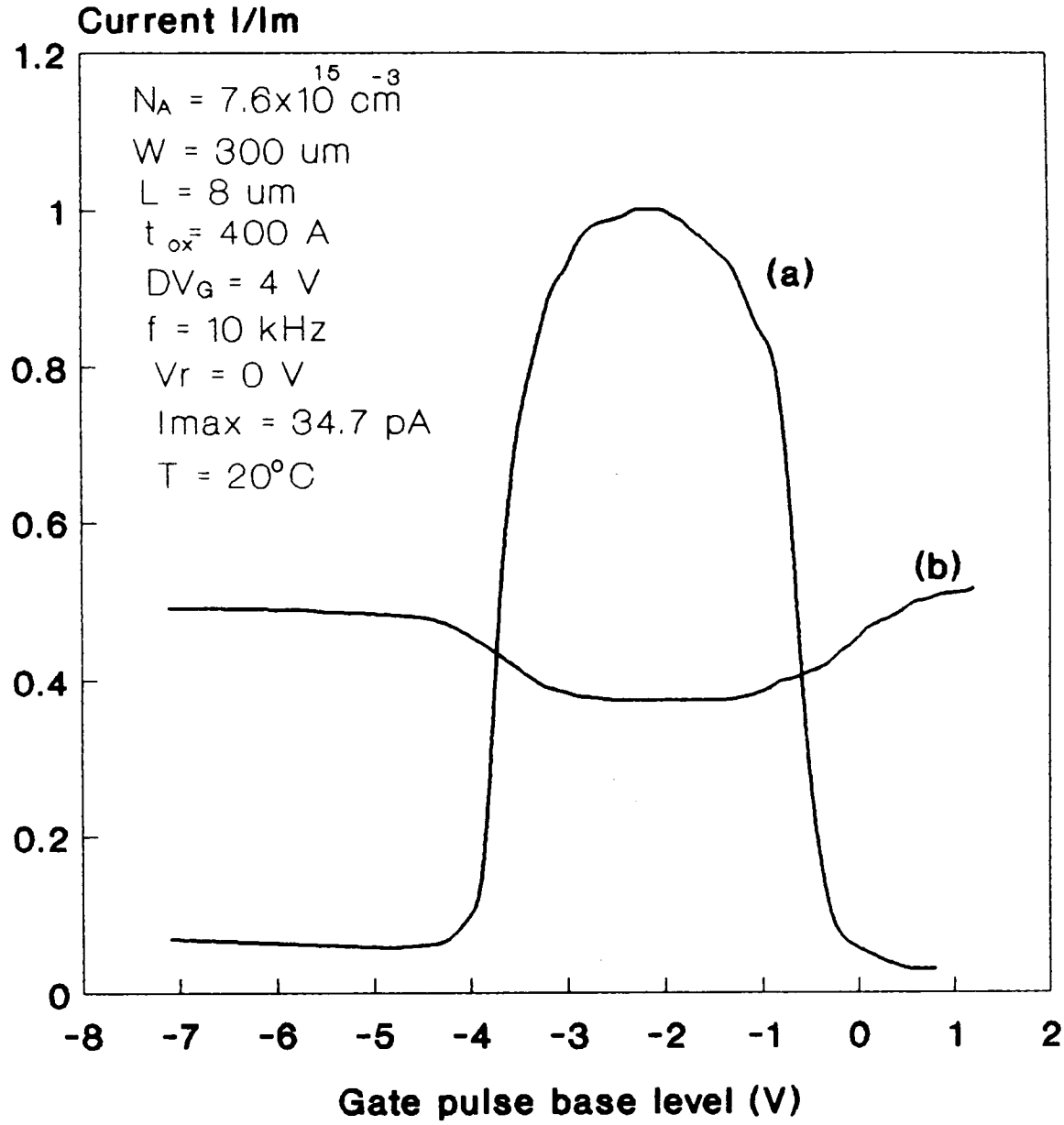


Fig.6.15 Comparaison of substrate current (a) and gate current (b) during measurement of charge pumping current using Elliot method.

of drain/source to substrate current altogether. An appreciable gate current was noticed even under this condition which is shown in Figs.6.16a,b. In order to remove any doubt if this current has origin from any leakage through the oxide, we measured the same current by applying a dc gate voltage equal to the rms value of the previous gate voltage signal. The current value is drastically reduced under this dc gate voltage which accounts only for a maximum of 5% of the gate current observed under an oscillating gate voltage. Yet another confirmation of the observed current was carried out by replacing the MOSFET by a MOS capacitor and it yielded the similar results which are given in Fig.6.17. This last experiment has left no chance of the existence of the usual charge pumping current for which charge is pumped from the drain/source and the observed current must be attributed to some other origin.

The observation of this gate current even in the absence of drain/source prompted us to use an alternative experimental approach to study the interface trap charges in which the device may be operated only in one regime in order to remove the uncertainty introduced due to the entry of the surface region of the device into two regimes. Obviously the regime of non-steady-state emission is a better choice because it can be easily isolated from the regime of steady state recombination by not allowing the gate voltage to exceed the depletion limits. This left us with a more or

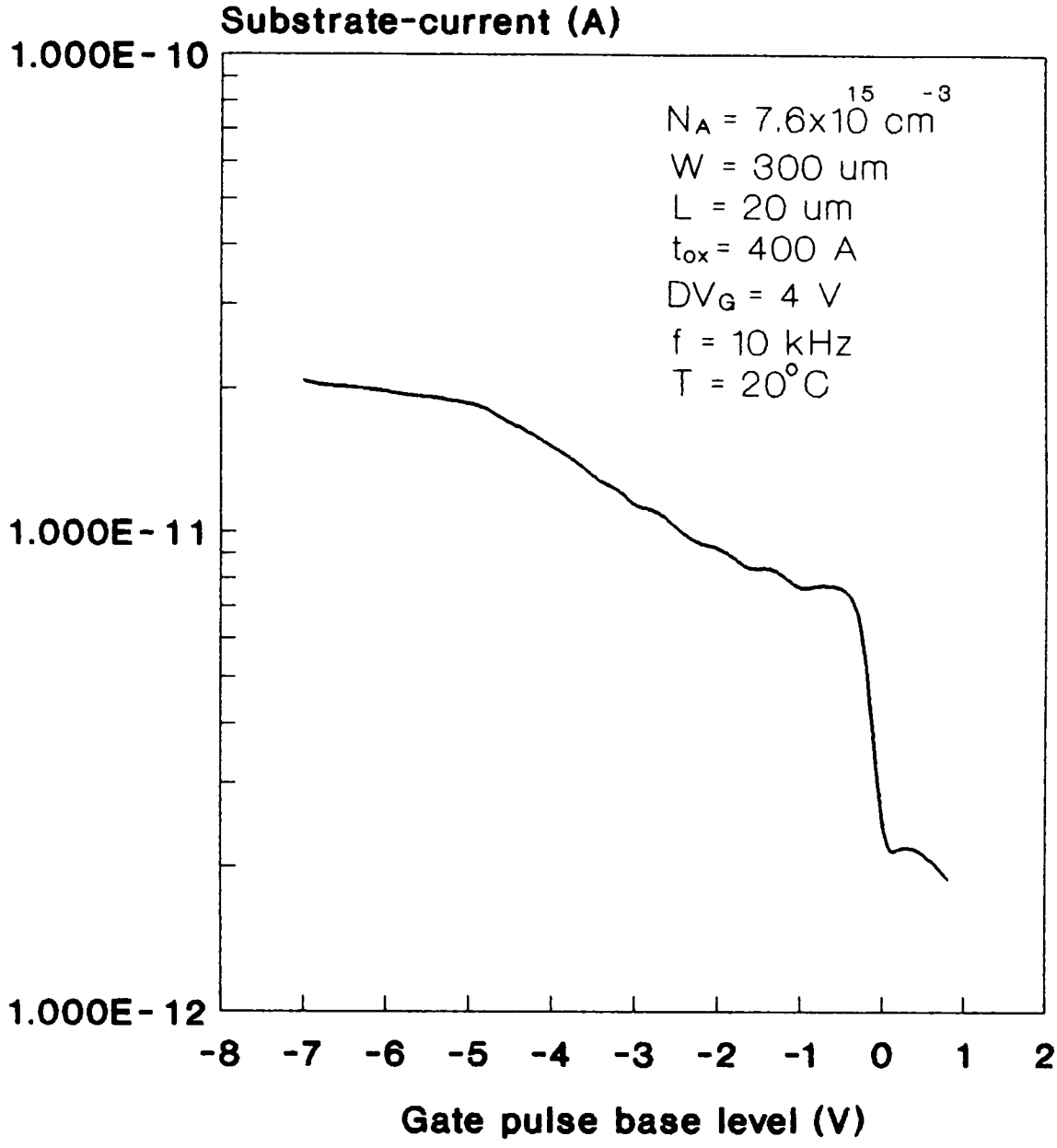


Fig.6.16a Substrate current as a function of base level of the gate voltage pulse using Elliot method for MOSFET with drain/source open (logarithmic scale).

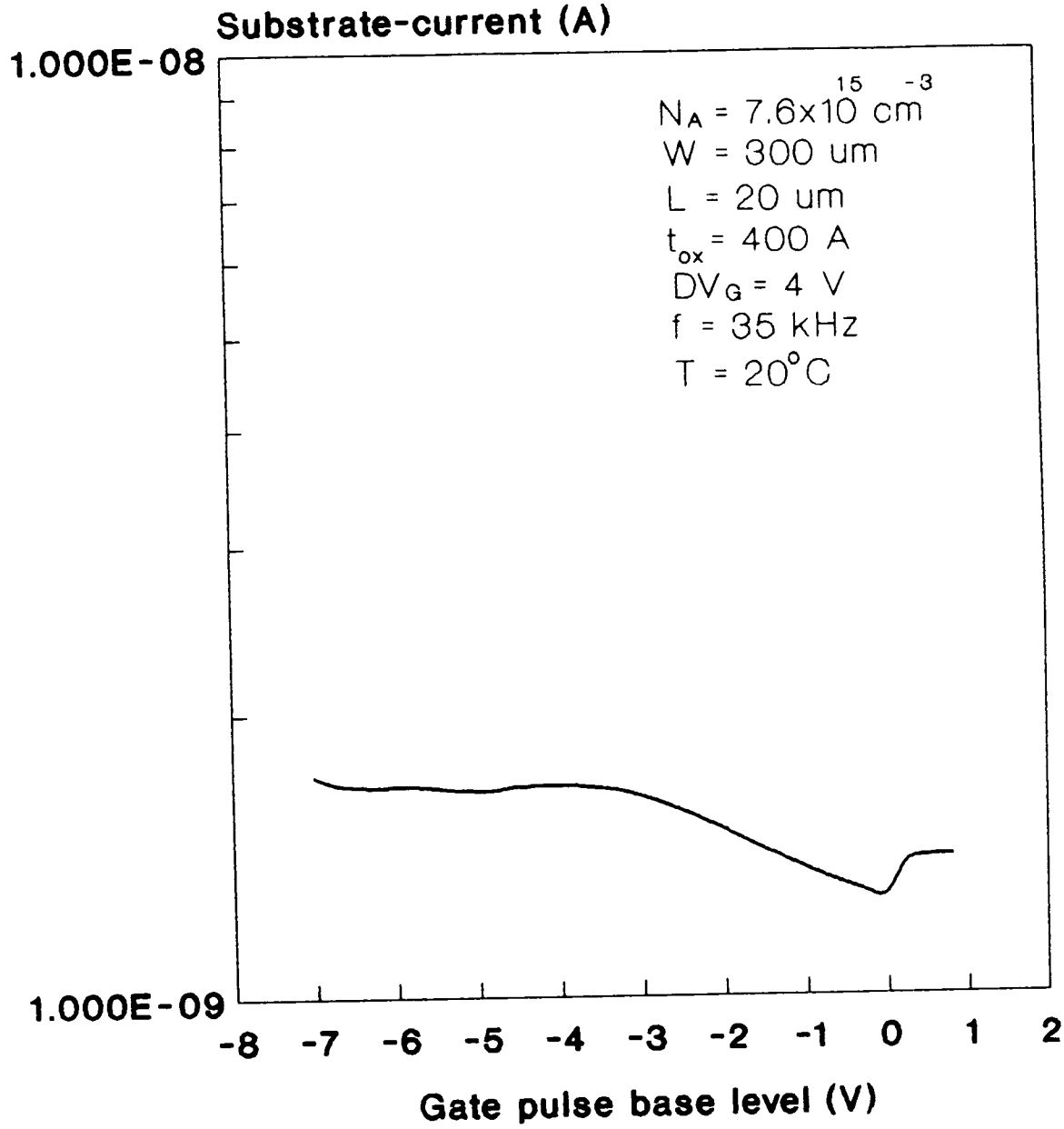


Fig.6.16b Substrate current as a function of base level of the gate voltage pulse using Elliot method with drain/ open (logarithmic scale).

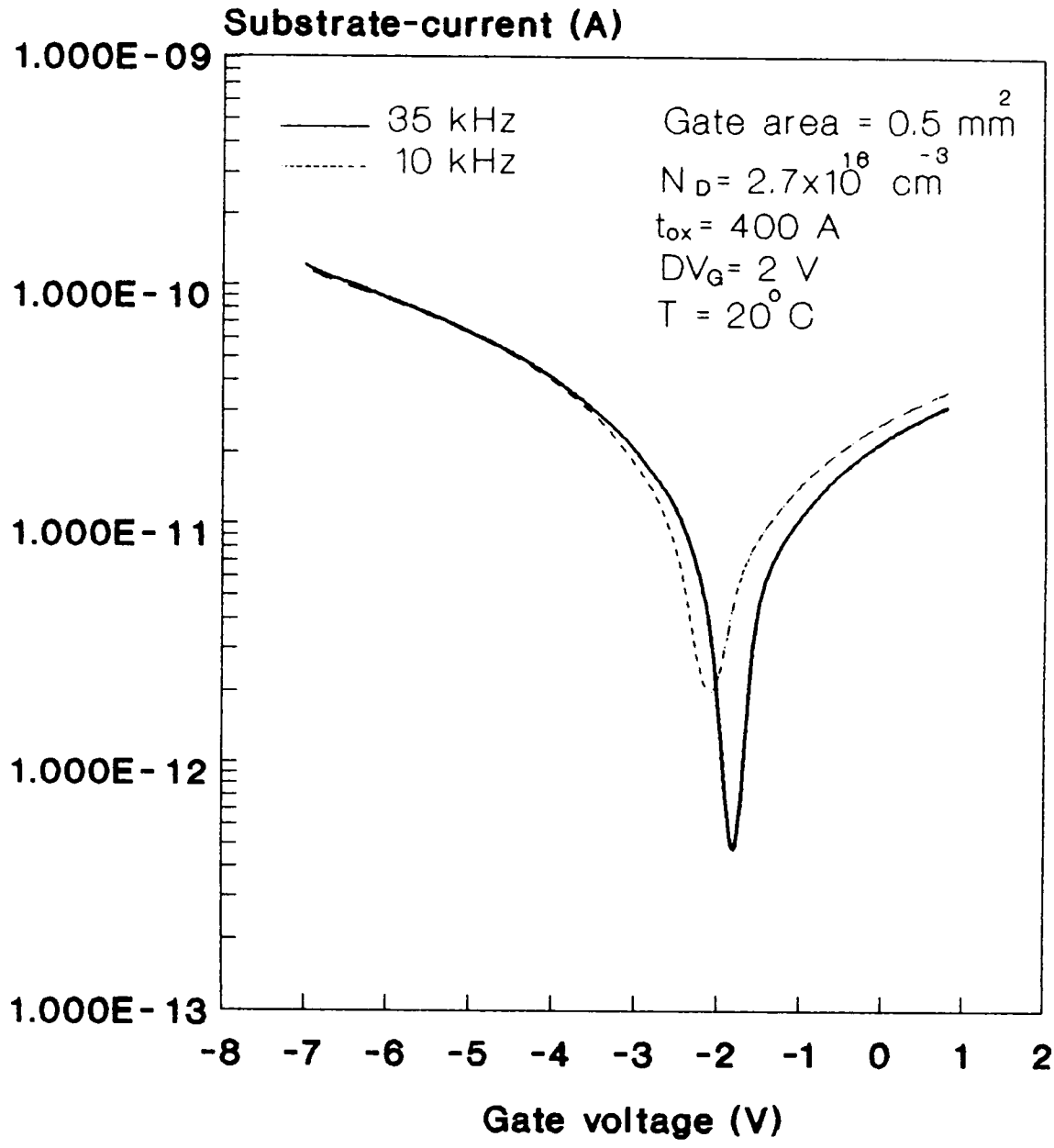


Fig.6.17 Substrate current as a function of base level of the gate voltage pulse using Elliot method for MOS diode.

less concrete choice for an alternative experimental approach in which an oscillating gate voltage signal of such an amplitude is to be applied to a MOSFET (with open drain/source) or MOS capacitor whose amplitude does not exceed depletion limits. The electrical circuit of the new experiment is shown in Fig.6.18a whereas the actual experimental setup is shown in the form of block diagram in Fig.6.18b. The gate current was measured at a fixed frequency by varying the gate voltage in such a way that it does not exceed V_{FB} on one extreme and V_T on the other. It leads to three experimental versions. In the first version the voltage is allowed to vary from a level V_o (corresponding to intrinsic level) to V_{FB}, in the second version from V_o to V_T and in the third version from V_{FB} to V_T. The measured current versus gate voltage curves are shown in Fig.6.19. It may be noted that even with such a limited gate voltage signal, there is a significant amount of dc gate/substrate current. Henceforth this current will be referred as substrate current in this new experimental approach since there is no drain/source to produce its drain/source to substrate current. Since the generation of this substrate current can not be explained by the theory of usual charge pumping current, in which the current is mainly produced by the steady state recombination of the interface traps with the free carriers of either inversion or accumulation layer, it necessitates a new theory to be worked out

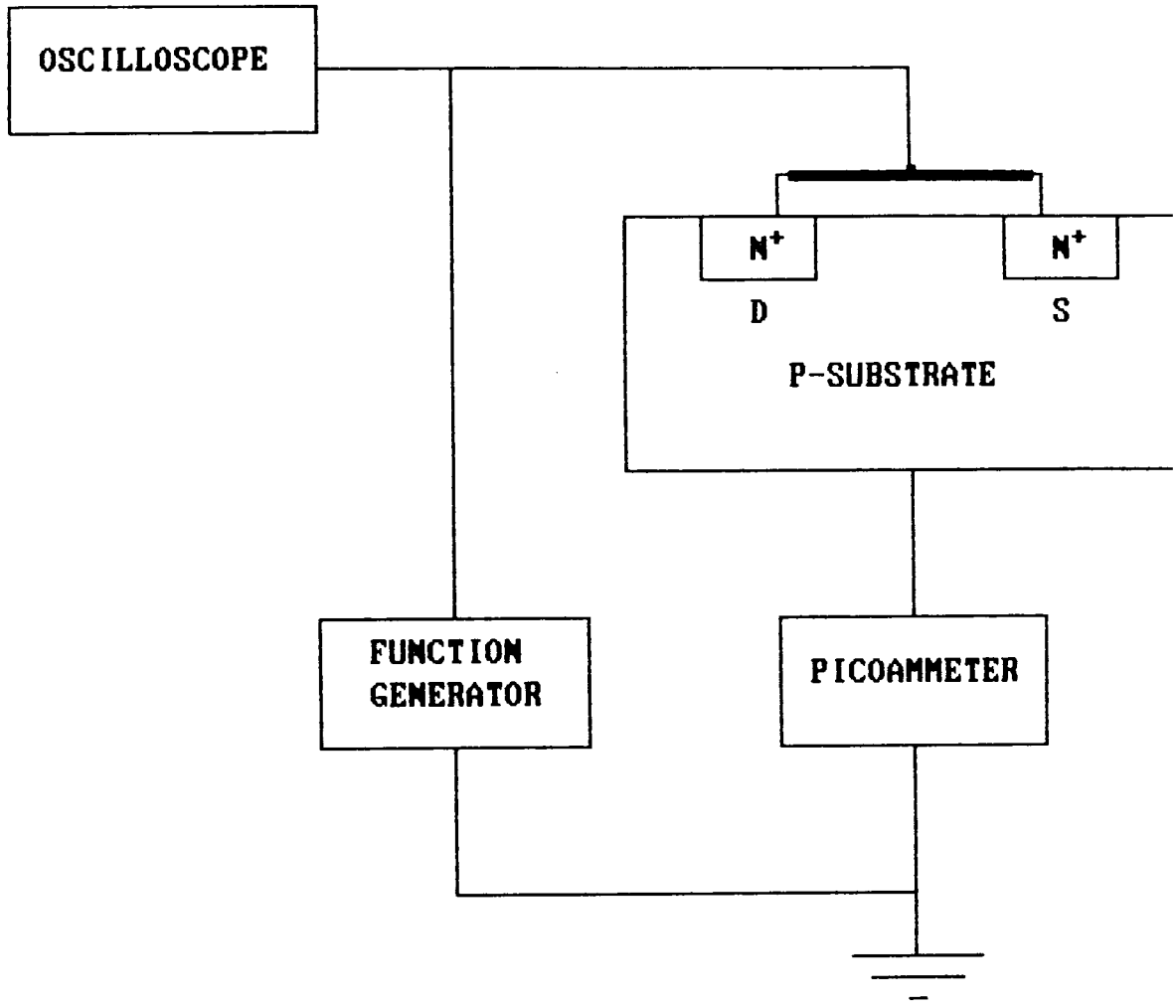


Fig.6.18a General setup illustrating the principle of th
new technique.

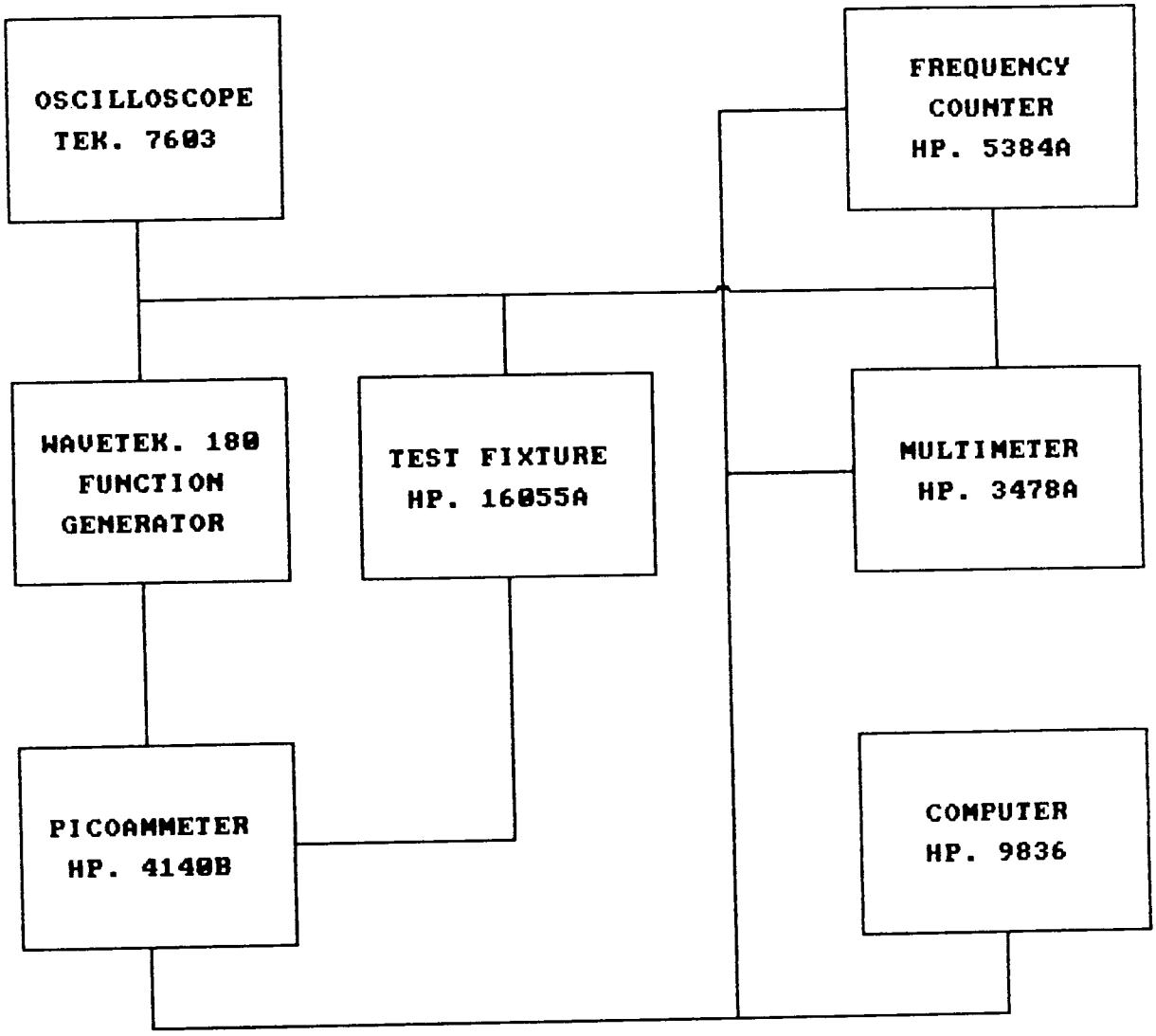


Fig.6.18b Experimental setup used in the present study.

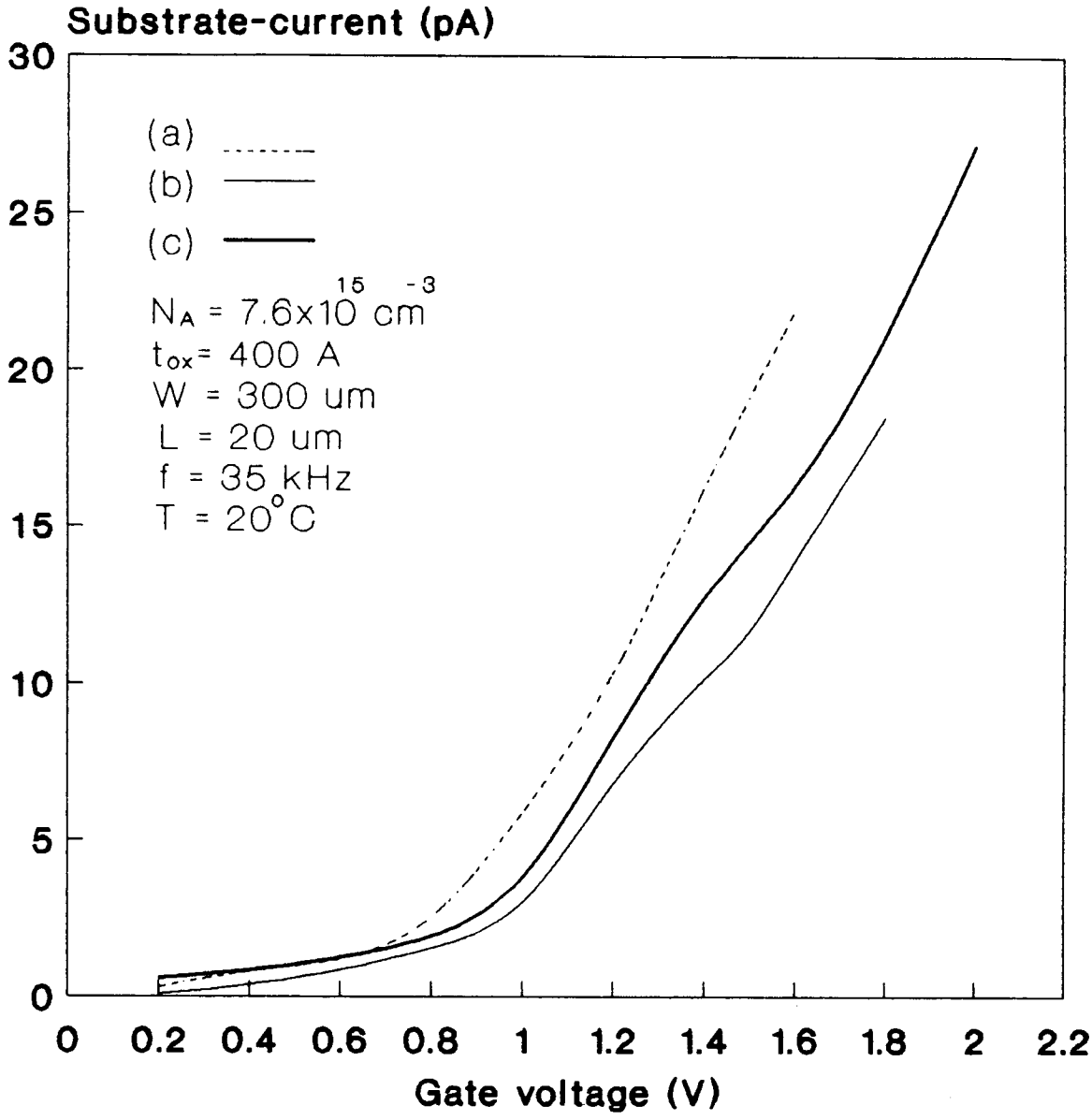


Fig.6.19 Experimental Isub-V curves for MOSFET for different potential sweeps (a) Ei to E_s (b) Ei to E_T (c) E_s to E_T.

before it could be utilized for studying the interface trap charges and other related aspects. Further, it may be pointed out here that this new dc substrate current in the absence of drain/source can not maintain its flow unless the charge needed to fill the empty interface traps is extracted from the gate through the oxide. Therefore it will not be inappropriate if this new current is called charge extraction current. The theory and the results of this charge extraction current are presented in details in chapter 7.

CHAPTER 7

CHARGE-EXTRACTION TECHNIQUE FOR STUDYING THE INTERFACE TRAPS IN MOS DEVICES

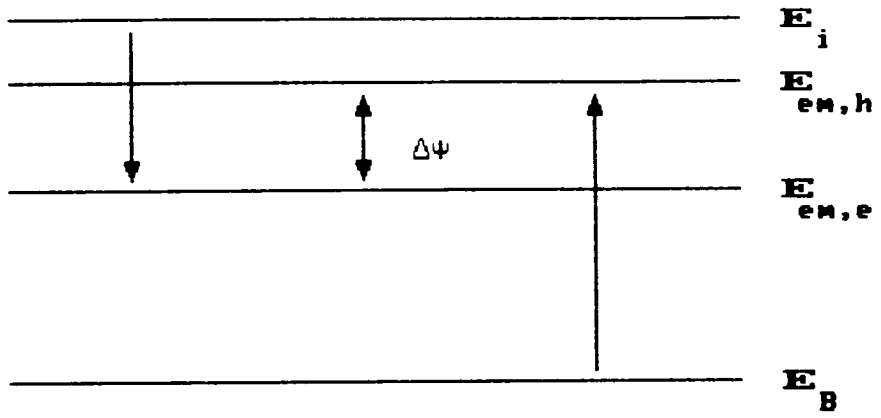
7.1 INTRODUCTION

In the present chapter, a new method for studying the surface-sates is developed which utilizes the measurement of the dc substrate- current in a MOS device but when it is operated under an ac gate-voltage signal within the depletion limits. This method provides an alternative approach to the charge-pumping technique for studying the surface-states in a MOSFET and at the same time removes its limitations. This new approach, which may be better called charge-extraction technique, can be equally applied to MOS diodes without imposing any constraint on the device-geometry.

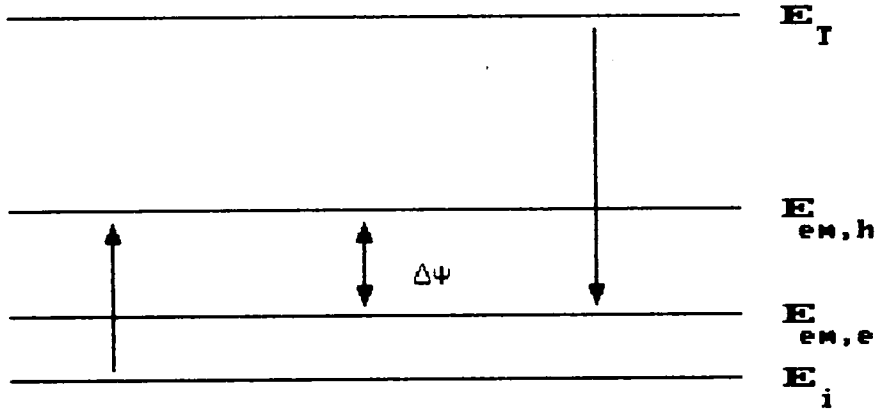
7.2 THEORETICAL MODEL

Referring to Fig.5.2, the present model applies to any MOS structure in which the surface-potential does not exceed the limit E_B on one side and E_T on the other during the gate-voltage swing. Accordingly, the gate-voltage V_G remains always below the threshold voltage V_T and above the flat-band voltage V_{FB}. During such a gate-voltage variation, since the surface-region of the device always remains under the depletion condition, any charging or discharging of the surface-states will be due to non-steady-state emission only and not due to steady-state recombination.

In order to realize the practical feasibility of the non-steady-state emission such that no effect of the steady-state recombination is introduced, it is convenient to use the surface-potential sweep only on one side of the intrinsic level E_i, that is, either from E_i to E_B or from E_i to E_T as shown in Figs.7.1a,b. It will be seen in the following discussions that, by doing so, the current-measurement becomes less susceptible to any effect of the steady-state recombination even if the surface-region enters into accumulation (Fig.7.1a) or inversion (Fig.7.1b). Therefore this practice will allow, without introducing any significant error, the use of the full surface-potential intervals $(E_i - E_B)$ or $(E_T - E_i)$ each of which has the value given by:



(a)



(b)

Fig.7.1 Surface-potential regions of non-steady-state electron and hole-emission, (a) surface-potential sweep from E_B to E_i (b) surface-potential sweep from E_i to E_T.

$$E_i - E_B = E_T - E_i = kT \ln \frac{N_A}{n_i} \quad , \qquad (7.1)$$

where N_A is the doping concentration in the substrate, n_i the intrinsic concentration, k the Boltzmann constant, and T the absolute temperature. It may be pointed out that the use of any other value of surface-potential interval would involve an additional task of finding its accurate value.

Any maintenance of the substrate-current in the MOS device due to charging and discharging of the surface-states is possible only if during the surface-potential sweeps (from E_i to E_B or E_i to E_T) the charging and discharging surface-potential regions overlap partly or wholly. For example in Fig.7.1a, the hole-emission or filling of surface-states occurs from the energy-level E_B to $E_{em,h}$ during one-half of the gate-voltage pulse. The emptying of the surface-states takes place from E_i to $E_{em,e}$ during the second half of the pulse. The surface-potential region from $E_{em,h}$ to $E_{em,e}$ is overlapped during the emptying and filling processes of the surface-states. It is the surface-states of this surface-potential region ($E_{em,h}$ to $E_{em,e}$) which can produce and maintain a net substrate-current provided the emptying and filling processes produce electric currents in the same direction. The emission of holes, that is, filling of the surface-states while going from E_B to E_i (Fig.7.1a) is a normal process and is acceptable. However, the reverse

process that is the absorption of holes from E_i to E_B amounts to the emission of electrons and is not normally expected because the electron-emitting states normally do not exist in a region below the intrinsic level. However, the experimental results of the present study show the presence of a net negative dc substrate-current (in p-substrate) even in the case of MOS diodes which are operated within the depletion limits, that is, either between E_i and E_B or E_i and E_T. This is possible only when the charging (hole-emission) and discharging (electron-emission) of the surface-states is sustained and when the emitted electrons travel from the gate to the Si-SiO_2 interface through the oxide. For the remaining surface-potential regions, that is, from E_B to $E_{em,e}$ and E_i to $E_{em,h}$ (Fig.7.1a), the emission is not sustained and they remain filled permanently with electrons and holes respectively during the time when emission between $E_{em,h}$ and $E_{em,e}$ is going on. However, the above state of affairs is changed as soon as the surface-potential goes below E_B so that the surface-region is flooded with holes due to accumulation condition. Under this accumulation condition, the surface-potential region between E_B and $E_{em,e}$ starts producing normal emission and absorption of holes to and from the substrate respectively contributing nothing to the net substrate-current.

Similar arguments apply to the surface-potential sweep between E_i and E_T as shown in Fig.7.1b. Electron-emission

$$E_m(t) - E_1 = -kT\,ln\left[1 - \left(1 - \exp\frac{E_1 - E_m(0)}{kT}\right).\right.$$

$$\left.\exp\left(-\upsilon\sigma N_c t.\exp\frac{E_1 - E_g}{kT}\right)\right] \quad ,(7.2)$$

where

$E_m(t)$: emission-level upto which surface-states are emptied at time t.

$E_m(0)$: emission level at t = 0.

E_1 : energy of the lowest surface-trap as measured from the top of valence band.

E_g : band-gap energy.

t : time for which emission has taken place from $E_m(0)$ to $E_m(t)$.

N_c : density of states in conduction band.

σ : cross-section for a given type of carrier.

υ : thermal velocity of carriers at $T°$ Kelvin.

k : Boltzmann constant.

In fact Eq.(7.2) in its present form applies to the case of electron-emission. For the hole-emission, the negative sign on the right-hand side of Eq.(7.2) is to be omitted. As applied to the present case, say, for the hole-emission (Fig.7.1a) which commences at $E_m(0) = E_B$ and can continue upto an extreme level $E_1 = E_t$, a few more terms of Eq.(7.2) become simplified. For example, it can be easily proved that

$$N_c \exp\frac{E_1 - E_g}{kT} = N_c \exp\frac{E_i - E_g}{kT} = n_i \quad , \qquad (7.3)$$

where n_i is the intrinsic concentration. Similarly, for the electron-emission which commences at $E_m(0) = E_i$ and can continue upto an extreme level $E_1 = E_B$, the following relation can be obtained :

$$N_c \exp\frac{E_1 - E_g}{kT} = N_c \exp\frac{E_B - E_g}{kT} = n_i \exp\frac{-\Psi_B}{kT} = \frac{n_i^2}{N_A} \quad , \qquad (7.4)$$

where

$$\Psi_B = E_B - E_i = kT \ln\frac{N_A}{n_i} \quad , \qquad (7.5)$$

N_A is the doping concentration of the substrate and Ψ_s the surface-potential difference between intrinsic and flat-band conditions. After Taylor's series-expansion of the time-dependent exponential term under first order approximation, Eq.(7.2) takes the following form in the present case of the electron and hole-emission respectively:

$$E_{em,e}(t) - E_B = -kT \ln\left[\frac{v\sigma_e n_i^2}{N_A} t_{em,e} + \exp\frac{E_B - E_i}{kT}\right], \qquad (7.6)$$

and

$$E_{em,h}(t) - E_i = kT \ln\left[v\sigma_h n_i t_{em,h} + \exp\frac{E_B - Ei}{kT}\right]. \qquad (7.7)$$

As already pointed out, under an oscillating voltage-pulse of frequency f at the gate in which the voltage sweeps a surface-potential Ψ_s, in general all the surface-states within Ψ_s will not undergo emission. The charging and discharging of the surface-states will occur only upto an intermediate level $E_{em}(t)$ as given by Eqs.(7.6) and (7.7) where t is the time that the voltage pulse spends in sweeping the surface-potential Ψ_s. This time t for one-side sweep will obviously be related to the frequency f by

$$t = \frac{1}{2f} \quad . \tag{7.8}$$

The actual sweep of the surface-potential within which the surface-states undergo electron-emission can be written as

$$\Psi_B - [E_{em,e}(t) - E_B] = \Psi_B - kT \left| \ln\left(\frac{v\sigma_e n_i^2}{2fN_A} + \exp\frac{-\Psi_B}{kT} \right) \right| , \tag{7.9}$$

or under first order approximation simply as

$$\Psi_B - [E_{em,e}(t) - E_B] = \Psi_B - kT \left| \ln\left(\frac{v\sigma_e n_i^2}{2fN_A} \right) \right| \quad . \tag{7.10}$$

Similarly for the hole-emission

$$\Psi_B - [E_i - E_{em,h}(t)] = \Psi_B - kT \left| \ln\left(\frac{v\sigma_h n_i}{2f}\right) \right| \quad . (7.11)$$

In fact, during charging and discharging of the surface-states due to emission of electrons and holes in the forward and reverse potential sweeps, it is the common surface-potential region $\Delta\Psi$ which is responsible for generating and maintaining an electric current. This common surface-potential region $\Delta\Psi$ for the case of gate-voltage swinging between E_1 and E_B (Fig.7.1a) can be written as

$$\Delta\Psi = \Psi_B - kT \left| \ln\left(\frac{v\sigma_e n_i^2}{2fN_A}\right) \right| - kT \left| \ln\left(\frac{v\sigma_h n_i}{2f}\right) \right| . (7.12)$$

Under the assumption of uniform density-distribution of the surface-states, the current I_{ce} resulting from the charging and discharging of the surface-states within the surface-potential region $\Delta\Psi$ may be written as

$$I_{ce} = 2qAfD_{it}\Delta\Psi = 2qAfD_{it}[\Psi_B - kT \left| \ln\left(\frac{v\sigma_e n_i^2}{2fN_A}\right) \right| - kT \left| \ln\left(\frac{v\sigma_h n_i}{2f}\right) \right|]. \quad (7.13)$$

As the net charge for this current is extracted in the form

of electrons from the gate, this current may be more appropriately called charge-extraction current I_{ce} in order to distinguish it from the charge-pumping current. The factor of 2 on the right-hand side of Eq.(7.13) accounts for the fact that both the processes of discharging and charging of surface-states give rise to equal currents, that is, one due to electrons coming out from the surface-states and other due to holes from the surface-states. Further, the distribution of the surface-states are supposed to exhibit some variation and therefore the above assumption of the uniform density of the surface-states would mean the average density $\overline{D_{it}}$. Equation (7.13) can therefore be rewritten in the following form :

$$I_{ce} = 2qAf\overline{D_{it}}\left[\Psi_B - 2kT\left|\ln\left(\frac{v\sqrt{\sigma_e\sigma_h}n_i^2}{2f\sqrt{n_i N_A}}\right)\right|\right] \quad .(7.14)$$

It may be noted that Eq.(7.14) does not require individual value of the capture cross-sections σ_e and σ_h but an average value $\sqrt{\sigma_e\sigma_h}$.

An inspection of Eq.(7.14) reveals that the variation of the charge-extraction current I_{ce} with the frequency f should give rise to a maximum at a certain optimum frequency f_m given by

$$f_m = \frac{v\sqrt{\sigma_e \sigma_h}\, n_i^2}{2\sqrt{n_i N_A}} \exp\left(\frac{\Psi_B}{2kT} - 1\right) \quad . \qquad (7.15)$$

Replacing back N_A in terms of Ψ_s with the help of Eq.(7.4), Eq.(7.15) takes the form

$$f_m = \frac{v\sqrt{\sigma_e \sigma_h}\, n_i}{2} e^{-1} \quad . \qquad (7.16)$$

As already discussed, the above theoretical model holds good equally well for both the cases of surface-potential sweeps from E_i to E_B and from E_i to E_T. Therefore Eqs.(7.14) and (7.16) can be applied as such to both the cases. Whereas Eq.(7.14) gives the average density $\overline{D_{it}}$ of the surface-states, Eq.(7.16) gives the frequency f_m of the maximum substrate-current in the two cases. Further in both the cases, the gate voltage can safely cross the depletion limit, that is, V_{FB} in Fig.7.1a and V_T in Fig.7.1b without introducing any error in the value of I_{cp} and f_m.

In the case of gate-voltage pulse sweeping the surface-potential from E_B to E_T the energy-region $\Delta\Psi_1$ below E_i and energy-region $\Delta\Psi_2$ above E_i, which are responsible for producing the current I_{cp}, can be evaluated separately. For the energy-region $\Delta\Psi_1$, the normal emission of holes commences at E_B and can go upto an extreme level E_T (Fig.7.2)

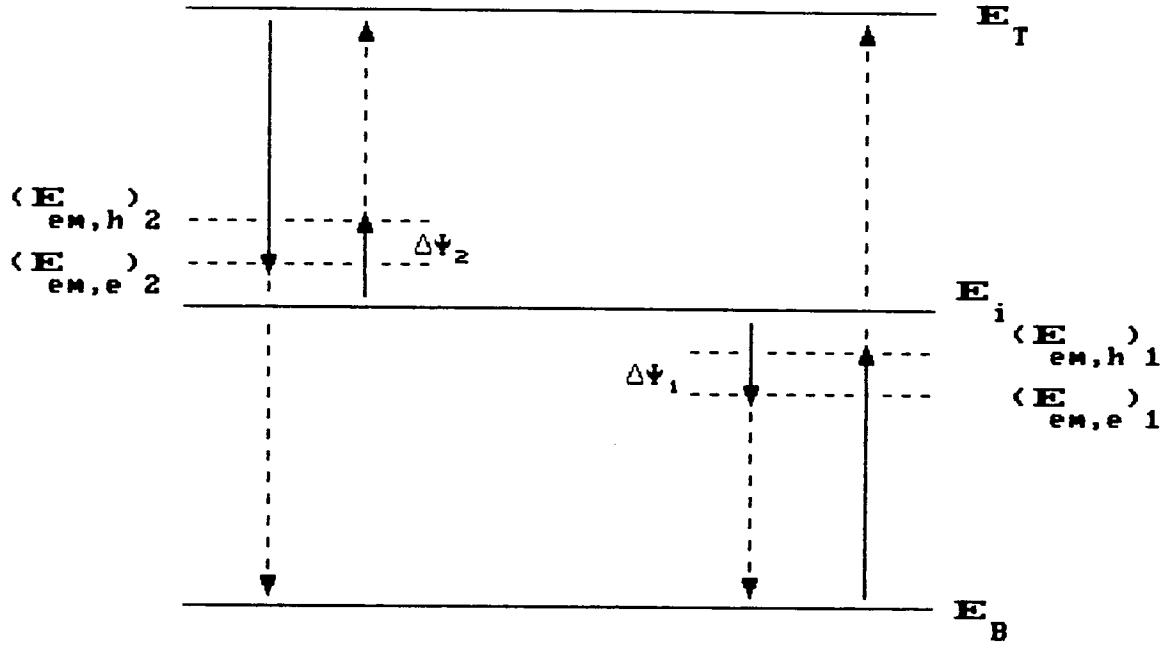


Fig.7.2 Energy-regions of non-steady-state emission for surface-potential sweep from E_B to E_T.

whereas the oxide-aided electron-emission commences at E_1 and can go upto an extreme level E_B. Referring to Fig.7.2, $\Delta\Psi_1$ can be written as

$$\Delta\Psi_1 = (E_{em,h})_1 - (E_{em,e})_1 = \left[2\Psi_B - kT \left| \ln\left(\frac{v\sigma_h' n_i^2}{2fN_A}\right) \right| \right] - kT \left| \ln\left(\frac{v\sigma_e n_i^2}{2fN_A}\right) \right| , \quad (7.17)$$

or

$$\Delta\Psi_1 = 2\left[\Psi_B - kT \left| \ln\left(\frac{v\sqrt{\sigma_e\sigma_h'} n_i^2}{2fN_A}\right) \right| \right] , \quad (7.18)$$

where σ_h' is the new hole capture cross-section for the case when the extreme hole-emission level lies at E_T. Similarly for the energy-region $\Delta\Psi_2$, the normal emission of electrons commences at E_T and can go upto an extreme level E_B whereas the oxide-aided hole-emission commences at E_1 and can go upto an extreme level E_T. Referring to Fig.7.2, $\Delta\Psi_2$ can be written as

$$\Delta\Psi_2 = (E_{em,e})_2 - (E_{em,h})_2 = \left[2\Psi_B - kT \left| \ln\left(\frac{v\sigma_e' n_i^2}{2fN_A} \right) \right| \right] - \left[kT \left| \ln\left(\frac{v\sigma_h n_i^2}{2fN_A} \right) \right| \right] \quad ,(7.19)$$

or

$$\Delta\Psi_2 = 2\left[\Psi_B - kT \left| \ln\left(\frac{v\sqrt{\sigma_e'\sigma_h} n_i^2}{2fN_A} \right) \right| \right] \quad , \qquad (7.20)$$

where σ_e' is the new electron capture cross-section for the case when the extreme electron-emission level lies at E_B. The total energy-region $\Delta\Psi$ producing current I_{ce} will be

$$\Delta\Psi = \Delta\Psi_1 + \Delta\Psi_2 = 4\left[\Psi_B - kT \left| \ln\left(\frac{v\sqrt{\bar{\sigma}_e\bar{\sigma}_h} n_i^2}{2fN_A} \right) \right| \right] \quad ,(7.21)$$

where $\bar{\sigma}_e = \sqrt{\sigma_e\sigma_e'}$ and $\bar{\sigma}_h = \sqrt{\sigma_h\sigma_h'}$. Therefore the current I_{ce}^* for this case can be written as

$$I_{ce}^* = 8qAf\overline{D_{it}}\left[\Psi_B - kT \left| \ln\left(\frac{v\sqrt{\bar{\sigma}_e\bar{\sigma}_h} n_i^2}{2fN_A} \right) \right| \right] . (7.22)$$

The corresponding relation for the optimum frequency f_m again comes out to be the same as Eq.(7.16) except for the difference that σ_e is replaced by $\bar{\sigma}_e$ and σ_h by $\bar{\sigma}_h$. However,

in this case, a certain error is likely to be introduced in the value of I^{*}_{ce}, as obtained with the help of Eq.(7.22), if either of the surface-potential limits E_T or E_B is exceeded. It is because the surface-region is flooded with electrons in the case of inversion and these electrons will also contribute to the observed current by filling-up the vacant states in the energy-region from $(E_{em,h})_1$ to E_i as shown in Fig.7.2. As this is an extra current, not covered by Eq.(7.22), it is expected to introduce error. This extra current will give higher value of charge extraction current and hence that of the density of interface traps than what is expected from theory. Similar arguments will apply to the case when surface-potential sweep exceeds the limit E_B so that deep accumulation prevails in the surface-region and holes are flooded. These holes will also contribute to the observed current by emptying the interface traps from $(E_{em,e})_2$ to E_i and introduce error. Not only the current-value I^{*}_{ce} will change, the optimum frequency f_m at which the maximum current is produced, will also change to some extent due to a change in the value of capture cross-sections from σ_e and σ_h to $\bar{\sigma}_e$ and $\bar{\sigma}_h$ respectively. The experimental results show that the entry of the surface-region into deep inversion or deep accumulation introduces quite significant error in the current I_{ce} and the frequency f_m, indicating thereby, that the oxide-controlled process of carrier-emission is overpowered by the effect of flooded carriers due to

entry of the surface region into either inversion or accumulation in the region from E_i to $(E_{em,e})_1$ and from E_i to $(E_{em,h})_2$. Therefore it is safer to use the surface-potential sweep only on one side of the inversion layer which avoids any chance of error due to the entry of surface-region into deep inversion or deep accumulation.

7.3 EXPERIMENTAL MEASUREMENTS.

The validity of the present theoretical model was verified by carrying out experimental measurements on a number of MOS devices in the form of MOSFETs. Since in the present study, the entry of the surface-region of the MOS device into deep inversion is to be avoided, the presence of drain/source in the device is not necessary and a simple electrical circuit as shown in Fig.6.18a can be used to illustrate the principle of the present charge-extraction technique. The detailed experimental setup is illustrated in the block diagram given in Fig.6.18b. The details of the experimental set up, equipment used and devices are already given in sections (6.2,3,5).

A gate-voltage pulse of amplitude equal to V_{FB} with base level corresponding to E_i was used in the first instance for obtaining the I_{ce}-f curves of Fig.7.3. Thereafter different versions of the experiment were employed by using different surface-potential intervals within the range E_B to E_T for

plotting I_{ce}-f curves. For example surface-potential intervals from E_i to E_T and from E_B to E_T were also used besides the one between E_B and E_i as discussed in the previous section. These curves are shown in Figs.7.4 and 7.5 respectively. As the expression (7.16) for f_m is independent of Ψ_s, nearly, the same value of f_m is anticipated for the surface-potential intervals (E_T - E_i) and (E_T - E_B) also. To remove chances of any error arising from the leakage current due to the dc voltage associated with the applied gate-voltage pulse, each main current-measurement for a given pulse was preceded by a leakage current-measurement using the rms value of the pulse-voltage and a correction was applied accordingly. In no case this correction exceeded 5% ensuring thereby that the main I_{ce} current, as measured in the present experimentation, originates from the charging and discharging of the surface-states.

7.4 RESULTS AND DISCUSSION.

A large number of silicon MOS devices have been used in the form of MOSFETs to verify the validity of the present model. However, I_{ce}-f curves of a few typical devices only are reproduced in Figs.(7.3) to (7.8). All these curves show a well defined peak in the value of I_{ce} at a frequency around 70 Hz as anticipated in the light of Eq.(7.16).

Equation (7.16) of the present model predicts that the value of f_m should be independent of all the parameters of

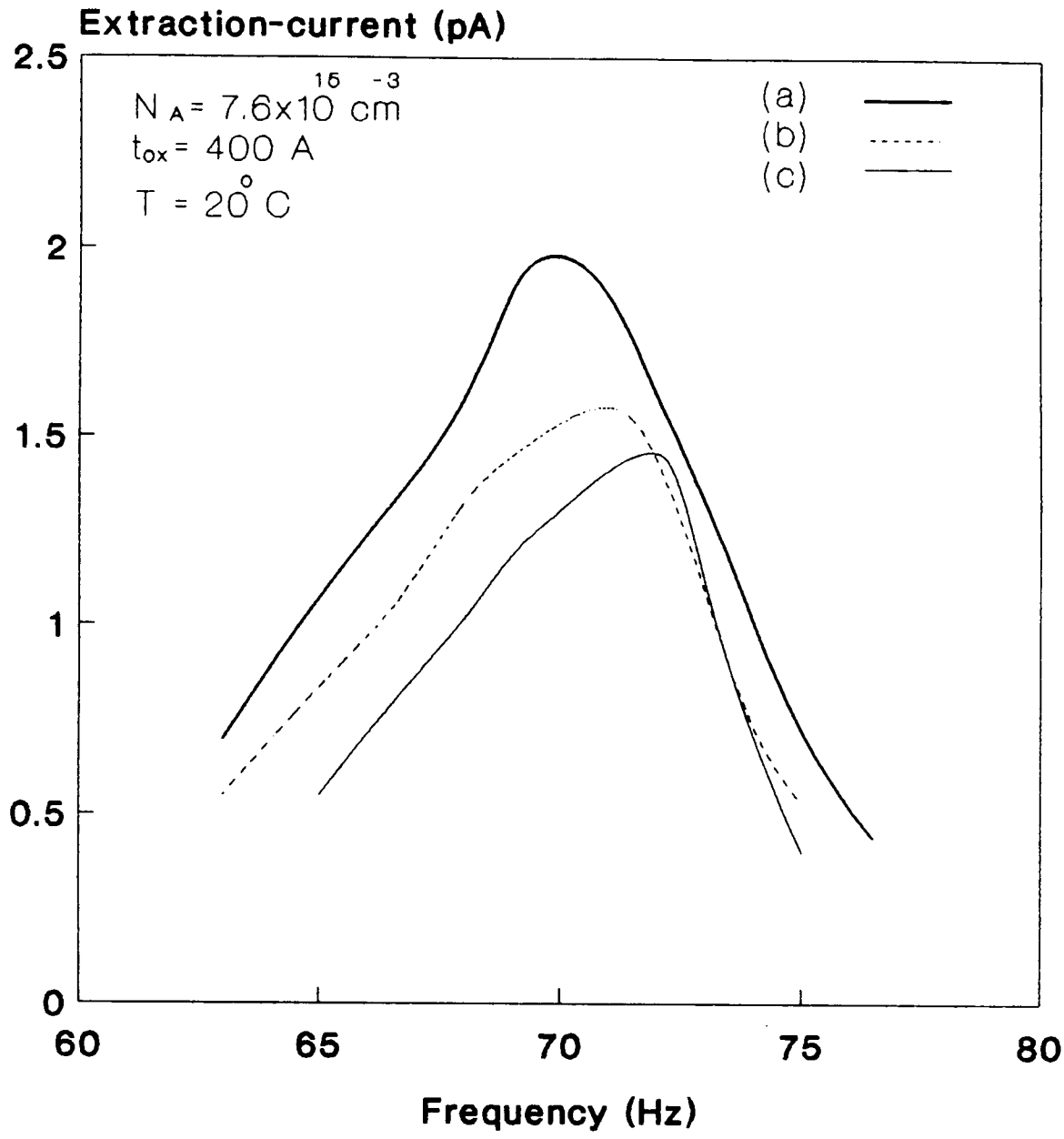


Fig.7.3 Experimental Ice-f curves for the surface-potential sweeps from E_B to Ei for MOS transistors of area, (a) 300x8, (b) 80x20, and (c) 80x8 um^2.

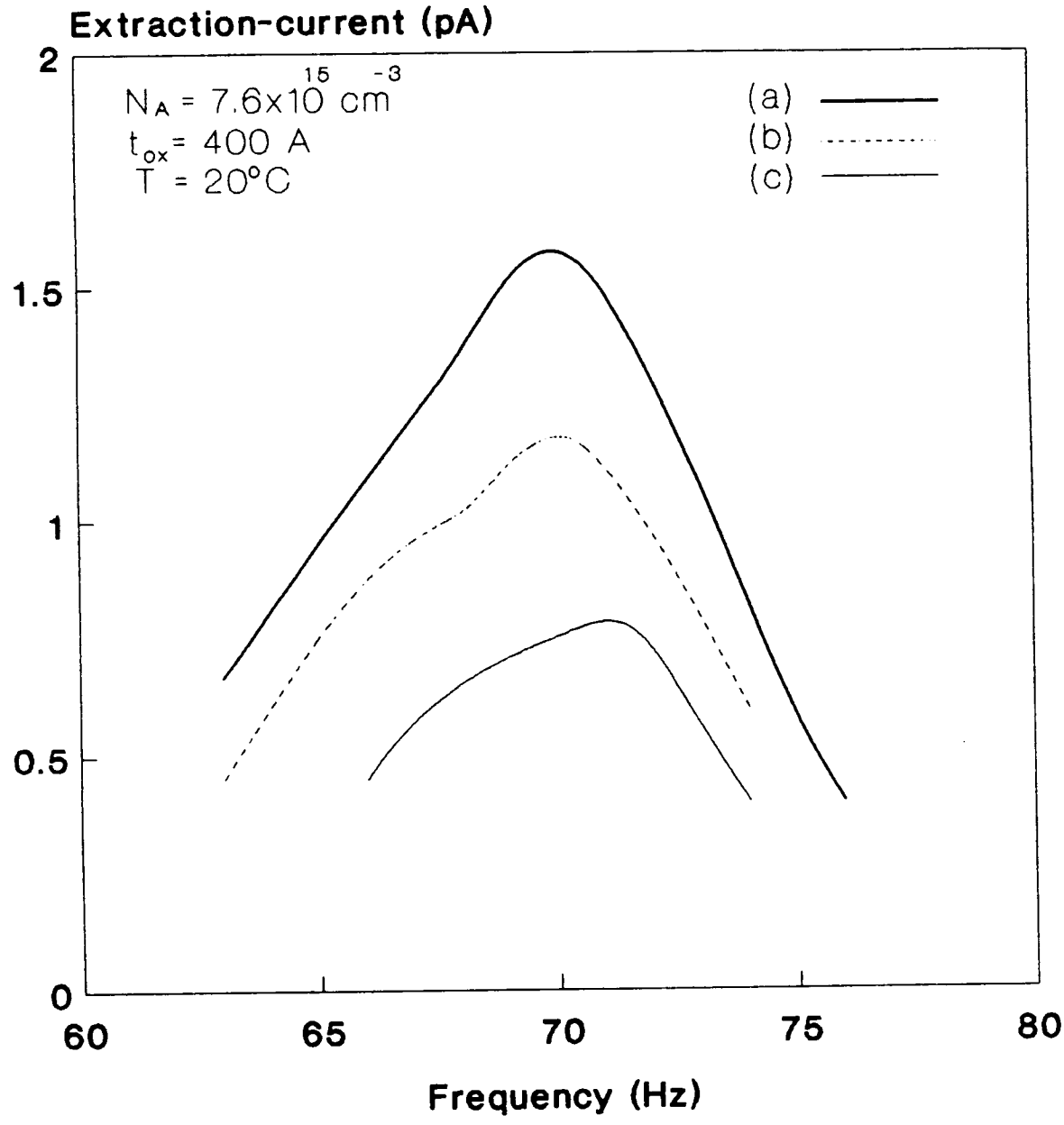


Fig.7.4 Experimental Ice-f curves for the surface-potential sweeps from Ei to E_T for MOS transistors of area, (a) 300x8, (b) 80x20, and (c) 80x8 um^2.

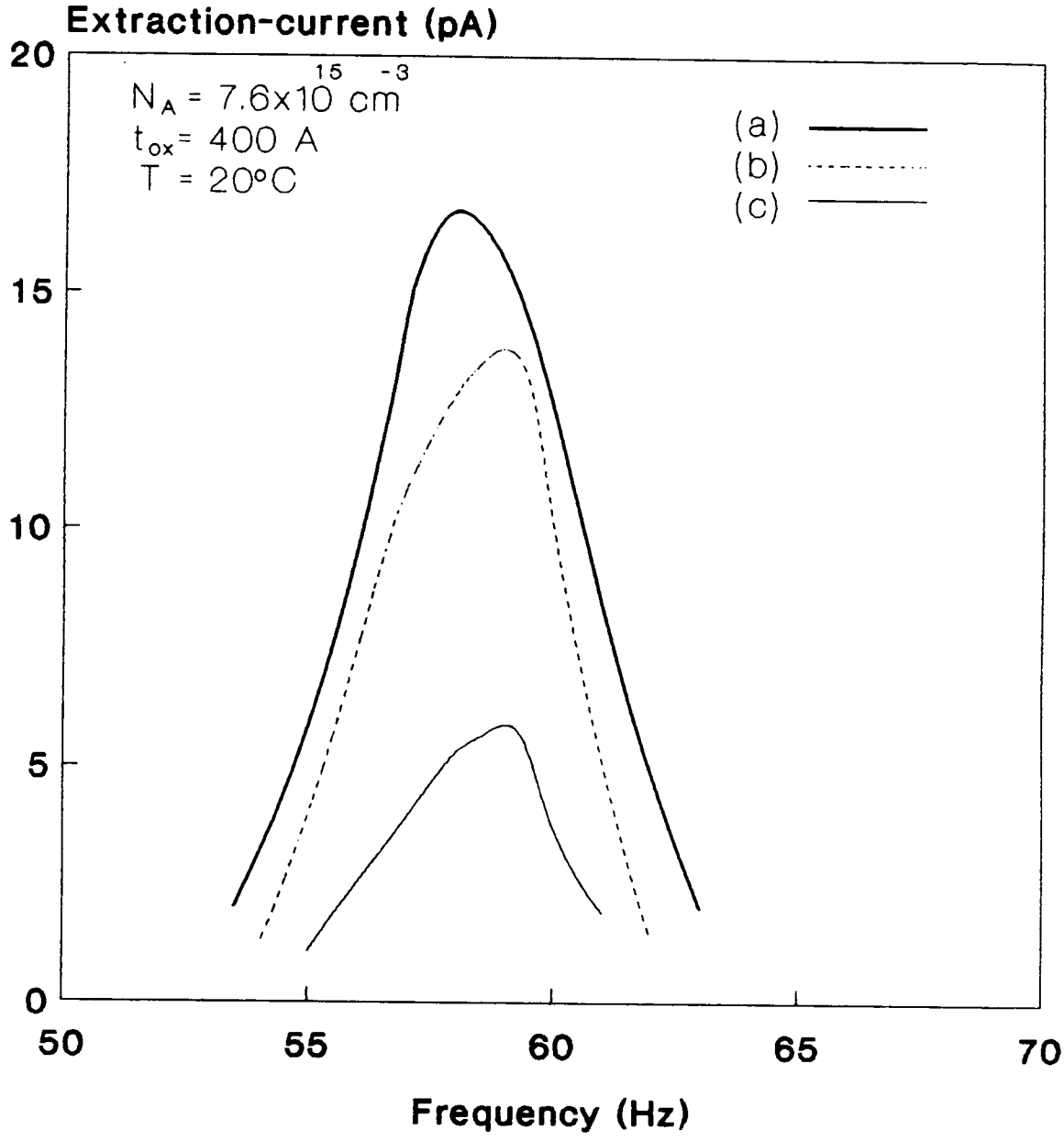


Fig.7.5 Experimental Ice-f curves for the surface-potential sweeps from E_B to E_T for MOS transistors of area, (a) 300x8, (b) 80x20, (c) 80x8 um^2.

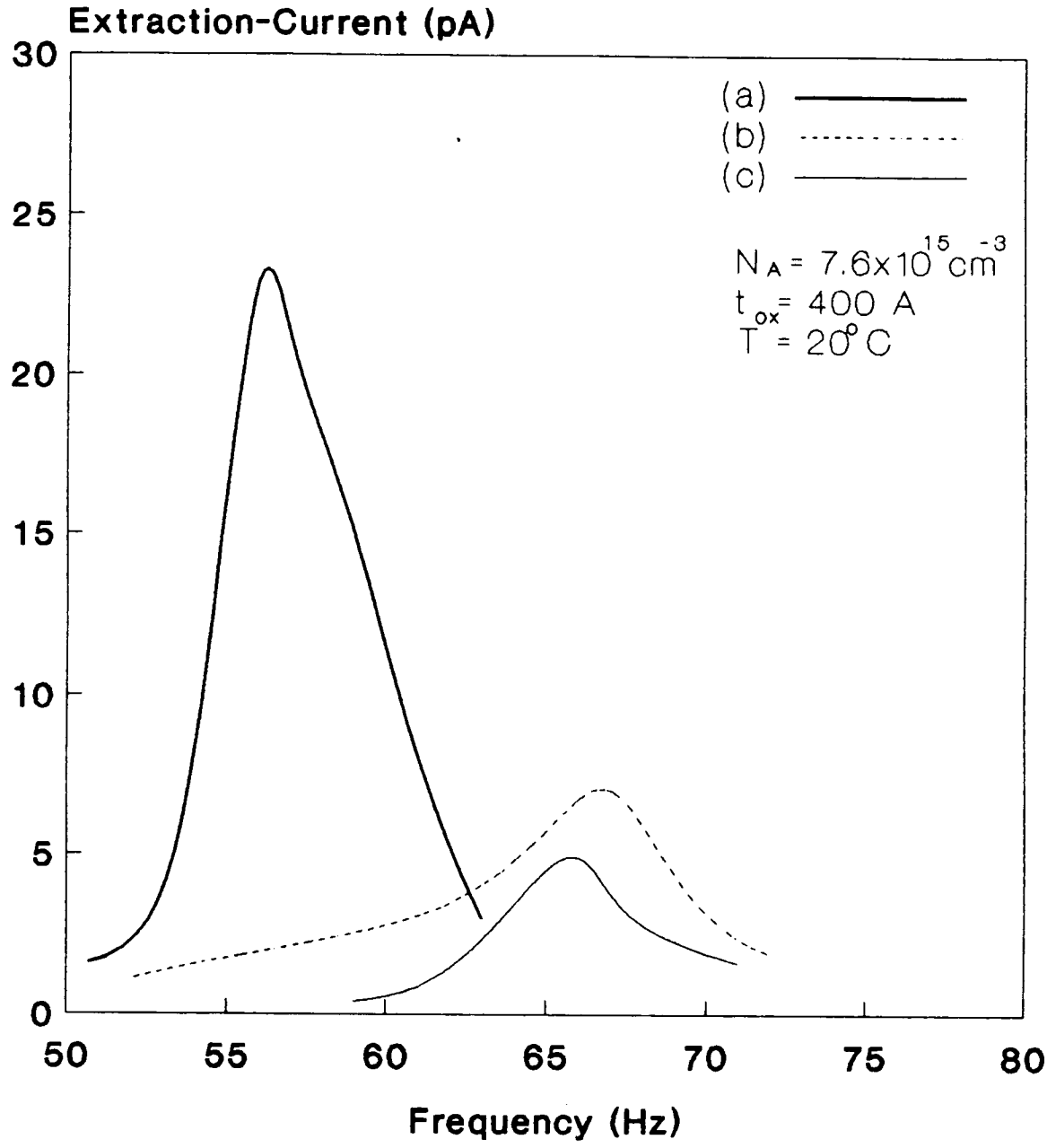


Fig.7.6 Experimental Ice-f curves for MOS transistor of area 80x80 um^2 for the surface-potential sweeps from (a) E_B to E_T (b) Ei to E_B and (c) Ei to E_T.

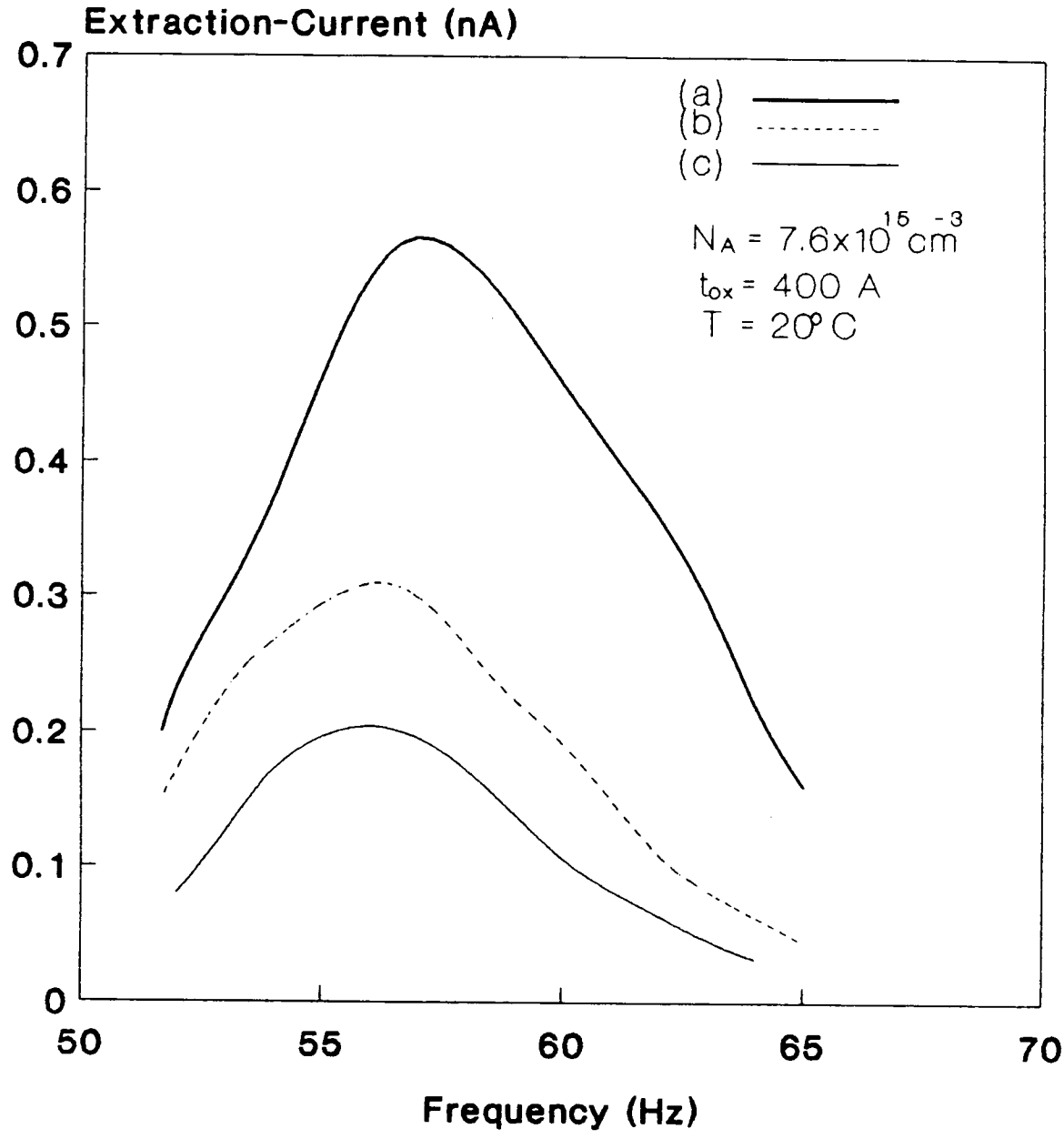


Fig.7.7 Experimental Ice-f curves for MOS transistor of area 300x300 um^2 for the surface-potential sweeps from (a) E_B to E_T (b) Ei to E_B and (c) Ei to E_T.

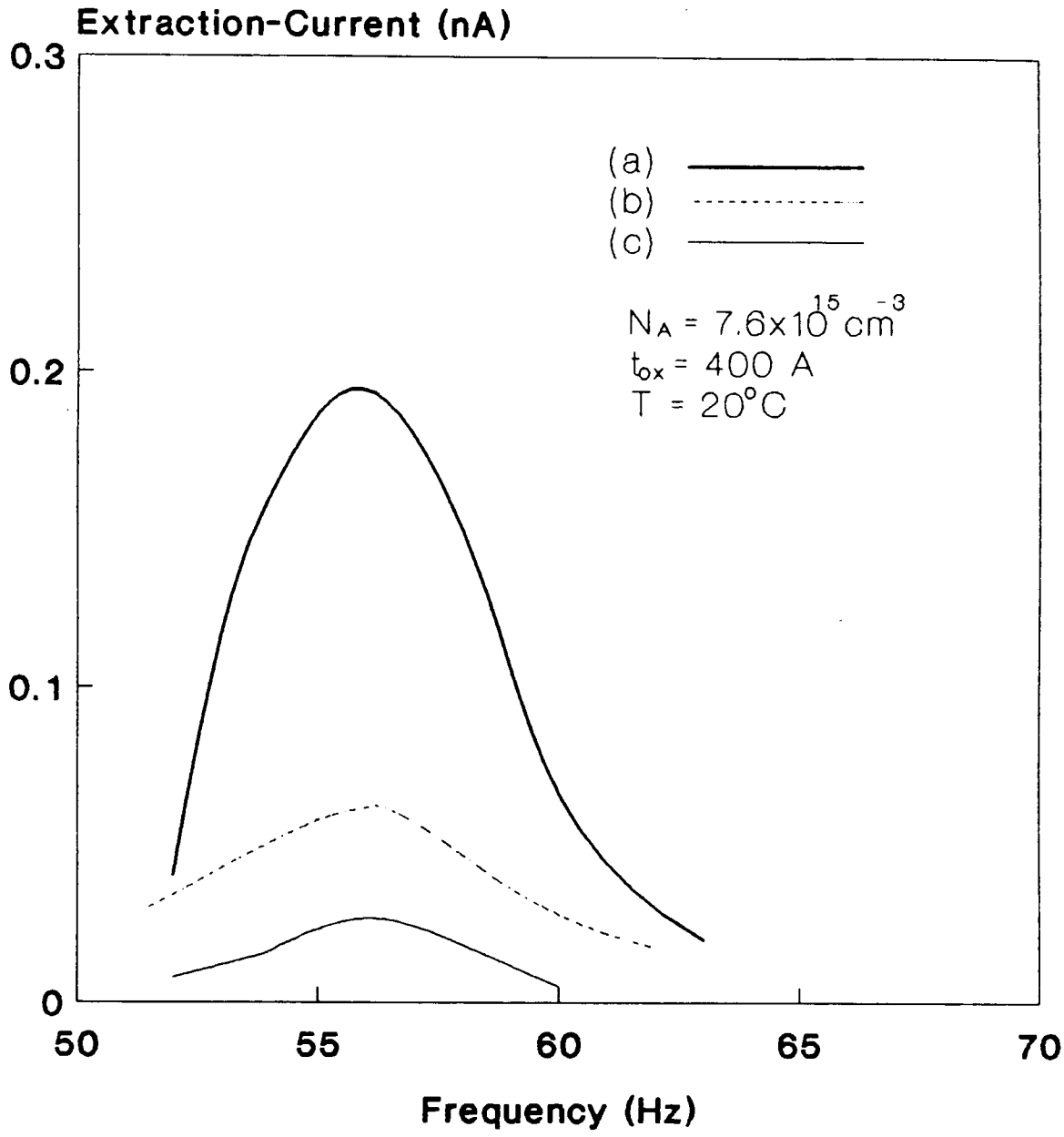


Fig.7.8 Experimental Ice-f curves for MOS transistor of area 300x80 um^2 for the surface-potential sweeps from (a) E_B to E_T (b) Ei to E_B and (c) Ei to E_T.

the device except for the value of the capture cross-sections σ_e and σ_h. Truly speaking, σ_e and σ_h are the parameters of the device-material rather than that of the device itself. The results of the present measurement are exactly the same and in perfect conformity with the above theoretical prediction. A value of f_m equal to 70 Hz (Table 7.1) has been obtained in most cases although devices of widely varying geometry have been used. However, in the case of surface-potential sweep from E_B to E_T, somewhat different value of f_m = 59 Hz was obtained. It may be noted that even this value of f_m = 59 Hz comes out same for all the devices. This indicates that there is a certain well-defined additional factor which brings about this change in the value of the optimum frequency f_m in the case of surface-potential sweep from E_B to E_T. This is exactly what is expected on the basis of the theoretical requirements for this case of surface-potential sweep from E_T to E_B (Fig.7.2). It may be pointed out that the average value $\sqrt{\bar{\sigma}_e\bar{\sigma}_h}$ of the capture cross-sections of electrons and holes, used for this case, is supposed to differ by a fixed amount from the corresponding value $\sqrt{\sigma_e\sigma_h}$ for the case of one-sided surface-potential sweep from E_i to E_B (Fig.7.1a) or from E_T to E_i (Fig.7.1b). A smaller value of f_m for the case of surface-potential sweep from E_T to E_B suggests that $\sigma_e' < \bar{\sigma}_e < \sigma_e$ and $\sigma_h' < \bar{\sigma}_h < \sigma_h$.

The value of f_m = 70 Hz corresponds to a value of $\sqrt{\sigma_e\sigma_h} = 1.8 \times 10^{-15} cm^2$ for silicon using $v = 1.5 \times 10^7 cm\,s^{-1}$ and

Table 7.1 Measured optimum frequency f_m for different devices (n-channel MOSFETs).

Area WxL (μm^2)	Value of f_m (Hz)		
	$\Delta\psi = E_i - E_B$	$\Delta\psi = E_T - E_i$	$\Delta\psi = E_T - E_B$
80x8	72	71	59
80x20	71	70	59
300x8	70	70	58
300x20	70	70	58
300x80	56	56	56
300x300	56	56	56

$n_t = 1.4x10^{10} cm^{-3}$. This average value of the capture cross-section $\sqrt{\sigma_e \sigma_h}$ differs by a factor of about 2 from the one obtained by using the values $\sigma_e = 1.2x10^{-15} cm^2$ and $\sigma_h = 6.0x10^{-16} cm^2$ as determined by the conductance method [9]. In fact, values of σ_e and σ_h as obtained [54-57] by different methods do not show any consistency. Even the values of σ_e and σ_h as determined by any single method differ quite appreciably. For example by using conductance method, the value of σ_e or σ_h itself vary by a factor more than 2.

The observed variation in the experimental value of f_m (Table 7.1) from one device to another may be attributed to a slight variation in the density-profile of their surface-states. In working out the present model, a uniform-density distribution of the surface-states has been considered, which is only approximately true. It is quite possible that the observed variation in the value of f_m is accounted for if a more general model is worked out after considering the density-distribution of the surface-states.

Equations (7.14) and (7.22) have been used to determine the average value of $\overline{D_{it}}$. The values of $\overline{D_{it}}$ for different devices so obtained are shown in Table 7.2 and are compared with those obtained by the charge-pumping method. As on the one hand, the charge-pumping method imposes a restriction on the device-geometry ($\frac{W}{L} \gg 1$) and on the other hand, devices with small gate-area produce very small current in the present method, only a very few devices could satisfy both

Table 7.2 Average values of the density of surface-states $\overline{D_{it}}$ for different devices (n-channel MOSFETs.) as obtained by the present method and their comparison with those obtained by the charge-pumping method (C-P.M).

Area WxL (μm^2)	$\overline{D_{it}}$ obtained by the present method ($cm^{-2}eV^{-1}$).			$\overline{D_{it}}$ obtained by the C-P.M ($cm^{-2}eV^{-1}$)
	$\Delta\Psi = E_i - E_B$	$\Delta\Psi = E_T - E_i$	$\Delta\Psi = E_T - E_B$	
80x8	$2.06x10^{11}$	$1.12x10^{11}$	$2.92x10^{11}$	$0.34x10^{11}$
80x20	$0.89x10^{11}$	$0.67x10^{11}$	$3.48x10^{11}$	$0.39x10^{11}$
300x8	$0.75x10^{11}$	$0.59x10^{11}$	$3.29x10^{11}$	$0.41x10^{11}$

The value of $\overline{D_{it}}$ as supplied by ES2 ranges from $0.9x10^{11}$ to $2.0x10^{11}$ $cm^{-2}eV^{-1}$.

requirements to compare the values of $\overline{D_{it}}$ obtained by the two methods. The value of $\overline{D_{it}}$ as supplied by the fabrication laboratory ranges from $0.9x10^{11}$ to $2.0x10^{11} cm^{-2}eV^{-1}$ from one device to another. It may be seen that the values of $\overline{D_{it}}$ as obtained by the present method show fairly good agreement with those supplied by the fabrication laboratory, whereas the values of $\overline{D_{it}}$ as obtained by the charge-pumping method show more deviation. This discrepancy in the value of $\overline{D_{it}}$ as obtained by the charge pumping-method may be attributed to the limitations and uncertainties as pointed out in section 5.5.

Another important finding of the present study is that the current I_{cb} comes out to be negative in all the cases, that is, flowing from the ground to the p-substrate. This observation is in contradiction to what has been anticipated and assumed in the charge-pumping method [12]. It may be recalled that in charge-pumping method the contribution of the non-steady-state emission of the surface-states to charge-pumping current has been ignored on the plea that the direction of this current-contribution is positive and it is nullified by its counterpart during the second half of the pulse. In fact the circuital conditions in the two methods are quite different. In the present method, using non-steady-state emission, the emitted carriers have only one possible way to flow out, that is, gate-substrate path whereas in the charge-pumping method there is an additional

drain-substrate bypass. Therefore, such carriers may find this drain-substrate bypass easier to flow in the charge-pumping method. However, it is also quite possible that a certain fraction of these carriers still flows in the gate-substrate circuit. If it is so, this may introduce an important error in the manipulation of $\overline{D_{it}}$ by the charge-pumping method. In order to test the validity of the above argument, the current at the gate during charge-pumping measurement, using Elliot method [32], was examined. A significant amount of gate-current was observed at certain specific frequencies. This gate-current has been ignored in the charge-pumping technique. However, at other frequencies, this gate-current is not appreciable and will not introduce any significant error if it is ignored. A comparison of the magnitude of the gate and substrate-currents during measurement of charge-pumping current by Elliot method is shown in Fig.6.15. This gate-current remains unaccounted in the charge-pumping method.

7.5 CONCLUSION

The present method does not involve two types of currents and is free from their implications. Besides, all other limitations which are inherent in the charge-pumping method due to the swing of the surface-region into two regimes, the regime of steady-state recombination and regime of non-steady-state emission as pointed out in section II, do

not apply to the present method. It is because the device uniquely remains under one regime of non-steady-state emission when the surface-potential sweep on one side of the intrinsic level is used. However, this imposes another limitation to this method, that is, a direct and full surface-potential sweep from one end to another in the energy-band gap can not be utilized. Further, devices with very small gate-area can also not be used in the present method, since the charge-extraction current drops to a value below picoampere range for which still more sophisticated charge-measuring instruments are required.

CONCLUSION

The aim of the present research work was to develop the charge-pumping technique using Groeseneken et al model [12] for studying the properties of interface traps in the laboratory. During the course of the proposed experimentation with the charge-pumping technique we have observed a considerable amount of dc substrate-current when the surface region of the MOSFET was periodically cycled between the flatband and threshold voltage. To investigate the possibility that charging and discharging of the interface traps under non-steady-state emission can also contribute to a net substrate current, measurements were done on MOSFET with open drain/source under a gate-voltage signal whose amplitude is not allowed to exceed V_{FB} on one extreme and V_T on the other so that the surface region always remains under the depletion condition. A net substrate-current was

observed even in this case. The experiment has been repeated by using MOS capacitors also which give similar results. This implies that a net charge in the form of electrons passes from the gate to the substrate through the oxide to fill the empty interface traps at the Si-SiO_2 interface during one half of the gate-signal swing whereas the same interface traps emit these electrons to the substrate during the other half. Based on the fact that the gate voltage in this method swings always within the flatband voltage on one side and threshold voltage on the other, it can be easily understood that this current arises due to the non-steady-state emission of carriers. This led to development of a new technique and experimentation. As in this technique the current extracts charge from the gate, it may be better called charge-extraction current in order to distinguish it from charge pumping current for which charge is pumped from the drain/source.

This new technique is based on the general theory [42] of the dynamic characteristics of a MIS capacitor having distributed interface traps. However unlike usual charge pumping method, it does not make use of the entry of the surface region into two regimes of steady state recombination and non-steady-state emission and therefore it is free from any assumption and limitation arising due to transfer of surface region from steady to non steady state regarding emission times, emission level and direction of currents in the two

regimes. Using this theory, quantitative expression for the charge extraction process has been obtained. Experimental results have been obtained on n-channel MOSFETs as well as MOS capacitors. A more accurate mean value for the capture cross section and average density distribution has been found using this method, giving fairly good agreement with the data of the experimental devices as supplied by the ES2 laboratory.

The measurement and calculation procedure are relatively simple and easy to implement, at the same time the method is expected to give more reliable and accurate results as compared to the usual charge pumping technique due to the elimination of certain assumptions. Moreover, It provides good scope for studying several aspects of the MOS structure because various quantities involved in the charging and discharging of the interface traps are determinable precisely in terms of the optimum frequency and this optimum frequency can be obtained very accurately. Also different versions of this experiment can be carried out giving variations in the optimum frequency and these variations in the optimum frequency can be used to obtain more information about the various processes taking place in the charge-extraction process. However this needs more detailed and deeper analysis on the phenomenon of charge-extraction current by taking more factors into account such as dependence of capture cross section electrons and holes on the frequency, surface

potential sweep and possibly on the exact mechanism of emission process whether it is oxide aided or silicon aided. Based on these considerations, the present technique of the study of interface property of MOS structure seems to bear much higher potentiality and capability of providing further information about device parameters. As regards the future scope of work on this technique, it will be worthwile to make an attempt to extend it for the determination of the density distribution of interface traps. It can be easily adopted for obtaining precise values of the flatband voltage and threshold voltage. Efforts may also be made to use this technique for obtaining more exact information and more precise value of the individual capture cross section of electrons and holes.

REFERENCES

[1] G. Liandrat, Conferences at College of France, 1935.

[2] W. Shockley and G. L. Pearson, "Modulation of Conductance of Thin Films Semiconductors by Surface Charges", Phys. Rev., Vol. 74, p. 232, 1948.

[3] C. J. Frosh and L. Derrick, J. Electrochem. Soc., 104,574, 1957.

[4] B. E. Deal, "The Current Understanding of Charges in the Thermally Oxidized Silicon Structure," J. Electrochem. Soc., Vol. 121, pp. 193C-205C, 1974.

[5] R. Jayarama, W. Yang, and C.G. Sodini, "MOS Electrical Characteristics of Low pressure Re-Oxidised Nitride-Oxide," IEDM Techn. Dig., p. 668, 1986.

[6] M. Kuhn, "A Quasi-Static Technique for MOS C-V and Surface State Measurements," Solid-State Electronics, Vol. 13, pp. 873-885, 1970.

[7] L. M. Terman, "An Investigation of Surface States at a Silicon/Silicon Oxide Interface Employing Metal-Oxide-Silicon Diodes," Solid-State Electronics, Vol. 5, pp. 285-299, 1962.

[8] R. Castagne and A. Vapaille, "Description of The Si-SiO_2 Interface by Mean of very Low Frequency MOS Capacitance Measurements," Surface Sci., Vol. 28, p. 557, 1971.

[9] E. H. Nicollian and A. Goetzberger, "The Si-SiO_2 Interface-Electrical Properties as Determined by the Metal-Insulator-Silicon Conductance Technique," Bell Syst. Tech. J., Vol. 46, pp. 1055-1133, 1967.

[10] P. V. Gray and D. M. Brown, "Density of SiO_2-Si Interface States," Appl. Phys. Lett., Vol. 8, No. 2, pp. 31-33, 1966.

[11] D. V. Lang, "Deep-Level Transient Spectroscopy: A Method to Characterize Traps in Semiconductors," J. Appl. Phys., Vol. 45, No. 7, pp. 3023-3032, 1974.

[12] G. Groeseneken, H. E Maes, N. Beltran, and R. F. DE Keersmaecker, "A Reliable Approach to Charge-Pumping Measurements in MOS Transistors," IEEE Trans. Electron Devices, Vol. ED-31, pp. 42-53, 1984.

[13] E. H. Nicollian and J. R. Brews, MOS (Metal Oxide Semiconductor) Physics and Technology, John Wiley & Sons, New York, USA, 1982.

[14] U. Cilingiroglu, "A General Model For Interface-Trap Charge-Pumping Effects in MOS Devices," Solid-State Electronics, Vol. 28, No. 11, pp. 1127-1141, 1985.

[15] U. Cilingiroglu, "Charge Pumping Spectroscopy with Pulsed Interface Probing", IEEE Trans. Electron Devices, Vol. ED-37, No. 1, pp. 267-272, 1990.

[16] S. M. Sze, Physics of Semiconductor Devices, John Wiley and Sons, New York, 1982.

[17] C. N. Berglund, "Surface States of Steam-Grown Silicon-Silicon Dioxide Interfaces," IEEE Trans. Electron Devices, Vol. ED-13, pp. 701-705, 1966.

[18] A. S. Grove, Physics and Technology of Semiconductor Devices, John Wiley & Sons, New York, USA, 1967.

[19] B. E. Deal and A. S. Grove, "General relationship for the Thermal Oxidation," J. Appl. Phys., Vol.36, p.3770, 1965.

[20] M. S. Liang and C. HU, "Electron Trapping in very Thin Thermal Silicon Dioxide," IEDM Techn. Dig., p. 396, 1981.

[21] H. R. Grinolds, S. S. Wong, T. W. Ekstedt, C. G. Sodini, S. H. Kwan, K. H. Jackson and L. Martinez, "Nitrid Oxides for Thin Gate Dielectrics in MOS Devices," IEDM Techn. Dig., p. 42, 1982.

[22] C. Hu, "Thin Oxide Reliability," IEDM Techn. Dig., pp. 368-371, 1985.

[23] S. Holland, I. C. Chen, T. P. Ma, and C. Hu, "Electrical Breakdown in Thin Gate and Tunneling Oxides," IEEE Elec. Dev. Lett., Vol. EDL-5, p. 302, 1984.

[24] I. C. Chen, S. E. Holland, and C. Hu, "On Physical Models for Gate Oxide Breakdown," IEEE J. Solid State Circuits, Vol. SC.-20, p. 333, 1985.

[25] R. R. Razouk and B. E. Deal, "Dependence of Interface State Density on Silicon Oxidation Process Variables," J. Electrochem. Soc., Vol.126, p. 1573-1581, 1979.

[26] B. E. Deal, M. Sklar, A. S. Grove, and E. H. Snow,

"Characterization of the Surface State Charge Q_{ss} of Thermally Oxidized Silicon," J. Electrochem. Soc., Vol.114, pp. 226-274,1967.

[27] P. Balk, Extended Abstracts, Electronics Division, Electrochem. Soc., 14,(1), 273, 1965.

[28] R. J. Van Overstraeten, G. Declerk, and P. A. Muls, "Theory of the MOS Transistor in Weak Inversion", IEEE Trans. Electron Devices, Vol. ED-22, pp. 282-288, 1975.

[29] K. L. Wang, and A. O. Evwaraye, "Determination of Interface and Bulk-Traps States of IGFET's Using Deep-Level Transient Spectroscopy," J. Appl. Phys., Vol 47, pp. 4574-4577, 1976.

[30] F. M. Klaasen, "Characterization of Low 1/f noise in MOS Transistors," IEEE Trans. Electron Devices, Vol.ED-18, p. 887, 1971.

[31] J. S. Brugler and P. J. A. Jespers, "Charge Pumping in MOS Devices," IEEE Trans. Electron. Devices, Vol. ED-16, pp. 297-301, 1969.

[32] A. B. M. Elliot, "The Use of Charge Pumping Currents to Measure Surface State Densities in MOS Transistors," Solid-State Electronics. Vol. ED-19, pp. 241-247, 1976.

[33] R. Williams, "Determination of Deep Centers in Conducting Gallium Arsenide," J. Appl. Phys. Vol. 37; p. 3411, 1966.

[34] D. V. Lang, "Fast Capacitance Transient Apparatus: Application to ZnO and O centers in Gap p-n Junctions," J.

Appl. Phys. Vol. 45, p. 3014, 1974.

[35] A. G. Milnes, Deep Impurities in Semiconductors. Edit John Wiley and Sons, New York, USA. Chapter 6, p.113, 1973.

[36] S. M. Sze, Semiconductor Device Physics and Technology. John Wiley and Sons, 1985.

[37] J. W. Walker and C. T. Sah, "Properties of 1.0 MeV Electron Irradiated Defect Center in Silicon," Phys. Rev. Vol. 7 (10), pp.4587-4605, 1973.

[38] C. T. Sah and J. W. Walker, Appl. Phys. Lett. 22, 384, 1973.

[39] G. Broux, R. Van Overstraeten, and G. Declerck, "Experimental Results on Fast Surface States and 1/f Noise in MOS Transistors," Electron. Lett., Vol. 11, p. 97, 1975.

[40] W. L. Tseng, "A New Charge Pumping Method of Measuring Si-SiO_2 Interface States", J. Appl. Phys. Vol. 62, No. 2, pp. 591-599, 1987.

[41] J. Bosch, thesis, Tech. Phys. Lab., Groningen State University, Groningen, Germany, 1979.

[42] J. G. Simmons and L. S. Wei, "Theory of Dynamic Charge and Capacitance Characteristics in MIS Systems Containing Discrete Surface Traps," Solid-State Electronics, Vol. 16, pp. 43-52, 1973.

[43] J. G. Simmons and L. S. Wei, "Theory of Dynamic Charge and Capacitance Characteristics in MIS Systems Containing Discrete Surface Traps," Solid State Electronics, Vol. 16, pp. 53-66, 1973.

[44] A. Goetzberger, E. Klausmann, and M. J. Shultz, "Interface States on Semiconductor/Insulator Interface," C.R.C. Reviews In Solid-State Sciences, Vol. 6-1, pp.1-43, 1976.

[45] G. Kaden and H. Reimar, Phys. Status Solidi (a), Vo. 32, p. 183, 1975.

[46] G. Kaden and H. Reimer, Phys. Status Solidi (a), Vol. 52, p. 35, 1979.

[47] W. Shockley and W. T. Read, Phys. Rev. Vol. 87, p. 835, 1952.

[48] R.N. Hall, Phys. Rev, Vol. 87, p. 387, 1952.

[49] W. V. Backensto and C. R. Viswanathan, "Measurement of Interface State Characteristics of MOS Transistor Utilizing Charge-Pumping Techniques," IEE PROC. Vol. 128, Pt. 1, No. 2, pp. 44-52, 1981.

[50] P. Hermans, J. Witters, G. Groeseneken, and H. E. Maes, "Analysis of the Charge Pumping Technique and its Application for the Evaluation of MOSFET Degradation," IEEE Trans. Electron Devices, Vol. ED-36, No. 7, pp. 1318-1335, 1989.

[51] T. J. Russel, C. L. Wilson, and M. Gaitan, IEEE Trans. Electron Devices, ED-30, p. 1663, 1983.

[52] U. Cilingiroglu, "A Pulsed Interface-Probing Technique for MOS Interface Characterization at Midgap Levels", IEEE Trans. Electron Devices, Vol. 35, pp. 2391-2396, 1988.

[53] T. Ouisse, S. Cristoloveanu, T. Elewa, H. Haddara, G. Borel, and D. E. Ioannou, "Adaptation of the Charge Pumping

Technique to Gated p-i-n Diodes Fabricated on Silicon on Insulator," IEEE Trans. Electron Devices, Vol. 38, No. 6, pp. 1432-1443, 1991.

[54] J. A. Cooper and R. J. Shultz, "Electrical Characteristics of the SiO_2-Si Interface Near Midgap and in Weak Inversion," Solid-State Electronics, Vol. 17, pp. 641-654, 1974.

[55] M. R. Boudry, "Theoretical Origin of N_{ss} Peaks Observed in Gray Brown MOS Studies," Appl. Phys. Lett., Vol. 22, p. 530, 1973.

[56] M. Schultz and N. M. Johnson, "Transient Capacitance Measurements of Hole Emission from Interface-States in MOS Structures," Appl. Phys. Lett., Vol. 31, pp. 622-625, 1977.

[57] H. Deuling, E. Klausmann and A. Goetzberger, "Interface-States in Si-SiO_2 Interfaces," Solid-State Electron., Vol. 15, pp.559-571, 1972.

A N N E X E

Liste et composition du jury en vue de la soutenance du Memoire de Magister en.....Electronique..Appliquée.....

de/)/)r..BOUDERBALA..Rachid.....

PRESIDENT /: Dr.M.BENZOHRA,Professeur, U.S.T.O.

RAPPORTEUR/: Dr.VED.MITRA, Professeur, I.N.E.L.E.C.

MEMBRES /: Dr.A.OUADJAOUT, Chargé de Recherche, UDTS (SERS).

Dr.K.HARICHE, Chargé de Recherche, INELEC

Dr.A.ABBABOU, Chargée de cours, USTHB.