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Arezki BENFDILA

Effect of Frequency on The Substrate Current in MOS Devices

Defended on November 14, 1992 before the jury:
President: Dr M. BENZOHRA, Professeur, USTO.
Members: Dr V. MITRA, Professeur, INELEC.
Dr A. CHIKOUCHE, Maitre de Recherche, UDTS.
Dr H. BOURDOUCEN, INELEC.
Dr A. AMROUCHE, Charge de Recherche, CDTA.

registration Number: 02/92.

DEDICATIONS

To my mother and father,

to my sister and brothers,

to all my parents;

To people who struggle for democracy and Algerianity,

to people who struggle for the official recognition

of the Amazigh language and culture;

To my students,

I dedicate the result of my reaserches

enclosed in the present thesis.

On Friday November 27, 1992.

BENFDILA AREZKI.

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On July 21, 1992.

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INTRODUCTION

Control of the electrical properties of the MOS (Metal Oxide Semiconductor) systems has been one of the major factors that has led to stable and high performance integrated circuits. The MOS capacitor (or MOS Diode) is used in both monitoring integrated circuit fabrication and studying the electrical properties of the MOS system. The MOS capacitor has the advantage of simplicity of fabrication and of analysis. Historically, the motivation behind the use of the MOS capacitor has been the fabrication of stable and high performance devices and integrated circuits.

Liandrat [1] proposed that the conductivity of a thin semiconductor layer could be modulated by an external field. This effect called *field effect* became one of the powerful tools in surface studies. The existence of quantum states on free semiconductor surface was demonstrated by Shockley and Pearson [2] in 1948 by a field effect experiment. Frosh and Derrik [3] found in 1957 that silicon dioxide acts as an effective barrier against commonly used impurities, thus preventing them from reaching the underlying silicon. Therefore, free semiconductor-surfaces are no more used, they have been replaced, in 1960, by the solid-solid interface between the semiconductor and the grown oxide film of known composition and structure. This process is termed as oxide passivation.

Lilienfeld [4] and Heil [5] made a proposal on the amplifying devices based on the field effect in 1920s and 1930s. However, there was not much understanding of the physical phenomena involved. In 1948 Shockley and Pearson [2] made a demonstration on the field effect which led to the development of the *field effect transistor (FET).* Weimer [6] described the first FET in 1961. The FETs are based on the principle of modulation of the inversion layer conductance. In fact, the idea of inversion layer arose as a problem in studying the bipolar transistor where, for npn transistor, an inversion layer was postulated to exist between the two pn junctions. Brown [7] and Ross [8] found

that the inversion layer could be induced electrically by an electrode deliberately placed in the vicinity of the base region of a bipolar transistor. At about the same time, the idea of putting an insulator between the semiconductor and the control gate came out. This marks the first introduction to the idea of metal-insulator-semiconductor (MIS) structure in the design of FETs. In 1958, Walmark [9] proposed a structure incorporating the native oxide of the semiconductor itself as an insulator in germanium realizing in this way MIS as MOS structure in practice. The first oxide used to fabricate MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is realized by Kahng and Attala [10] and Attala [11] in 1960. Attala [11] suggested that a thermally grown Si-SiO_2 can also be used as a gate insulator. These oxides were grown by Ligenza [12]. Practical MOSFETs were fabricated only after the interface properties of the oxidised silicon surface and the nature of the drift and ionic contamination have been understood and controlled. The MOSFET is largely used in VLSI (very large scale integration) because of its low fabrication cost, small size, and low power consumption.

The fabrication of MOS capacitor (Metal Oxide Silicon) uses the same processing as used in the fabrication of integrated circuits. Therefore, the MOS capacitor provides direct measurements and monitoring of the MOS system

as it is actually fabricated and used in the integrated circuits. Three regions of MOS system are important: the bulk oxide, the silicon-silicon dioxide interface, and the silicon itself. Charges in all three regions play an important role in integrated circuits. In the oxide and in the interface, these charges are undesirable because they adversely affect the device performance and stability. In the silicon, charges such as dopant are intentionally introduced for device operation. The three regions of a MOS system are described below.

The bulk or substrate is the silicon added with impurities which form the desired charges. Depending on the type of these impurities, the silicon can be of p-type if it is added with donor type impurities and of n-type if it is added with acceptor type impurities. The amount of impurity atoms added to silicon is called doping concentration. Traps can be present in the bulk semiconductor but they are of less importance compared to that of interface or that of oxide.

The oxide bulk (SiO_2) is made up of silicon dioxide grown on the silicon. The transport properties of the oxide thus depend on the structure of the oxide which are directly related to the fabrication process. Two major properties of the oxide are of paramount importance: the level of oxide charges and the dielectric breakdown strength. The oxide charges are three types, the oxide fixed charges which

result after interface annealing, the interface trapped charges which are usually located at the silicon-oxide interface, and the mobile ions which are caused by the presence of ionized alkali metal such as potassium and sodium.

The oxide-silicon ($Si-SiO_2$) interface (also resulting from fabrication process) is characterized essentially by the surface (or Interface) states that it contains. The most important parameters of the surface states are 1) the surface state density, 2) the density distribution, 3) the capture cross section, and 4) the type of the surface states. The surface states characteristics have been studied by various methods. The most commonly known and used methods are: C-V (Capacitance Voltage) [13-17], DLTS (Deep Level Transient Spectroscopy) [18-20], PCTS (Photocapacitance Transient Spectroscopy) [21] and Conductance [22]. Recently, some techniques based on the study of substrate current have been developed. The most common method is the charge pumping technique [13-27]. However, the charge pumping technique is thought to suffer with certain limitations [24],[27],[29-34].

In an attempt if the existing limitations of the charge pumping technique can be removed or an alternate approach can be developed which is free from such limitations, we carried out a study on the gate and substrate currents in different MOS devices under varied conditions.

During this study an unusual phenomenon marked by the presence of a new current has been observed. This current is found to exhibit quite distinct properties so as to distinguish it not only from the charge pumping current but also from any hitherto known substrate current. The present work is devoted to carry out at first an extensive experimentation to serve the purpose of as much more fact-finding and data collection as possible. The data and information so collected is then put to some practical applications. However, before taking up the proposed work, a few earlier chapters are devoted to the background study of MOS structure and other related phenomena which are needed for the further understanding and development of the subject.

In chapter 2, a study of the MOS structure operated under different modes is presented. As the present study involves dc conduction through the oxide, various dc conduction phenomena in the oxide are described in chapter 3. One of the characterization technique recently developed, using the substrate current as a means to extract information, is the charge-pumping technique. As the present study is also based on the measurement of the substrate current, which is supposed to arise due to some process of charging and discharging of the surface traps in charge pumping technique, the present technique based on the observed new phenomenon may be supposed as an alternate approach to the charge pumping technique. Based on these considerations the charge

pumping technique needs special treatment which is presented in chapter 4.

After preparing the required background, chapter 5 is used to describe the experimental set-up and devices used in the present experimentation. All experimental details how the whole experimental arrangement is made to operate and give output results automatically are also given in the same chapter. The different results obtained in this work along with the various conclusions drawn on the basis of these results are presented in Chapter 6.

In chapter 7, one of the most important use of the present study, which is the determination of the flatband and threshold voltages in MOS devices, is presented.

Finally, chapter 8 concludes with certain remarks on the future scope and usefulness of the present study. However they are rather qualitative because of the poor understanding of the physical phenomena involved.

THE MOS STRUCTURE

A simple method of controlling the surface conductivity of a semiconductor is to apply an electric field normal to that surface. The electric field is due to the potential difference between the semiconductor bulk and a metallic plate parallel to the semiconductor surface. The applied field causes a redistribution of the mobile charge within a certain layer near the surface, and therefore, a modulation of the conductivity of this layer. This field effect is experimentally observed when the metallic electrode is very close to the semiconductor surface. A practical way to obtain this is to construct a metal-insulator-semiconductor (MIS) structure.

2.1. INTRODUCTION.

Metal-insulator-semiconductor structures have been instrumental in gaining knowledge about the insulator-semiconductor interface. Most of the reliable results have been obtained in thermally oxidized silicon, but the physical picture emerging from these results is generally applicable to any semiconductor-insulator interface. When the insulator used in the MIS structure is silicon dioxide grown on the silicon substrate, the structure is given the name of MOS (metal oxide semiconductor). The MOS structure is one of the simplest heterostructures; it is made up of a metal (gate), oxide (dielectric), and silicon (substrate). The presence of a dielectric material between the gate and the substrate gives rise to a capacitor, hence the MOS structure (also called MOS Diode) exhibits the properties of a capacitor. The study of the behaviour of MOS capacitor under a varying signal applied to the gate with respect to the substrate is a powerful way of investigating the characteristics of the oxide (SiO_2) and oxide-substrate Si-SiO_2 interface. The MOS capacitor can be used in principle for the determination of semiconductor properties (minority carrier life time, doping concentration), interface properties (interface state density, capture cross section), and the oxide properties (mo-

bile or fixed charges in the oxide). The study of the MOS capacitor is based on the comparison of the ideal to the non ideal MOS structure characteristics.

2.2 THE IDEAL MOS STRUCTURE.

A MOS structure is ideal, if it satisfies the following conditions:

1) no current flows through the structure whatever the applied bias may be. It follows that the Fermi-level in the metal and that in the semiconductor remains flat or the metal and semiconductor work functions are equal, that is, $\Phi_M = \Phi_{SC}$.

2) the electric field is nil everywhere when the applied bias is nil, that is, there is no charges in the oxide SiO_2 ($Q_{ox}=0$) and in the interface Si-SiO_2 ($Q_{if}=Q_{it}=0$).

Under an alternating voltage signal applied to the gate, the MOS structure experiences three different modes observed under different gate voltages. These modes are: 1) accumulation, 2) depletion, and 3) inversion.

2.2.1 The Accumulation Mode.

In the accumulation mode, the MOS structure is biased in such a way that the majority carriers are attracted towards the gate. In an n-type silicon (see Fig.2.1a) under a positive bias (or a negative bias for a

p-type silicon), a space charge layer (SCL) builds up near the metal oxide interface. It is due to an electron depletion or to a local reduction in the density of free carriers in the metal. Likewise, a layer of negative charges is generated in the silicon near the oxide-silicon interface. It is due to an electron accumulation or to a local increase in the density of free carriers in the silicon as shown by Fig.2.1b. The condition of neutrality occurs when the amount of charges on the metal is equal but opposite in sign to that on the semiconductor that is,

$$Q_M + Q_{SC} = 0 \tag{2.1}$$

Figure 2.1c shows that in the bulk of the metal, the electric field E(x) is equal to zero. Hence, the presence of the charge Q_M is the reason for a positive discontinuity of the field E(x) at the Si-SiO_2 interface. The electric field E(x) remains constant throughout the oxide of thickness t_{ox}, this is due to the absence of charges in it.
At the oxide-silicon interface, we observe another discontinuity of the electric field ($E_{ox} \longrightarrow E_s$) since the dielectric constant of the oxide ϵ_{ox} is different from that of silicon ϵ_s. The electrostatic potential $\Psi(x)$ in the metal as shown in Fig.2.1d remains constant and equal to V_G upto the metal oxide interface.

- In the oxide, $\Psi(x)$ decreases linearly until it reaches the value Ψ_s at the oxide-silicon interface.
- In the silicon, $\Psi(x)$ decreases rapidly from Ψ_s to zero. Since the accumulation layer is very thin, Ψ_s is very small (a few mV). It follows that the applied gate bias is given by:

$$V_G = V_{ox} + \Psi_s = V_{ox} = E_{ox} t_{ox} \qquad (2.2)$$

where V_{ox} is given by

$$V_{ox} = \frac{Q_M}{C_{ox}} \qquad (2.3a)$$

and the capacitance of the oxide C_{ox} by

$$C_{ox} = \frac{\epsilon_o \epsilon_{ox}}{t_{ox}} \qquad (2.3b)$$

The energy band diagram of the MOS structure is shown in Fig.2.1e. The figure shows the variations of the potential $E_P(x)$ in the three materials. Near the oxide-silicon interface, the energy bands bend so that the conduction band at the interface Ec moves towards the Fermi-level which is kept horizontal since the structure is in equilibrium. This is consistent with an increase of the probability of occupation

of the states by the majority carriers near the semiconductor interface.

Figure 2.1.e-f shows the same treatment for a p-type material.

2.2.2 The Depletion Mode.

In the depletion mode, the MOS structure is biased in such a way the majority carriers of the substrate are repelled away from the $Si-SiO_2$ interface towards the bulk. Thus, for an n-type silicon (Fig.2.2a) $V_G<0$ and for a p-type $V_G>0$.

When the metal is negatively biased, a layer of negative charges builds up at the metal-oxide interface. It is due to an electron accumulation or to a local increase of the density of free carriers of the metal. A layer of positive charge is generated in the silicon near the $Si-SiO_2$ interface because the electrons of the substrate which have been repelled by the field, leave behind the fixed positively ionized doping atoms (Fig.2.2b). The condition of electric equilibrium gives rise to a charge Q_M on the metal such that:

$$Q_M + Q_{SC} = 0 \tag{2.4}$$

where

$$Q_{SC} = qN_D W_{SC}, \tag{2.5}$$

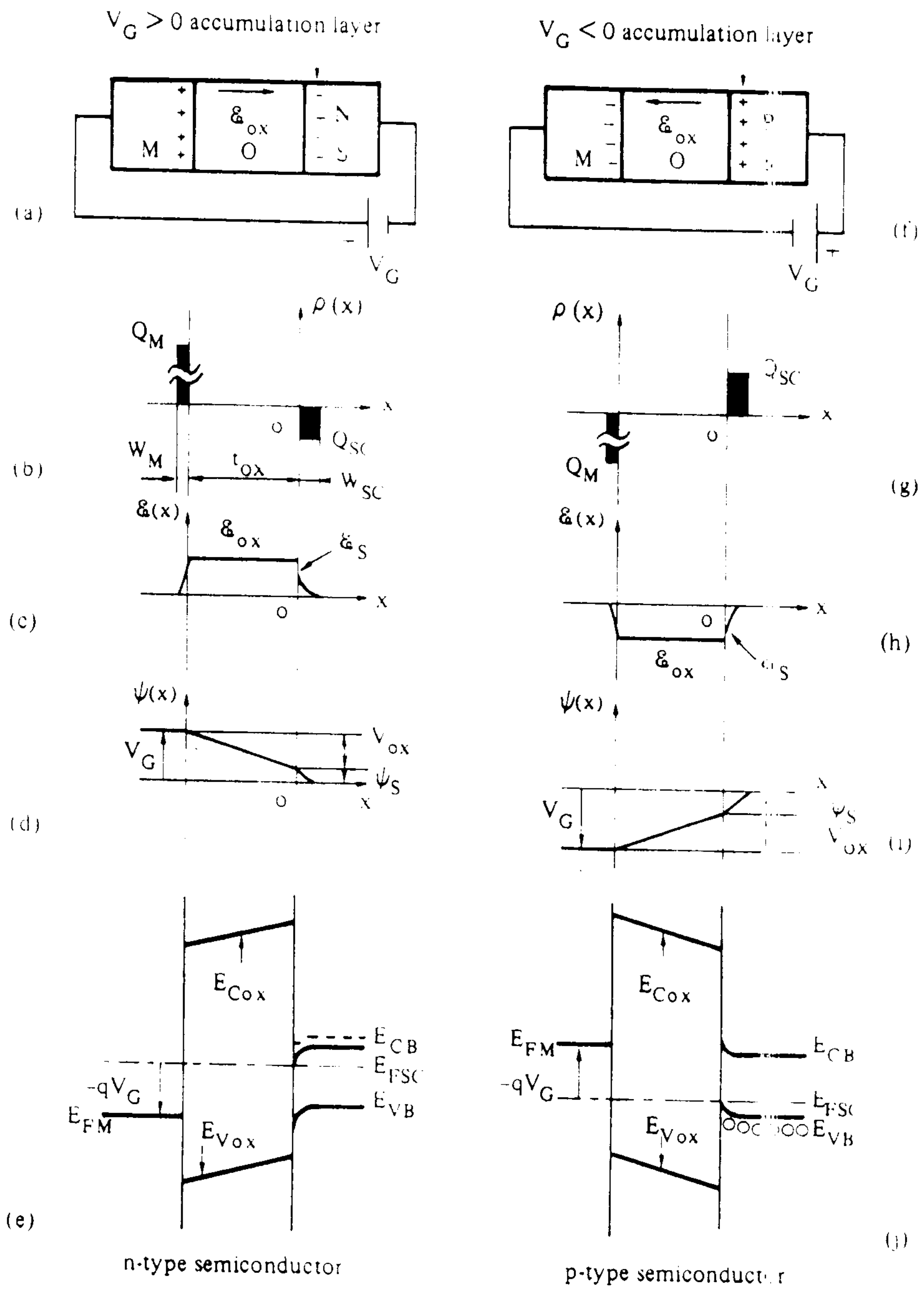


Fig.2.1. a-e MOS structure under bias in accumulation mode, for an n-type silicon. a) Biasing conditions, b) Charge distribution, c) Field distribution, d) Potential distribution, and d) Energy band diagram. f-j Same as above but for p-type semiconductor. (After [35]).

N_D is the doping concentration and W_{SC} is the width of the charge layer.

The field and the potential distribution can be obtained from the charge distribution illustrated in Fig.2.2b. Figure 2.2c shows that the electric field is zero in the bulk of the metal, hence the presence of Q_M is responsible for a negative discontinuity of E(x) at the metal-oxide interface. The electric field remains constant throughout the oxide layer since the oxide contains no charge.

At the $Si-SiO_2$ interface, a discontinuity of the electric field has been observed, it is due to the same phenomenon as discussed in section 2.2.1. Within the space charge layer, the electric field varies linearly with distance **x**, where **x** is measured from the interface $Si-SiO_2$. Poisson's equation, with the boundary conditions E(x)=0 at x=0 and E(x)=0 for x>Wsc shows that the potential $\Psi(x)$ remains constant and equal to V_G as it is shown in Fig.2.2d. In the oxide, $\Psi(x)$ increases linearly until it reaches the value Ψ_s at the $Si-SiO_2$ interface. In silicon, $\Psi(x)$ increase with respect to **x** from Ψ_s to zero in a quadratic manner. For x=0, the surface potential is given by:

$$\Psi_s = \frac{qN_D W_{SC}^2}{2\epsilon_o \epsilon_{sc}} \qquad (2.6)$$

When Eqs.(2.3a) and (2.6) are used in Eq.(2.2), the expression of V_G becomes:

$$V_G = \frac{Q_M}{C_{ox}} + \frac{qN_D W_{sc}^2}{2\epsilon_o \epsilon_{sc}} \qquad (2.7)$$

Figure 2.2e illustrates the energy band diagram of the MOS structure. In the silicon, near the surface the bands are bent upward leading to a lower probability of occupation of the allowable states in the conduction band.

The same discussion can be carried out for a p-type silicon as described in Fig.2.2f to Fig.2.2j.

2.2.3. The Inversion Mode.

The inversion mode starts when the bands experience a banding equal or greater than twice the bulk potential Φ_B. This happens if for a negatively biased n-type MOS structure, the amplitude of the gate signal is increased. This increase of gate signal brings negative charges on the metal electrode, which must be balanced by an equivalent increase on the semiconductor side. This is obtained by increasing W_{sc}. Consequently, the band bending increases and the top of the valence band (Ev) at the surface gets closer to the Fermi-level. However, as band bending increases, the density

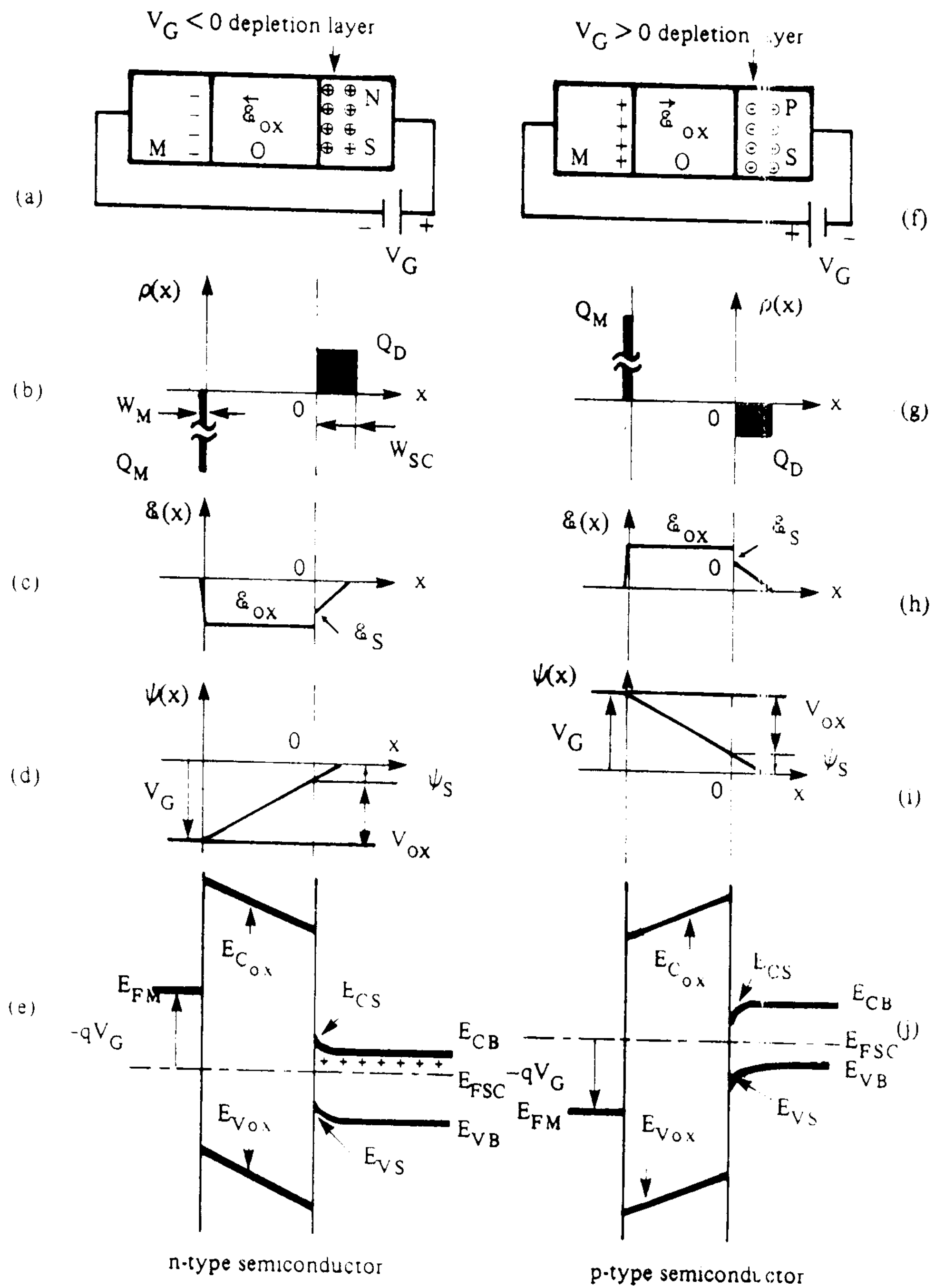


Fig.2.2. a-e MOS structure under bias in depletion mode, for an n-type silicon. a) Biasing conditions, b) Charge distribution, c) Field distribution, d) Potential distribution, and d) Energy band diagram. f-j Same as above but for p-type semiconductor. (After [35]).

of minority carriers (holes in the case of an n-type substrate) becomes important. When the hole concentration (p) at the silicon surface becomes larger than the concentration of the doping atoms (N_D), an inversion layer [which is separated from the bulk of the silicon by depletion layer] builds up. The built up of the inversion layer is a threshold phenomenon. The threshold condition arises when the doping concentration equals the concentration of minority carriers at the surface. This condition can be written as:

$$p = N_v \exp\left(\frac{E_{is} - E_F}{kT}\right) = N_D = n_B = N_C \exp\left(\frac{E_F - E_C}{kT}\right) \quad (2.8)$$

where Nv is the effective density of the states in the valence band, Ev the energy level of the valence band edge at the surface, E_{is} the midgap level at the surface, N_C the effective density of the states in the conduction band, n_B the concentration of the electrons in the bulk of the silicon and E_C the lower edge of the conduction band in the bulk.

To avoid comparison of minority carriers with the majority carriers, the former are expressed in terms of n_i, the intrinsic concentration, and E_i, the intrinsic energy level at midgap, so that Eq.(2.8) can be written as :

$$p = n_i \exp\left(\frac{E_{is} - E_F}{kT}\right) = n_B = n_i \exp\left(\frac{E_F - E_{iB}}{kT}\right) \qquad (2.9)$$

where E_{iB} is the midgap level at the bulk. From Eqs.(2.8) and (2.9), the surface potential $\Psi_{s,inv.}$ required to reach the inversion can be expressed by:

$$q\Psi_{s,inv.} = E_{is} - E_{iB} = 2kT\ln\left(\frac{n_B}{n_i}\right) = 2kT\ln\left(\frac{N_D}{n_i}\right) \qquad (2.10)$$

At the onset of inversion, the depletion layer reaches a limiting value given by:

$$W_m = q\left(\frac{2\epsilon_o\epsilon_{sc}\left|\Psi_{s,inv.}\right|}{qN_D}\right)^{1/2} \qquad (2.11)$$

and the charge contained within the depletion layer reaches the value

$$Q_{DM} = qN_DW_m \qquad (2.12)$$

The gate voltage necessary to reach the onset of the inversion, referred as threshold voltage and having a symbol V_T is defined by:

$$V_T = -\frac{Q_{DM}}{C_{ox}} + \Psi_{s,inv.} \qquad (2.13)$$

Once the inversion is reached, the distribution of charges, electric fields and potentials, and the energy band diagrams experience a change that is shown in Fig.2.3a to 2.3e. Figure 2.3b shows the negative charge Q_M balanced by the sum of the charge contained in the inversion layer and that contained in the depletion zone, that is,

$$Q_M + Q_{inv.} + Q_{DM} = 0 \qquad (2.14)$$

Since Q_D remains constant, any increase in Q_{DM} is cancelled by an increase in $Q_{inv.}$. The field and potential distributions are similar to those of depletion except for the inversion region. Since the inversion layer has a negligible thickness, the potential Ψ_s and $\Psi_{s,inv.}$ are nearly equal, thus

$$V_G = -V_{ox} + \Psi_{s,inv.} \qquad (2.15a)$$

$$V_G = -\frac{Q_{inv.} + Q_{DM}}{C_{ox}} + \Psi_{s,inv.} \qquad (2.15b)$$

It is clear that when V_G increases, $\Psi_{s,inv.}$ increases since V_{ox} is constant.

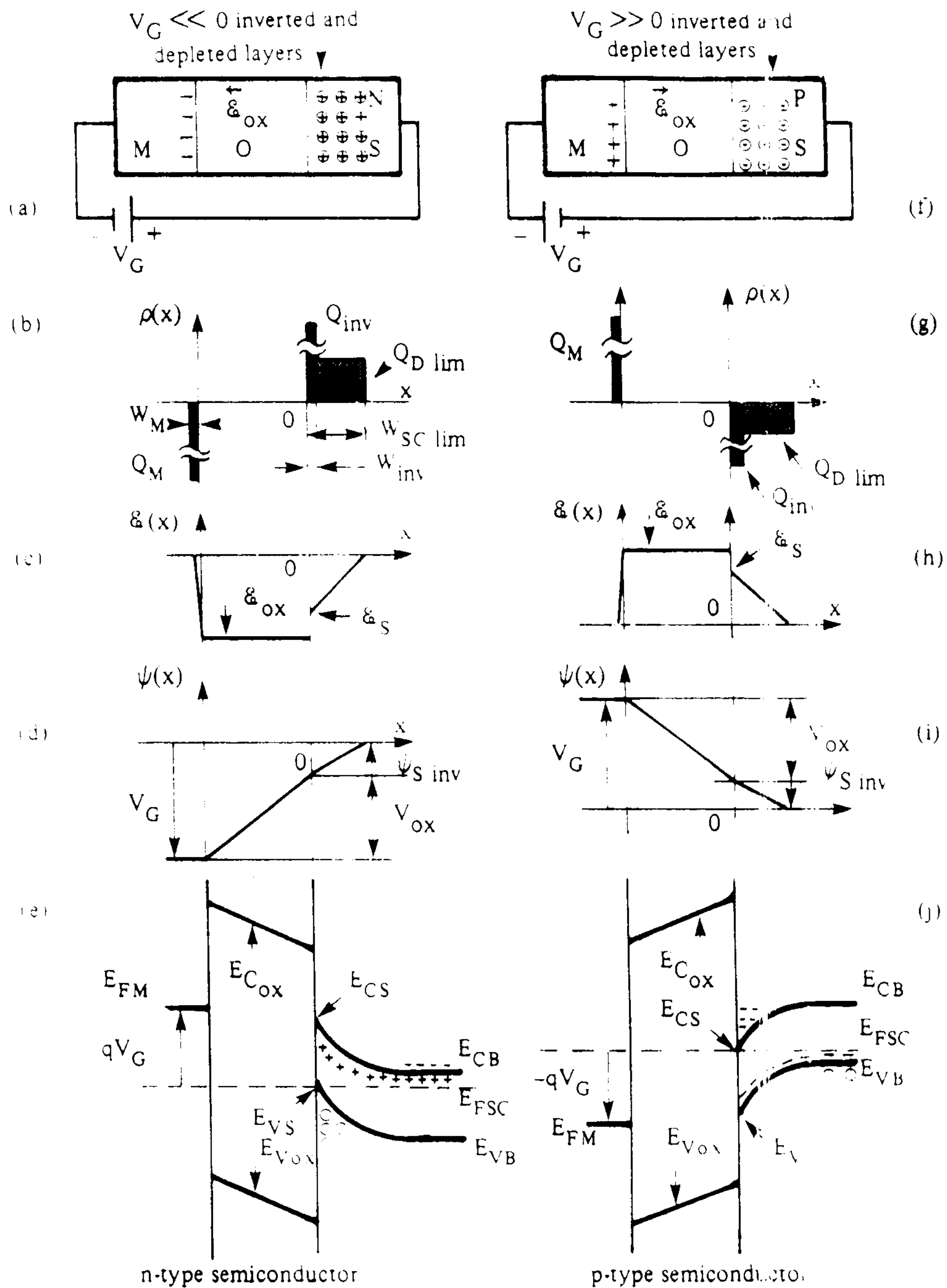


Fig.2.3. a-e MOS structure under bias in inversion mode, for an n-type silicon. a) Biasing conditions, b) Charge distribution, c) Field distribution, d) Potential distribution, and d) Energy band diagram. f-j Same as above but for p-type semiconductor. (After [35]).

2.3. THE NON IDEAL MOS STRUCTURE.

A real or non-ideal MOS structure contains always charges located in the bulk oxide and/or at the oxide-semiconductor interface. These charges are traditionally classified into four groups which are: 1) the mobile charges, 2) the fixed interface charges, 3) the interface trapped charges, and 4) the oxide trapped charges. These charges introduce a difference in the metal and semiconductor work functions that is, $\Phi_M \neq \Phi_{sc}$. This gives rise to an electric field in the insulator as well as in the semiconductor even under no bias.

The mobile charges (Q_m) are in fact foreign ions mobile in the silicon network under the action of an electric field in a temperature range usually taken from zero to 400° C.

The fixed interface charges also called oxide fixed charges (Q_f) are located close to the Si-SiO_2 interface. They are impervious to the action of electric fields and are only affected by high temperature annealing.

The defects or impurities located at the Si-SiO_2 interface can act as carrier traps if their presence introduces energy levels in the silicon forbidden gap. They are then referred to as interface or surface states (or traps). These surface states can interchange carriers with both silicon bands and possibly with those of the oxide. The carriers temporarily

or permanently trapped in the interface form the so-called interface-trapped-charge (Q_{it}) and the amount of this charge depends on the applied bias.

The above mentioned charges influence the MOS diode characteristics in a different manner.

2.3.1 Influence of The Metal-Semiconductor Work Function Difference.

In the case of ideal MOS structures, the surface potential of the metal is equal to that of the semiconductor; no fundamental change in the physical behaviour of the MOS structure occurs when the surface potentials are different. However, in this case there exists an electric field in the oxide (insulator) and in the top layer of the silicon. A bias must be applied to the MOS diode to flatten the silicon bands. This bias, henceforth called *flat-band voltage*, is given by:

$$V_{FB0} = \frac{\Phi_M - \Phi_{SC}}{q} = \frac{1}{q}\left[\Phi_M - \chi + \frac{E_G}{2} \pm kT\ln\left(\frac{N}{n_i}\right)\right] \qquad (2.16)$$

The sign (+) or (-) depends on the type of the semiconductor, (+) for a p-type and (-) for an n-type. In general, the MOS diode is studied by C-V methods [13-17], the effect of the work function difference is to shift the actual C-V curve with respect to the ideal one.

2.3.2 Influence of The Oxide-Charges.

The oxide-charges can be mobile ions or oxide fixed charges which are distributed unevenly in the oxide bulk. The distribution of these charges is represented by a volume density $\rho(x)$ which varies with distances and depends on time in case of electrically stressed MOS structures.

To study the influence of the charge distribution on MOS structures, the origin of the distance axis ($\mathbf{x}$) is defined to be the metal-oxide interface and the various effects and phenomena occurring in the oxide and at the interface are integrated in the interval zero (the interface) to t_{ox} (the oxide thickness).

Using Gauss's law, the electric field experiences a discontinuity δE_{ox} when crossing the charge layer and this discontinuity is given by:

$$\delta E_{ox} = \frac{\rho(x)dx}{\epsilon_o \epsilon_{ox}} \quad (2.17)$$

For flatband conditions in the silicon, the electric field should be equal to zero at the right hand side of the discontinuity, that is, the corresponding voltage giving flatband conditions is given by:

$$\delta V_{FB} = -\frac{\rho(x)x dx}{\epsilon_o \epsilon_{ox}} \quad (2.18)$$

The effects of all layers in the oxide is similar and hence can be added together, it comes out that the voltage necessary for flatband conditions is:

$$V_{FB1} = \int_{o}^{t_{ox}} \frac{\rho(x) x dx}{\epsilon_o \epsilon_{ox}} \tag{2.19}$$

The oxide fixed charges Q_f are positive and have a different effect from that described before. These charges are produced due to the structural defects created during fabrication. The oxide fixed charges cause a band bending which can be corrected by a corresponding voltage given by:

$$V_{FB2} = \frac{Q_f t_{ox}}{\epsilon_o \epsilon_{ox}} \tag{2.20}$$

2.3.3. Influence of The Interface Trapped Charges.

Interruption of the silicon lattice at the interface with the oxide introduces electronic states whose energy levels are distributed in the forbidden gap of the silicon. In a semiconductor, energy levels below Fermi-level E_F are occupied and above it are not occupied and hence, there exists a trapped charge at the interface.

Any increase in the charge Q_M on the metal electrode due to an increase of gate bias will be balanced on the silicon side by an increase of the space charge layer which results

in an increase in the charge trapped in the interface states because the increase of the gate bias produces a filling of more surface states due to the displacement of the Fermi-level.

The interface traps do not react to high frequency signals, this is the reason why the overall capacitance in the high frequency C-V curves do not show any shift in conjunction to the surface states as it is the case in the low frequency C-V curves. When the flatband conditions are met, the charge trapped in the surface states (that can not follow the rapid change of the high frequency signal) are responsible for the shift of the high frequency C-V curve with respect to the low frequency C-V one. The value of the corresponding voltage necessary for the flatband conditions is given by:

$$V_{FB3} = \frac{Q_{it}(FB)t_{ox}}{\epsilon_o \epsilon_{ox}} \qquad (2.21)$$

At low frequencies, the interface traps modify both the overall capacitance as well as the C-V curves. This can be explained by the time available for the surface states to follow the gate signal variations.

2.3.4 Influence of The Dielectric Polarization.

In general, the polarization effect under normal

condition can be neglected in the case of SiO_2 dielectrics. However, it can be very important in other dielectrics or SiO_2 added with PSG layers. The application of an electric field $\vec{E}$ generates dipoles which align themselves in the direction of the field. To quantify the polarization effect, the polarization vector **P** which is the sum of the dipolar moments per unit volume **qR** is introduced as

$$\vec{P} = \frac{\Sigma q\vec{R}}{volume} \tag{2.22}$$

The polarization is proportional to the electric field and is given by:

$$\vec{P} = \epsilon_o \chi_p \vec{E} \tag{2.23}$$

where χ_p is the polarizability of the material.

The polarization does not modify the charge density in the bulk since, the overall charge of the dipole is equal to zero. However, the polarization gives birth to a superficial positive charge at the interface where the electric field is directed outwards and to a negative charge at the other interface. The charge densities of these superficial layers are equal to the polarization P.

2.3.5 The Concept of Flat-band Voltage.

To calculate the capacitance of a MOS diode using

the flatband voltage on a C-V curve, one has to consider the resulting flatband voltage which is the sum of all the previously described flatband voltages and is given by:

$$V_{FB} = V_{FB0} + V_{FB1} + V_{FB2} + V_{FB3} + V_{FB4} \qquad (2.24)$$

with V_{FB4} being the flatband voltage due to the polarization. This term is considerable in case of PSG added oxides and very small in pure Silicon-oxide.
The sum of the actions of the flatband voltages V_{FB1}, V_{FB2} and V_{FB3} can be represented by an image charge Q_{im} given by:

$$Q_{im} = -C_{ox}(V_{Fb1} + V_{FB2} + V_{FB3}) \qquad (2.25)$$

which can be expressed as:

$$Q_{im} = \int_{o}^{t_{ox}} \frac{\rho(x)x\,dx}{t_{ox}} + Q_f + Q_{ifFB} \qquad (2.26)$$

Except V_{FB0} and V_{FB4}, the other flatband voltages can not be calculated. They have to be measured. This makes the determination of the net flatband voltage V_{FB} quite difficult and accurate methods of measurements do not exist, especially for short channel MOS transistors.

CONDUCTION IN THIN INSULATING FILMS

In integrated circuit technology, insulating layers are widely used. They can be used to passivate a surface or allow field effects in a semiconductor. If these insulators were perfect, they would block the flow of any current. In fact, under certain specific temperature and or field conditions, several physical processes allow electrical charges (electrons, holes, or ions) to move in insulators, thus leading to a sizable current densities, especially when the insulating films are thin (typically less than 1 μm).

3.1 INTRODUCTION.

An electric current in an insulator can result from the flow of electrons and/or ions. The present chapter deals only with electronic conduction. Electrons can either be intrinsic (belonging to the insulator) or extrinsic (injected from nearby layers -electrode-).

In the case of intrinsic electrons, the carrier density is low (there are few conduction electrons naturally available in an insulator) and conduction is of the ohmic type with very high resistivity.

Two cases are possible in case of extrinsic electrons. 1) The electrodes behave as unlimited sources. The current is then only limited by the bulk of the insulator (Poole-Frenkel effect, space charge limited current, hoping conduction). 2) The electrodes make limited carrier injection. The electrons once introduced travel in free flight inside the insulator (Schottky effect if the energy of the electrons is sufficient to propel them into the insulator conduction band; tunnel effect otherwise).

The different conduction cases that will be discussed next, suppose that the insulating layer is wholly homogeneous. This condition is satisfied for layers thicker than 50 nm but rarely satisfied for thinner layers. When the insulator is not homogeneous, it is difficult to introduce,

in the mathematical models, the parameters defined by geometrical considerations. In addition, the range of applied bias should not exceed the rigidity of the insulator that is, the electric field should not exceed 5.10^6 $V.Cm^{-1}$.

3.2. THE SCHOTTKY (OR THERMIONIC) CURRENT.

The thermionic current or schottky current is due to the electrons which transit above the potential barrier, i.e, those of energy $E > \Phi_m$ and is given by [35]:

$$J = \frac{4\pi m^* q k^2 T^2}{h^3}\left(1 - \exp\left(-\frac{V}{kT}\right)\right)\exp\left(-\frac{\Phi_m - \xi}{kT}\right) \qquad (3.1)$$

where:

m* is the electron effective mass, q the coulombic charge, h the Planck's constant, k the Boltzman's constant, T the temperature in Kelvin, V the bias voltage, and $\Phi_m - \xi$ is the effective metal-insulator barrier.

We notice that for V/kT>>1, the expression [1-exp(-V/kT)], which takes into account the flux of electrons in both directions, tends towards 1. At room temperature, this condition corresponds to V>>25 mV.

As expected, the current flow is a thermally activated process (the electrons must get over the barrier to cross the insulator). The activation energy is $\Phi_0 - \beta_s \xi^{1/2}$, where Φ_0 is the difference between the insulator-metal

barrier height and $\beta_s \xi^{1/2}$ is the barrier lowering due to image force. A plot of $\ln(J/T^2)$ *versus* $1/T$ yields a straight line with a slope determined by the permittivity ϵ_i of the insulator.

3.3. THE TUNNELLING CURRENT.

The tunnel emission is caused by field ionization of trapped electrons into the conduction band or by electrons tunnelling from the metal Fermi energy into the insulator conduction band.
The tunnelling current density J(V,T) is given by [36]:

$$J(V,T) = \frac{4\pi m^* q}{h^3} \cdot \frac{\exp(-b_1)}{c_1^2} \cdot \frac{\pi c_1 kT}{\sin \pi c_1 kT} \cdot (1 - \exp(-c_1 V)) \tag{3.2}$$

with

$$b_1 = \alpha^* \int_{x_{11}}^{x_{21}} (\Phi(x) - \xi_1)^{1/2} dx \tag{3.3}$$

$$c_1 = \frac{\alpha^*}{2} \int_{x_{11}}^{x_{21}} (\Phi(x) - \xi_1)^{-1/2} dx \tag{3.4}$$

$$\alpha^* = \alpha \left(\frac{m^*}{m} \right)^{1/2} \tag{3.5}$$

where $\alpha = 10.25$ ($in\ eV^{-1/2}.nm^{-1}$) (the other symbols have their previous meanings). x_{11} *and* x_{21} are the abscissae of the turning points for electrons whose energy is equal to the Fermi level in the metal.

The tunnel emission is strongly dependent on the applied voltage but essentially independent of temperature. When the bias is high, the effective thickness is changed to $X_{21} = t_i.\Phi_o/V$, X_{11} being still nil. Replacing the value X_{11} and X_{21} in Eq.(3.3) and (3.4), the tunnelling current expressed by Eq.(3.2) becomes:

$$J = \frac{q^2}{8\pi h}.\frac{V^2}{t_i \Phi_o}.\exp\left(-\frac{2}{3}.\alpha^*.t_i.\frac{\Phi_o^{3/2}}{V}\right) \qquad (3.6)$$

with t_i being the thickness of the insulator. Equation (3.6) describes the Fowler-Nordheim type of current.

3.4. THE POOLE-FRENKEL CURRENT.

The Poole-Frenkel emission is due to field-enhanced thermal excitations of trapped electrons into the conduction band. For trap states, the expression of the current density is identical to that of the Schottky emission. The barrier height however, which is the depth of the trap potential well and the quantity $\xi^{1/2}$ is larger than in the case of Shottky emission by a factor of two because the barrier

lowering is twice as large due to the immobility of the positive charges. The expression of the Poole-Frenkel current depends on the insulator thickness and on trap sites presence in the insulator. Three major cases can be distinguished [35]:

1) Thick insulator without traps.

The current in this case is given by :

$$J = q(N_C N_D)^{1/2}.\mu.\exp\left(-\frac{\Phi_D}{2kT}\right).\exp\left(\frac{\beta_{BF}}{2kT}\xi^{1/2}\right)\xi \qquad (3.7)$$

where:

Nc is the equivalent density of states in the insulator conduction band, N_D the concentration of donor atoms, Φ_D the potential of the donor states with respect to the conduction band of the insulator, μ, the mobility of electrons, and β_{BF} is given by $(q/(\pi\epsilon_o\epsilon_i))^{1/2}$.

2) Thick insulator with traps.

The poole-Frenkel current for this case is found to be:

$$J = q.N_C.\left(\frac{N_D}{N_t}\right)^{1/2}\mu.$$

$$\exp\left(-\frac{\Phi_D+\Phi_t}{2kT}\right).\exp\left(\frac{\beta_{PF}}{2kT}.\xi^{1/2}\right).\xi \qquad (3.8)$$

where N_t is the spatial density of the carrier traps of the insulator and Φ_t is the potential of the traps with respect to the conduction band of insulator.

3) Thin insulator with or without traps.

The current for the case of thin or thick insulator is identical and given by:

$$J = q.N_c.\mu.\exp\left(-\frac{\Phi_o}{kT}\right).\exp\left(\frac{\beta_{PF}}{kT}.\xi^{1/2}\right).\xi \qquad (3.9)$$

In all cases, the quantity $\ln(J/\xi)$ varies linearly with $\xi^{1/2}$.

3.5. THE HOPPING CURRENT.

In the case of hopping conduction, the energy of the electron is inferior to the maximum energy of the potential energy barrier between two sites. The electrons can still transit using the tunnelling effect. The hopping current can be derived, using the following equation:

$$J = \frac{q^2}{kT}.n^*.\Gamma_s.a^2.\xi \qquad (3.10)$$

where n^* is the electron density on the sites, a is the distance between two sites, and Γ_s is the hopping frequency and is given by:

$$\Gamma_s = \frac{1}{\tau_o}.\exp\left(\frac{-4\pi m^*}{h}.\Phi_m.a\right) \qquad (3.11)$$

where τ_o is a time constant and Φ_m is the energy corresponding to maximum barrier (the other symbols have their usual meanings).

The corresponding current comes out to be:

$$J = \frac{q^2}{kT}.\frac{a^2}{\tau_o}.n^*.\xi.\exp\left(\frac{-4\pi m^2}{h}.\Phi_m.a\right) \qquad (3.12)$$

When the insulator contains no traps, the hopping conduction does not depend on temperature. When the insulator contains traps, the conduction depends strongly on temperature. In any case, the current J is always proportional to bias.

3.6. THE SPACE CHARGE-LIMITED CURRENT.

In the case of Poole-Frenkel and hopping conductions, the electric field is assumed constant. When the electron injection is strong, this hypothesis is no more valid and the potential distribution should be calculated using Poisson's equation. The space charge current results from a carrier injection into the insulator where no compensating charge is present. This current has different expressions for different injections.

1) Very weak injection.

When the injection is very weak, the insulator charge density is nil and the electric field is therefore constant. This ohmic mode occurs as long as the insulator is electrically quasi-neutral, i.e, as long as all donor centers are not filled. The current is then given by:

$$J = q.n(x).\mu.\frac{V}{t_i} \qquad (3.13)$$

where n(x) is the number of conduction electrons, t_i the insulator thickness, and V the applied bias.

2) Strong injection.

In case of strong injection, the insulator traps fill up and a space charge appears. The current is then given [35] by:

$$J = \frac{9}{8}.\mu\frac{\epsilon_i.\epsilon_o}{t_i^3}.\theta.V^2 \qquad (3.14)$$

where

$$\theta = \frac{N_C}{N_D}.\exp\left(-\frac{\Phi_t}{kT}\right) \qquad (3.15)$$

with N_t is the trap density, N_C the density of states in conduction band, and Φ_t the energy difference between the conduction band and trapping site.

3) Very strong injection.

In this case, all traps being filled the space charge is due to conduction electrons and the current is given by:

$$J = \frac{9}{8}.\mu.\frac{\epsilon_i.\epsilon_o}{t_i^3}.V^2 \qquad (3.16)$$

At low voltage and high temperature, current is carried by thermally excited electrons hopping from one isolated state to another. This mechanism yields an ohmic characteristic exponentially dependent on temperature.

3.7. OTHER TYPES OF CONDUCTION.

The ionic conduction is similar to a diffusion process. Generally the dc ionic conductivity decreases during the time the electric field is applied, since ions can not be readily injected or extracted from the insulator. After an initial current flow, positive and negative space charges will build up near the metal-insulator and the semiconductor-insulator interfaces. This causes a distortion of the potential distribution. When the applied field is removed large internal fields remain, which cause some, but not all of the ions to flow back toward their equilibrium position, thus resulting in a hysteresis effects. The ionic current is proportional to $E.T^{-1}.\exp(-\Delta E_{ai}/kT)$ where ΔE_{ai} is

the ion activation energy, E is the electric field, and T is the temperature in K degree.

The ohmic conduction is basically identical to the ionic conduction except that the ohmic current resulting from the ohmic conduction increases with temperature. Whereas in ionic conduction, the ionic current decreases drastically with increase of temperature. The ohmic current in insulators is always referred to as leakage current. The ohmic current is found to be proportional to $E.\exp(-\Delta E_{ae}/kT)$ where ΔE_{ae} is the electron activation energy.

The hot carrier conduction phenomenon occurs under special condition and in particular devices. This type of conduction is encountered in MOSFETs; when the channel is under the action of a high field, the hot carriers originating from the drain moving towards the source or vice versa can tunnel through the oxide or go to the substrate where they recombine. This results in a gate to substrate current that flows through the oxide. The gate and substrate current are not usually equal [37-38]. There is no standard formula expressing hot carrier currents in terms of insulator parameters.

For a given insulator, each conduction process may dominate in a certain range of temperature and bias. The tunnel emission has the strongest dependence on the applied

voltage and the shottky emission has the strongest dependence on the temperature. The space charge limited process is dependent on temperature but shows quite an important dependence on the applied gate voltage. The Poole-Frenkel process is important at moderate temperature and field. The ohmic and ionic conduction processes are of less importance among the above described phenomena however, the ionic process is severely affected by high temperature. The hopping process shows the same dependence on temperature and voltage as the ionic process. The hot carrier process occurs only at very high field and or temperature. The processes are not also exactly independent of one another and should be carefully examined. For example, for the large space-charge effect, the tunnelling characteristic is found to be similar to the Shottky-type emission [39].

Basic Conduction Processes in Insulators.

Conduction Mode	Expression of current	Dependence on temperature and field
Schottky	$4\pi m^* q \frac{k^2T^2}{h^3}\left(1-\exp\left(-\frac{V}{kT}\right)\right).\exp\left(-\frac{\Phi_m-\xi}{kT}\right)$	$T^2\exp\left(a.\frac{V^{1/2}}{T}\right)$
Tunnelling	$\frac{q^2}{8\pi h}\frac{V^2}{t_i\Phi_o}\exp\left(-\frac{2}{3}\alpha^* t_i\frac{\Phi_o^{3/2}}{V}\right)$	$V^2\exp\left(-\frac{b}{V}\right)$
Poole-Frenkel	$qN_c\mu\exp\left(-\frac{\Phi_o}{kT}\right)\exp\left(\frac{\beta_{PF}}{kT}\xi^{1/2}\right)\xi$	$V\exp\left(2a\frac{V^{1/2}}{T}\right)$
Space charge limited	$\frac{9}{8}.\mu\frac{\epsilon_i.\epsilon_o}{t_i^3}.V^2$	$c.V^2$
Ohmic	$A.E.\exp\left(-\frac{\Delta E_{ae}}{kT}\right)$	$V\exp\left(-\frac{d}{T}\right)$
Ionic	$B.\frac{E}{T}\exp\left(-\frac{\Delta E_{ai}}{kT}\right)$	$\frac{V}{T}\exp\left(-\frac{f}{T}\right)$
Hot-carrier	No standard known formula.	Increases with field and temperature

All symbols have their previous meanings. The constants a, b, c, d, and f are positive and independent of temperature and field. A and B are constants.

THE SUBSTRATE CURRENT STUDIED BY THE CHARGE PUMPING TECHNIQUE

The charge-pumping phenomenon is one of the chief sources which can give rise to the substrate current in MOS transistors. As the present study is also based on the measurement of the substrate current which is supposed to arise due to the same process of charging and discharging of the surface states as used in the charge pumping, the present technique may be supposed to be an alternative approach to charge pumping technique. Therefore, a thorough study of the charge pumping current is necessary to understand the different physical phenomena related to the generation of substrate current.

4.1. INTRODUCTION.

Since the existence of the surface states at the silicon-silicon dioxide interface was demonstrated, several techniques have been proposed for the determination of the density of these states and of their energy distribution in the forbidden energy band gap of silicon. Most of these techniques are based on measurements on MOS capacitor [13-22] and have been studied in great details. Consequently they have became sufficiently reliable to be used in most laboratories. For the determination of the surface state density on MOS transistors only a few techniques are reliable. However, they are not commonly used, partly because of poor quantitative reliability and partly because they are not very practical to use. Therefore, none of these techniques can be qualified as generally accepted for MOS transistors.

Recently, a new method called charge-pumping technique is developed to characterize MOS transistors. The charge pumping technique was evidenced by Brugler and Jespers in 1969. They have shown [23] that repetitive gate pulses of magnitude sufficient to invert the conductivity type in the channel of a MOS transistor can stimulate a net flow of majority carriers from the source and drain to the substrate. This current is observed as a dc substrate current.

The charge pumping technique is based on the recombination process at the silicon-silicon dioxide (Si-SiO_2) interface involving the surface states. This induces a substrate current which can be related to the surface states density. In spite of its capability for measurements on small area MOS transistors, it never became a standard technique because of some ill-understood phenomena which made the method qualitative rather than quantitative.

4.2. THE CHARGE PUMPING TECHNIQUE.

In a MOSFET, there exists a possibility of charging and discharging the surface states with carriers originating from the drain and source terminals of the device. This phenomenon can occur under the effect of a train of gate voltage pulses which charge and discharge the surface states provided that the amplitude of these pulses is such that their bottom (base) level is within the deep accumulation region and their top level is within the inversion region. This produces a dc current that is detected at the substrate. This current is found to have a direction opposite to that of the transistor's p-n junctions leakage currents.

4.2.1 Basic Principles of The Charge Pumping Technique.

The experimental set up used in the charge pumping method was first described by Brugler and Jespers [23]. It

is illustrated in Fig.4.1a. To an n-channel MOS transistor, a gate voltage signal of amplitude such that it can sweep the energy interval from the deep accumulation to the deep inversion is applied. The drain and source are short-circuited together and connected to a dc reverse-biasing voltage source. The substrate is connected to the ground through a dc picoammeter which measures the resulting charge pumping current.

4.2.2 Theory of The Charge Pumping Technique.

When a transistor is pulsed into inversion, the surface region becomes deeply depleted and electrons will flow from the source and drain regions into the channel where some of them will be captured by the surface states. When the gate pulse is driving the surface back into accumulation, the mobile charges drift back to the source and drain under the influence of the reverse bias, but the charges trapped in the surface states will recombine with the majority carriers from the substrate and give rise to a net flow of negative charges into the substrate. The charge Q_{ss} that will recombine is given by:

$$Q_{ss} = A_g . q . \int D_{it}(E) dE . \qquad (4.1)$$

It can also be expressed as

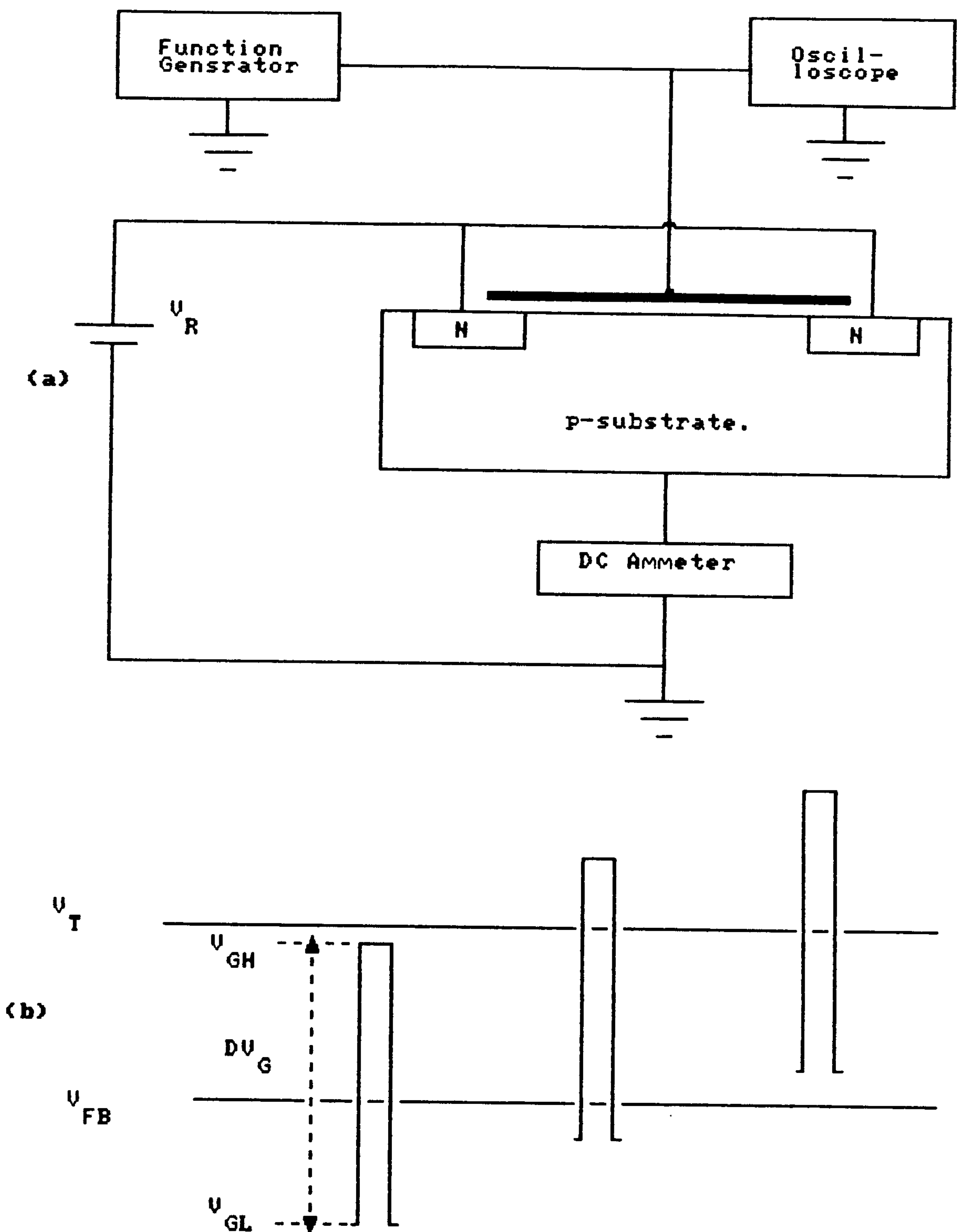


Fig.4.1 (a) Basic experimental set-up for charge pumping measurements.
(b) Illustration of the base level method on an n-channel MOSFET.

$$Q_{ss} = A_g . q^2 . \overline{D_{it}} \Delta \Psi_s \qquad (4.2)$$

where:

-A_g is the area of the channel of the MOSFET (Cm^2).

-q is the electron charge (C),

-$\Delta\Psi_s$ is the total sweep of the surface potential V,

-$\overline{D_{it}}$ is mean surface state density averaged over the energy level swept by the Fermi-level Cm^{-2} eV^{-1}).

-$D_{it}(E)$ is the surface density of state at energy E.

When applying repetitive pulses to the gate with frequency f, this charge Q_{ss} will give rise to a current in the substrate. This current can be written as:

$$I_{cp} = f . Q_{ss} = f . A_g . q^2 . D_{it} . \Delta \Psi_s \qquad (4.3)$$

By measuring this substrate current, an estimate of the mean capture cross-section and the interface-states density over the energy range swept by the gate pulse can be obtained. However, this substrate current is found to consist of two components, the surface states component and the geometric component. The geometric component is an undesirable effect. Brugler [23] concluded that to eliminate this undesirable component of the current, the experimental device should show a ratio of the length (L) and the width (W) larger than unity (W/L >> 1).

4.2.3 Techniques of Sweeping The Surface Potential.

The charge pumping measurements have been performed in different manner. All of these measurement methods are based upon the way of applying the gate voltage signal to the MOS transistor. The most commonly used methods are listed below :

1. keeping the pulse base level in accumulation and pulsing the surface into inversion with increasing amplitude [23].

2. varying the pulse base level from inversion to accumulation while keeping the amplitude of the pulse constant [25] as illustrated in Fig.4.1b.

3. keeping the pulse base level in accumulation and pulsing the surface into inversion with a sufficient amplitude. However, the pulse base level does not reach the accumulation level while coming back from the inversion region. It goes through an intermediate position which is referred to as a step voltage before reaching the accumulation region [29].

4. keeping the pulse base level between the flatband voltage and the threshold voltage and pulsing the surface into inversion and then into accumulation alternately [32].

In the first method, a saturation level of the charge pumping current is expected when the top of the gate pulse exceeds the threshold voltage of the MOS transistor. This saturation value is reached when the surface potential

sweep $\Delta\Psi_s$ reaches its maximum value. However, this saturation value, beside the surface potential, depends on the value of the reverse biasing voltage V_R.

In the second method, the charge pumping current is found to be very small when the gate pulse is less than the flatband voltage V_{FB} or greater than the threshold voltage V_T. The maximum value of the current is obtained when the pulse amplitude ΔV_G is greater than the value $|V_{FB}-V_T|$ and the amplitude of the pulse is such that its base level is below the flatband voltage V_{FB} and its top level is beyond the threshold V_T while the reverse biasing voltage V_R is equal to zero. This method allows the complete sweep of the surface potential.

The third method provides the knowledge, which of the surface states act as traps and which as recombination centers. It is also used to measure the surface states at the Si-SiO_2 interface.

The last method, called modified charge pumping technique or interface probing, enables uninterrupted scanning of bandgap and provides the mean value of capture cross section of the carriers. It also allows an experimental characterization of the distribution of capture cross section and elimination of a number of potentially distorting effects associated with the original charge pumping technique.

4.3. THE IDEA OF EMISSION OF CARRIERS FROM THE SURFACE STATES.

The idea of carrier emission was introduced by Groeseneken et al [27]. It is based on the emission theory described by Simmons and Wei [40-41].

When a transistor is switched from accumulation towards inversion and vice versa, the state of the channel goes through three different modes each of which can be characterized by a different time constant and essentially corresponds to one of the conventional operating regions of the MOS structure (i.e., accumulation, depletion, and inversion). For the sake of simplicity, let us consider an n-channel transistor. A gate signal of a given fall and rise times and known amplitude and frequency is applied to the gate of a MOSFET. When the surface region is in accumulation, all of the surface-states below the quasi-Fermi level of the minority carriers are filled with electrons, while those above it are empty. The states are thus in equilibrium with the energy bands. When the gate voltage increases (starting from deep accumulation to deep inversion), the surface potential is changing at a certain rate. Therefore, holes that have to be emitted from the surface states towards the valence band in order to maintain equilibrium, will flow back to the substrate. Initially, the rate of emission of trapped charge is able to meet the one

that is required to keep the trap occupation in dynamic equilibrium with the voltage sweep. The channel is in the steady state condition as long as [40] the rate of change of the trapped charge density required to maintain steady state condition is greater than the real rate of the change of trapped charge density as imposed by the emission of holes to the valence band. As soon as this rate of change of trapped charges imposed by the emission process becomes smaller than the one required by the voltage sweep at the gate, the channel enters the non-steady state regime and the emptying of the traps is completely controlled by the emission process described by Simmons and Wei [40] and Kaden and Reimer [42]. The transition from the non-steady state to the steady state occurs at a certain gate voltage correspon-ding to the flatband voltage V_{FB}. The surface potential sweeps very fast from the flatband position to the strong inversion through the depletion region. In this depletion region, the concentration of carriers is very small. There-fore, the time constant is only controlled by that of the hole emission. Because of this high rate of change of the surface potential, the steady state condition will cease very shortly after reaching the flatband conditions and hence, starting from the flatband voltage the channel is in the non-steady state regime. When the gate voltage is near the threshold voltage V_T, the trapping time constant is approximately given by [23]:

$$\tau_t = \frac{1}{V_{th}\sigma_n n_s} \tag{4.4}$$

where n_s is the surface concentration of minority carriers, V_{th} is the thermal velocity of carriers, and σ_n is the capture cross section of electrons. This time constant becomes gradually smaller and consequently, electrons will be trapped by the surface states not yet emptied. This process will become important when the gate voltage exceeds the threshold voltage. At this time, the electrons coming from the drain and source junctions will fill the remaining traps. The same mechanisms operate when the gate is pulsed back to accumulation.

It has been found [27] that, during the voltage sweep from accumulation to inversion and vice versa, a steady state is followed by a non-steady state emission of carriers. During the total sweep from deep accumulation to deep inversion while assuming the average density $\overline{D_{it}}$ of the surface states constant, four currents that are shown in Fig.4.3a have been observed. These currents are:

$$I_1 = -A_g q^2 f \overline{D_{it}} \Delta\Psi_e \tag{4.5}$$

$$I_2 = A_g q^2 f \overline{D_{it}} \Delta\Psi_{ee} \tag{4.6}$$

$$I_3 = -A_g q^2 f \overline{D_{it}} \Delta\Psi_h \tag{4.7}$$

$$I_4 = A_g q^2 f \overline{D_{it}} \Delta\Psi_{he} \tag{4.8}$$

The net charge pumping current measured at the substrate is:

$$I_{cp} = I_3 + I_4 = A_g q^2 f \overline{D_{it}} (\Delta\Psi_{he} - \Delta\Psi_h) \tag{4.9}$$

and the source/drain current is:

$$I_{S/D} = I_1 + I_2 = A_g q^2 f \overline{D_{it}} (\Delta\Psi_{ee} - \Delta\Psi_e) \tag{4.10}$$

Simmons and Wei [41] found that the emission levels of surface states for electrons are :

$$E_{em,e} - E_i = -kT \ln\left(V_{th}\sigma_n n_i t_{em,e} + \exp\left(\frac{E_i - E_{F,inv}}{kT} \right)\right), \tag{4.11}$$

and for holes:

$$E_{em,h} - E_i = kT\, ln\left(V_{th}\sigma_h n_i t_{em,h} + \exp\left(\frac{E_{F,acc.} - E_i}{kT} \right)\right) \tag{4.12}$$

where $t_{em,e}$ and $t_{em,h}$ are respectively the non-steady state emission times of electrons and holes and the exponential terms are introduced to account for the case when the emission levels are situated closer to the band edges than to the quasi-Fermi levels. Groeseneken et al showed [27] that the emission times of the electrons and holes can be expressed respectively as:

$$t_{em,e} = \frac{|V_{FB} - V_T|}{|\Delta V_G|} t_f , \qquad (4.13)$$

$$t_{em,h} = \frac{|V_{FB} - V_T|}{|\Delta V_G|} t_r \qquad (4.14)$$

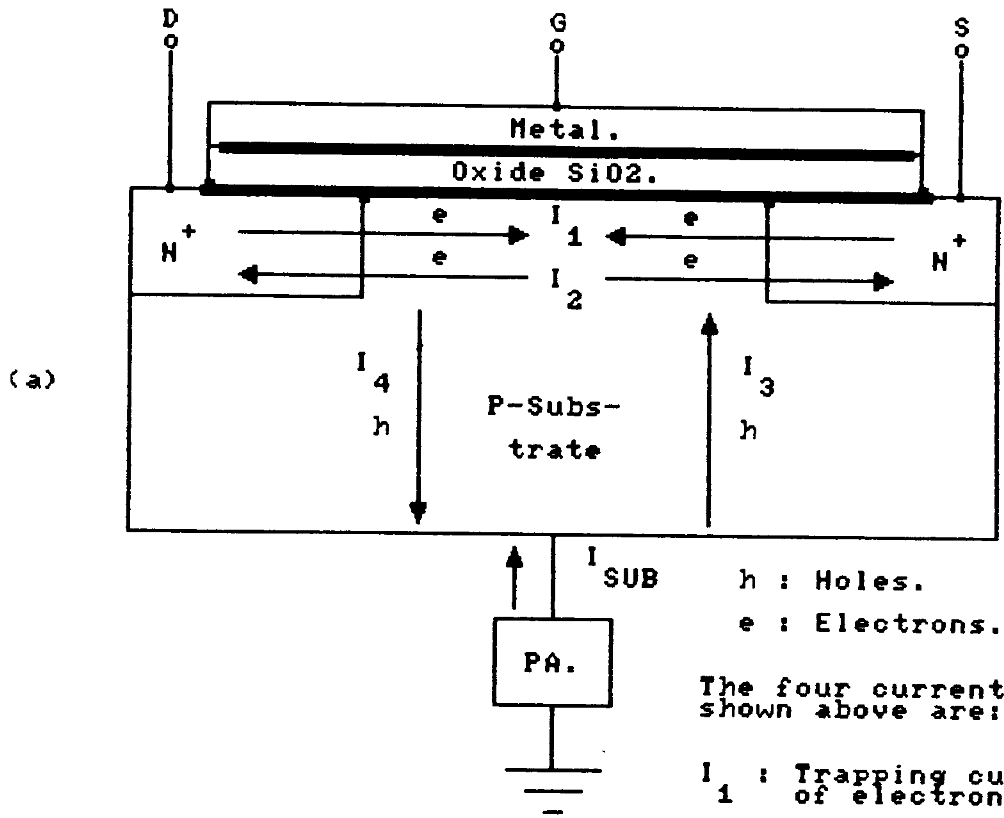
for square pulses and:

$$t_{em,e} = \frac{|V_{FB} - V_T|}{|\Delta V_G|} . \frac{1}{f} . \alpha \qquad (4.15)$$

$$t_{em,h} = \frac{|V_{FB} - V_T|}{|\Delta V_G|} . \frac{1}{f} . (1 - \alpha) \qquad (4.16)$$

for triangular pulses.

Where V_{FB} is the flat band voltage, V_T the threshold voltage, ΔV_G the amplitude of the pulse, t_r and t_f the fall and rise times of the pulses as shown in Fig.4.2b, f the frequency of the signal, and α the fraction of the pulse when it is rising.



The four currents shown above are:

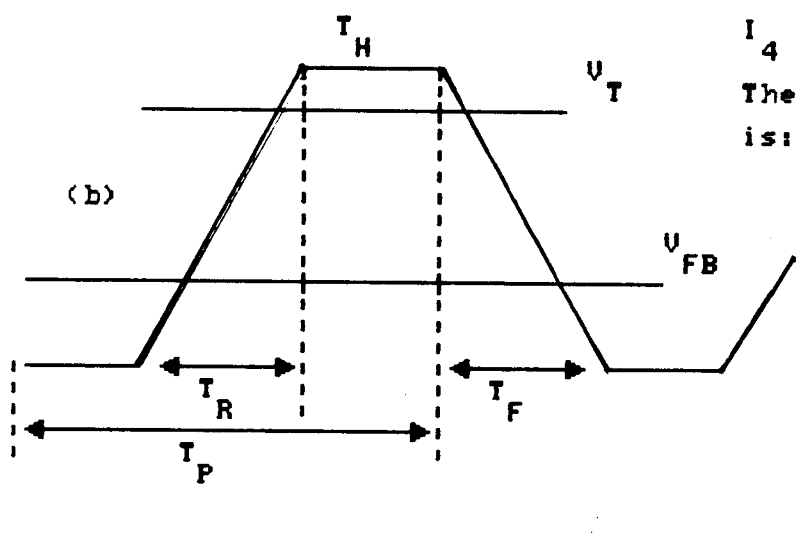
I_1 : Trapping current of electrons.

I_2 : emission current of electrons.

I_3 : Trapping current of holes.

I_4 : Emission current of holes.

The measured current is: $I_{SUB} = I_3 + I_4$



T_F : Fall time.

T_R : Rise time.

T_H : Hold time.

T_P : Period time.

V_T : Threshold voltage.

V_{FB} : Flatband voltage.

Fig.4.2 (a) Different currents generated under charge pumping effect.
(b) Gate pulse shape applied to the MOSFET.

The charge pumping current obtained after manipulating Eq.(4.2) using the Eqs.(4.11), (4.12), (4.13), (4.14), (4.15), and (4.16) is found to be:

$$I_{cp} = 2qf\overline{D_{it}}A_g.kT.[\ln(V_{th}.n_i.\sqrt{\sigma_h\sigma_n}) + \ln\left(\frac{|V_{FB}-V_T|}{|\Delta V_G|}.\sqrt{t_f t_r}\right)] \quad (4.17)$$

for square pulses and by:

$$I_{cp} = 2qf\overline{D_{it}}A_g kT[\ln(V_{th}.n_i.\sqrt{\sigma_h\sigma_n}) + \ln\left(\frac{|V_{FB}-V_T|}{|\Delta V_G|}.\frac{1}{f}\sqrt{\alpha(1-\alpha)}\right)] \quad (4.18)$$

for triangular pulses.

At higher frequencies, the charge pumping current is found to vary in a non linear manner with respect to frequency. Hence the previous formulae are not valid, even though they do not show any ambiguity or do not have any of their terms adversely affected by very high frequencies. Groeseneken et al explained this phenomena based on the surface states response time. The surface states need a certain time to capture the carriers present in the channel and hence, the linearity of the I_{cp} versus f curves is valid upto the stage

where the inversion time becomes smaller than the trapping time constant of the surface states. At this stage, the surface states will no longer be completely filled and the charge pumping current decreases as it is shown in Fig.4.3.

4.4. EFFECT OF THE FREQUENCY ON THE CHARGE PUMPING CURRENT.

The charge pumping current [given by Eq.(4.2)] is directly proportional to frequency. This is due to the fact that, the charge pumping current is the result of the charges produced under the effect of a gate signal. When a gate pulse is applied to the gate of a MOSFET, the charges are produced in each cycle and the electric current is constituted by the charges of all cycles in one second which explains the proportionality of the current to frequency. Figure 4.3 illustrates the dependence of the charge pumping current on the frequency. This current is not only affected by the frequency, but also by the shape of the gate signal.

Groeseneken et al found that the linear dependence of the current on frequency is due to the constant fall and rise times of the gate pulse. This gives a constant amount of emitted charge per cycle or a constant amount of the recombining charge per cycle. However, for triangular pulses the frequency dependent fall and rise times give rise to a frequency dependent emitted charge and therefore, to a frequency dependent charge recombining with the substrate

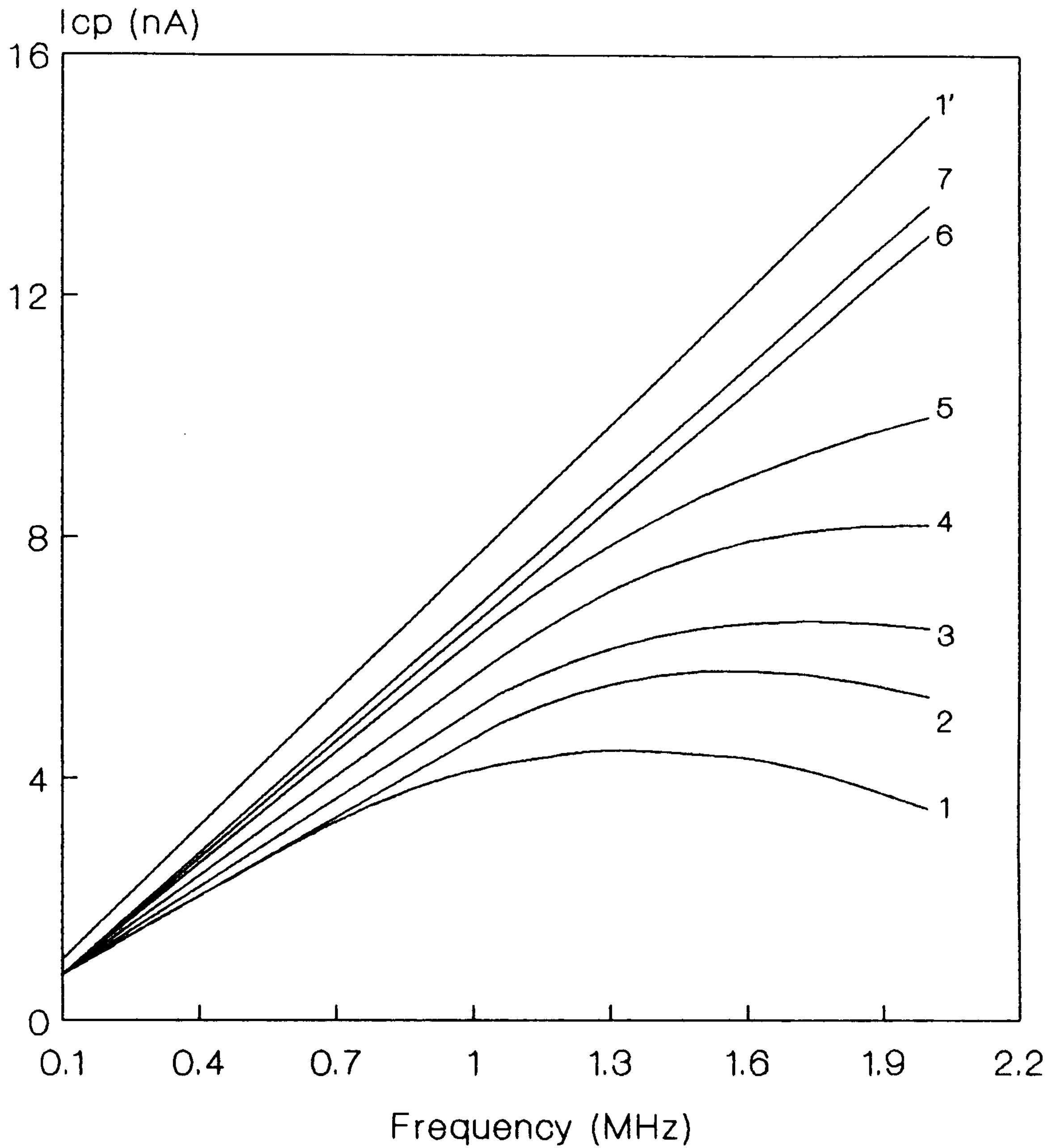


Fig.4.3 Charge pumping current versus frequency. Curve 1' is for square pulses; curves 1 to 7 are for triangular pulses with Vgh increasing from Vt (cur.1) to Vt+4 V (cur.7). Influence of trapping time constant. (After [27]).

majority carriers as expressed by Eq.(4.18). This charge-frequency dependence is used to determine some transistor (MOSFETs) parameters.

4.4.1. Determination of capture cross-section of carriers.

A train of triangular pulses of 15% rise and 85% fall times (or a sawtooth signal shape) is applied to the gate of a MOSFET with the source/drain connected to a reverse biasing voltage. The charge per cycle is measured and plotted with respect to frequency on a semilogarithmic plot. The variation of the amount of charge is found to be linear with respect to logarithmic variation of frequency and is given by:

$$Q_{ss} = \frac{I_{cp}}{f} \tag{4.19}$$

Replacing I_{cp} by its expression given by Eq.(4.18), the charge Q_{ss} becomes:

$$Q_{ss} = 2qA_g\overline{D_{it}}kT[\ln(V_{th}.n_i\sqrt{\sigma_h\sigma_n}) + \ln\left(\frac{|V_{FB}-V_T|}{|\Delta V_g|}.\frac{1}{f}.\sqrt{\alpha(1-\alpha)}\right)] \tag{4.20}$$

The extrapolation of the curve Q_{ss} versus $log(f)$ to the zero value of the charge gives a certain frequency f_o which can

be used to obtain the value of the geometrical mean capture cross section. It is obtained by solving Eq.(4.20) for $Q_{ss}=0$ so that:

$$\sqrt{\sigma_h \sigma_n} = \frac{1}{V_{th}.n_i} \cdot \frac{|\Delta V_G|}{|V_{FB} - V_T|} \cdot \frac{f_o}{\sqrt{\alpha(1-\alpha)}} \qquad (4.21)$$

4.4.2. Determination of The Average Density Distribution of The Surface States.

The slope of the Q_{ss} versus *log(f)* curve ,shown by Fig.4.4 and described by Eq.(4.20), is found to be:

$$\frac{dQ_{ss}}{dlog(f)} = \frac{2.q.kT.\overline{D_{it}}}{\log(e)}.A_g \qquad (4.22)$$

Equation (4.22) allows the determination of the average density of the surface states which is given by:

$$\overline{D_{it}} = \frac{dQ_{ss}}{d\log(f)} \cdot \frac{\log(e)}{2.q.kT.A_g} \qquad (4.23)$$

The value of the average density $\overline{D_{it}}$ so obtained by Groeseneken et al comes out to be in the range of the known values of their experimental devices. However the values of

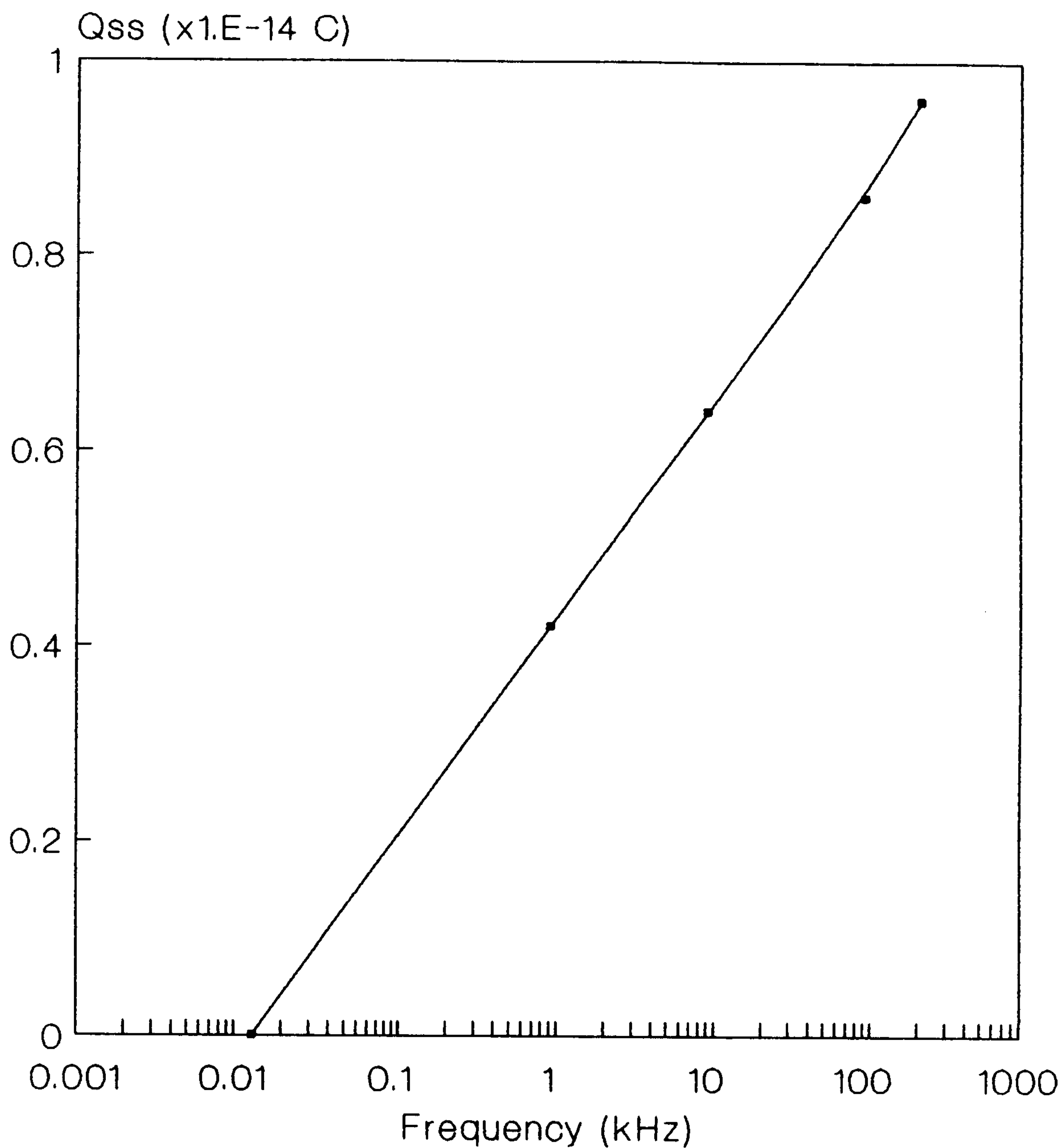


Fig.4.4 Qss verus frequency used to determine the capture cross section and the average density distribution of surface-states. (After [27]).

the capture cross sections as obtained previously by Nicollian [16],[22] are not in a good agreement compared to that obtained by the charge pumping method. This disagreement may be due to the fact that Groeseneken et al introduced the idea of the geometrical mean capture cross section of carriers, which necessitates the use of electrons as well as holes capture cross sections in the same material whereas commonly it is assumed that a p-type semiconductor is characterized by the hole capture cross section (σ_h) and an n-type by (σ_n).

The charge pumping method, which has become a conventional technique for the study of interface properties in MOSFETs, has been extensively used and several modified versions have been developed by different workers [28-34].

EXPERIMENTAL SET-UP AND DEVICES

The present study was commenced primarily with the same experimentation as used in the conventional charge pumping technique with the aim to verify the earlier results. During the above study, certain theoretical considerations and reasoning led to the development of a new technique and experimentation. However, the basic experimental set-up remains essentially the same as used in the charge pumping technique which is described in this chapter.

5.1. THE EXPERIMENTAL DEVICES.

The devices used in the experiments are two types: a) Commercial devices and b) special devices in wafer-form fabricated for this project.

5.1.1. The Commercial Devices.

The commercial devices used are the standard MOS transistors having the reference 3N 170. They are manufactured by the National Semiconductor Company USA. The 3N 170 MOSFETs are four terminal devices having isolated drain, source, gate, and substrate. Among the device parameters, only the threshold voltage is known.

5.1.2. The Wafers.

The devices in the form of wafers are manufactured by the ES2 (European Silicon Structures, France) laboratory via the CDTA (Centre de Developement des Technologies Avancees, Algerie) research center. Figures 5.1 and 5.2 show different sets of devices manufactured. The devices shown in Fig.5.1 are manufactured using the 1.2 μm *CMOS* technology and those shown in Fig.5.2 are manufactured using the 2 μm *CMOS* technology. The wafers consist of MOS transistors and MOS diodes of different dimensions. However, the value of the doping concentration and the oxide thickness is the same in all the

wafers. Figure 5.1 shows wafers consisting of sets of transistors having the source, the gate, and the substrate common. There are two series of transistors of the same dimensions, one series is an n-channel and the other is a p-channel transistors. Figure 5.2 shows wafers consisting of transistors that are five terminal devices, having isolated gate, substrate, drain, source, and well. Each terminal is independently accessible. The transistors are n-channel. In addition, there are some capacitors that are build in the n-type substrate. Some of these wafers are encapsulated in a 64 PGA package to allow their use without the help of microscope-prober. The wafers of Fig.5.1 are used in the first stage experiments meant for the observation of the physical phenomena. Devices shown in Fig.5.2 are used for experiments carried out to analyse the physical phenomena. These devices are fabricated according to the requirements of the present experiment. Table 5.1 gives the dimensions and data of these wafers.

5.2. THE BASIC EQUIPMENTS.

The capital equipment used in the present experiment includes the following:

5.2.1. The Picoammeter.

The picoammeter that has been used is the HP 4140B,

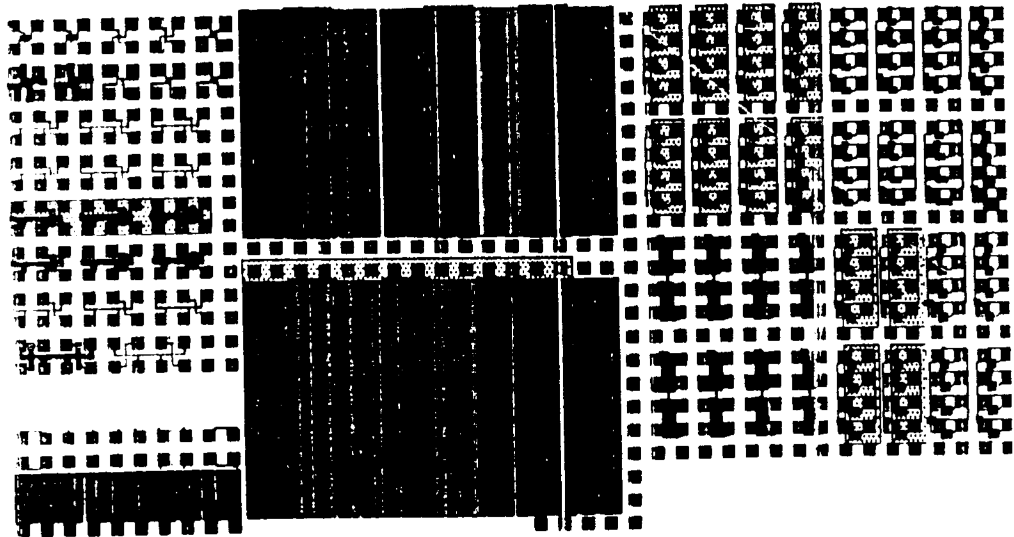


Fig.5.1a. General view of the 1.2 um process technology wafer.

(After ES2 Laboratory).

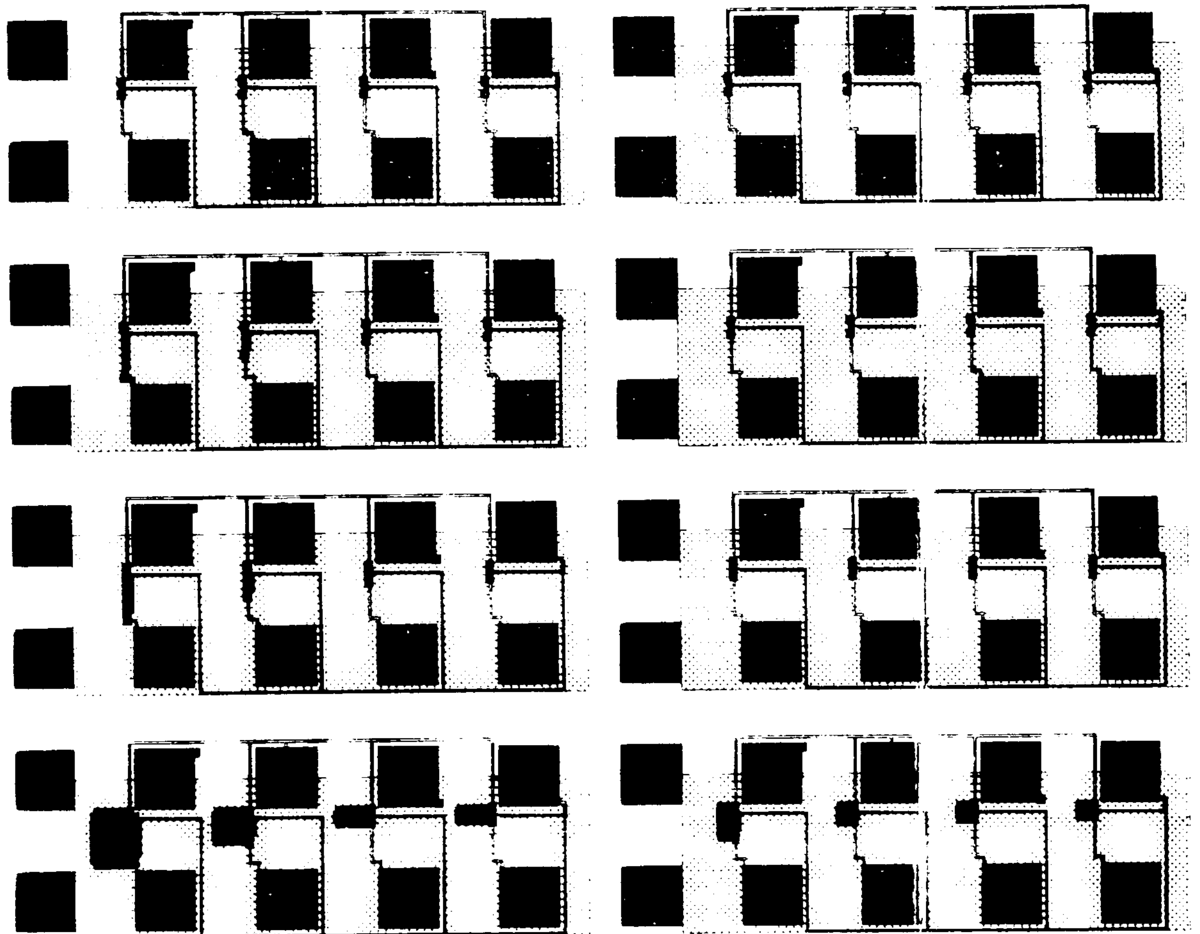


Fig.5.1b. MOS transistors included in the 1.2 um process technology wafers.
(After ES2 Laboratory).

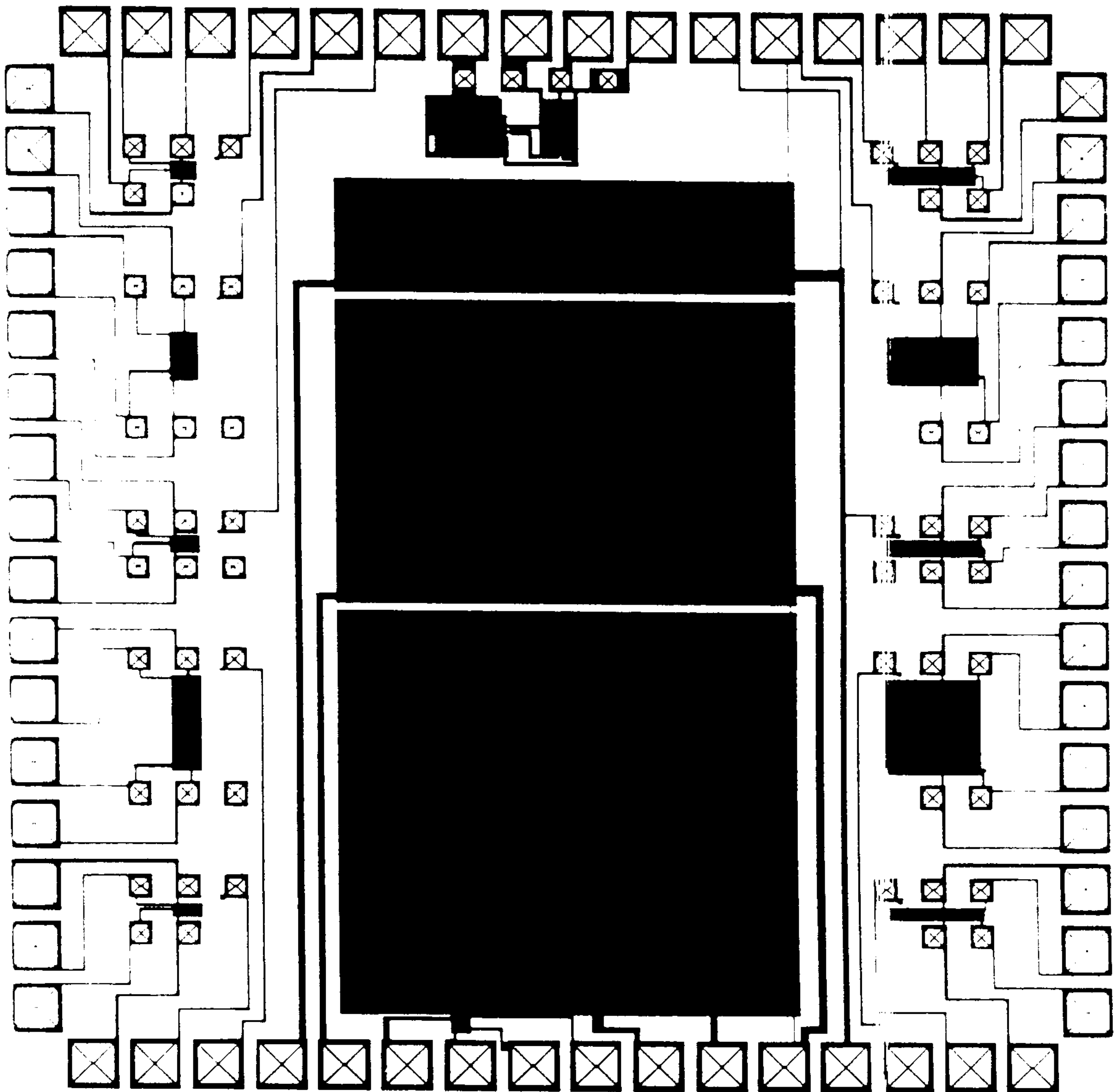


Fig.5.2 Wafers manufactured using the 2um process technology.
(After ES2 Laboratory).

it has a sensitivity of 0.001 pA. It has been used in earlier experiments [43] where required information involve current value of the order of 0.025 pA.
The HP 4140B is provided with two dc voltage sources: The first (V_A) is programmable and can supply variable voltages from -20 to 20 Volts either in a ramp function or stairs function increment. The second source (V_B) is a variable output source and supplies a constant voltage of different values ranging from -100 to +100 V. In addition, it can serve for the low frequency C-V measurements where the capacitance is measured to the 0.001 pF sensitivity or as a percentage of a normalized capacitance of known normalizing capacitance value. The input channel of the current is followed internally by a filter that filters out the incoming noise. The HP 4140B is an HP-IB compatible equipment. Programs are supplied to the picoammeter through the corresponding computer.

5.2.2. The Digital Multimeter.

The multimeter used in the present experiment is the universal HP 3478A multimeter. It can measure resistance, current, and voltage. The resistance measurement can be done using two point or four point terminals. The former is used to determine the resistivity and subsequent parameters of

materials used in building integrated circuits. The sensitivity of the instrument is 0.1 milliohm for resistances, 1 microampere for currents, and 1 microvolt for voltages. The multimeter is an HP-IB compatible instrument.

5.2.3. The Frequency Meter.

The frequency of the applied signal is measured with the help of the HP 5325A frequency counter. The instrument measures both the frequency as well as the period of a voltage signal, the sensitivity for frequencies is 1 microhertz and for period 1 nanosecond. The instrument is an HP-IB compatible.

5.2.4. The Function Generator.

Three function generators and one pulse generator are used either individually or in suitable combination to generate the desired signal. The pulse generator is the Tektronix RG. 501 which can generate sawtooth signals of different period and fall and rise times. The function generators are the Tektronix FG 504, the HP 3311A and the Wavetek 180. The first is used to supply a high frequency signal of a maximum frequency equal to 40 Megahertz. The second has the floating ground feature, and is suitable to be used in series with either of the generator to produce a special output. The last function generator is characterized

by its output fine adjustment and the VCO (Voltage Controlled Oscillator) input. It is used to supply a signal of constant amplitude and variable frequency.

5.2.5. The Oscilloscope.

The oscilloscope used in this work is the Tektonix 7603. It has a dual input channel and a sensitivity of 1 millivolt and 0.1 microsecond. It is used to display the shape of the signal and eventually to read its amplitude and period.

5.2.6. The Microscope-Prober.

The wafers can only be used with the help of a microscope-prober which allows an access to the different device terminals. The microscope-prober used is the Karl-Sauss MP 5 prober. It is also HP-IB compatible and can be operated by a computer. The prober movement are controlled automatically. It has 100 probe fix points and a microscope with a variable magnification scale.

5.2.7. The Test-Fixture Box.

The HP 16055A test-fixture box with its corresponding accessories and cables is used. However, the test-fixture allows only the use of encapsulated devices. Devices under test are protected against electromagnetic and light noises when they are mounted within this box.

5.2.8. The HP Computer.

The computer (HP 9836) is used to control the overall setting including all the compatible equipments and instruments. It is used to read data from different measuring equipments and to supply data to the picoammeter for proper functioning. Various softwares have been developed to achieve the above mentioned tasks and to analyse and to output data in the form of plots or data tables. Different current versus voltage (I-V) and current versus frequency (I-f) curves of interest have been plotted on the HP 2631G printer.

5.3. DESCRIPTION OF THE EXPERIMENTAL SET-UP.

The experimental set-up used in the charge-pumping technique is shown in Fig.4.1a (*see chap.4*). For different purposes, the function generator used is the FG 504 for generating high frequency signals and the HP 3311A combined with the sawtooth generator RG 501 to supply sawtooth signal. The latter is used to determine the density of surface-states [27]. The HP 4140B picoammeter, which is used to measure the charge pumping current, is also used to supply a variable output voltage through the programmable source (V_A). This voltage source is used in combination with the HP 3311A generator to generate an oscillating signal of variable base level. This kind of signal is used to sweep

the total surface potential in a MOSFET [25]. The drain and source short-circuited together, are connected to the second source (E_B) of the HP 4140B. The shape of the signal and its position are displayed on the Tek. 7603 oscilloscope.

When the picoammeter is shifted to the gate, during the charge-pumping experiment, an irregular type of current variation has been observed under different experimental conditions. The magnitude of substrate current showed strong dependence on the frequency of the gate voltage signal and this led to the modification of the experimental set-up to study this irregularity of the current variation. Observation of this gate current is indicative of some limitation of the charge pumping technique. Understanding this limitation needs reviewing of the process of charging and discharging of the surface states at the Si-SiO_2 interface when the surface potential is swept from deep accumulation to deep inversion. When the surface potential changes from deep accumulation to deep inversion, the charging and discharging of the surface states can occur under two regimes. One regime is of non-steady state and the other of steady state emission [27]. In all charge pumping techniques the regime of steady state is considered to contribute to charge pumping current whereas regime of non-steady state emission is supposed to contribute zero substrate current. In order to verify whether the regime of non-steady state emission actually contributes or not to substrate current in

the charge pumping technique, it is worthwhile to measure the substrate current when the surface region remains absolutely under the regime of non-steady state emission. Such a condition can be practically obtained by applying the gate voltage signal of such an amplitude that it neither crosses the flatband voltage V_{FB} on one extreme and the threshold voltage V_T one the other. Under such a condition, the surface region is supposed to remain under depletion condition throughout the gate voltage sweep. Further in order to isolate the current of non-steady state emission from that of steady state recombination, it is essential to cut off all possibilities of charges pumped from the drain/source under the steady state recombination. This can be achieved if the substrate current is measured in a MOSFET with open drain/source or in a MOS capacitor under a gate voltage signal swinging within the limits V_{FB} on one extreme and V_T on the other. Accordingly the basic experimental set-up needs a modification. The basic experimental set-up after modification is shown by the general block diagram of Fig.5.3. The equipments used and their interconnection are illustrated in Fig.5.4. The drain and source of the transistor are left open in all the experiments, that is the MOS transistor is used as a MOS capacitor. The main equipment is the HP 4140B which is also used for current measurement and for programmable output

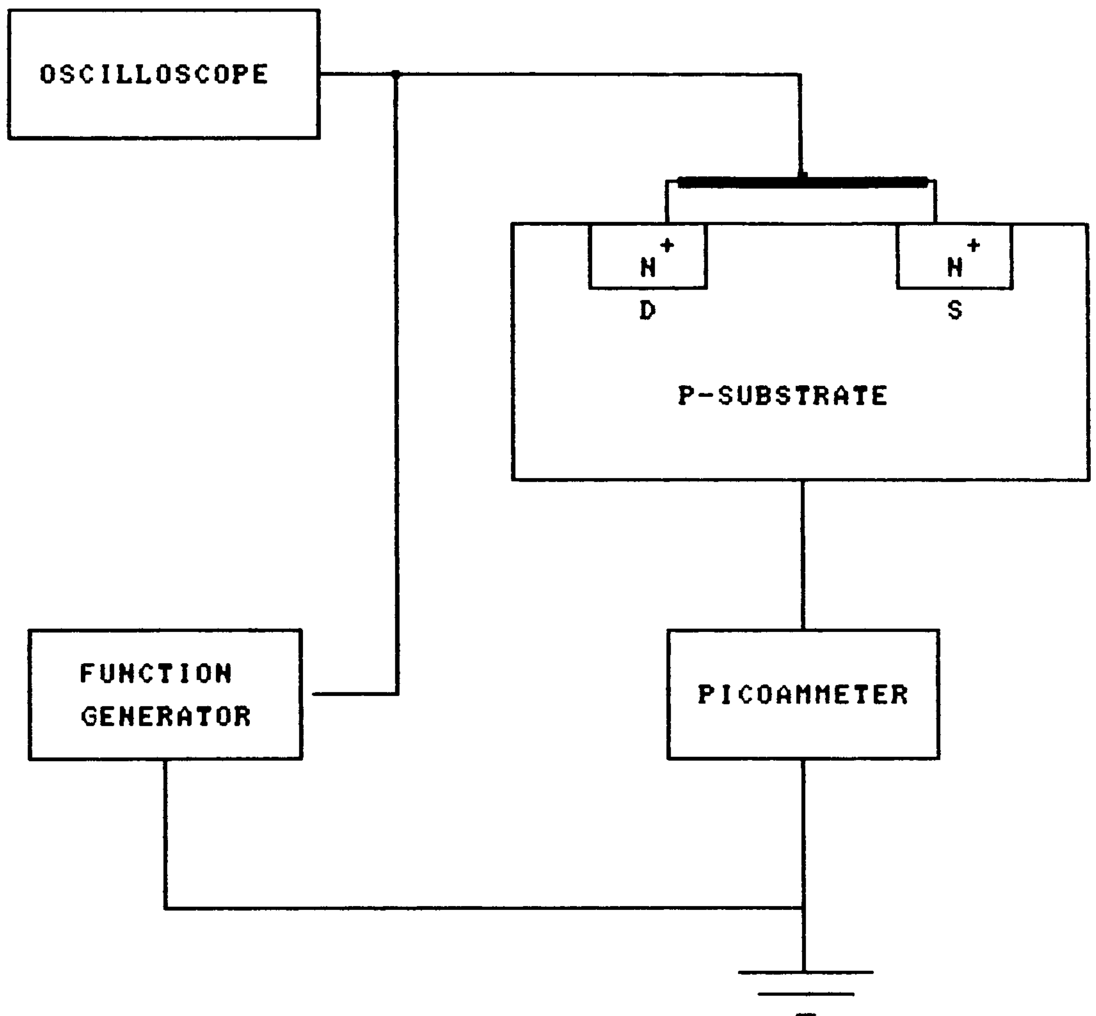


Fig.5.3 General set-up illustrating the principle of the experimental method introduced in the present study.

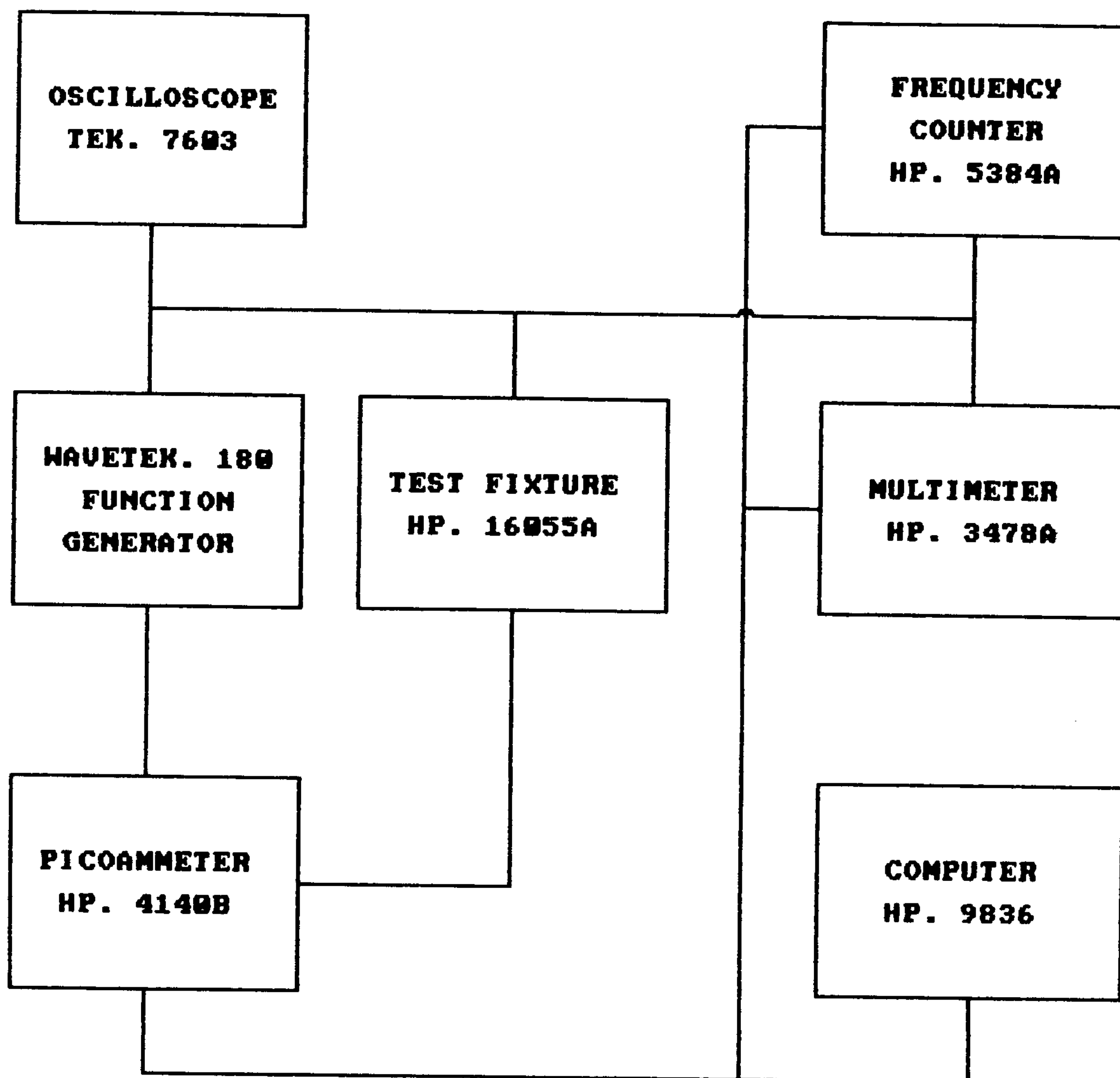


Fig.5.4 Experimental set-up and different equipments used in the present study.

voltage supply. This output voltage is fed to the VCO input of the Wavetek 180 function generator to give a variable frequency signal.

5.4. OPERATING PRINCIPLE OF THE EXPERIMENTAL SET-UP.

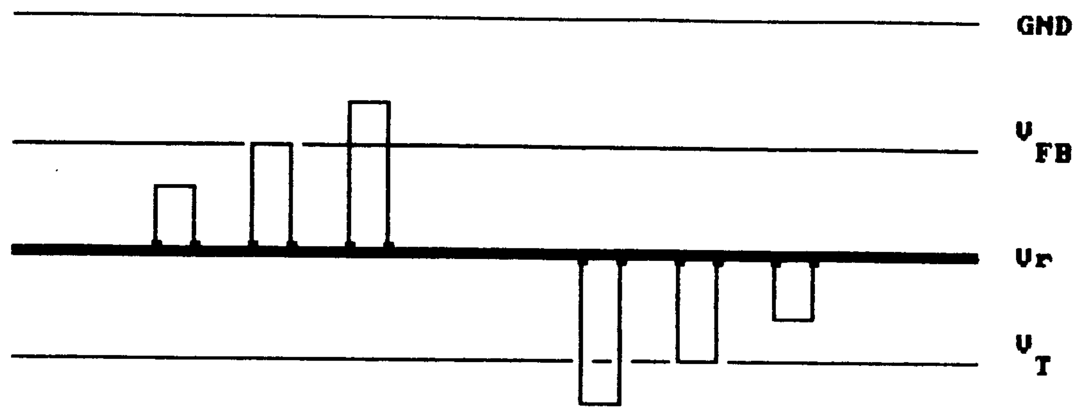
The HP 9836 computer is programmed to coordinate the operation of all the HP compatible equipments used in the experiment. The HP 4140B is programmed to generate a staircase signal of a fixed increment value and delay time. This produces a constant and linear variation of the frequency of the signal generated by the Wavetek 180. The signal frequency is read on the HP 5874A and its amplitude is read on the HP 3478A multimeter. For each VCO increment the frequency, amplitude and the current values are read and stored in the computer that treats them and produce accordingly an output which is either a curve or a data table. To have proper attenuation of the signal amplitude during any increase of frequency to large value, the signal displayed on the oscilloscope is adjusted to its original value through the generator fine adjustment control.

The experimental devices are enclosed in the test fixture box in the case of commercial or incapsulated devices. If the devices are not encapsulated, they have to be used by the help of a microscope-prober and precautions are to be taken to avoid the influence of any external

source capable of inducing or generating any noise. Several software programs have been developed for different versions of the experiments. Each program produces an output either in the form of curves or data tables. Different I-V and I-f curves are drawn accordingly. By varying the experimental conditions, that is, by varying different parameters (amplitude of the signal, position of the signal...), different outputs are obtained.

5.5. DESCRIPTION OF THE EXPERIMENTS.

Basically, three versions of the experiment have been carried out, which will be referred as version 1, version 2, and version 3. In the first version, the voltage signal applied to the gate of the MOS device is varied from the voltage V_r corresponding to the intrinsic level E_i to the flatband voltage V_{FB}. The gate voltage is varied from V_r to V_T, the threshold voltage, for the second version. In the last version, the gate voltage is varied from the flatband voltage V_{FB} to the threshold voltage V_T. For n-type substrate devices, the intrinsic level is found to be negative and corresponds to the value -0.7 V for some devices whereas, for p-type substrate devices, the intrinsic level is found to be around 0.10 V. Figure 5.5 illustrates how the signal is applied to different devices of different substrates.



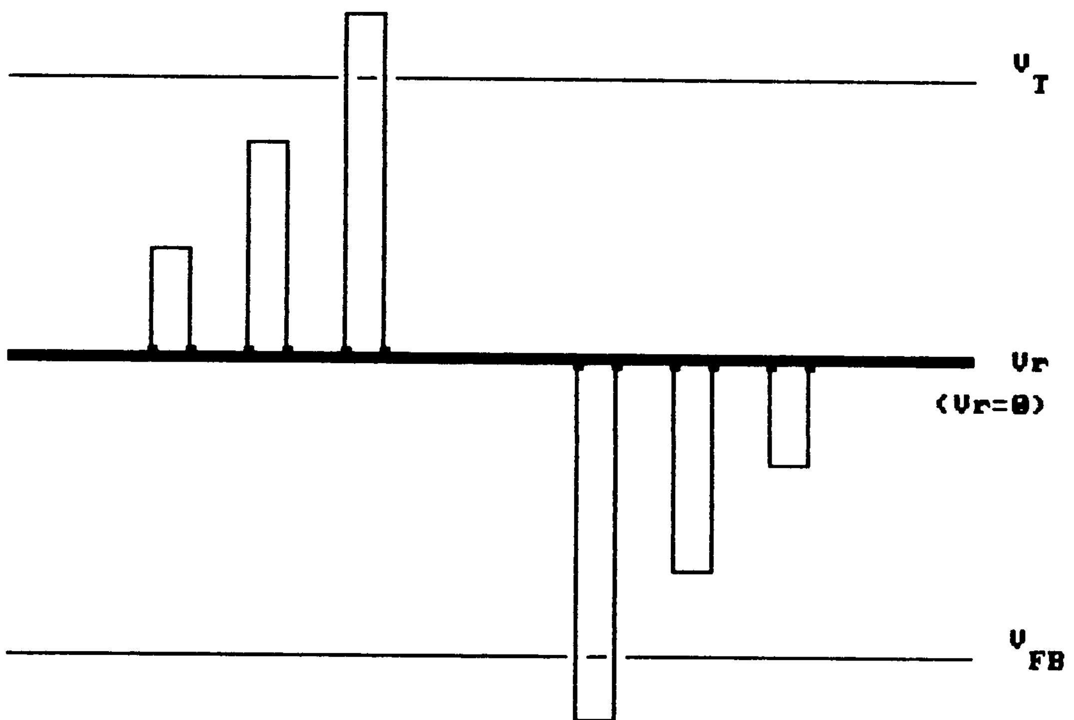


Fig.5.4 Way of applying the gate pulse signal to a MOS device. (a) n-type substrate (b) p-type substrate devices.

For a given version of the experiment, the amplitude of the signal is kept constant and the frequency is varied step by step form a certain minimum value around 40 Hz to a maximum around 100 kHz. The step of increment is suitably chosen for different frequency ranges. The current and frequency are measured after each step of increment and, when the frequency range is completely swept, the current versus frequency curve is plotted. This is done for each value of the voltage amplitude that varies from a certain minimum to a maximum value. A survey of different results obtained in the above experimentation will be presented in the next chapter.

TABLE 5.1. Device Parameters of Wafers Shown by Fig.5.2.

MOS device.		Width W. (um)	Length L. (um)
TRANSISTOR	1.	80	2
//	2.	80	8
//	3.	80	20
//	4.	80	80
//	5.	80	300
//	6.	300	2
//	7.	300	8
//	8.	300	20
//	9.	300	80
//	10.	300	300
CAPACITOR or DIODE		Area A. (mm^2)	
DIODE	1.	0.500	
//	2.	1.500	
//	3.	2.000	
DOPING CONCENTRATION N_x		$7.6.10^{15}$ cm^{-3}	
OXIDE THICKNESS t_{ox}		400 A	

EXPERIMENTAL RESULTS

In the charge pumping technique, only the steady state recombination of the interface states is considered to contribute a net dc substrate current called charge pumping current, whereas the contribution of the non steady state emission is thought to be insignificant. The present experiment utilizes only the non steady state emission of the interface states. The results so obtained are presented in this chapter which not only disprove the earlier contention of neglecting this current but impart to it such distinct characteristics which distinguish it from the usual charge pumping current as well as from any other hitherto known substrate current.

6.1 A SURVEY OF EXPERIMENTAL RESULTS.

The experiment has been carried out under three different versions. The first version consists of applying to a MOS device a gate signal of an amplitude varying between the voltage V_r (corresponding to the intrinsic level E_i) and the flatband voltage V_{FB}. The second version consists of applying to the same device a gate signal of amplitude varying between V_r and V_T, the threshold voltage. The third version is a combination of the two version described above, that is applying a gate signal the amplitude of which varies between V_T to V_{FB}. In all the cases an appreciable amount of dc substrate current was observed. It was further ascertained that this current is not due to leakage of the applied gate voltage through the oxide. For this purpose, a gate voltage corresponding to the rms value of the ac signal was applied to the gate to see if it can account for the observed current. In fact this could account only for 5% of observed current proving thereby that it does not originate from leakage. Furthermore the observed dc substrate current is found to be independent of the polarity of the gate voltage signal which confirms that it does not originate from leakage. Since this current is produced without using drain/source and even in MOS capacitors, it can not be identified with the usual charge pumping current. It is then anticipated that this new current arises due to the

charging and discharging of the surface states at the Si-SiO_2 interface under non steady state emission which is ignored in the charge pumping technique. This current is found to have strong dependence on the frequency of the applied voltage signal. At certain frequencies, the value of this gate-substrate current is quite appreciable and can not be ignored. It is this current which appears in the gate circuit of the charge pumping technique which attracted our attention and provided motivation for the present investigation. The present experimentation to measure this current has been carried out quite extensively by varying different device parameters and experimental versions. The results are described in the following.

6.1.1 Experimental Results of Version 1.

Several experiments have been carried out on different devices of different types and dimensions. The results obtained for the case of p-substrate devices can be classified broadly into two categories the first of short-channel and the other of long-channel. In the case of short-channel, during the sweep of the gate signal frequency from 40 Hz to 100 kHz (*see chap.5 for more details*), two main maxima in current have been observed. These current maxima or peaks occur at around 70 Hz for the first and at 44 kHz for the second. The amplitude of the 44 kHz peak is greater than that of the 70 Hz. Figure 6.1 and 6.2 show a

sample of the results obtained in these experiments. In the case of long-channel devices, three current peaks as shown in Figs.6.3 and 6.4 are detected within the same range of frequencies from 40 Hz to 100 kHz. The first peak occurs near 56 Hz, the second (which is not observed in the short-channel devices) occurs near 9 kHz, and the third occurs near 33 kHz.

The commercial devices tested in these experiments showed the same behaviour as in the case of short-channel devices, this is illustrated in Fig.6.5. However, their geometry is unknown. This is a handicap in knowing the reason for the non appearance of the second peak in these devices because the channel length is not that small in commercial devices. In case of n-substrate devices which are long-channel devices (*see Fig. 5.3 chap 5*) some devices show two peaks and some other devices show three as shown in Figs.6.6 and 6.7.

6.1.2. Experimental Results of Version 2.

The same experiment is repeated using the second version as in the case of version 1 and the results show the same trend. The short-channel devices show only two peaks of current, one near 70 Hz and the third near 44 kHz (the numbering of the peaks is so done that the peak occurring in the very low frequency range 50 to 70 Hz is referred as first, that occurring in the range 7 to 10 kHz as second

peak and the one occurring in the range 33 to 44 kHz as third peak). However, the current amplitude is small as compared to that obtained correspondingly in version 1 experiments. Figures 6.8 and 6.9 illustrate the short-channel devices behaviour as a function of frequency in the second experimental version. Not all the long-channel devices show a second peak as it is the case in version 1. However, in the devices where the second peak is not visible the data table corresponding to that device shows a maximum current value, but the maximum is very flat. The first peak occurs near 70 Hz, the second near 10 kHz, and the third occurs near 44 kHz. Figures 6.10 and 6.11 show a sample of the devices that show the three peaks. In the case of commercial devices, shown in Fig.6.12, only two peaks are observed. Their amplitudes are smaller to the corresponding peaks in version 1. The n-substrate devices also show only two peaks, the first and the third peak as it is illustrated in Figs.6.13 and 6.14. However the amplitudes of the currents are larger than the corresponding peaks in the version 1. This behaviour is opposite to that of p-type substrate devices.

6.1.3. Experimental Results of Version 3.

In this version of experiments, all the devices show the same trend. They show three distinct peaks as illustrated in Figs.6.17 to 6.21. Except for short-channel

devices (Figs.6.15 and 6.16) which show a very small second peak, all the others show the three peaks in current. The current values found in this case are large compared to their corresponding peaks in the first and second versions. However, the amplitude ratio of the three current peaks show the same general trend as in the first and second experimental versions, this is, $I_{ce2}<I_{ce1}<I_{ce3}$ where the suffix 1,2 and 3 represent the versions as shown in Figs.6.15-6.21. The current peaks occur respectively at 56 Hz, 9kHz, and 34 kHz. These values are the same as the one obtained in version 1 and in version 2 in the case of long-channel n- or p-substrate MOS devices. An important variation is noticed only in short-channel devices where the first peak is displaced from 70 to 56 Hz and the third one is moved from 44 kHz to 34 kHz. In general a decrease of 20% in the value of the optimum frequency of the first and third peaks is observed in the results of the third experimental version as compared to that of the first and second experimental versions. In the case of n-substrate devices it has been observed that the second peak value is larger than that of the first peak as it is illustrate in Figs.6.20 and 6.21.

An other type of experiments is repeated in all the experimental versions in which the amplitude of the gate signal, as applied to p-substrate devices, is increased from V_r to V_{FB} by an increment of 0.1 V. For each increment, the

entire frequency range from 40 Hz to 100 kHz is swept in all the three experimental versions. The variation of the optimum frequency of the first peak with respect to gate voltage variation could not be detected. However, the optimum frequency shows a variation with the amplitude of the applied signal in the third peak and it decreases with an increase of the gate voltage. At a certain value of the gate voltage, the optimum frequency becomes constant and does not vary further with an increase in the gate voltage. When an n-type substrate device is used under the above condition, instead of decreasing and then becoming constant, the optimum frequency increases and then becomes constant after a certain value of the gate voltage. The same results have been obtained when the gate voltage is varied from V_r to V_T. The last type of experiment achieved is characterized by the variation of the amplitude such that half of it is below the reference V_r and the other half is above it. In this case, the optimum frequency of the third peak decreases with an increase of the gate voltage and stabilizes to a constant value after a certain value of the gate voltage for the devices showing the first peak at 70 Hz and the third at 44 kHz. The other devices do not show any noticeable change with respect to the variation of signal amplitude.

6.2. SUMMARY OF OBSERVATIONAL FACTS.

After a careful inspection and analysis of the experimental results obtained for different devices under different conditions, a certain number of observational facts have been concluded [44]. The main conclusions are listed below:

1. A significant dc substrate current is observed both in MOSFETs (with drain and source open) as well as MOS diodes when they are operated under an oscillating gate voltage (see Figs.6.1-6.21).

2. The current is always found to flow from the ground to the substrate irrespective of the substrate nature (whether p or n type) and polarity of the gate voltage signal (whether upper half or lower half of the ac signal).

3. The current shows a strong dependence on the frequency of the applied signal showing in general three current peaks at certain specific frequencies (see Figs.6.1 to 6.21).

4. Depending on the gate voltage sweep V_r-V_{FB}, V_r-V_T, and $V_{FB}-V_T$, which give respectively the currents I_{ce1}, I_{ce2}, and I_{ce3}, the following current relationship is found: $I_{ce2}<I_{ce1}<I_{ce3}$ in p-MOS as well as in n-MOS devices as it is illustrated in all figures.

5. Besides the three maxima, the current versus frequency curve shows a critical minimum nearly at 26 kHz.

6. Broadly speaking, the results of the substrate current

can be divided into two categories: 1) short-channel and 2) long-channel. Short-channel devices give two peaks at 70 Hz and 44kHz (see Figs.6.1-6.2 and 6.15-6.16) and long-channel devices give three peaks at 56 Hz, at 9 kHz, and at 34 kHz (see Figs.6.6-6.7, 6.12-14 and 6.18-21).

7. In version 3 of the present experiment, both the short-channel and long-channel devices show three peaks at 56 Hz, 9 kHz, and at 34 kHz (see Figs.6.15 to 6.21).

8. Except for the first peak, the optimum frequency is found to vary with the gate voltage signal in the first and second versions. This frequency f_m is found to decrease with the gate voltage till it becomes constant at a particular value. In the third version, only the optimum frequency of the second peak varies with the gate signal. It decreases with an increase of the gate voltage signal. The optimum frequency in the other peaks in this third version remains constant and corresponds to the value of the first and second versions.

9. In all cases f_m has the same value for the first and second versions but not for the third.

Fig.6.1 I-f curve for a 300x8um^2 MOSFET. Voltage sweep from Vr=0 to Vfb=-1.0 V.

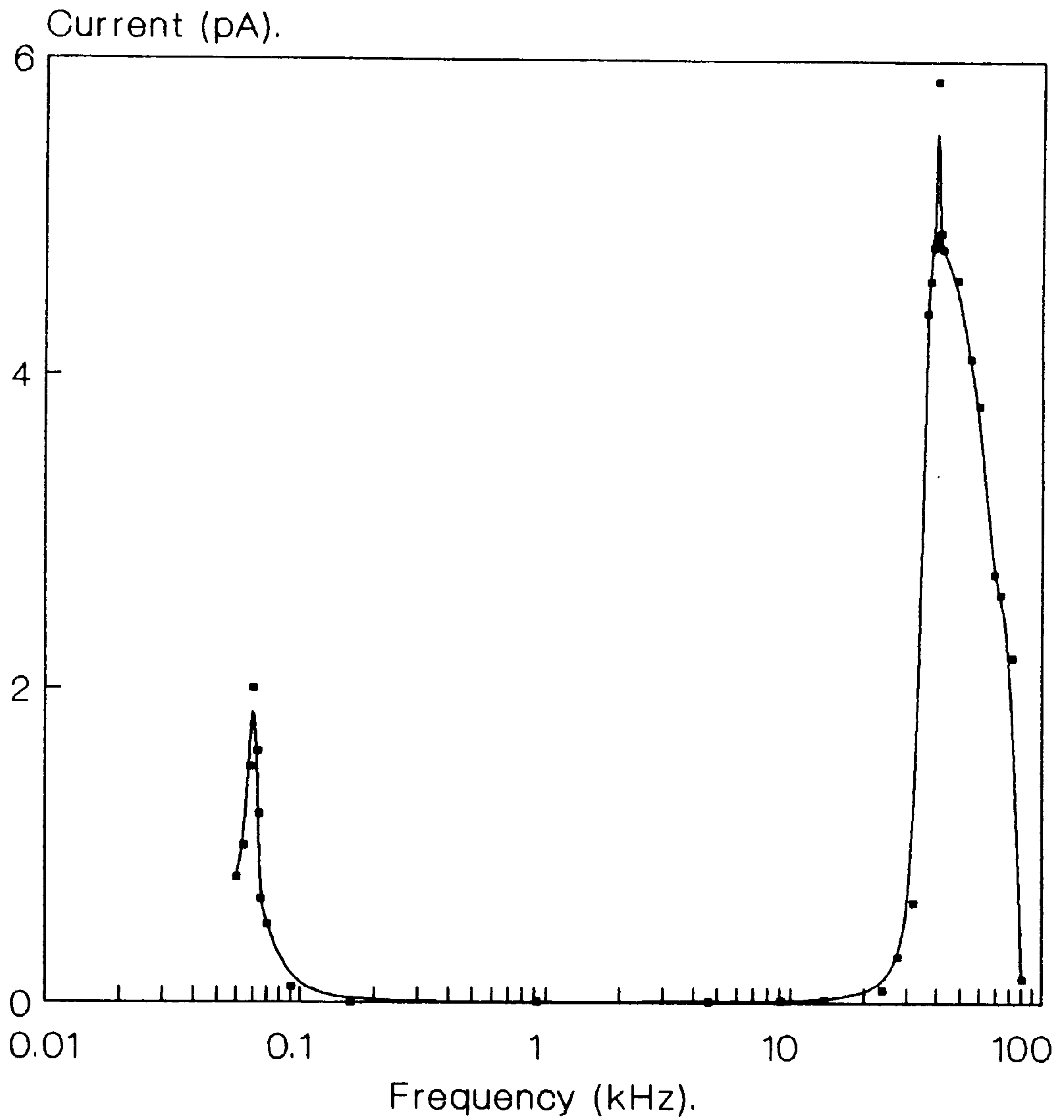


Fig.6.2 I-f curve for a 300x20um^2 MOSFET. Voltage sweep from Vr=0 to Vfb=-1.1 V.

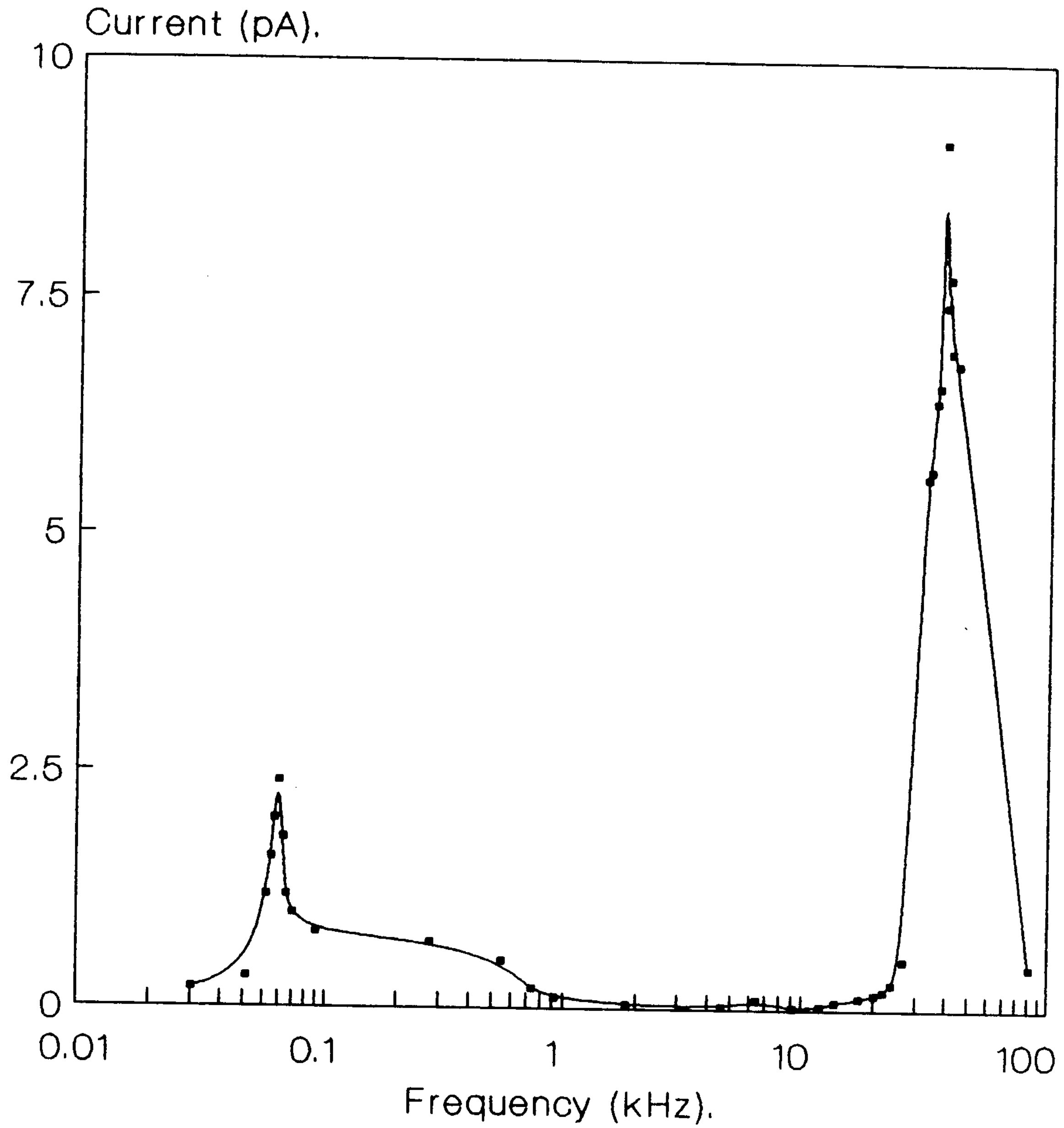


Fig.6.3 I-f curve for a 300x80um^2 MOSFET. Voltage sweep from Vr=0 to Vfb=-0.9 V.

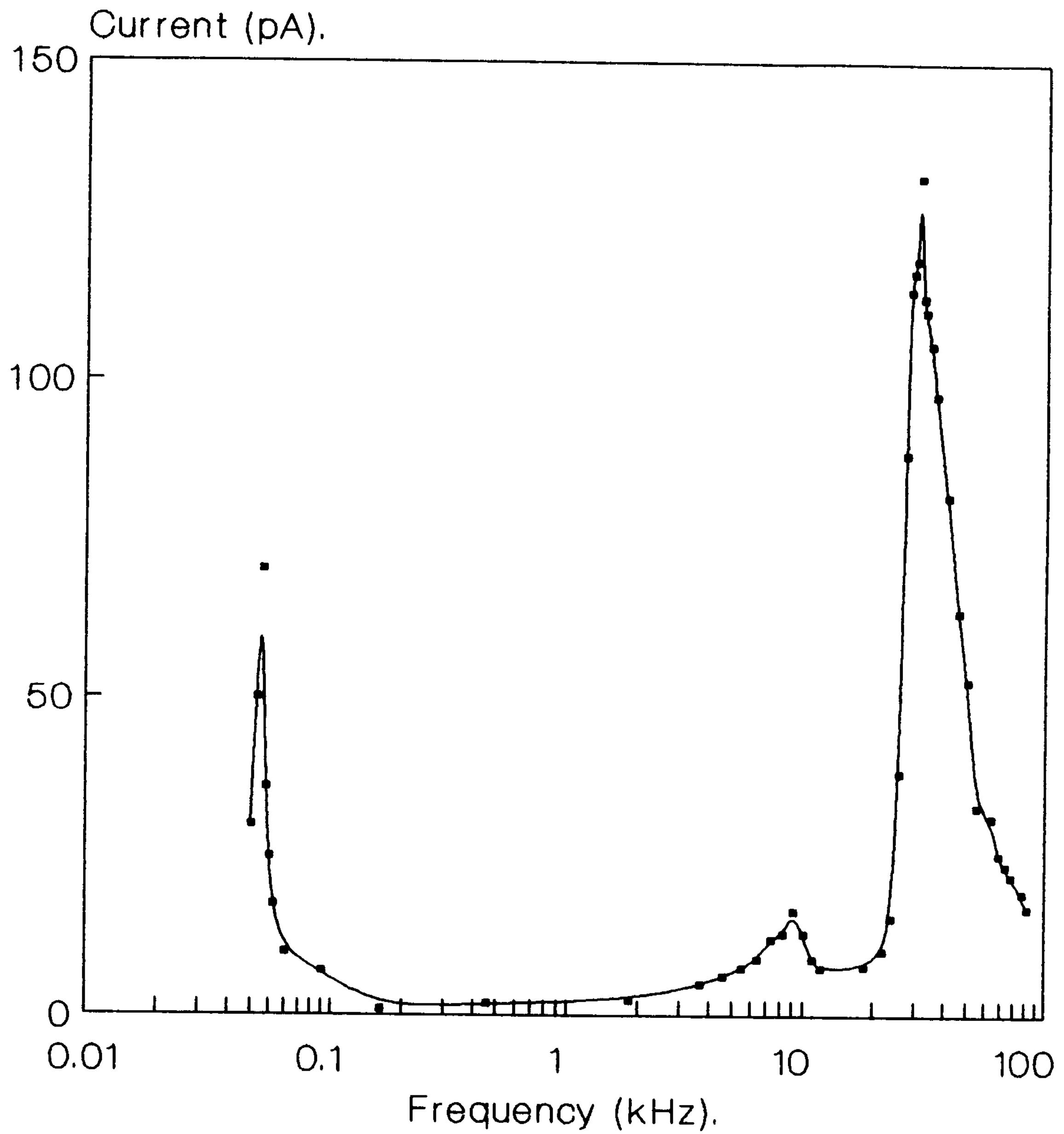


Fig.6.4 I-f curve for a 300x300um^2 MOSFET
Voltage sweep from Vr=0 to Vfb=-0.9 V.

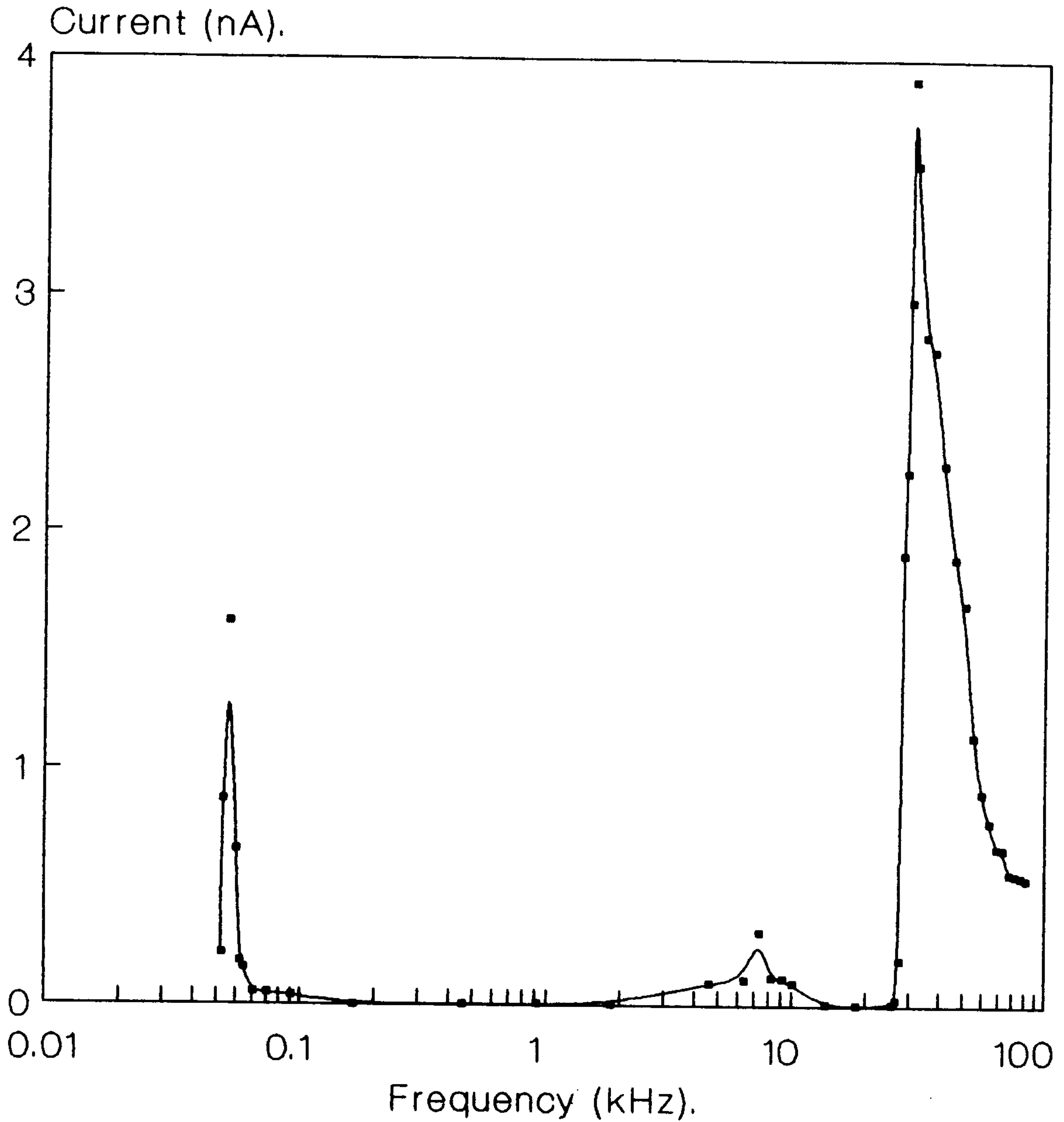


Fig.6.5 I-f curve for a 3N 170 MOSFET. Voltage sweep from Vr=0 to Vfb=-1.6 V.

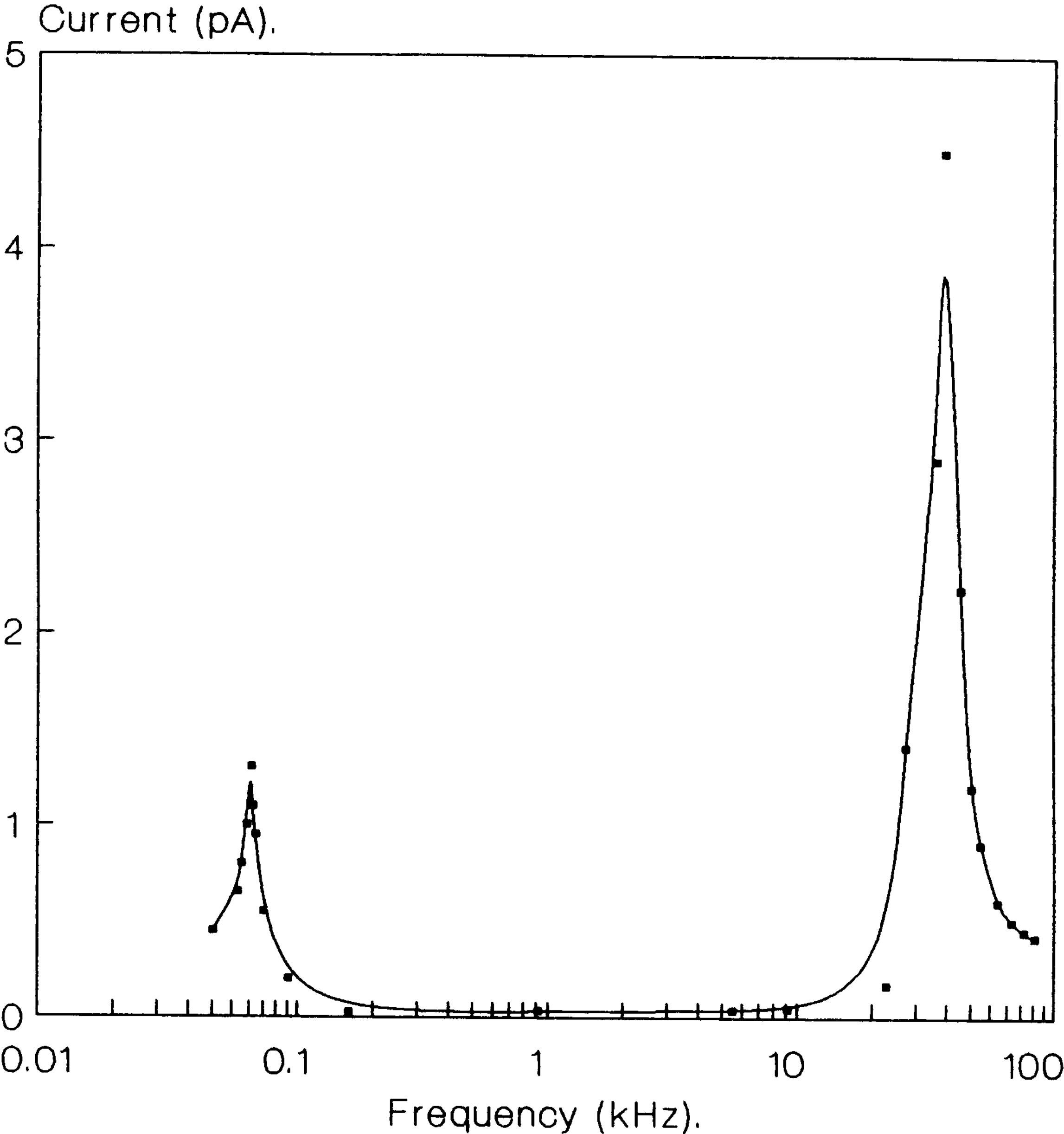


Fig.6.6 I-f curve for a 0.5 mm²MOS Diode Voltage sweep from Vr=-0.7 to Vfb=-0.4V.

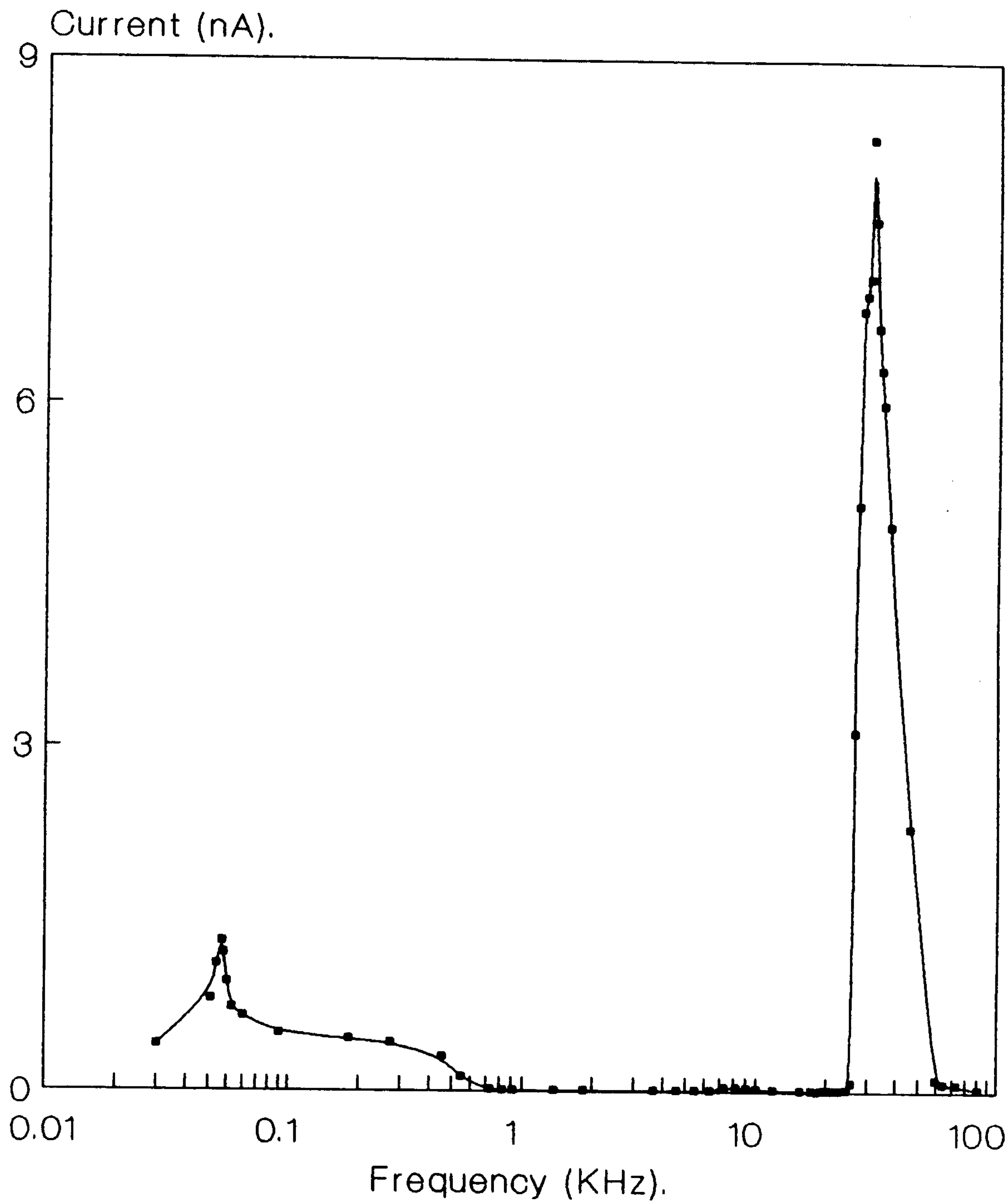


Fig.6.7 I-f curve for a 2 mm^2 MOS Diode. Voltage sweep from Vr=-0.7 to Vfb=-0.4V.

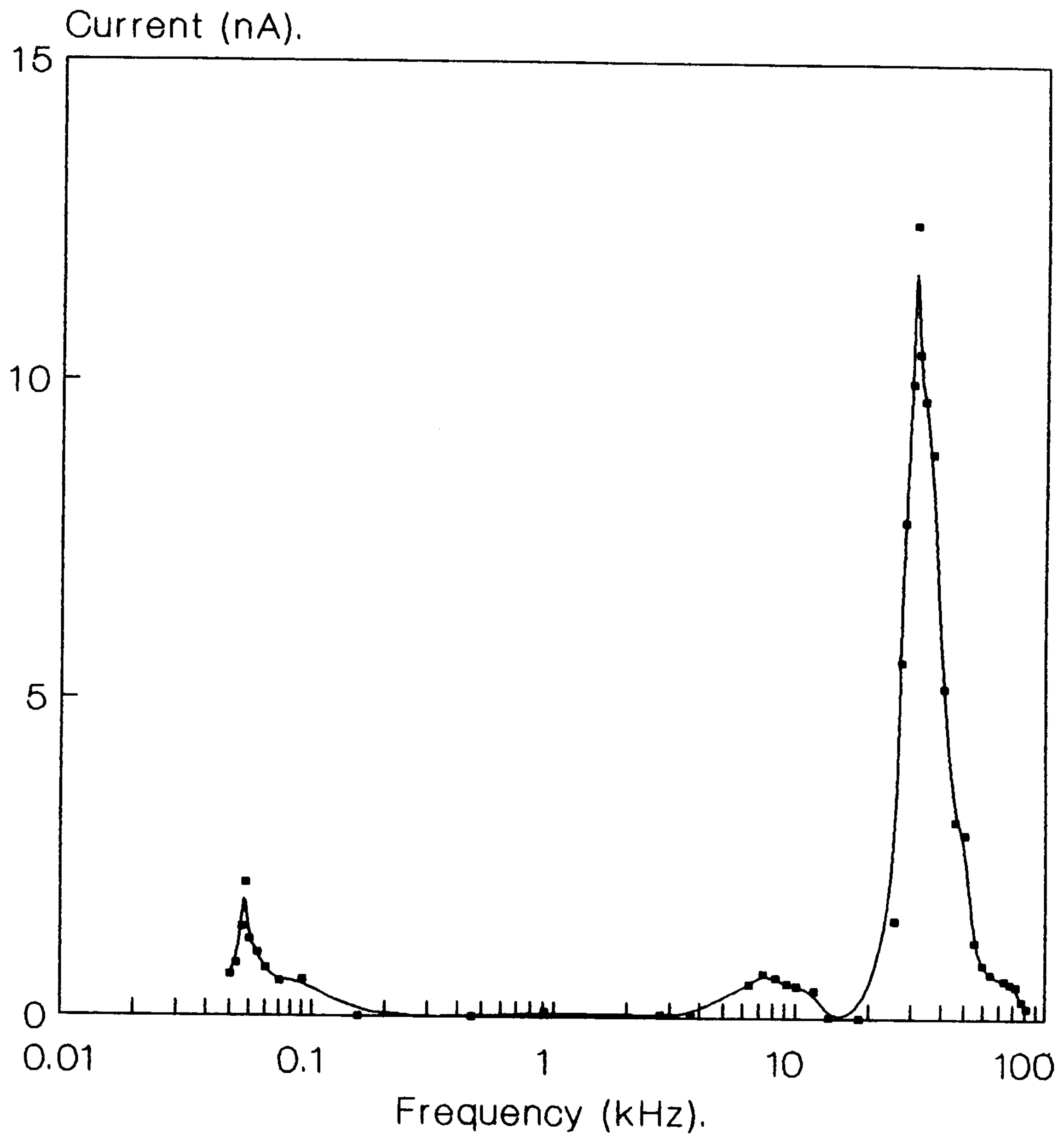


Fig.6.8 I-f curve for a 300x8um² MOSFET. Voltage sweep from Vr=0 to Vt=1.2 V.

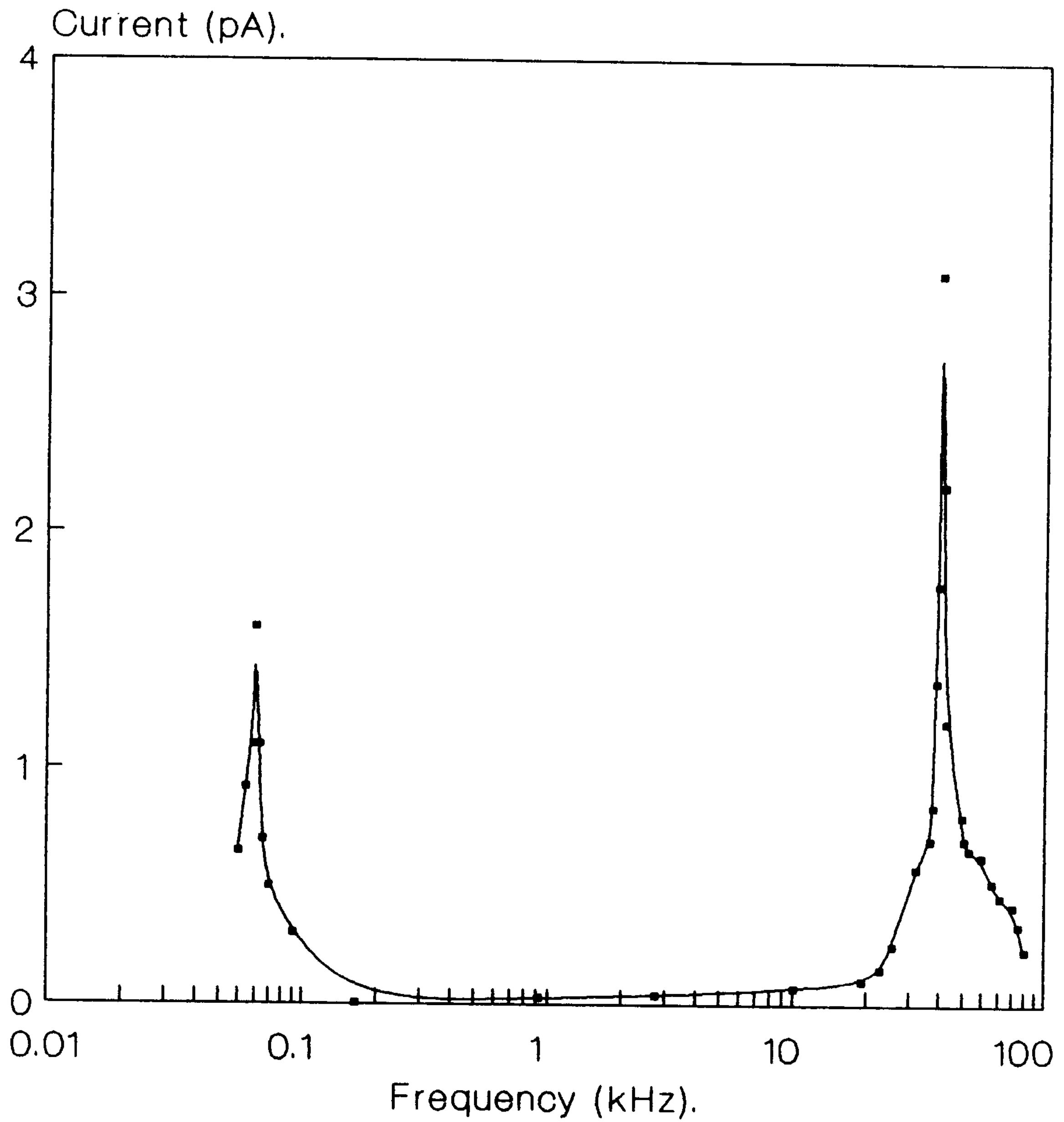


Fig.6.9 I-f curve for a 300x20um² MOSFET. Voltage sweep from Vr=0 to Vt=1.2 V.

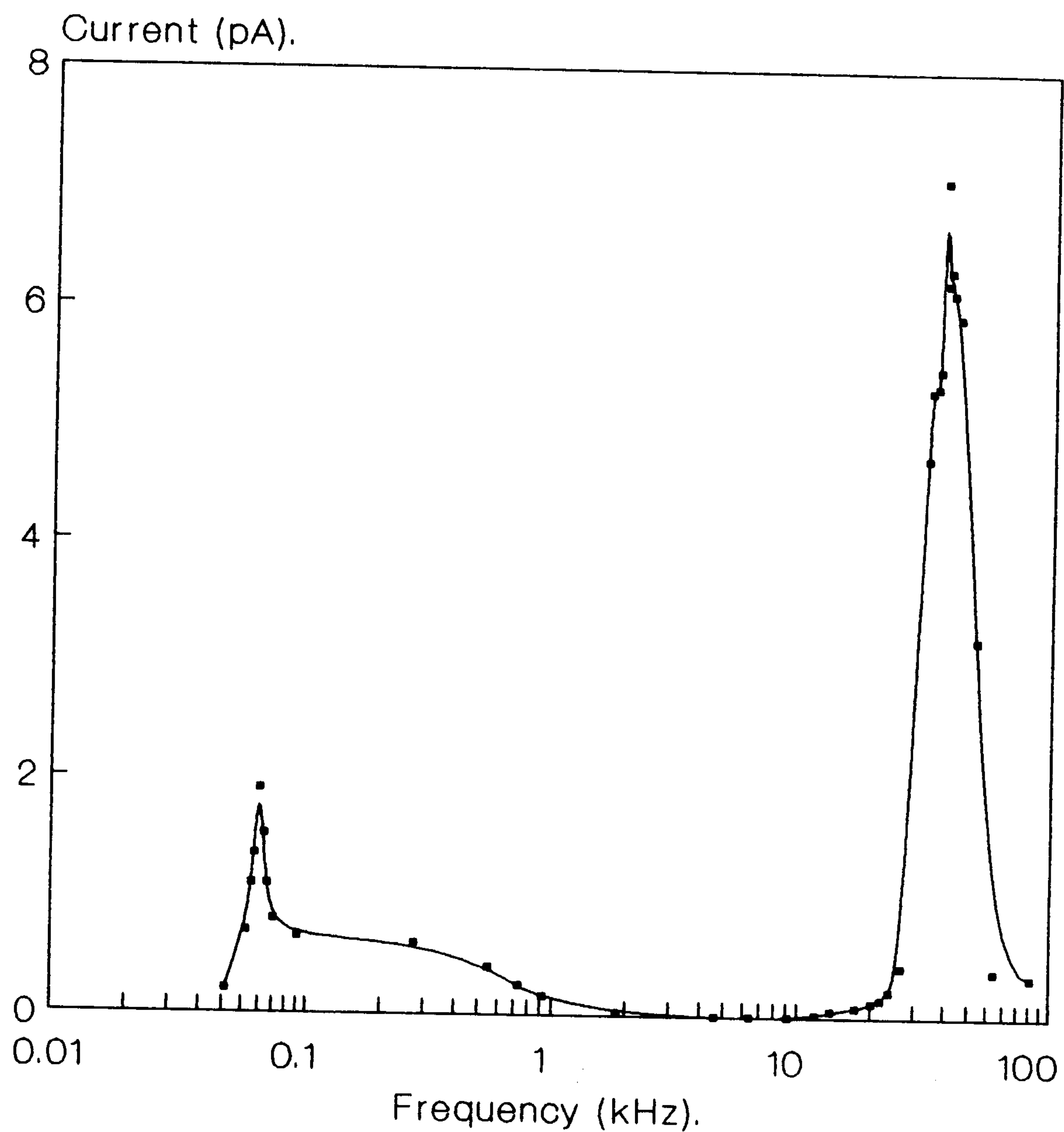


Fig.6.10 I-f curve for a 300x80um^{2}MOSFET
Voltage sweep from Vr=0 to Vt=1.0 V.

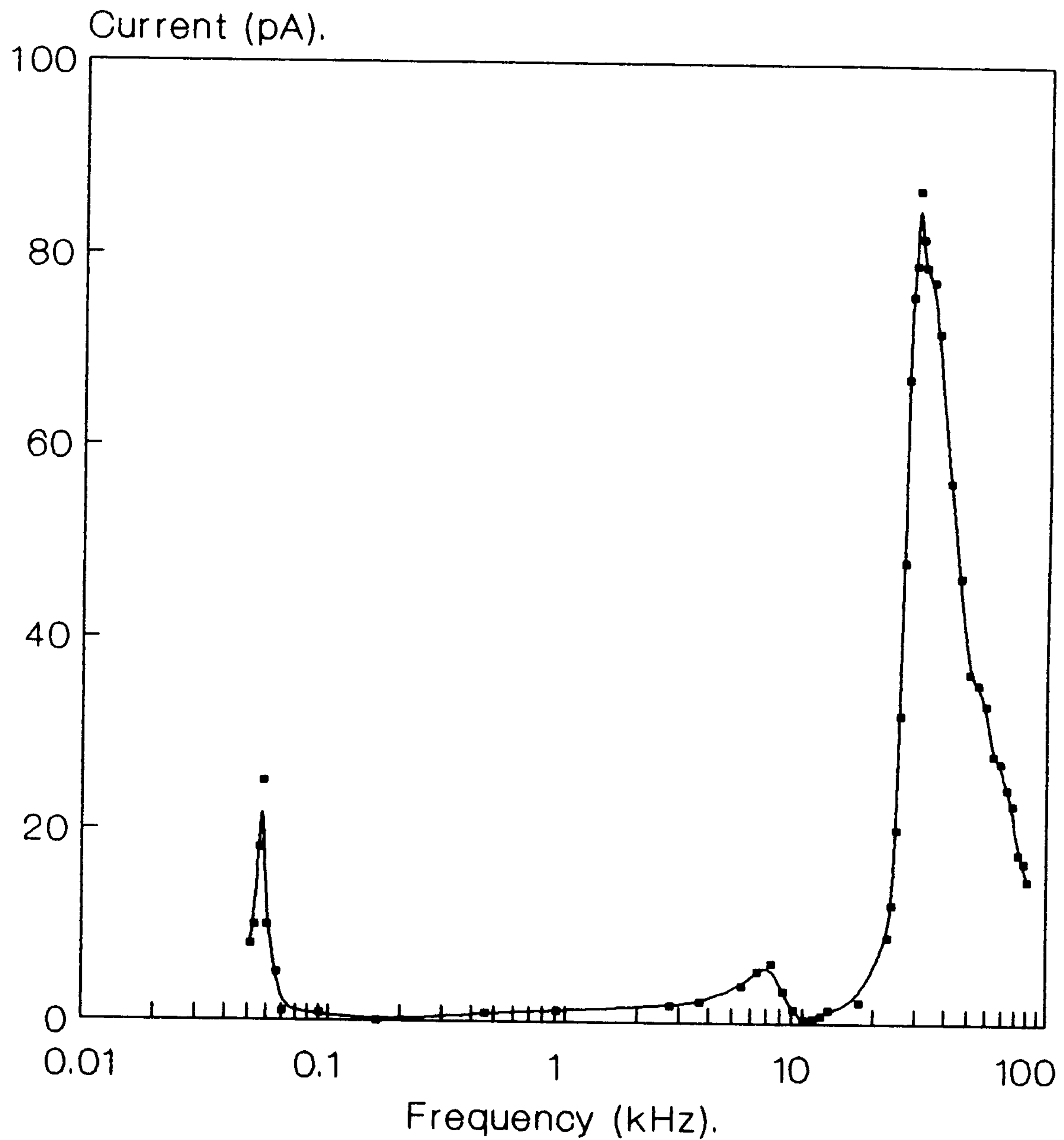


Fig.6.11 I-f curve for a 300x300um^{2}MOS-FET. Voltage sweep from Vr=0 to Vt=1.0V.

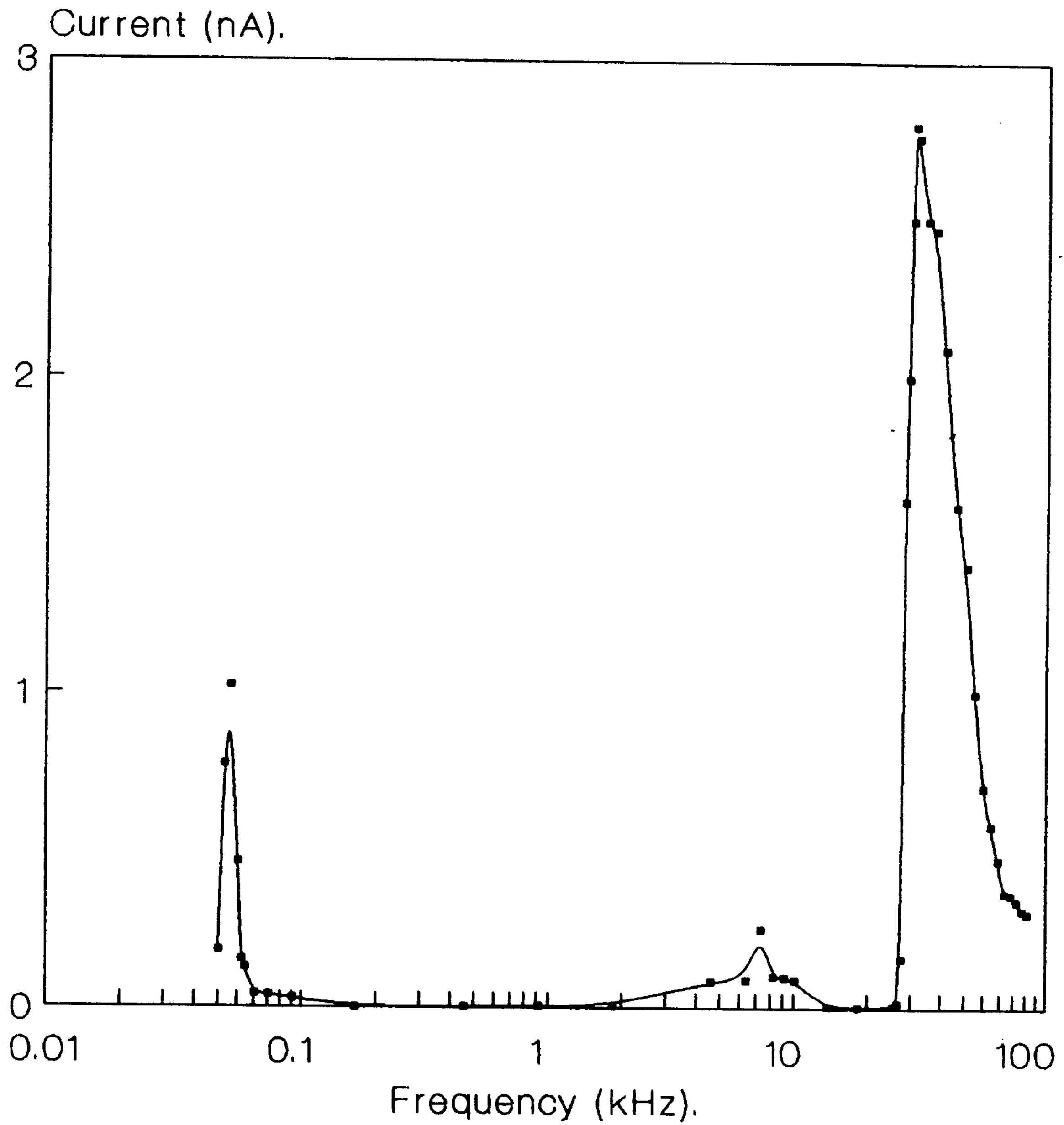


Fig.6.12 I-f curve for a 3N 170 MOSFET. Voltage sweep from Vr=0 to Vt=1.4 V.

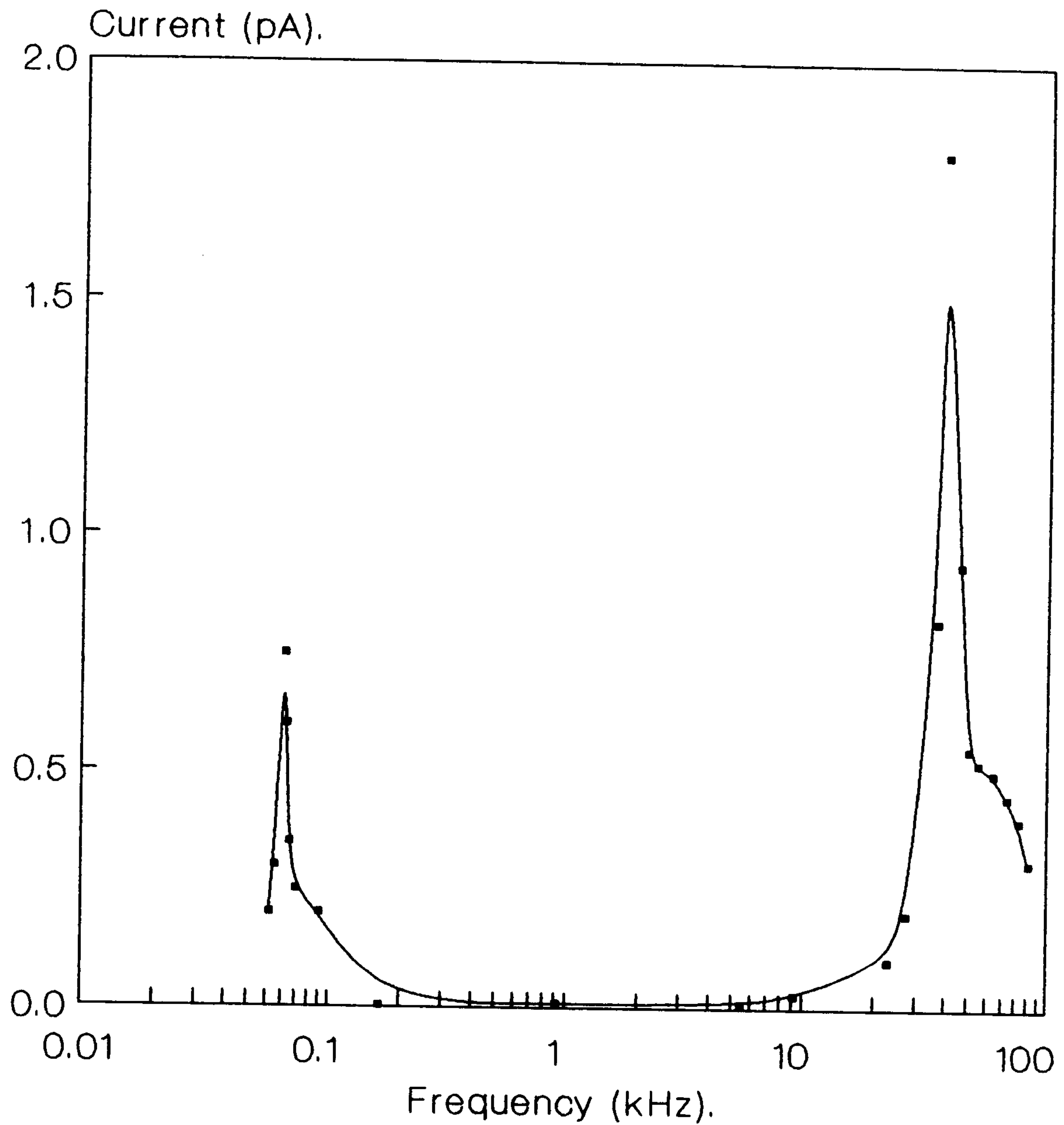


Fig.6.13 I-f curve for a 0.5mm²MOS diode Voltage sweep from Vr=-0.7 to Vt=-1.1 V.

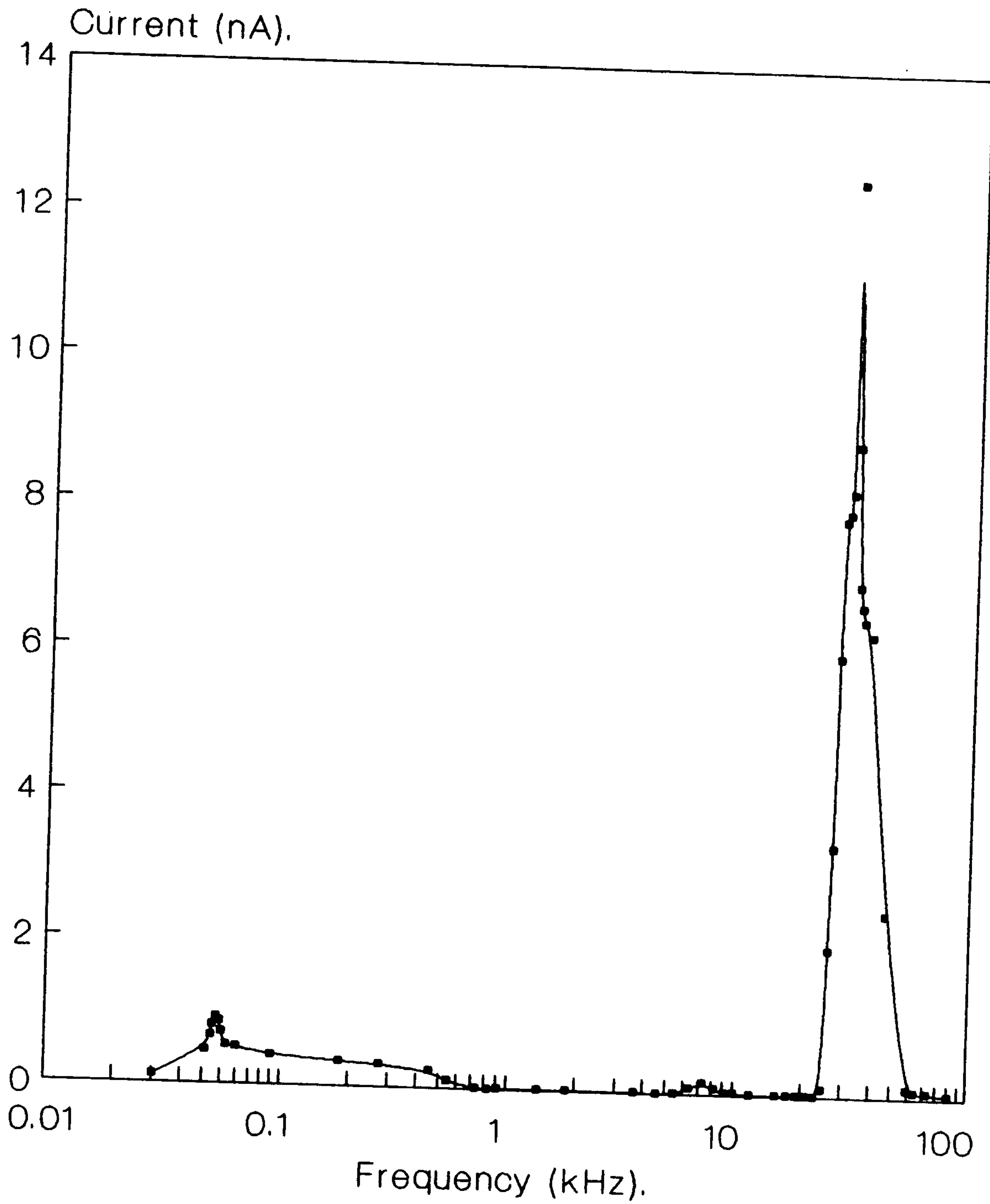


Fig.6.14 I-f curve for a 2 mm^2 MOS Diode. Voltage sweep from Vr=-0.7 to Vt=-1.1V.

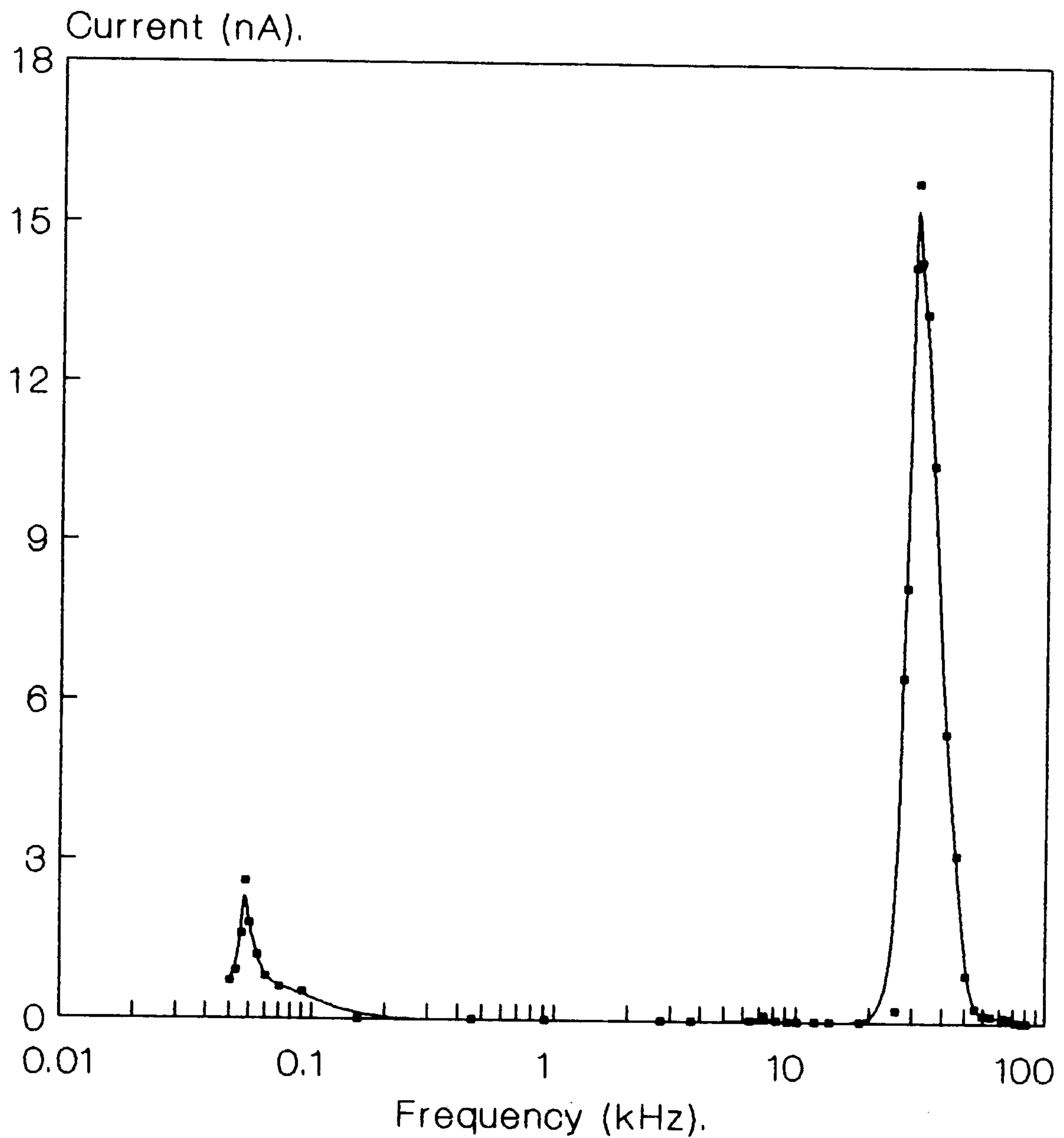


Fig.6.15 I-f curve for a 300x8um²MOSFET. Voltage sweep from Vfb=-1 to Vt=1.1 V.

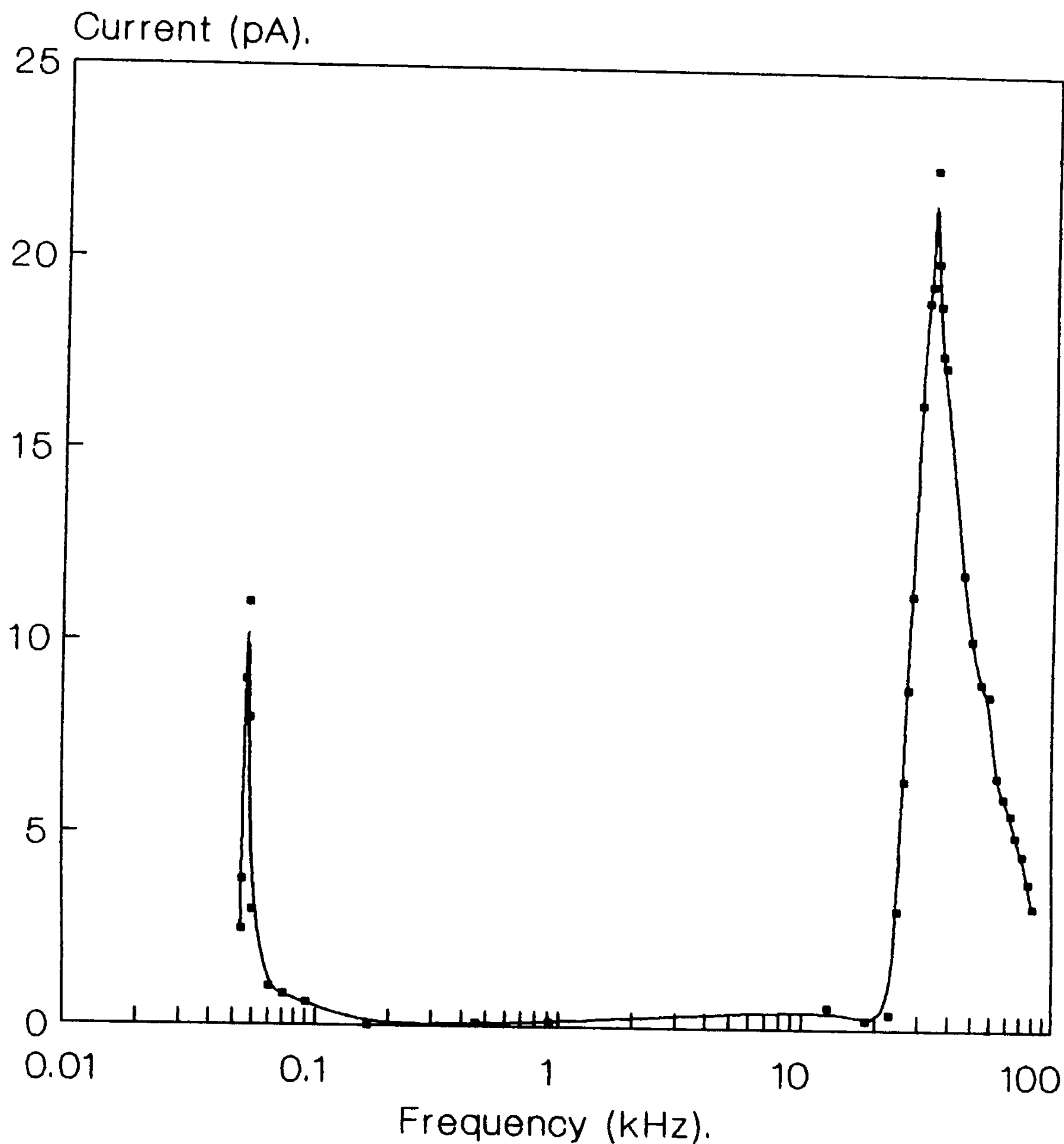


Fig.6.16 I-f curve for a 300x20um² MOSFET
Voltage sweep from Vfb=-1.1 to Vt=1.2V.

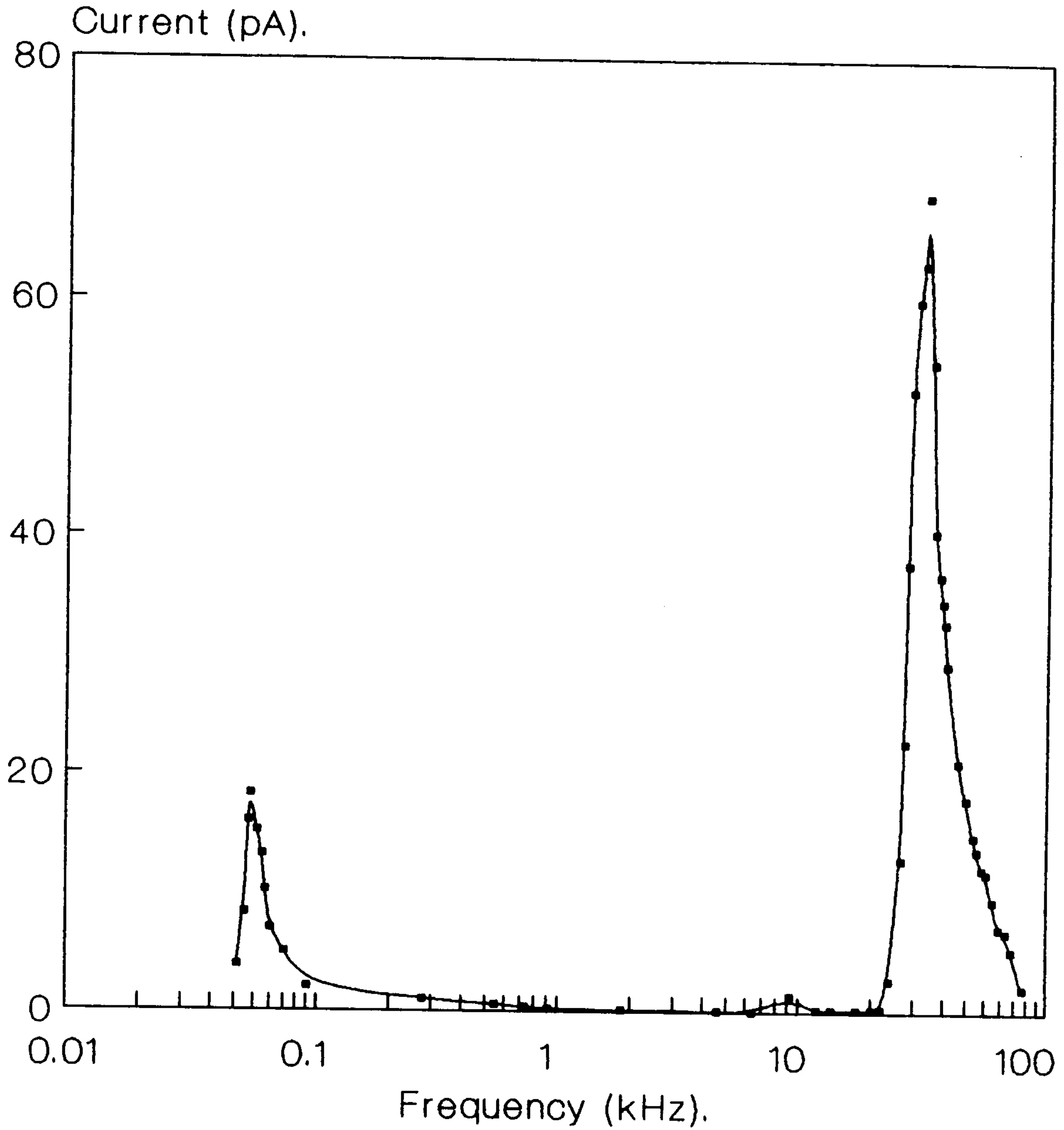


Fig.6.17 I-f curve for a 300x80um^2 MOSFET Voltage sweep from Vfb=-0.9 to Vt=1.0V.

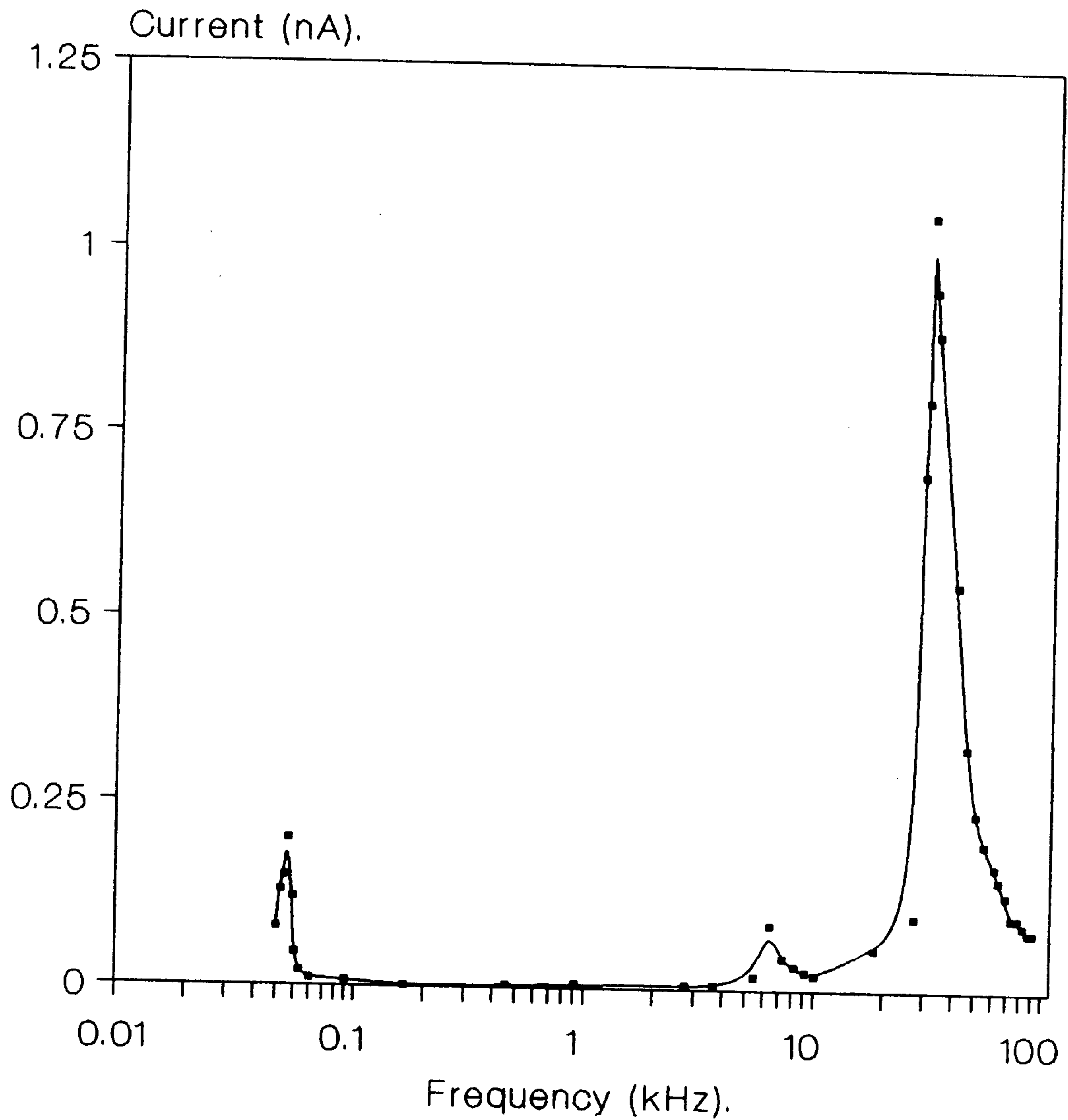


Fig.6.18 I-f curve for a 300x300um^{2}MOST. Voltage sweep from Vfb=-.9 to Vt=1.0V.

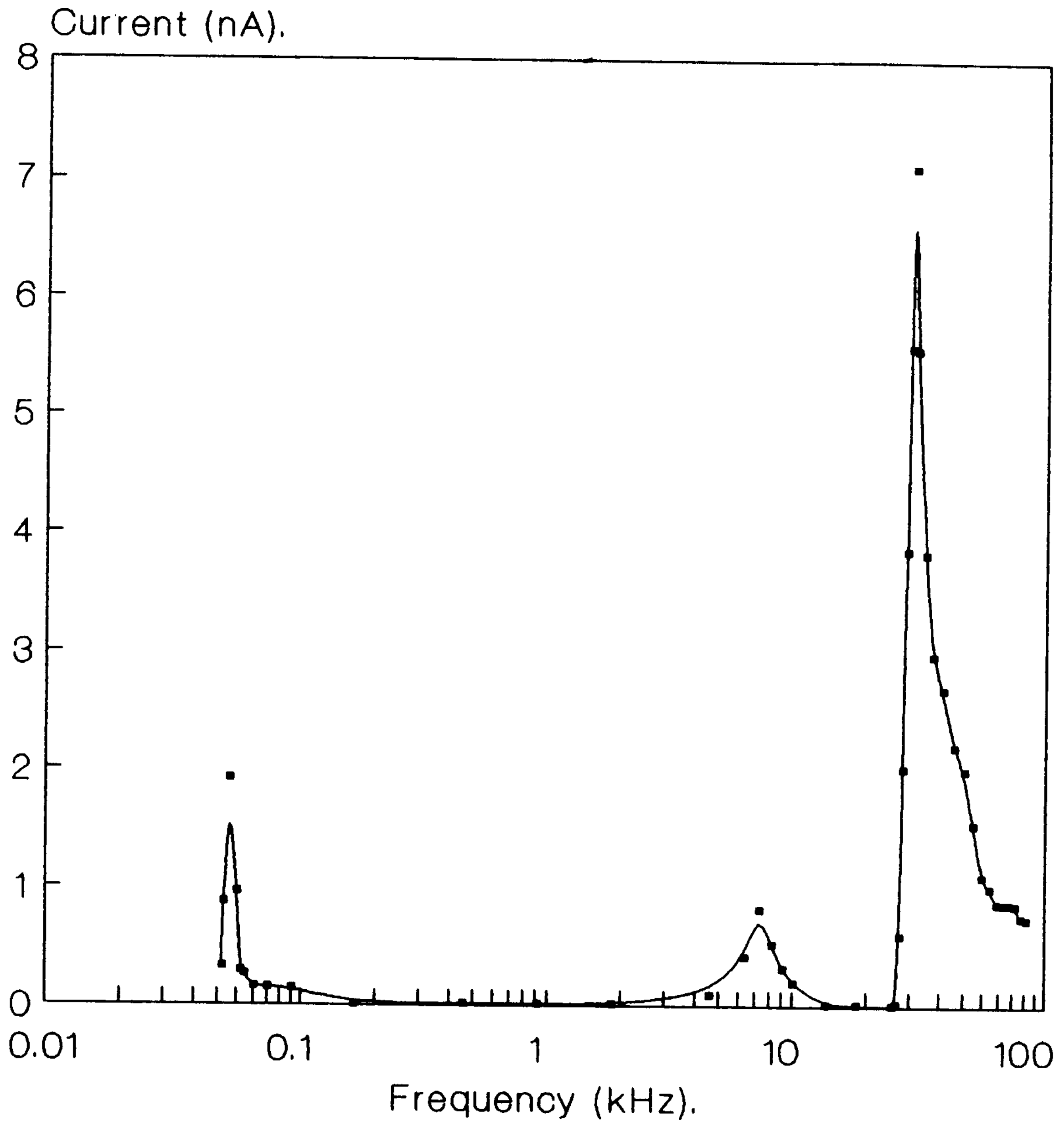


Fig.6.19 I-f curve for a 3N 170 MOSFET. Voltage sweep from Vfb=-1.6 to Vt=1.4V.

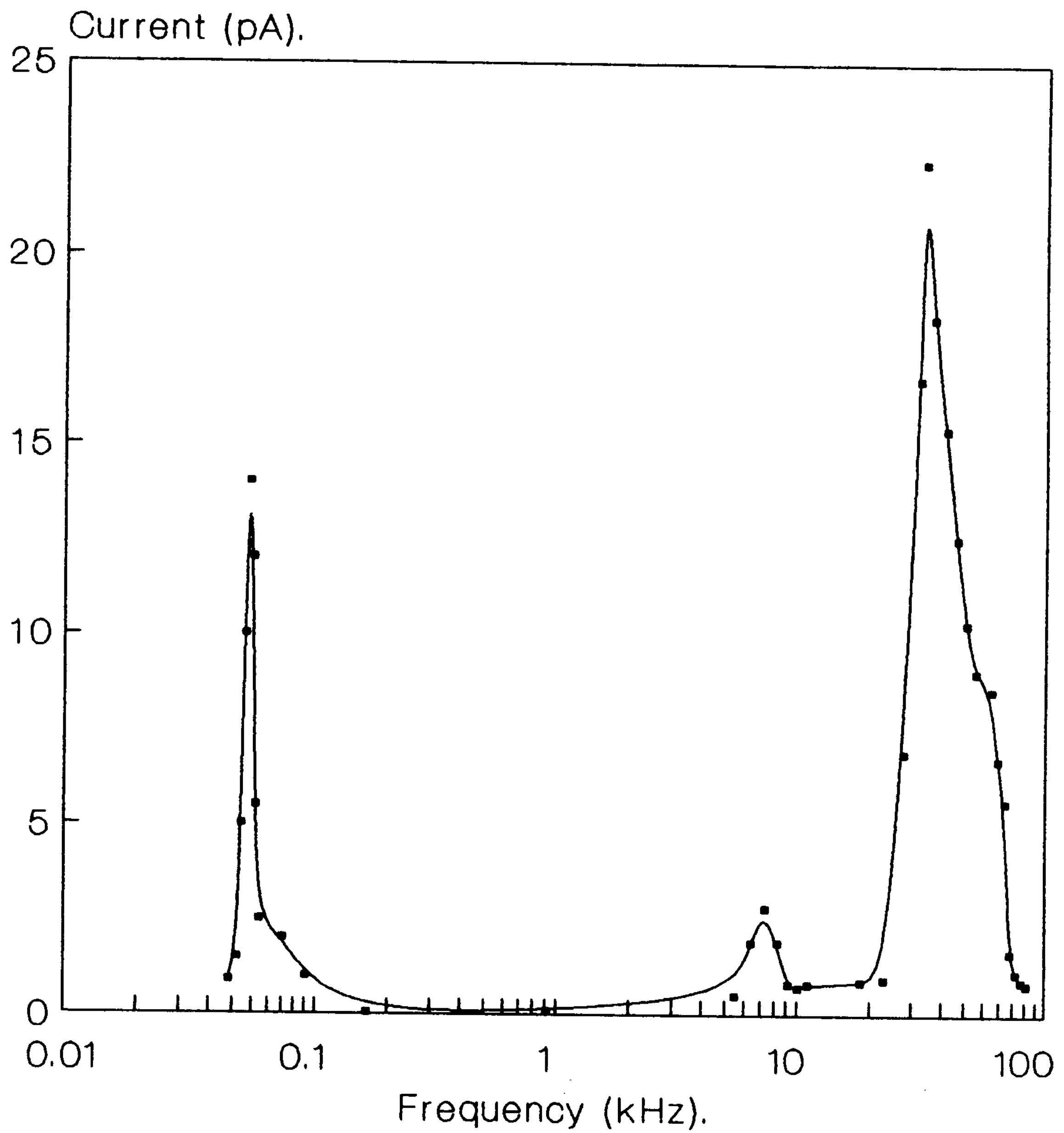


Fig.6.20 I-f curve for a 0.5mm^2 MOS diode
Voltage sweep from Vfb=-0.4 to Vt=-1.1V.

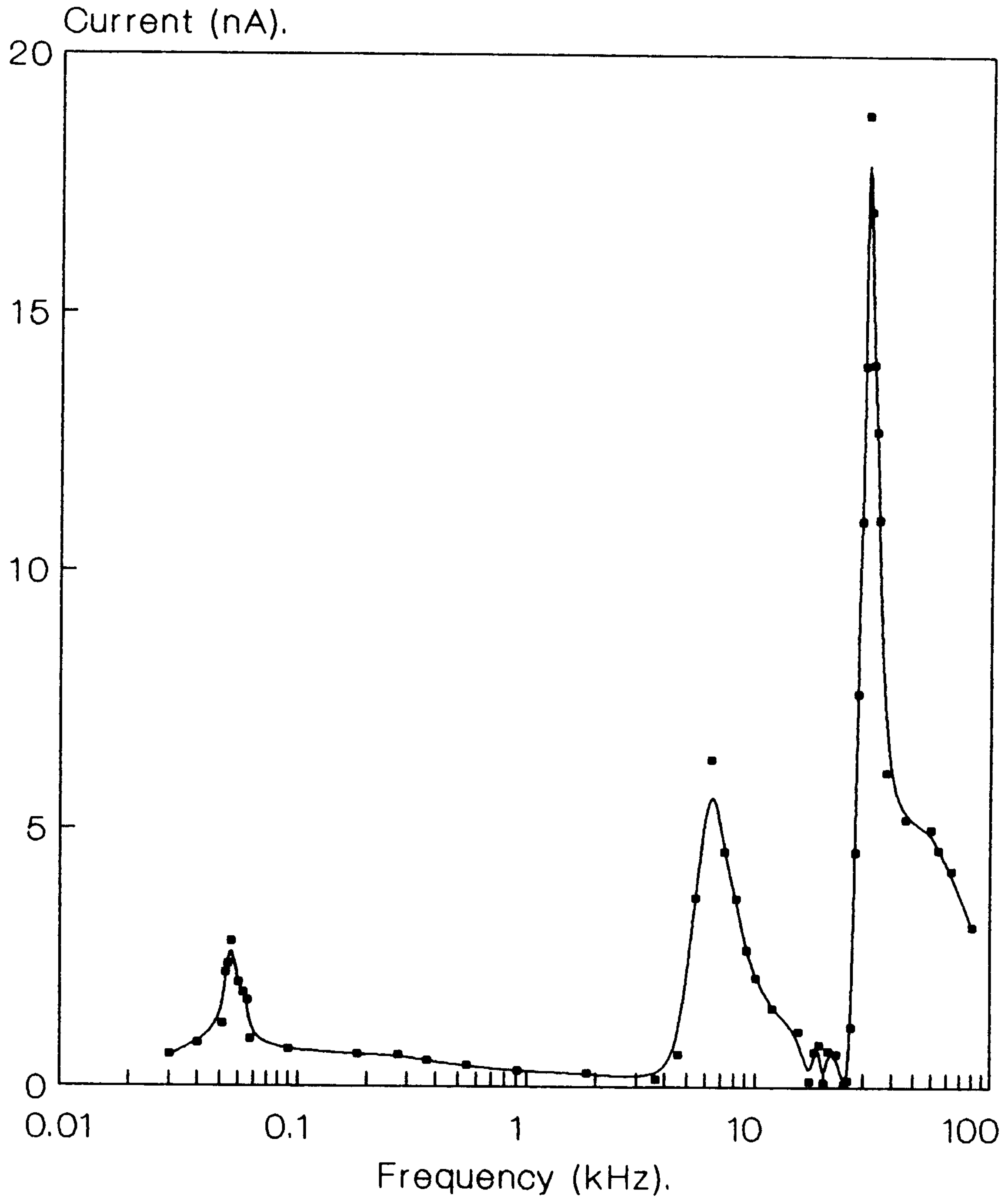
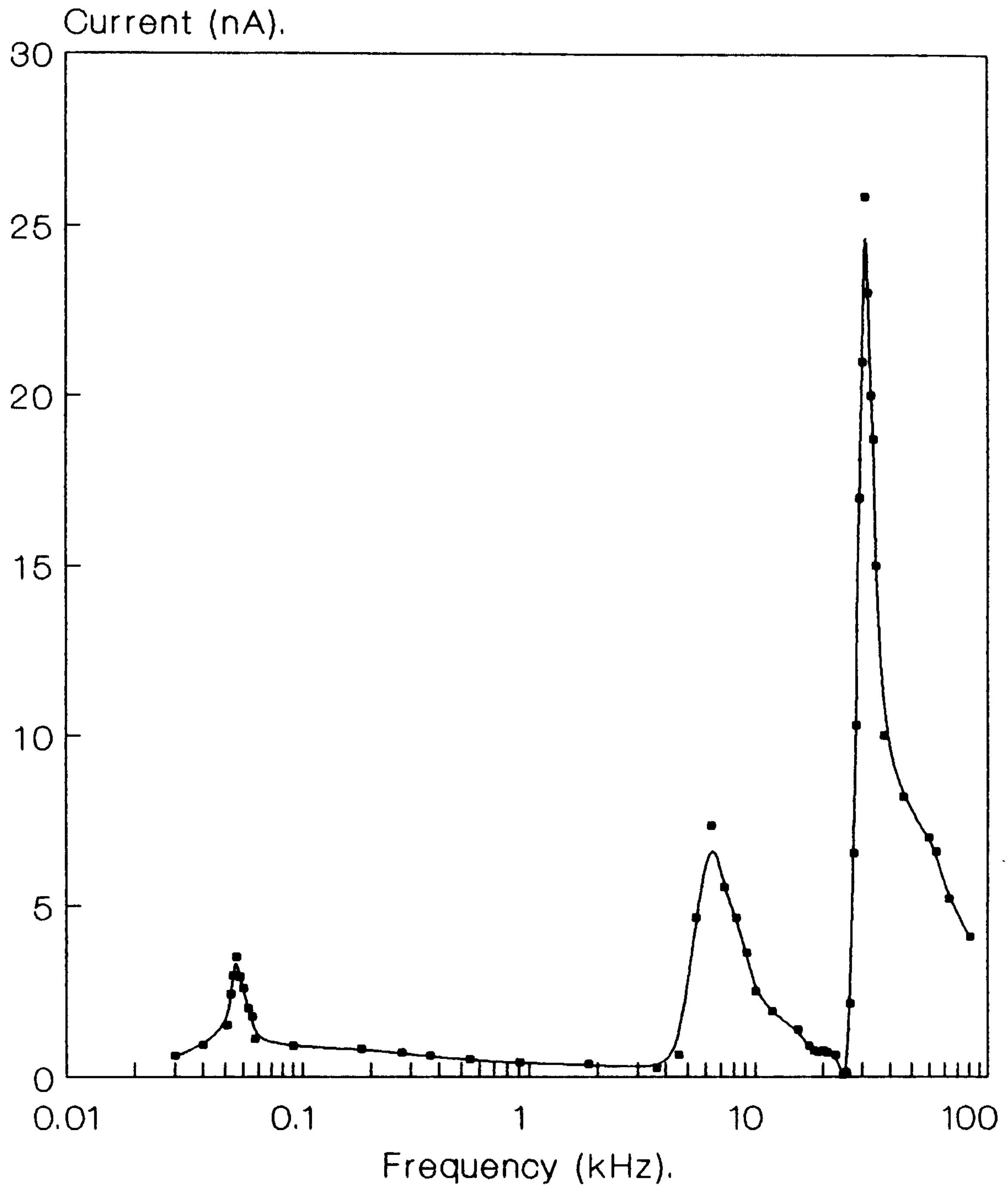


Fig.6.21 I-f curve for a $2mm^2$ MOS diode. Voltage sweep from Vfb=-0.4 to Vt=-1.1V.



DETERMINATION OF FLATBAND AND THRESHOLD VOLTAGES IN MOS DEVICES

In this chapter the optimum frequency corresponding to the third current peak, that has been obtained in the previous experimental results, is used to determine the flatband voltage and the threshold voltage of MOS devices. This study is based on the variation of the optimum frequency with respect to the gate voltage signal as revealed by the f_m-V_G curves.

7.1. INTRODUCTION.

It is already shown in chapter 6 that the current-frequency curves in the complete frequency range from a few tens of hertz to a few hundreds of kilohertz show in general three peaks. The third peak appears in the frequency range from 33 kHz to 44 kHz for the different devices. The exact optimum frequency f_m of the third peak is found to depend upon the following factors:

1. The device geometry (whether it is short or long channel).
2. The location of the bottom and the top levels of the applied gate voltage signal which determines the different experimental versions of the present study.
3. The amplitude of the gate voltage signal.

In order to study the effect of the amplitude of the gate voltage signal on the optimum frequency $\mathbf{f_m}$ of the third peak of the observed substrate current, one of the two extremes (bottom or top) of the signal is fixed at the voltage V_r corresponding to the intrinsic level E_i and the other extreme is changed either towards the threshold voltage V_T or towards the flatband voltage V_{FB} respectively. The optimum frequency $\mathbf{f_m}$ is then measured at different values of the amplitude of the gate voltage signal. The direction of the voltage change required in the different cases are shown for the p and n substrate MOS devices in Fig.5.6 (chap.5).

7.2. DETERMINATION OF THE FLATBAND VOLTAGE.

For the determination of the flatband voltage V_{FB}, the top level of the gate voltage signal for a p-substrate (or bottom level of gate voltage signal for an n-substrate) MOS device is fixed at the voltage V_r and the bottom level (top level for n-substrate) of the signal is increased towards the flatband voltage. The optimum frequency f_m is then obtained at different values of the amplitude V_G of the gate voltage signal and an f_m-V_G curve is plotted. Such graphs, for certain typical devices, are shown in Figs.7.1 to 7.7. Figures 7.1 to 7.5 belong to p-substrate MOSFETs whereas Figs.7.6 and 7.7 belong to n-substrate MOS capacitors.

It may be noted that, in general, all these f_m-V_G curves show in the beginning a decrease in the value of f_m with increase of the amplitude V_G of the gate voltage signal in the case of p-substrate devices. When a certain value of f_m is reached, the f_m-V_G curves show an abrupt decrease between the points A and B. After this abrupt change which terminates at point B, the value of f_m becomes constant and does not show any change with further increase of the amplitude of the signal. However, in the case of n-substrate devices, the curves show an abrupt increase of f_m at the point A and then reaches to another point B after which the value of f_m becomes constant and does not show any change

with any increase of the amplitude of the signal. In fact the total region of abrupt change, which lies between points A and B, is indicative of some change in the physical phenomena governing the MOS structure. However, the region of MOS structure which is most sensitive to the gate signal is the interface $Si-SiO_2$ (see chap.2). Hence, the expected physical phenomena is most likely to be associated with the interface $Si-SiO_2$ behaviour under an oscillating gate voltage. One such physical phenomenon which is known to occur at the $Si-SiO_2$ interface is the switching over of the surface region from depletion to accumulation which occurs at the flatband voltage. When the gate signal is increased towards flatband voltage, the depletion layer starts decreasing till finally it is supposed to vanish at a gate voltage V_G equal to the flatband voltage and this marks the commencement of accumulation layer in the surface region. However, the depletion layer, while decreasing, can not go below the limit defined by the Debye length L_D. It is so because at the depletion width equal to Debye length, the charges on one side of the layer starts exerting their direct influence on the other side. Therefore upto this limiting width of the depletion layer, the surface region remains under depletion condition after which it abruptly changes into accumulation. Accordingly the limits, first when the thickness of the depletion layer is L_D and the other when the depletion layer completely vanishes, should correspond to the points A and B

on the f_m-V_G curve. Based on our above contention the point B on the f_m-V_G curves must correspond to the true value of flatband voltage V_{FB}. Therefore if the point B can be located accurately on the f_m-V_G curve, it can give the precise and accurate value of V_{FB}. However the point B is not obtainable sharply in an experimental f_m-V_G curve due to the limited sensitivity of the function generator. In fact the slanting straight portion AB of the curve represents the abrupt fall in the value of f_m. If this branch could be obtained precisely, then its point of intersection with the remaining horizontal portion of the curve could give precise value of V_{FB}. In practice due to limited sensitivity of the voltage measuring instruments, even the slope of the straight portion AB depends upon how precisely and accurately the points lying on it are determined. Under such limitation of measurements, the present method may be supposed to fix the upper and lower value of V_{FB}. Accordingly, the value of V_{FB} may be taken equal to the average value $(V_1+V_2)/2$ where V_1 and V_2 are the value of the voltages corresponding to two experimental points closest to B with minimum and maximum value of V_{FB} ranging from V_1 to V_2.

It may be pointed out that tracing of the f_m-V_G curves does not require an accurate setting of the voltage V_r and hence the exact knowledge of the intrinsic level E_i. An approximate value of V_r corresponding to E_i can serve the

purpose. In fact the purpose of the knowledge of V_r is to safeguard against any chance of the voltage sweep to enter the other side of E_i. This chance can be avoided, even without knowing the exact value of V_r, by setting the top level of the pulse in the case of p-substrate after leaving a certain margin below V_r. In the case of p-substrate devices, an approximate value of V_r near the ground level, that is, V_r=0 may be initially chosen and the top level of the signal may be fixed a little below V_r. In the case of n-substrate devices, this value of V_r can be obtained only tentatively and right value can be reached only after a few trials. However, once the final value of V_{FB} and V_T are obtained by the present method, the voltage V_r corresponding to E_i can be determined quite accurately. In fact the interval between V_r and V_{FB} in the case of n-substrate is quite small ranging from 0.3 to 0.6 V in most cases and one can not afford to leave a margin of 0.1 or 0.2 V between the top level of signal and V_r and therefore, it is desirable to obtain the value of V_r accurately before plotting the f_m-V_G curves. This value of V_r in the case of n-substrate devices was found to be -0.7 V in the present study. On the other hand, the interval between V_r and V_{FB} is quite large in the case of p-substrate devices and therefore an approximate value of V_r was taken at V_G=0 and a margin of 0.1 to 0.2 volts was left between the top level signal and ground.

Reference is made here to an other method for

measuring the flatband voltage V_{FB}, which has been described by some workers [30,33]. This method is based on the charge pumping technique employing the Elliot version of measuring the charge pumping current [25]. A similar phenomenon has been observed in the case of charge pumping current plotted with respect to the base level of the gate voltage signal [30,33]. The charge pumping current I_{cp} undergoes an abrupt increase from zero to its maximum value after a certain position of the gate pulse base level. It has been assumed that the value of the base voltage corresponding to the half of maximum current $I_{cpm}/2$, in the I_{cp}-V_G curve [25], is the flatband voltage [33]. This assumption is a gross assumption that has no argument and justification. Typical I_{cp}-V_G curves obtained for a sample of devices are shown in Figs.7.15 to 7.17. A comparative study (Table 7.1) is made between the results obtained by the charge pumping method and those obtained by the present technique. Table 7.1 shows that the value as obtained by the present method comes out in general little higher than that obtained by using charge pumping method. Based on the physical arguments as given earlier regarding the process of the occurrence of the abrupt change in the f_m-V_G curve, the present method is supposed to give the true and more reliable value than the charge pumping method. An additional advantage of the present method is that it can be applied equally well to MOS diodes and MOSFETs without any geometric constraints whereas

the charge pumping method applies only to MOSFETs satisfying geometric condition in which channel width W to channel L ratio (W/L) is quite larger than unity.

The present method of measuring the flatband voltage has distinct advantages even on C-V method. It is because the C-V method can only be applied on MOS diodes of large area. Further, the C-V method is quite cumbersome in use. Therefore, its accuracy is subjected to the accuracy of the parameters involved in finding the flatband voltage [13-17]. Besides, the C-V method can not be applied to small area devices. On the other hand in the present method, one can read V_{FB} directly from the f_m-V_G curves and tracing of such a curve does not require the knowledge of any device parameter. For example we could measure the flatband voltage of a commercial 3N 170 n-MOSFET by using the present method which comes out to be -1.6 V volts after reading it directly on the f_m-V_G curve in Fig.7.5. Besides, the method is applicable to small as well as big area devices and also to MOSFETs as well as to MOS diodes. The accuracy of the present method does not depend upon the device parameters and hence the same order of accuracy is expected in small and big area devices. The present method does not involve absolute measurement of either the substrate current or capacitance and hence any uncertainty in the measurement of current or capacitance does not affect the results. The method requires simply the measurement of the frequency at

which the maximum current occurs and the corresponding amplitude of the gate signal. As the current peaks are found to be sharp in the third peak, the determination of the optimum frequency can be obtained quite accurately. In the experiments that have been achieved in the present work, the minimum voltage increment that could be reached is 50 mV and the increment of frequency is 1 kHz, the value of the flat-band voltage as found by this method is subjected to a maximum error corresponding to half of this 50 mV increment. The accuracy can be increased further by the use of more sensitive equipment.

7.3. DETERMINATION OF THE THRESHOLD VOLTAGE.

The first version of the present experimentation employs one extremity of the gate voltage signal to be fixed at V_r and the other extremity is allowed to swing towards the flatband voltage V_{FB} of the given MOS device. It has been shown in section 7.2 how it can be exploited for the determination of the flatband voltage of the device. In a similar manner, the second version of the experiments employs one extremity of the gate voltage signal to be fixed at V_r and the other is allowed to swing towards the threshold voltage V_T of the given MOS device.

Referring to Fig.5.6, it may be seen that, in the case of p-substrate MOS devices, the second version of

experiments necessitates fixing the bottom of the gate voltage signal at V_r and its top to increase towards V_T which is positive. For the n-substrate MOS devices, as shown in the same figure, the top level of the gate voltage signal is fixed at V_r whereas the bottom level of the signal is increased towards V_T which is negative. In both cases, the optimum frequency f_m is measured for different values of the gate voltage V_G. The f_m-V_G curves have been plotted for the same typical devices as used earlier in the last section for the determination of the flatband voltage. These curves are shown in Figs.7.8 to 7.12 for p-substrate MOSFETs and in Figs.7.13 and 7.14 for n-substrate MOS diodes. In both the cases, the f_m-V_G curves show the same general trend as in the case of the determination of the flatband voltage. In the case of p-substrate devices, the value of f_m at first decreases with increase of the amplitude V_G of the gate signal towards positive side till the value of f_m reaches the first point A of the abrupt change. Thereafter, f_m drastically decreases to another point B where it attains a constant value and does not show any further change with increase of the amplitude of the gate voltage. The interval defined by the points A and B represents the region during which the device switches over from depletion condition to inversion condition in the surface of the device. Following the same argument as in the case of the flatband voltage it

is the point B where the switching process should be complete and should correspond to threshold voltage V_T.

The other methods which are used for the determination of the threshold voltage are only applicable to MOSFETs. The conventional method employs plotting of I_D-V_{GS} curve [45,46]. However, this method is subjected to errors involved in the extrapolation of the value of V_T from the I_D-V_{GS} curve. The value of V_T corresponds to the gate voltage V_{GS} at which the surface region enters into inversion and the channel starts conducting. The current I_D is taken to be the measure of the channel conduction. A certain criterion is fixed about the value of the current at which the surface region is supposed to enter into inversion. According to this criterion, the appropriate value of V_T corresponds to the gate voltage necessary for the channel to conduct a current of 10 $\mu Amps$ when the drain and source are connected to a known voltage source (in commercial devices, this value of the voltage source is specified by the manufacturer).

Another method used to determine the threshold voltage is the charge pumping technique. This technique is used in the same manner as for the case of flatband voltage determination but the current abruptly decreases from its maximum value to zero [25,30]. However, the value of the base voltage corresponding to $I_{cpm}/2$ is not the threshold voltage but, it is the value $V_T-\delta V$ where δV is the pulse

amplitude [25]. The curves giving the threshold voltage as given by the charge pumping technique are illustrated in Figs.7.15 to 7.17. The values of threshold voltages obtained by the present method as well as the charge pumping method for typical devices are given in table 7.1. Table 7.1 shows that the values obtained by the present method are somewhat different from that obtained by the charge pumping method.

Both the charge pumping technique as well as the I_D-V_{GS} method are not applicable to MOS diodes. So far, there is no known method used to determine the threshold voltage in MOS diodes. However the present method gives the threshold voltage for MOS transistors as well as for MOS diode as it is illustrated in Figs.7.8 to 7.14. In addition, it gives the "true threshold" voltage for MOS transistors that is, the threshold voltage is not related to the conduction of the channel of the transistor.

Table 7.1 Threshold and flatband voltage values as obtained by the charge pumping technique and their corresponding values obtained by the present technique for typical devices.

MOS Transi-stror. Geometry (um)	Results obtained using the Charge Pumping Technique		Results obtained using the present (proposed) method	
	Flatband Voltage.	Threshold Voltage.	Flatband Voltage.	Threshold Voltage.
300x8	-0.9 V	1.0 V	-1.1 V	1.3 V
300x20	-0.8 V	1.1 V	-1.0 V	1.2 V
3N 170	-1.4 V	1.5 V	-1.6 V	1.6 V

Fig.7.1 Maximum frequency (fm) versus gate voltage for a 300x8 um^{2}n-MOSFET.

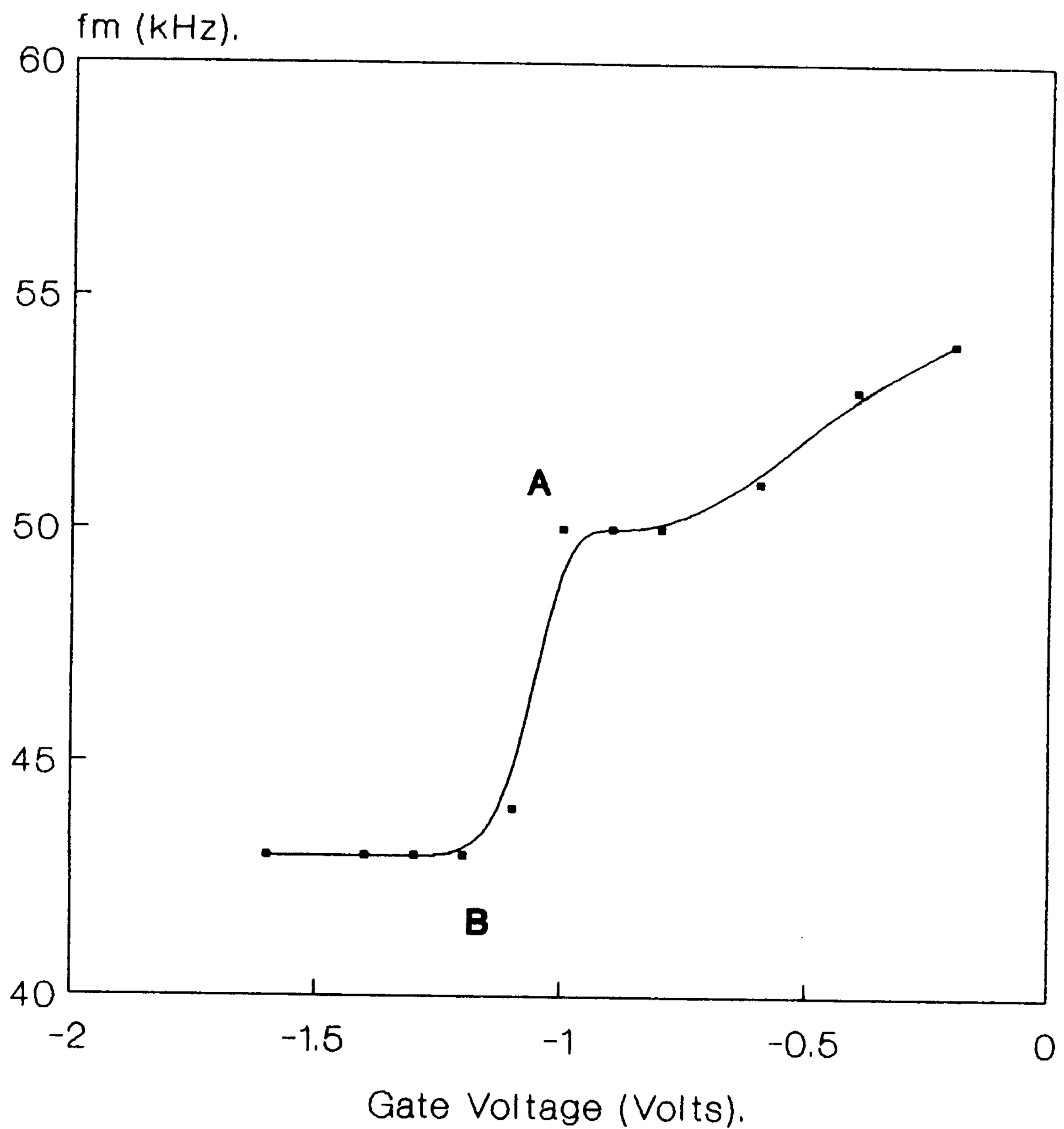


Fig.7.2 Maximum frequency (fm) versus gate voltage for a 300x20 um^2 n-MOSFET.

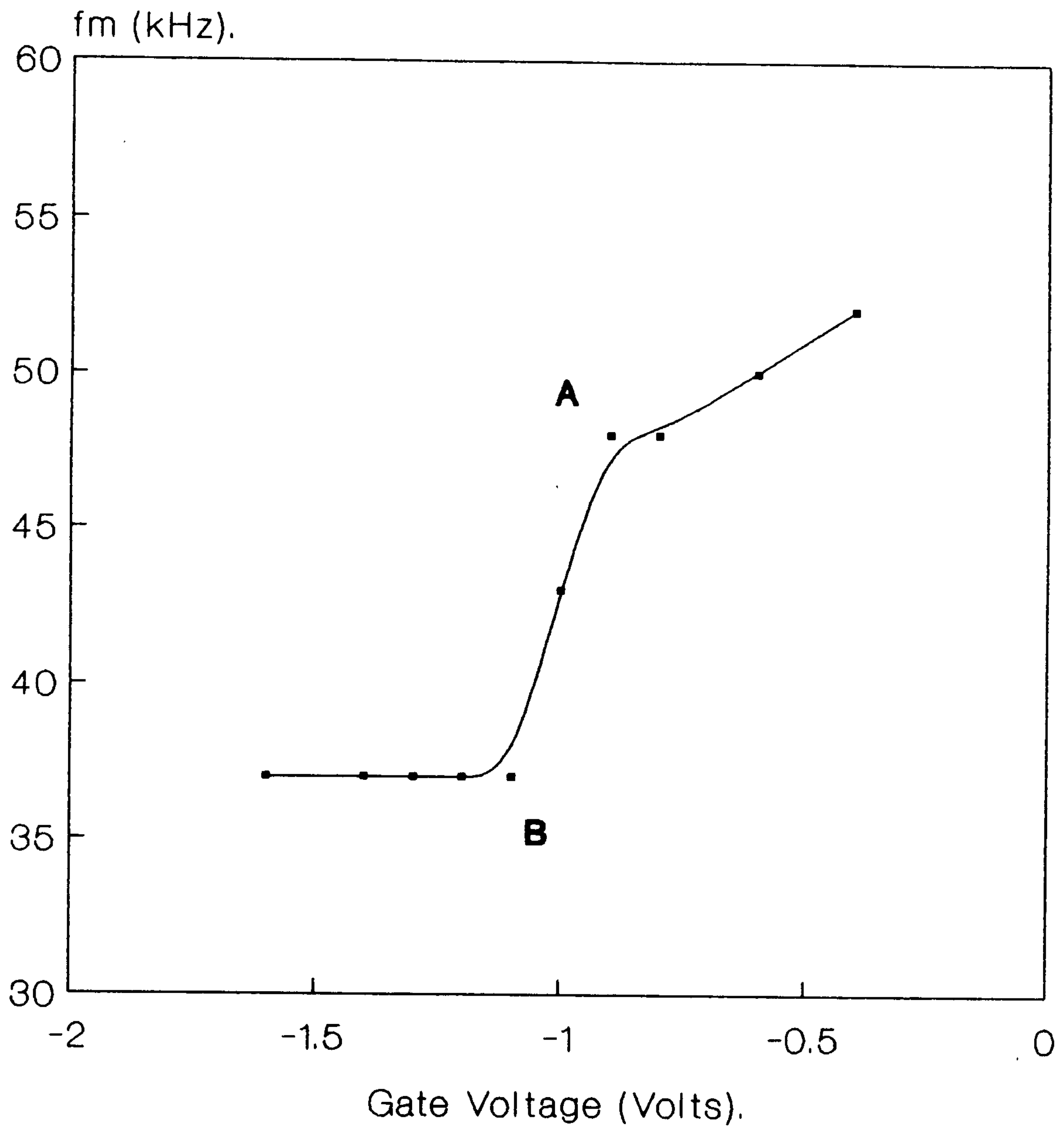


Fig.7.3 Maximum frequency (fm) versus gate voltage for a 80x80 um^2 n-MOSFET.

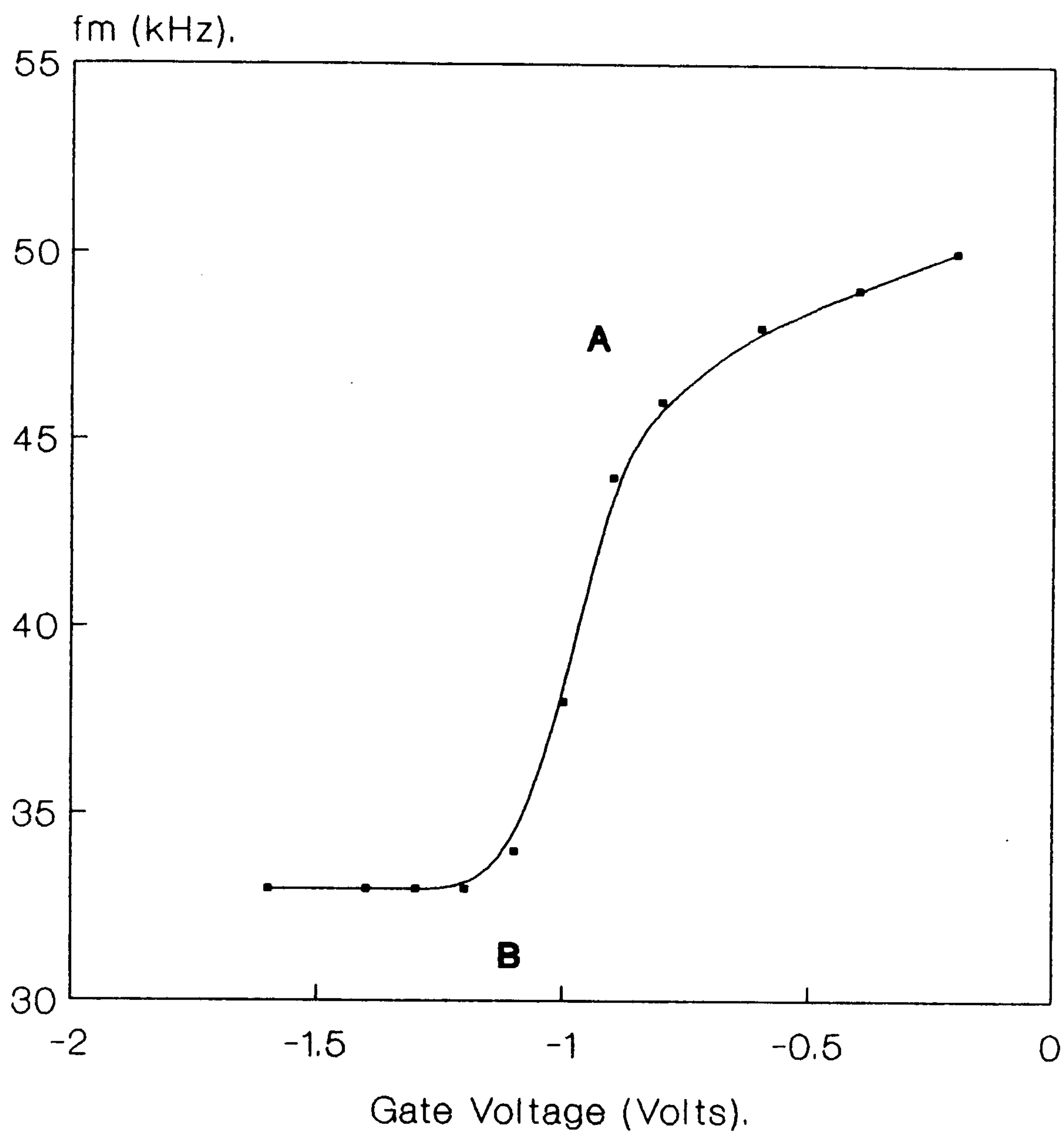


Fig.7.4 Maximum frequency (fm) versus gate voltage for a 300x80 um^2 n-MOSFET.

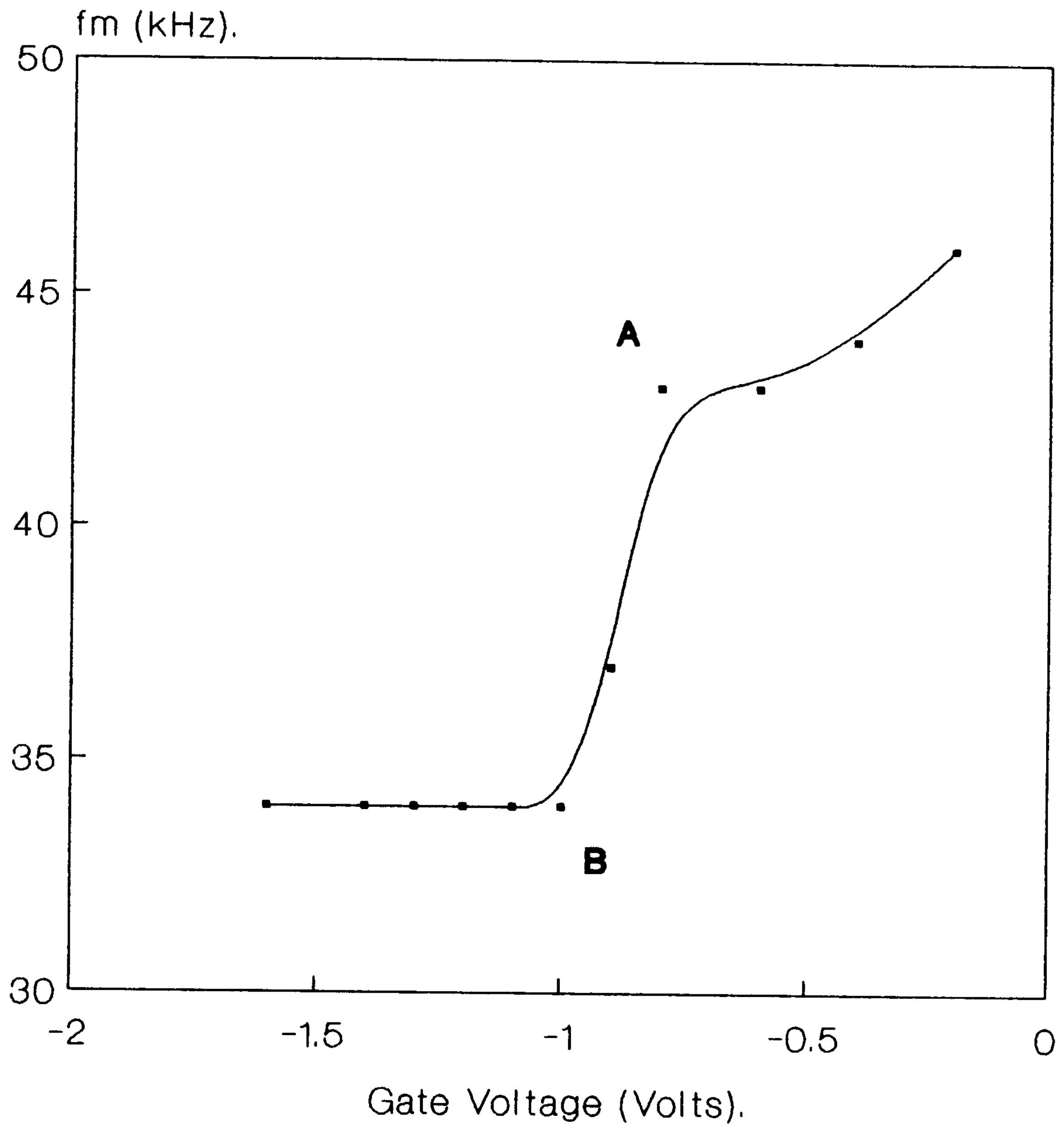


Fig.7.5 Maximum frequency (fm) versus gate voltage for a 3N 170 n-MOSFET.

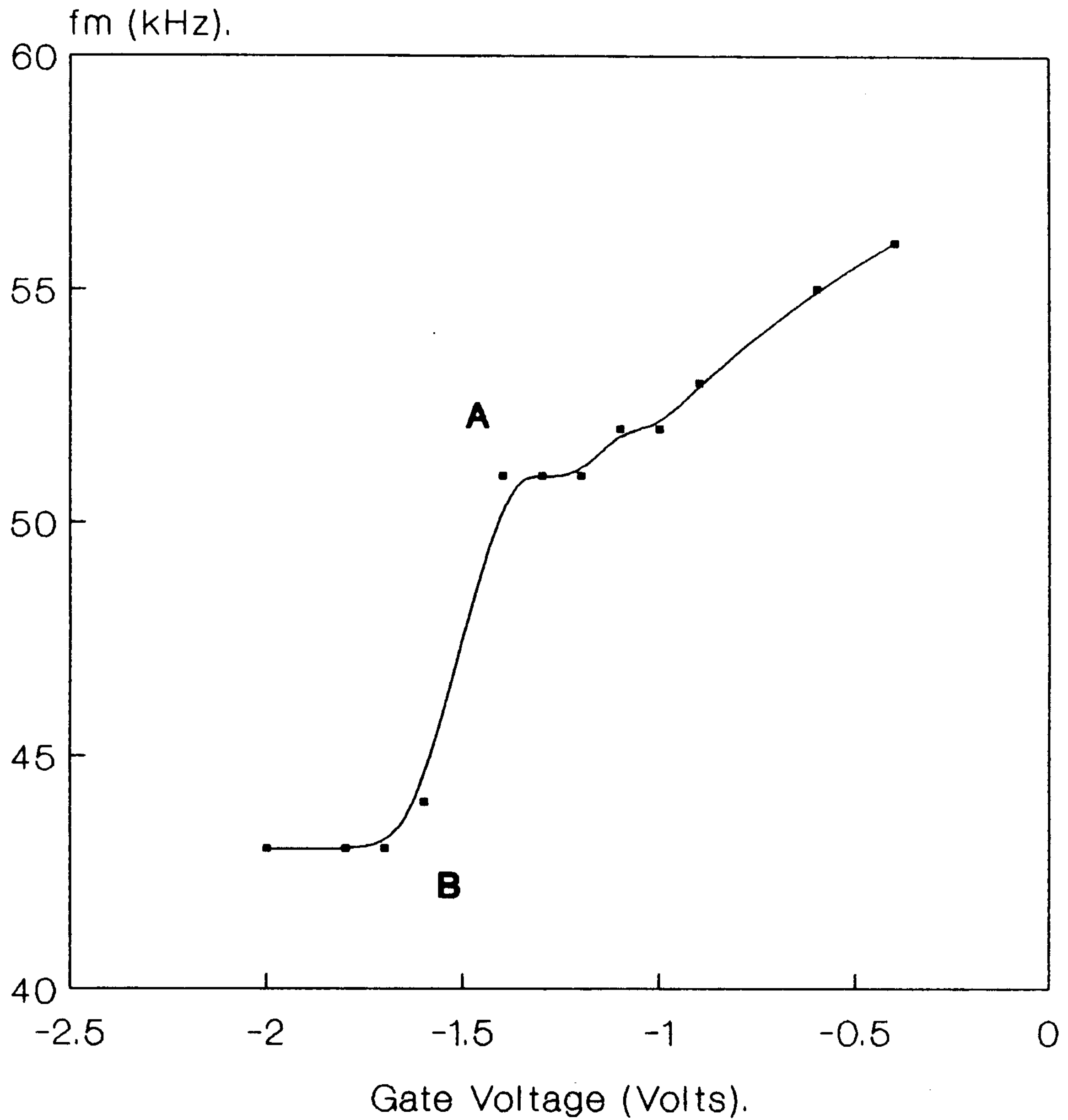


Fig.7.6 Maximum frequency (fm) versus gate voltage for a 0.5 mm^2 n-MOS diode.

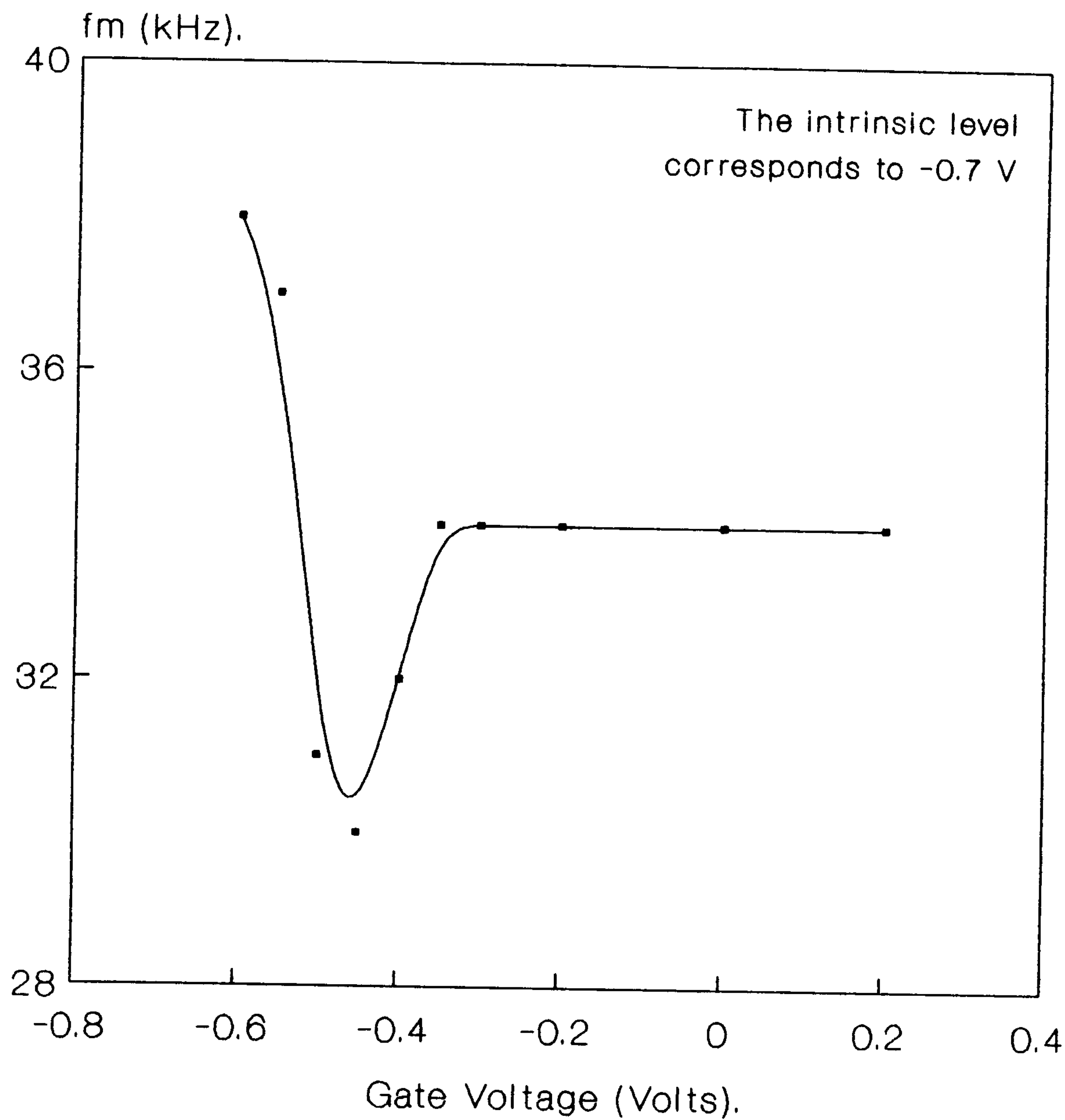


Fig.7.7 Maximum frequency (fm) versus gate voltage for a 2 mm^2 n-MOS diode.

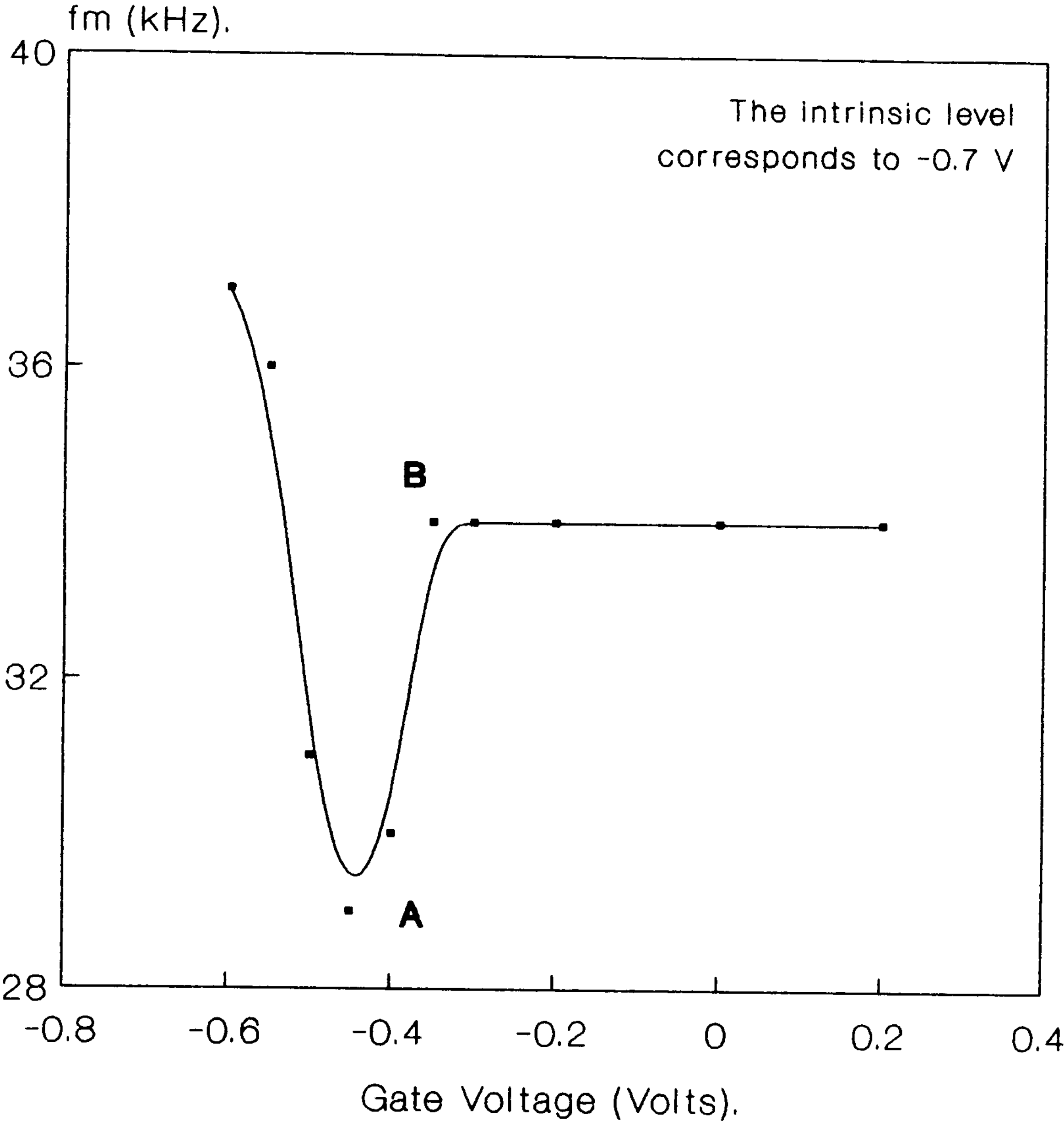


Fig.7.8 Maximum frequency (fm) versus gate voltage for a 300x8 um^2 n-MOSFET.

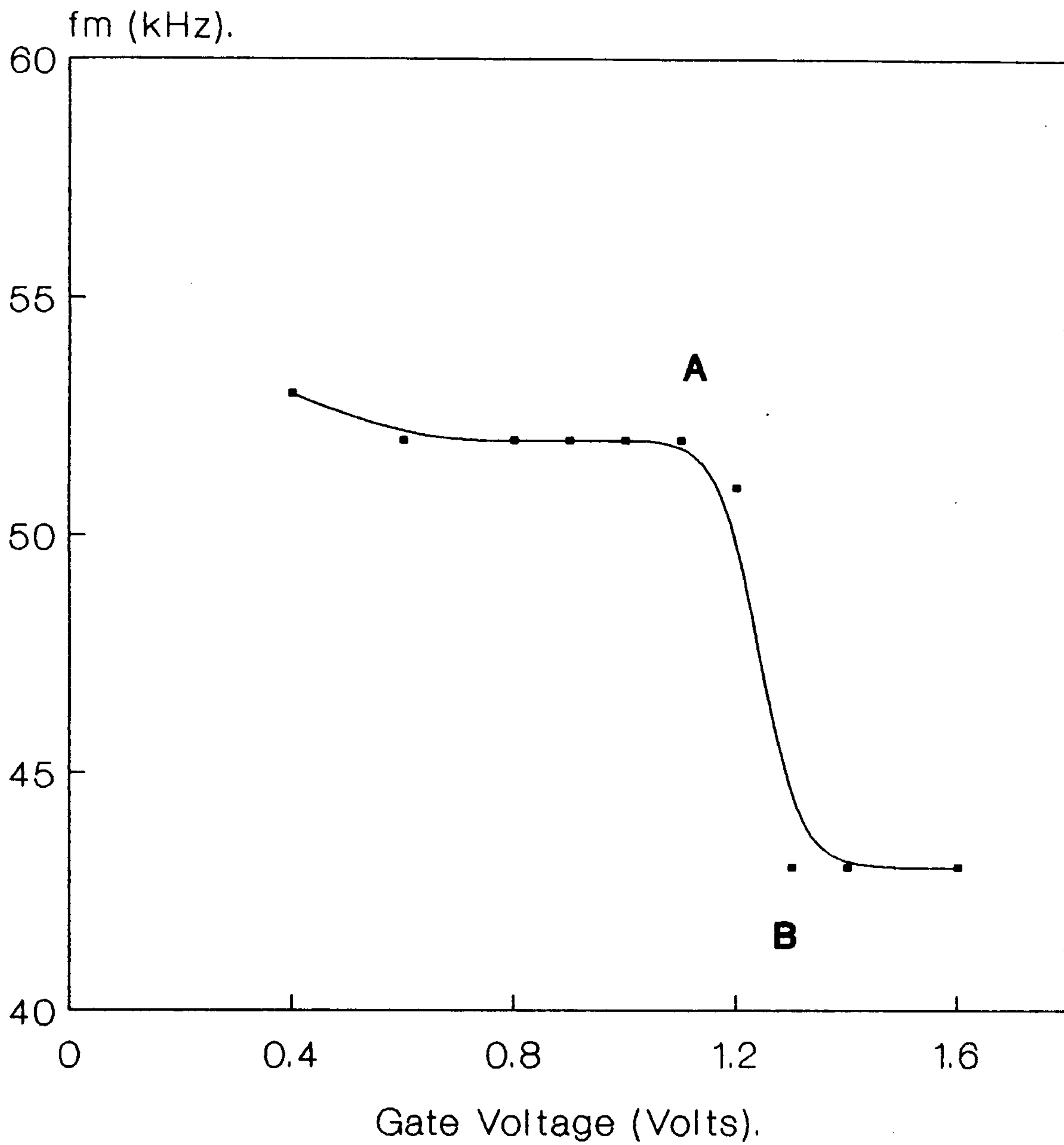


Fig.7.9 Maximum frequency (fm) versus gate voltage for a 300x20 um^2 n-MOSFET.

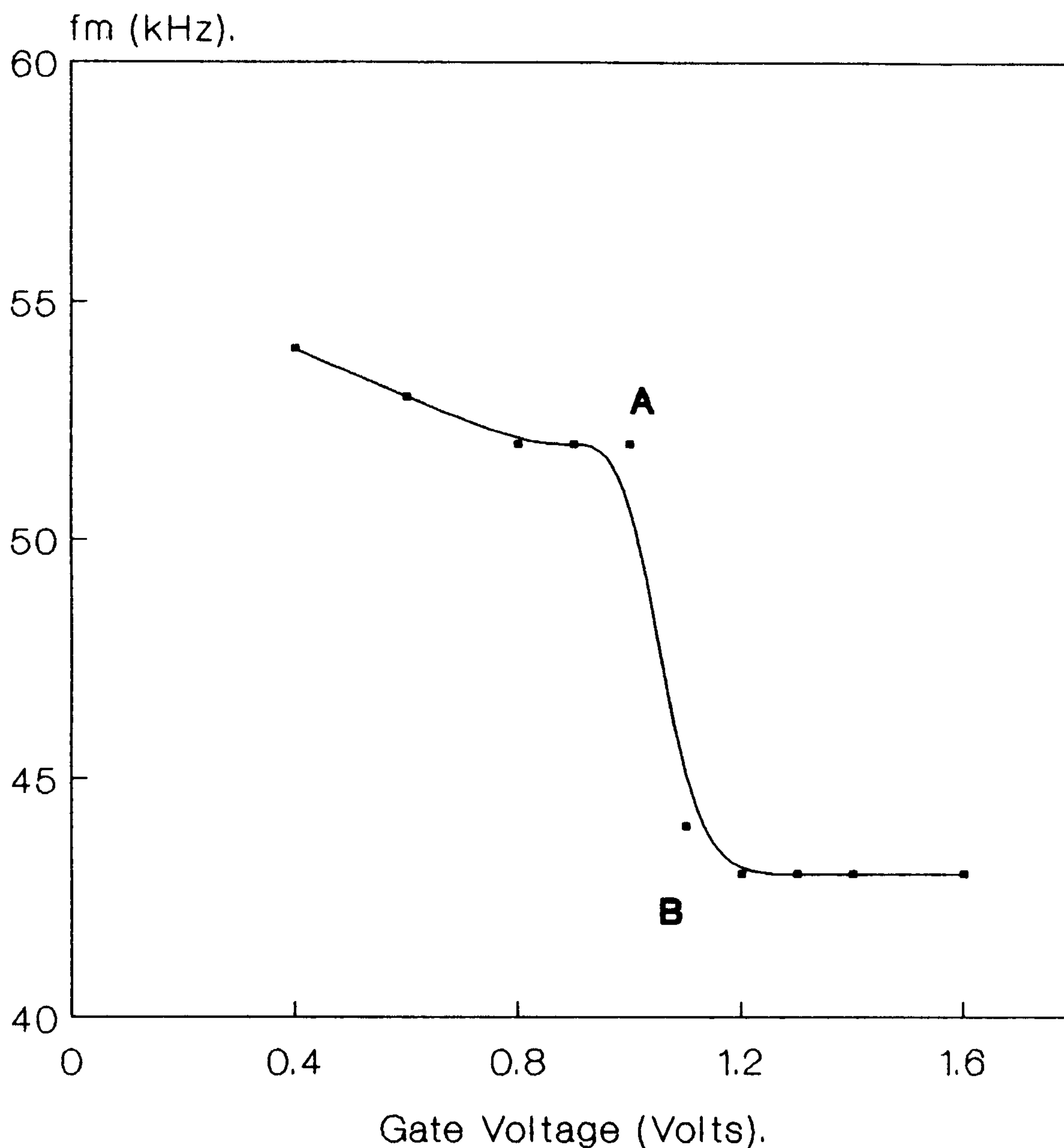


Fig.7.10 Maximum frequency (fm) versus gate voltage for a 80x80 um² n-MOSFET.

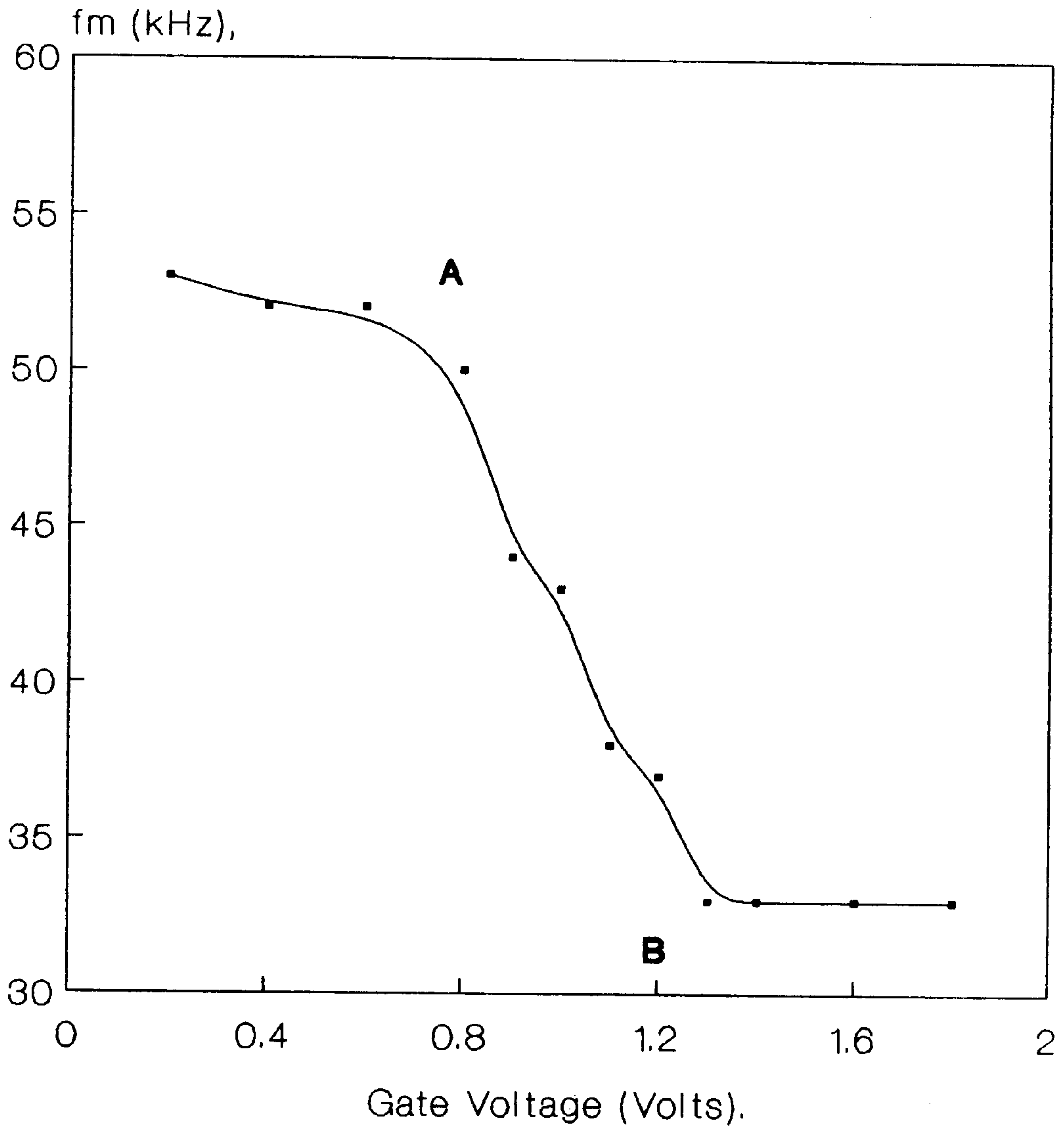


Fig.7.11 Maximum frequency (fm) versus gate voltage for a 300x80 um^2 n-MOSFET.

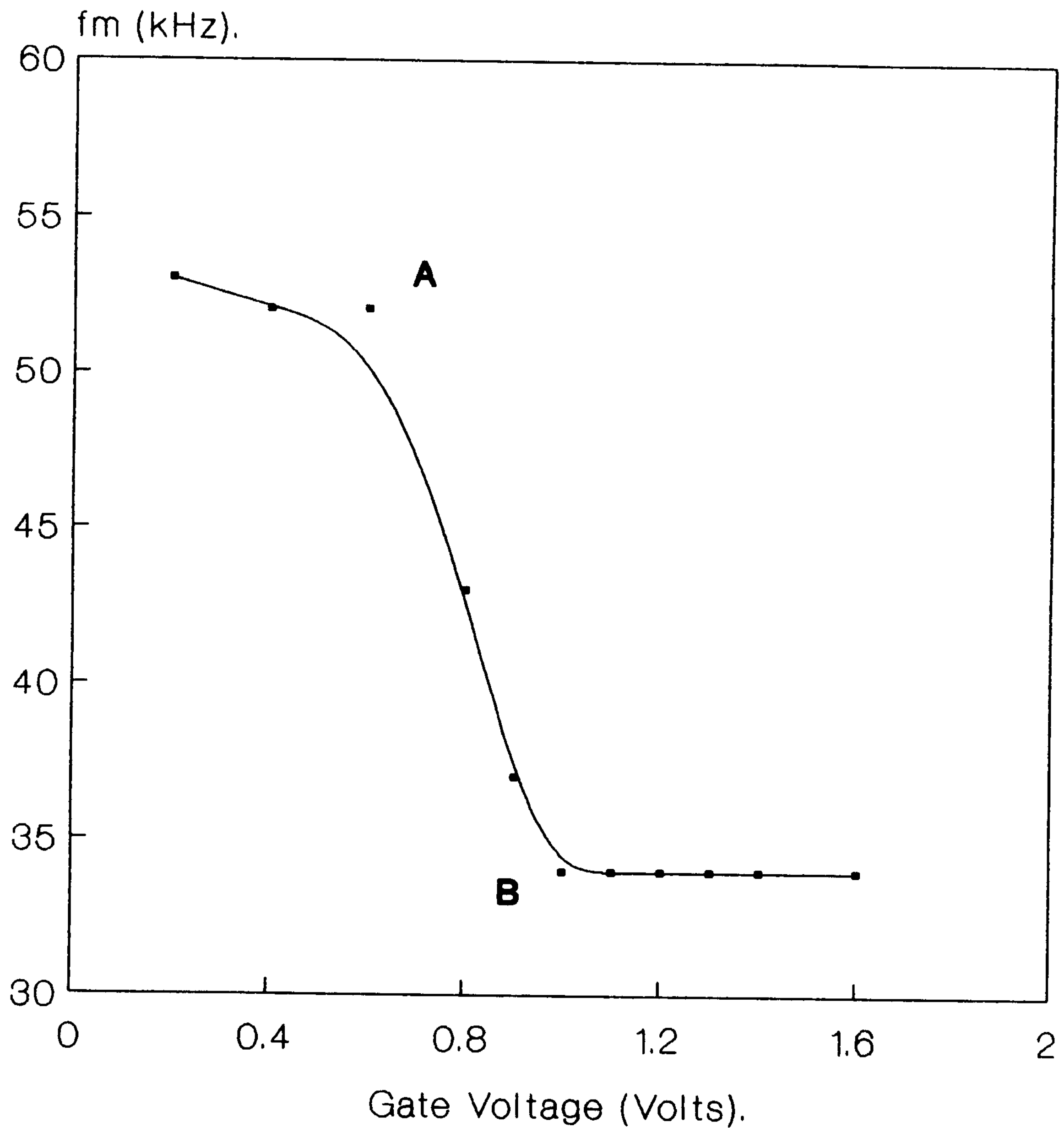


Fig.7.12 Maximum frequency (fm) versus gate voltage for a 3N 170 n-MOSFET.

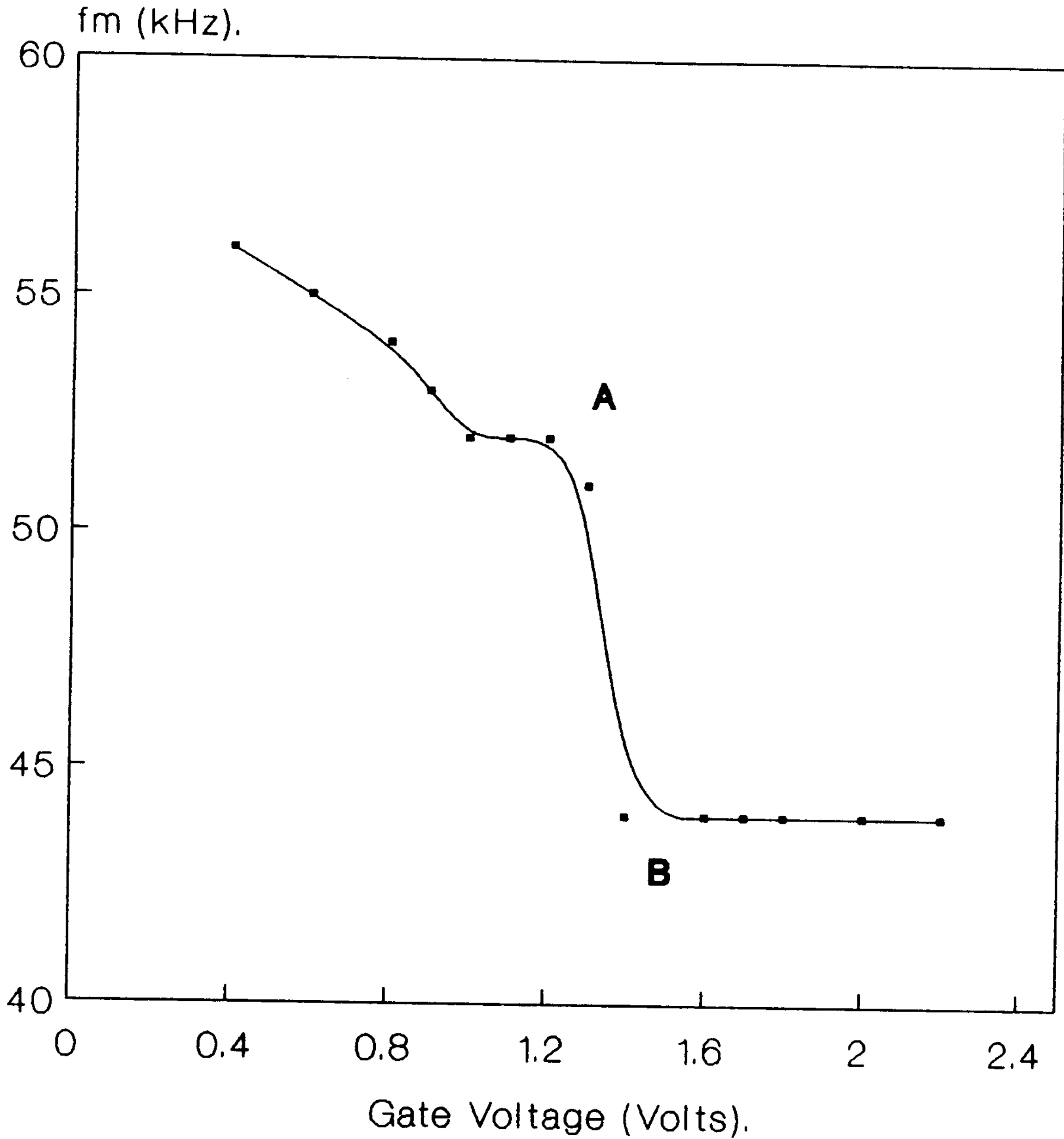


Fig.7.13 Maximum frequency (fm) versus gate voltage for a 0.5 mm^2 n-MOS diode.

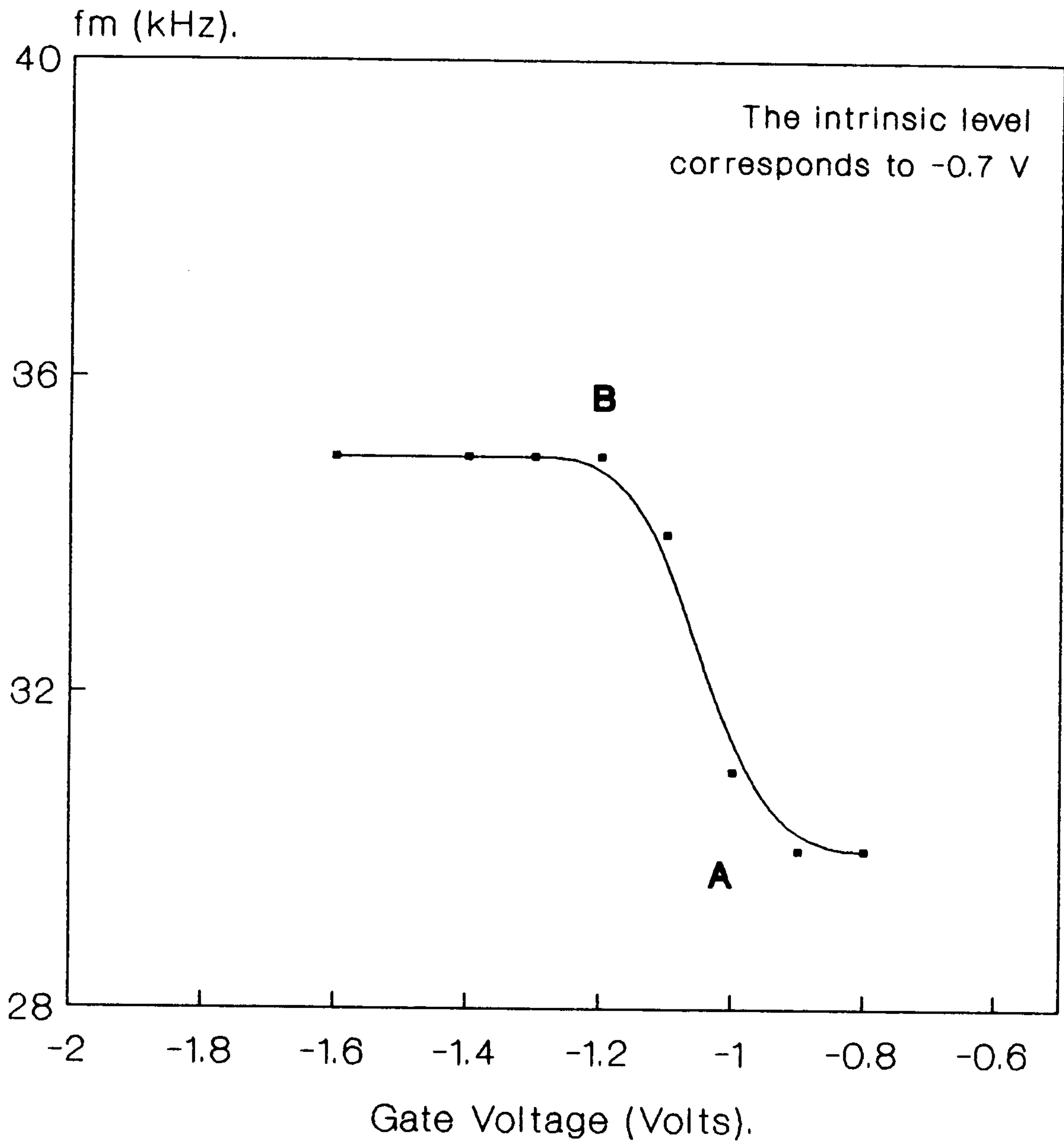


Fig.7.14 Maximum frequency (fm) versus gate voltage for a 2 mm^2 n-MOS diode.

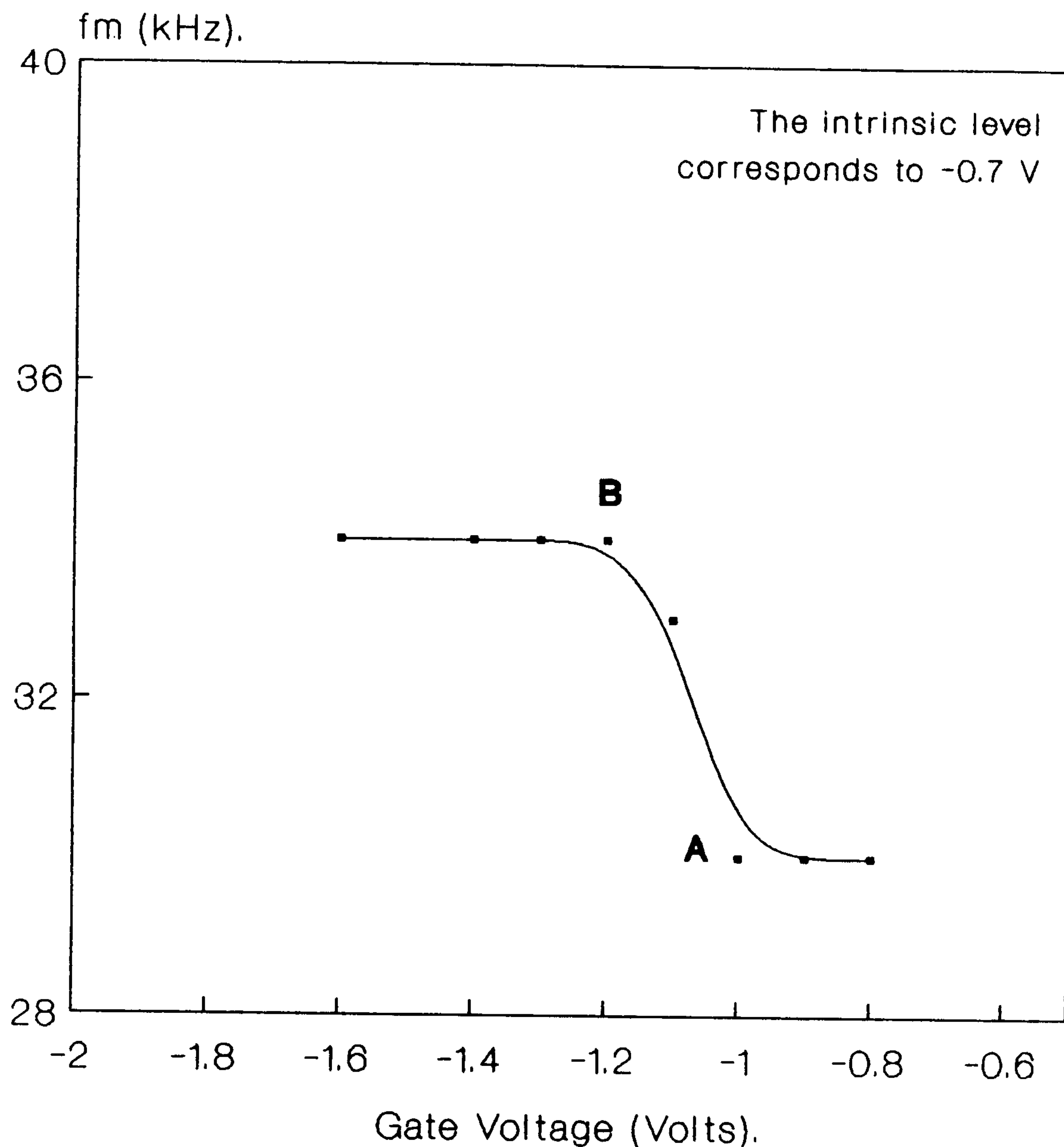


Fig.7.15 Elliot curve of charge pumping current measurement for a 300x8 um^2 n-MOSFET. Dv=5.0V, Vr=0.3V, and f=10 kHz.

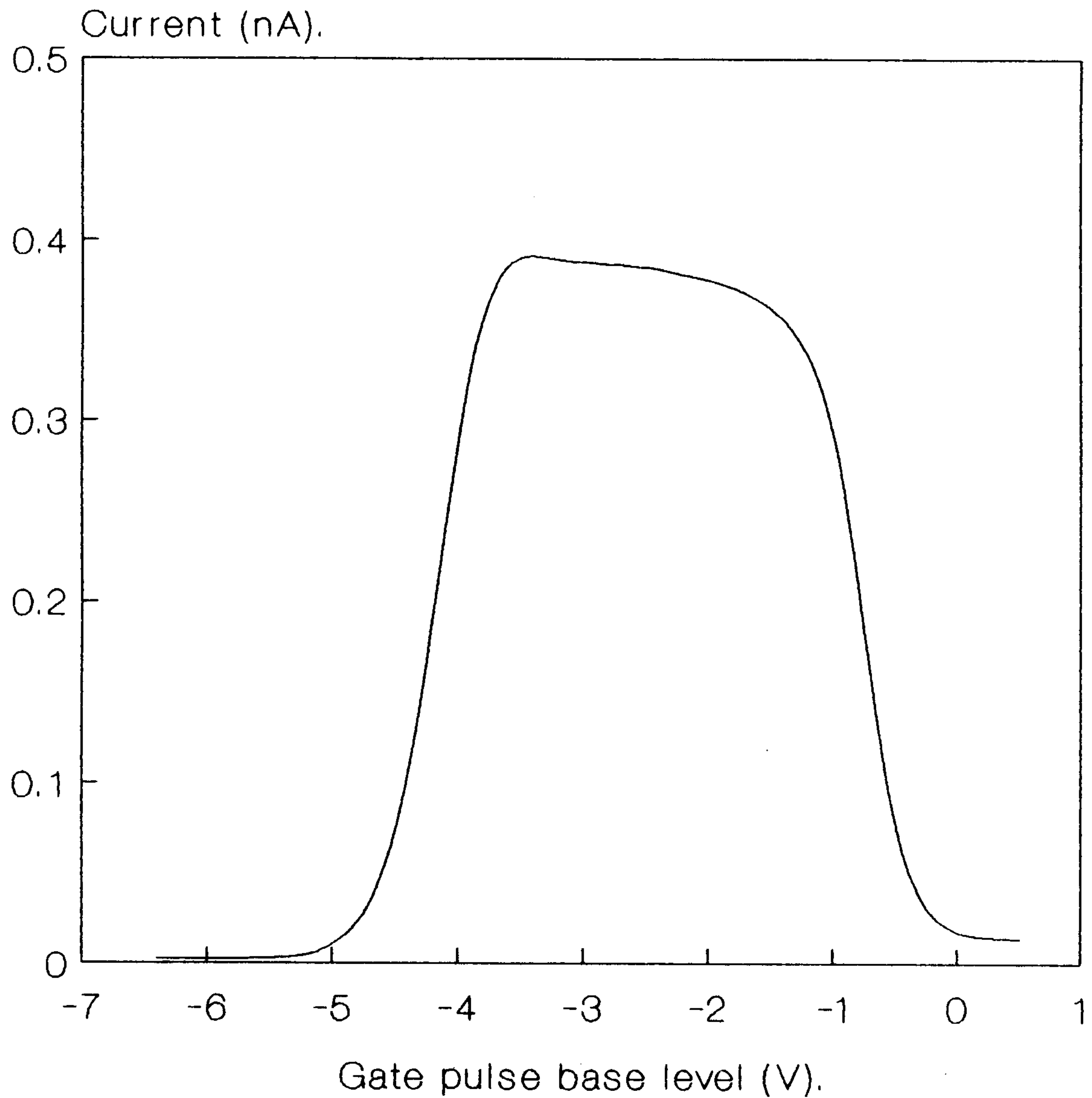


Fig.7.16 Elliot curve of charge pumping measurement for a 3N 170 n-MOSFET. Dv=7 V, Vr=0.5 V, and f=20 kHz.

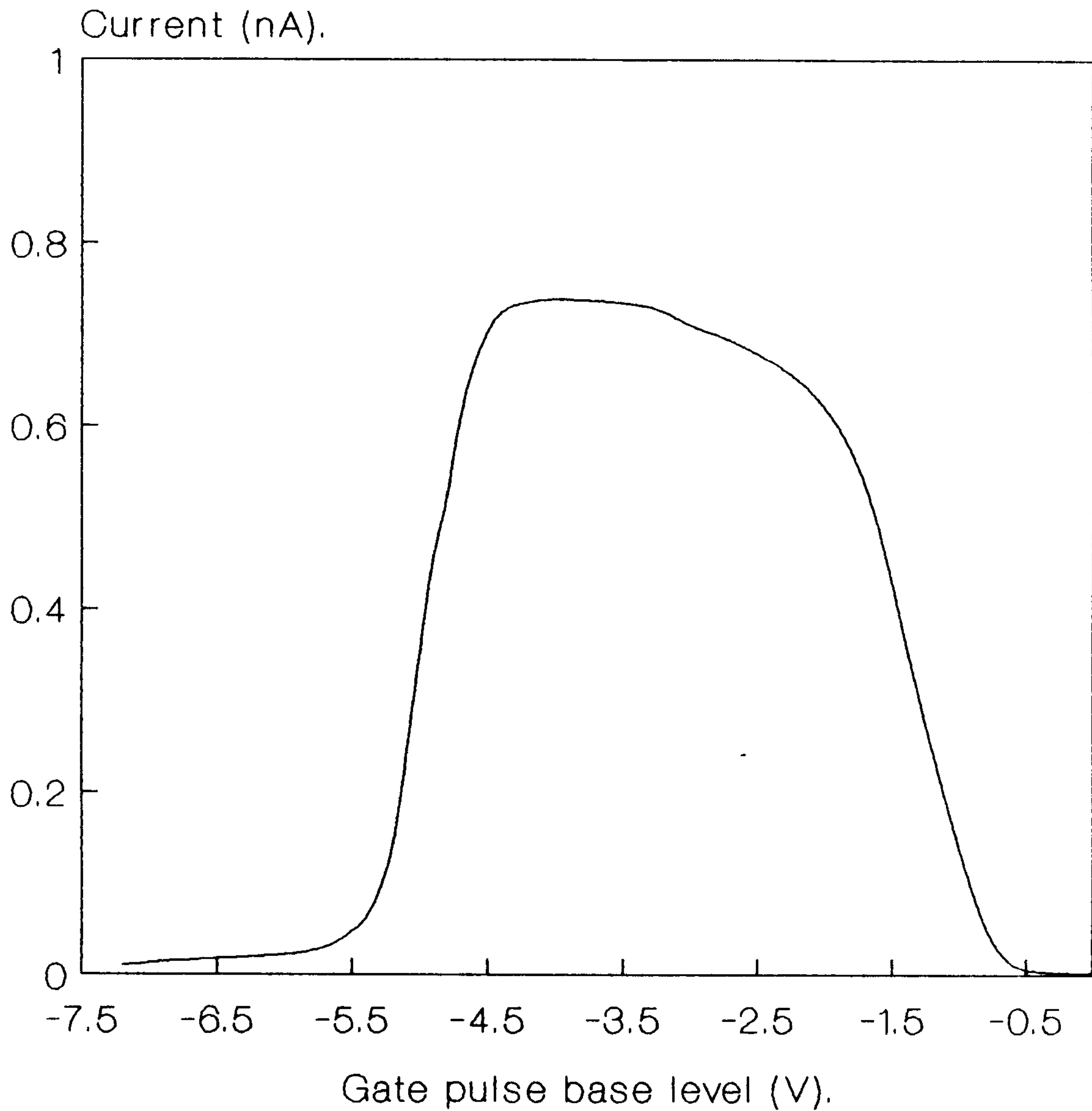
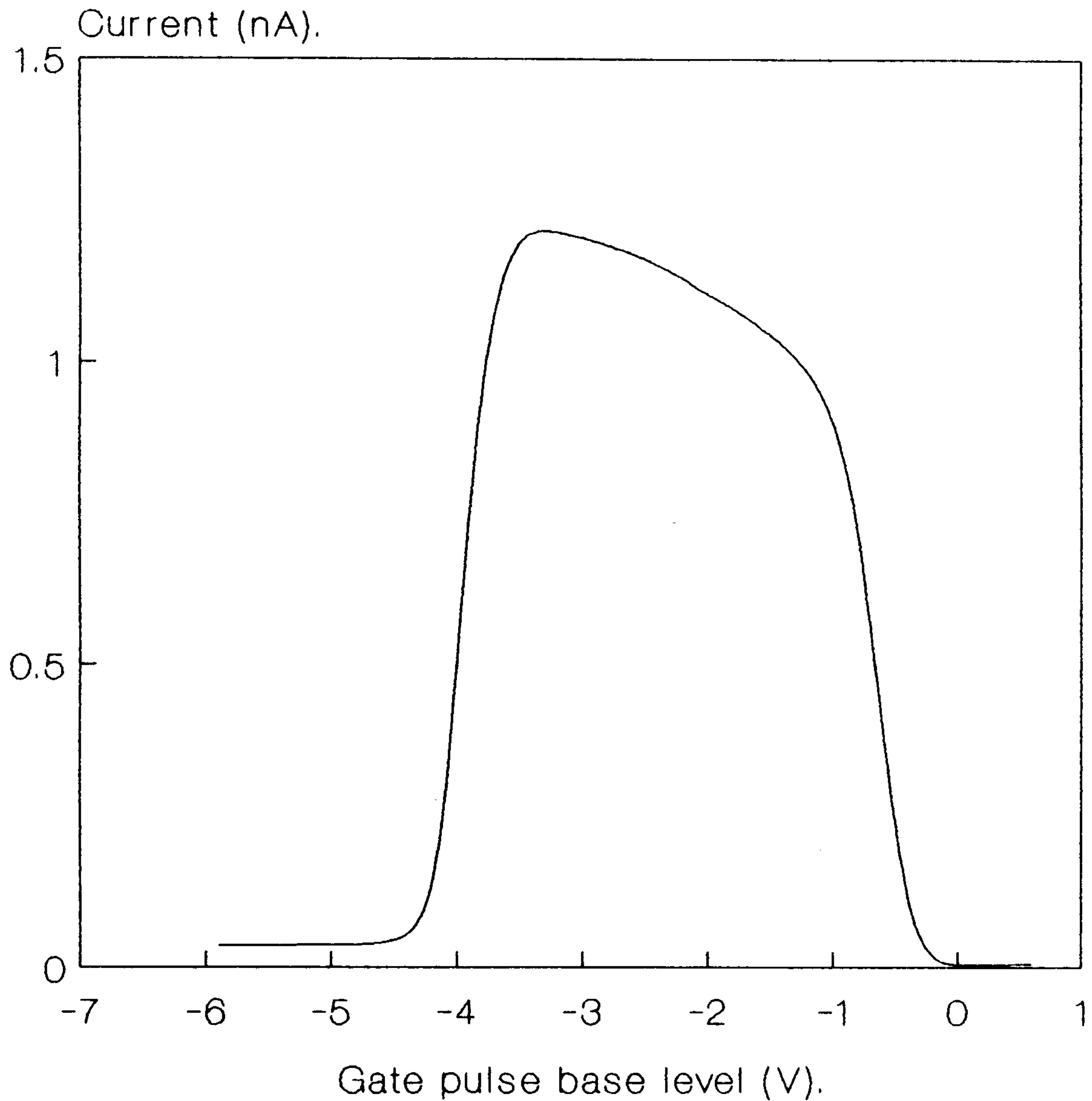


FIG.7.17 Elliot curve of charge pumping current measurement for a 300x20 um^2 n-MOSFET. Dv=5.0V, Vr=0.2V, and f=10kHz



CONCLUSION AND FURTHER SCOPE

The aim of the present work was to study the effect of frequency, amplitude, and position of the gate pulse signal on the substrate current in MOS devices. Broadly, the work can be divided into three parts. The first part deals with the experimental development that made possible various experiments that have not been yet carried out on MOS device. The purpose of the second part was to collect data and achieve a survey of the experimental results. The last part was meant for the interpretation and use of the experimental observations.

The experimental work was achieved on MOS devices fabricated for this research by the ES2 laboratory. These devices include both MOS transistors as well as MOS diodes. Besides, commercial devices have been also used. In all cases, when the frequency of the gate pulse signal is varied from a few tens of hertz to a few hundreds of kilohertz, in general, three current peaks have been observed in substrate current versus frequency curves. The large area devices, either MOSFETs or MOS diodes, show three current peaks; the first occurs at 56 Hz, the second at 9 kHz, and the third at 33 kHz. The small area devices show only two current peaks; the first occurs at 70 Hz and the third at 44 kHz (the second peak is not present). The occurrence of the current peaks is found in both n-type as well as p-type MOS devices.

The present study has been carried out basically with the purpose of observing if the non-steady state emission of the surface traps existing on the $Si-SiO_2$ interface can also contribute to the substrate current. Accordingly, as stated in chapter 6, the gate voltage pulse was not allowed to exceed the flatband voltage V_{FB} on one side and the threshold voltage V_T on the other so that the surface region does not enter the inversion or accumulation condition. This is in contrast to the charge pumping method in

which the gate voltage pulse is allowed to exceed V_{FB} and V_T so that the surface region enters alternately into accumulation and inversion resulting into alternate charging and discharging of the surface traps. This charging and discharging of the surface traps results into a net dc substrate current. The necessary charge to maintain this current is supplied by the drain and source during the gate voltage swing when the surface region enters into inversion. Since in our experiments, the surface region is not allowed to enter into inversion, the use of the drain/source is not necessary and is avoided by either keeping the drain/source open in the case of MOSFETs or by making use of MOS capacitors. The occurrence of dc substrate current even in this case, leaves only one possibility in which the charge required for this current is extracted from the gate through the oxide. This current is henceforth called *charge extraction current*. Each main dc current measurement is preceded by a leakage current measurement by applying the rms value of the gate voltage signal and this leakage current is never found more than 5% of the observed dc substrate current. The only other process which can explain the existence of the observed dc substrate current is the charging and discharging of traps existing on the Si-SiO_2 interface of the MOS structure under the action of an oscillating gate voltage signal as a result of which a net negative charge, flowing from the substrate to ground, is derived from the gate

through the oxide.

Based on this idea a theoretical model to explain the occurrence of the first current peak in the I_{sub}-f curves has been put forward by some other member of our research group [47] which explains the observed optimum frequency of the first peak. This model is based on the general theory of Simmons and Wei [41] of the dynamic characteristics of a MIS capacitor having distributed surface traps. According to the theoretical model, if the surface potential is changed under an oscillating gate voltage signal from a certain higher to lower value or vice versa, the carriers are emitted from the interface traps upto a certain lowest level whose value depends upon the emission time or the frequency of the applied gate voltage signal. Thus holes are emitted during the forward half and electrons during the reverse half of the applied gate voltage signal. Out of the two surface potential sweeps corresponding to the forward and reverse gate voltage polarity, the common surface potential interval is supposed to be the required energy interval in which alternate charging and discharging of the surface traps can be obtained and give rise to a net dc substrate current. The commonly observed value of the capture cross sections of electrons and holes as determined by the conductance method [22] fit nicely in the expression of the optimum frequency f_m of the first current peak obtained after following these lines of analytical approach.

However at higher frequencies corresponding to the second or third peak, a different value of the carrier capture cross section is needed. In order to work out a general model which can explain the occurrence of all the observed current peaks one needs a precise dependence of the capture cross section on the other factors such as frequency which is not known. An alternative approach could be to make an attempt for a model using the idea of cumulative emission of carriers in which the same condition of optimum frequency as for the first peak is satisfied after each fixed number of cycles of the applied gate voltage. A third approach, in which second and third current peaks are produced under the combined effect of the above two effects, may also be used. However before such a model could be worked out successfully, it needs clear understanding of the capture cross section of carriers itself. A great deal of confusion and misunderstanding seems to be prevailing over this quantity and different estimate yield different values differing by several orders of magnitude. One striking point about the variation of the value of the capture cross section is that it mainly depends upon the oxide properties. Therefore the contention which has been already advanced in working out the model [47] of the optimum frequency of the first peak that there seems to be two values of capture cross section for carriers, one silicon aided and the other oxide aided, seems to bear relevance with the main crux of the problem

and needs thorough investigations. Therefore a more general model needs solving a few more fundamental issues before it can be worked out. In view of this, the attention of the present study was focussed mainly to see a possibility if some practical use of the present observations can be made. Accordingly use of the third peak has been made successfully to measure the flatband and threshold voltages.

A survey of the different observations, either in the form of data or curves, reveals that these observations can throw light on certain other characteristics of the device. Accordingly these observations can be put to some other applications also besides the determination of the flatband and threshold voltages.

A study of f_m-V_G curves, as shown in Figs.7.1 to 7.14 can help in identifying the type of the substrate used in MOS devices, that is, whether it is n- or p-type. An inspection of these f_m-V_G curves shows that the overall shape of the curve is quite different for n and p substrate MOS devices. Whereas p substrate devices show an abrupt decrease, n substrate devices show an abrupt increase in the value of frequency f_m before it attains a final constant value. The idea about the type of substrate can be had from the determination of I_{sub}-f curves also. For example the polarity of the gate voltage pulse needed to obtain these curves are different in the two cases. In p-substrate

devices, keeping one extremity of the gate voltage pulse fixed at V=0, the other extremity of the gate voltage may be varied either to positive or negative side and both the cases give rise to the identical current peaks (two for small channel and three for large channel devices). However in n substrate devices, if the same procedure is followed, that is fixing one extremity of the gate voltage pulse at V=0 and the other is varied towards negative or positive sides, three peaks are obtained in the former whereas no peak is obtained in the latter. In this way mere plotting of I_{sub}-f curves under the case when base level of the gate voltage pulse is at V=0 and top level is varied towards positive voltage, can give the idea what type of substrate is used in a given device. If the above procedure shows current peaks in the I_{sub}-f curve it is a p substrate device, if not then it is an n substrate device.

The present study can be used to determine the average density distribution and energy distribution of surface traps at the Si-SiO_2 interface. Determination of the average density of surface traps is already done [47] by other member of our research group using the present method. Determination of the density distribution of surface traps needs a more general model which can give the optimum frequency of the other current peaks as well. However a rough idea how energy distribution affects the optimum frequency

can be obtained using energy distribution D_{it} characterized by an assumed simple form $D_{it} \propto E^n$ where E is measured from the intrinsic level E_i and n is an index. Numerical computation under this simple case shows that the optimum frequency of the first peak decreases with increase of power index n. Earlier investigations on the energy distribution of the surface traps [48-51] show that it is nearly of a parabolic form. Therefore, a more general distribution of the form $D_{it} = A + B.(E - E_o)^n$ may be assumed which needs four known equations in terms of D_{it} for computation. Two equations, first relating the optimum frequency of the first current peak and the other for its corresponding current, are already known from the model of the first peak. If a similar model is developed for one or more peaks, then it will be sufficient to compute the overall energy distribution of the surface traps without going into point to point experimental determination of the density of surface traps at different energies.

An other striking observation is about the optimum frequency of the current peaks especially the first and third peaks. The optimum frequency of these peaks shows dependence on the channel length of the device. For small channel length, the optimum frequencies of these peaks are 70 Hz for the first and 44 kHz for the third peak. These values are 56 Hz and 33 kHz for large channel length

devices. This difference of behaviour seems to be related to some change caused in the device due to the diffusion of the drain/source. In large channel devices, the effect of drain/source diffusion is not likely to cause significant change in the behavior of the device as evidenced by the fact that the optimum frequencies for large channel devices are the same as for MOS capacitors. On the other hand in short channel devices this effect is expected to be quite pronounced. As the occurrence of the current peaks is supposed to be associated with the charging and discharging of the surface traps, it would mean that the energy distribution of surface traps is affected appreciably by the drain/source diffusion in the device. According to our rough calculations showing that the optimum frequency decreases with increase of power index n in the simple energy distribution $D_{it} = A.E^{n}$, it may be concluded that in large channel devices or devices without drain/source the index n has a higher value than the small channel devices. Conversely, it would suggest that by the introduction of drain/source in the devices, the index value is decreased in general. However it produces a significant effect only in small channel devices by way of increase of optimum frequency of the first current peak. This would further suggest that if the drain/source diffusion in the device produces additional surface traps, these traps will be produced more towards the midbandgap.

Based on the above remarks and discussions about the practical utility of the present study, it may be anticipated that it is full of potentiality and versatility and may be put to the study of many characteristics of the MOS devices. However it needs more detailed study both experimental as well as theoretical before achieving this objective.

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APPENDIX

Software Programs Designed For The Automation Of The Experiments Achieved In The Present Work.

```
1       ! Program to draw Elliot curve of Charge Pumping
2       ! current measurements in MOS Transistors.
3       ! ********************************************
7       DIM File$(1200)[40]
8       DIM A$[40],X(100),Y(100),K(100),Z(100)
9       FOR J=0 TO 100
10      X(J)=0
11      Y(J)=0
12      NEXT J
13      ! ********************************************
15      OUTPUT 717;"F2RA1I3A3B1L3M3"
16      OUTPUT 717;"PS0 ;PTB  ,PE.10NPH4;PD4,PB.20"
17      OUTPUT 717;"PS"
18      OUTPUT 717;"W1"
19      FOR I=0 TO 79 STEP 1
20      ENTER 717;A$
21      DISP A$
22      B$=A$[4,13]
23      Y(I)=VAL(B$)
28      C$=A$[16,21]
30      X(I)=VAL(C$)-7
33      PRINT "I=";Y(I),TAB(25);"V=";X(I)
35      PRINT
36      NEXT I
37      ! ********************************************
39      ! Routine that searches the maximum value
40      ! of the current.
42      Icp=ABS(Y(0))
43      FOR I=1 TO 79
44      IF Icp>ABS(Y(I)) THEN 46
45      Icp=ABS(Y(I))
46      NEXT I
47      PRINT
48      PRINT "Icpmax=";Icp
56      GOTO 92
57      ! ********************************************
58      ! Routine to make the graphics and frame.
60      GINIT
61      PLOTTER IS 3,"INTERNAL"
62      GRAPHICS ON
63      X_gdu_max=100*MAX(1,RATIO)
64      Y_gdu_max=100*MAX(1,1/RATIO)
65      LORG 6
66      CSIZE 5.5,.5
67      FOR I=-.1 TO .1 STEP .1
68      MOVE X_gdu_max/1.5+I,Y_gdu_max
69      LABEL "I-V CHARACTERISTICS"
70      NEXT I
77      DEG
```

```
78    LDIR 90
79    CSIZE 3.5
80    MOVE .10*X_gdu_max,1.6*Y_gdu_max/2
81    LABEL "Icp/Icpmax"
82    LORG 4
83    LDIR 0
84    MOVE 1.90*X_gdu_max/2,.08*Y_gdu_max
85    LABEL "VOLTS"
86    VIEWPORT .2*X_gdu_max,.98*X_gdu_max,.15*Y_gdu_max,.9*Y_gdu_max
87    FRAME
88    RETURN
89    ! ************************************************
91    ! Routine to plot the LOG scale graph.
92    GOSUB 60
93    WINDOW -80,20,0,3
94    AXES 1,0,-80,0,10,1,3
95    CLIP OFF
96    CSIZE 2.5,.5
97    LORG 6
98    FOR I=-7 TO 1
99       S=I*10
100      MOVE S,-.06
101      LABEL USING "#,K";I
102   NEXT I
103   LORG 8
104   FOR I=0 TO 3
105   S=10^(I-13)
106   MOVE -82,I
107   LABEL USING "#,K";S
108   MOVE -78.9,I
110   LABEL "-"
111   NEXT I
112   ! ************************************************
114   ! Routine to plot points on the graph.
115   FOR I=0 TO 79 STEP 1
116   K(I)=LGT(ABS(Y(I)))+12
117   Z(I)=X(I)*10
118   MOVE Z(I),K(I)
119   CSIZE 2
120   LABEL "+"
121   NEXT I
133   PRINT " PRESS  CONTINUE KEY  FOR NORMALIZED SCALE"
134   PAUSE
135   ! ************************************************
137   ! Routine to plot normalized linar scale.
138   GOSUB 60
139   WINDOW -80,20,-0,1.1
140   AXES 1,1,-80,0,10,1,3
141   CLIP OFF
```

```
142    LORG 6
143    FOR I=-7 TO 1
144       S=I*10
145       MOVE S,-.05
146       LABEL USING "#,K";I
147    NEXT I
148    LORG 8
149    FOR I=.1 TO 1 STEP .1
150    MOVE -78,I
151    LABEL "-"
152      MOVE -83,I
153      LABEL USING "#,K";I
154    NEXT I
164    ! *********************************************
233    ! Pot of points in normalized form.
234    FOR I=0 TO 79
235    K(I)=-Y(I)
236    Z(I)=10*X(I)
237    MOVE Z(I),ABS(K(I))/Icp
238    CSIZE 2
239    LABEL "+"
240    NEXT I
241    END
```

```
1   ! Program to draw I-F curve of the present
2   ! study current measurements for a MOS  device.
3   ! Frequency variation from 1 to 200 kHz or 10 to 100 Hz.
4   ! The complete curve is for frequency from 40 Hz to 100 kHz.
5   ! **************************************************
7   DIM File$(1200)[40]
8   DIM A$[40],X(100),Y(100),K(100),Z(100)
9   FOR J=1 TO 100
10  X(J)=0
11  Y(J)=0
12  NEXT J
13  ! **************************************************
17  OUTPUT 717;"F2RA1I3A3B1L3M3"
18  OUTPUT 717;"PS0 ;PT1.0,PE.01NPH4;PD4,PB0"
19  OUTPUT 717;"PS"
20  OUTPUT 717;"W1"
21  FOR I=1 TO 100
22  ENTER 717;A$
23  B$=A$[4,13]
24  Y(I)=VAL(B$)-5.E-14
28  C$=A$[16,21]
30  X(I)=2+VAL(C$)/.01
33  PRINT "I=";Y(I);"f=";X(I),
36  NEXT I
37  ! **************************************************
38  ! Routine to find the maximum and minimum value of current.
47  Icp=ABS(Y(1))
48  F=X(1)
49  FOR I=2 TO 100
50  IF Icp>ABS(Y(I)) THEN 54
51  F=X(I)
52  Icp=ABS(Y(I))
54  NEXT I
55  PRINT "Icpmax=";-Icp;"F=";F
56  GOTO 72
58  !***************************************************
59  Ic=ABS(Y(1))
60  F=X(1)
61  FOR I=2 TO 100
62  IF Ic<ABS(Y(I)) THEN 65
63  F=X(I)
64  Ic=ABS(Y(I))
65  NEXT I
66  Ic=-1*Ic
68  PRINT "Icpmin=";Ic;"F=";F
69  ! **************************************************
```

```
70      ! Routine to make the graphics and framing.
73      GINIT
74      PLOTTER IS 3,"INTERNAL"
75      GRAPHICS ON
76      X_gdu_max=100*MAX(1,RATIO)
77      Y_gdu_max=100*MAX(1,1/RATIO)
78      LORG 6
79      CSIZE 5.5,.5
80      FOR I=-.1 TO .1 STEP .1
81      MOVE X_gdu_max/1.5+I,Y_gdu_max
82      LABEL "I-F CHARACTERISTICS"
83      NEXT I
84      CSIZE 3.5
85      MOVE .15*X_gdu_max,1.9*Y_gdu_max/10
86      CSIZE 3
87      MOVE .12*X_gdu_max,Y_gdu_max/1.25
88      DEG
89      LDIR 90
90      LABEL "Icp/Icpmax"
91      LORG 4
92      LDIR 0
93      MOVE 1.90*X_gdu_max/2,.10*Y_gdu_max
94      LABEL "[Hz]"
95      VIEWPORT .2*X_gdu_max,.98*X_gdu_max,.15*Y_gdu_max,.9*Y_gdu_max
96      FRAME
97      ! ******************************************************
99      !  Routine to plot SEMILOG scale I-F curves.
100     WINDOW 0,5,0,20
101     AXES 1,0,0,0,2,2,2
102     CLIP OFF
103     CSIZE 2.5,.5
104     LORG 6
105     FOR I=0 TO 4
106        S=10^(I+1)
107        MOVE I,+.60
108        LABEL "!"
109        MOVE I,-.40
110        LABEL USING "#,K";S
111        FOR J=1 TO 9
112        M=I+LGT(J)
113        MOVE M,.44
114        LABEL "!"
115        NEXT J
116     NEXT I
117     LORG 8
```

```
118   FOR I=2 TO 20 STEP 2
119   MOVE -.12,I
120   LABEL USING "#,DD.D";I
121   MOVE +.08,I
122   LABEL "-"
123   NEXT I
124   K1=LGT(X(1)*1.E+3)-1
125   Z1=ABS(Y(1))*1.E+9
126   FOR I=1 TO 100
127   Z(I)=ABS(Y(I))*1.E+9
128   K(I)=LGT(X(I)*1.E+3)-1
129  !DRAW K(I),Z(I)
130   MOVE K(I),Z(I)
131   LABEL "o"
132   CSIZE 1.5
133   NEXT I
215   END
```

```
1      ! Program to plot the I-F curve of the present current
2      ! measurements. The starting frequency is variable.
3      ! The program can also plot any portion of the curve when
4      ! magnification of the x-ais scale is needed.
5      ! ***************************************************
7      DIM File$(1200)[40]
8      DIM A$[40],X(100),Y(100),K(100),Z(100)
9      FOR J=1 TO 100
10     X(J)=0
11     Y(J)=0
12     NEXT J
13     ! ***************************************************
15     PRINT "ENTER THE NUMBER OF FREQ. TO BE USED"
16     INPUT N
17     FOR J=1 TO N
18     OUTPUT 703;"IN"
19    OUTPUT 703;"FU1,AT1,FI1,ML0,GA1,DN"
20    ENTER 703;B$
21    DISP B$
22    X(J)=VAL(D$)
23    OUTPUT 717;"F1A6B0L3M3"
24   OUTPUT 717;"E"
25   ENTER 717;A$
26   DISP A$
27   C$=A$[4,13]
28   Y(J)=VAL(C$)
29   PRINT "F=";X(J);"I=";Y(J);"Q=";Y(J)/X(J)
30   PRINT "CHANGE THE FREQ. AND CONTINUE"
31   PAUSE
32   NEXT J
33     FOR I=1 TO N
34     PRINT "-------------------------------------------------"
36     PRINT "F=";X(J);"I=";Y(I);"Q=";Y(J)/X(J)
38     NEXT I
48     ! ***************************************************
70     GINIT
71     PLOTTER IS 3,"INTERNAL"
72     GRAPHICS ON
73     X_gdu_max=100*MAX(1,RATIO)
74     Y_gdu_max=100*MAX(1,1/RATIO)
75     LORG 6
76     CSIZE 5.5,.5
77     FOR I=-.1 TO .1 STEP .1
78     MOVE X_gdu_max/1.5+I,Y_gdu_max
79     LABEL "I-F CHARACTERISTICS"
80     NEXT I
```

```
81    CSIZE 3.5
82    MOVE .15*X_gdu_max,1.9*Y_gdu_max/10
83    CSIZE 3
84    MOVE .15*X_gdu_max,Y_gdu_max/1.12
85    LABEL "Qit"
86    LABEL "[C]"
88    LORG 4
89    LDIR 0
90    MOVE 1.90*X_gdu_max/2,.08*Y_gdu_max
91    LABEL "KHz"
92    VIEWPORT .2*X_gdu_max,.98*X_gdu_max,.15*Y_gdu_max,.9*Y_gdu_max
93    FRAME
94    RETURN
97    GOSUB 70
99    WINDOW 0,3.3,0,1.1
100   AXES 1,1,0,0,1,1,2
101   CLIP OFF
102   CSIZE 2.5,.5
103   LORG 6
104   FOR I=0 TO 3
105      S=10^(I-1)
106      MOVE I,+.040
107      LABEL "|"
108      MOVE I,-.04
109      LABEL USING "#,K";S
110      FOR J=1 TO 9
111      M=I+LGT(J)
112      MOVE M,.03
113      LABEL "|"
114      NEXT J
115   NEXT I
116   LORG 8
117   FOR I=.1 TO 1 STEP .1
118   MOVE -.1,I
119   LABEL USING "#,K";I
120   MOVE +.04,I
121   LABEL "-"
122   NEXT I
123   FOR I=1 TO 100
125   Z(I)=(ABS(Y(I))/X(I))*1.E+14
126   K(I)=LGT(X(I))-2
127   MOVE K(I),Z(I)
128   CSIZE 2
129   LABEL "+"
130   NEXT I
131   PRINT "ENTER CONTINUE FOR LINEAR "
132   PAUSE
133   ! ********************************************************
```

```
140    ! Routine for curve in linear scale.
141    GOSUB 70
150    WINDOW 0,300,0,4
160    AXES 5,.1,0,0,10,10,3
170    CLIP OFF
180    CSIZE 2.5,.5
190    LORG 6
200    FOR I=0 TO 2.5 STEP .50
210    S=I*100
211    MOVE S,-.20
212    LABEL USING "#,K";S
213    NEXT I
214    LORG 8
215    FOR I=0 TO 3
216    MOVE -10,I
217    LABEL USING "#,K";I
218    NEXT I
219    FOR I=1 TO 100
220    MOVE X(I),ABS(Y(I))*1.E+11
221    CSIZE 2
222    LABEL "+"
223    NEXT I
232    END
```

A N N E X E

Liste et composition du jury en vue de la soutenance du Memoire de Magister en......Electronique..Appliquée.....................

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