Abstract

In this paper, we develop a semianalytical model that predicts the geometric component in charge-pumping (CP) measurements for local oxidation of silicon (LOCOS) and lightly doped drain (LDD) transistors. It is not only based on thermal diffusion, drift field, and self-induced drift field but also on the contribution of the active CP area and the low-level voltage of the gate signal. By adding this model to constant-amplitude CP components, such as LOCOS, LDD, and effective channel regions, we will be able to compute characteristics of LDD-MOSFET devices with LOCOS structure. In addition, we compare the geometric component model against numerous experimental data obtained from transistors of different gate lengths and widths. The calculated characteristics with geometric component model are found in good correlation with the experimental data and are more accurate than the calculated CP without the geometric component. This modeling approach can be extended for MOSFET stress reliability evaluation such as negative bias temperature instability and radiation degradations