Abstract

The concentration profile of Si-SiO_2 interface traps in metal-oxide-semiconductor transistors has been studied using an equilibrium voltage step techniques. The Equilibrium Voltage Step (EVS), usually applied to extract the slow states profile in 3 dimensions, was used to deduce the in-depth profile of the slow states of the Si-SiO_2 interface. The profile of the slow states decreased between 7Å and 17Å awing