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To be defended before the jury composed of :

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ABSTRACT

Nowadays, Phasor measurement units (PMU) may be used to enhance power grid protection due to their flexibility, security and dependability properties. The decision of the digital protective relay highly depends on the digital signal filtering computing the fundamental phasors of line voltages and currents. However, during a transient condition, line current and voltage may include unwanted components such as dc exponentially decaying associated with the harmonics and sub-harmonics especially in the smart grid. The used digital algorithms always need few cycles for obtaining the accurate fundamental phasors which are undesirable in the protection field. The first approach proposed in this research work for reliable phasor estimation algorithm is to remove disturbance signals using optimized digital filter (ODF) and DFT algorithm. The obtained phasor algorithm has the required characteristics to remove the dc component and dump the sub-harmonic as well as harmonic components. The performance of the developed digital relay is tested using estimated disturbance test signals or generated signal obtained from the power system network simulator with thyristor-controlled switched capacitor (TCSC) compensator that has been developed for this purpose.

In this research thesis, Root Cause Analysis based on fault tree technique is used to identify disturbances first and root cause of false trips of a protective relay which may lead in cascading to blackout. Once the critical root causes are identified, conventional mitigation measures have been used first and then blocking and unblocking functions and digital filters in view of increasing the reliability of the considered protection system are proposed.

The placement of phasor measurement units (PMUs) in electric transmission systems has also gained much attention for enhancing the control as well as the protection scheme. In this research work, a binary teaching learning based optimization (BTLBO) algorithm for the optimal placement of phasor measurement units (PMUs) is proposed. The optimal PMU placement problem is formulated to minimize the number of PMUs installation subject to full network fault observability at the power system buses. The effectiveness of the proposed method is verified by the simulation of the IEEE14-bus.

Key-words: Power grid, Protection System, digital filter, PMU, Placement, Teaching Learning optimization, smart grids, observability, phasors, wide area measurement systems, IEEE-bus systems.

خلاصة

في الوقت الحاضر ، يمكن استخدام وحدات قياس (PMU) لتعزيز حماية شبكة الطاقة بسبب مرونتها وأمنها وخواص اعتماديتها . يعتمد قرار المرحل الوقائي الرقمي بشكل كبير على ترشيح الإشارة الرقمية لحسا ب القيم الأساسية للتوترات والتيارات. ومع ذلك ، خلال حالة عابرة ، قد يشمل التيار والجهد مكونات غير مرغوب فيها مثل المكونات المستمرة DC المتحللة بشكل أسي المرتبطة، التوافقيات والتوافقيات الفرعية وخاصة في الشبكة الذكية. تحتاج الخوارزميات الرقمية المستخدمة دائمًا إلى بعض الدورات للحصول على القيم الأساسية الدقيقة للجهود الفولتية والتيارات phasors وهذا غير مرغوب فيه في مجال الحماية. يتمثل المنهج الأول المقترح في هذا البحث في خوارزمية تقدير موثوق للطور لإزالة إشارات الاضطراب باستخدام مرشح رقمي محسن (ODF) وخوارزمية DFT. تحتوي خوارزمية phasor التي تم الحصول عليها على الخصائص المطلوبة لإزالة مكون التيار المستمر وتفريغ المكونات التوافقية الفرعية بالإضافة إلى المكونات التوافقية. يتم اختبار أداء التتابع الرقمي المطور باستخدام إشارات اختبار اضطراب مقدرة أو إشارة مولدة تم الحصول عليها من جهاز محاكاة شبكة نظام الطاقة المعوض بالتبادل الثايرستور (TCSC) الذي تم تطويره لهذا الغرض.

في هذه الرسالة البحثية ، تم استخدام تحليل السبب الجذري المستند إلى تحليل الشجرة الصدئة لتحديد الأسباب الأولى والسبب الجذري للإنقطاعات الخاطئة لترحيل الحماية التي قد تؤدي بالتتالي إلى التعتيم التام للشبكة. وبمجرد تحديد الأسباب الجذرية الحرجة ، تم استخدام تدابير التخفيف التقليدية أولاً ثم تم اقتراح وظائف الحجب والمرشحات الرقمية من أجل زيادة موثوقية نظام الحماية المدروس.

كما اكتسب وضع PMUs في أنظمة نقل الكهرباء الكثير من الاهتمام لتعزيز السيطرة وكذلك مخطط الحماية. في هذا البحث ، تم اقتراح خوارزمية تحسين القائمة على التعليم الثنائي (BTLBO) من أجل الوضع الأمثل لوحدات قياس PMUs. تم صياغة المشكلة المثلى لوضع وحدات PMU لتقليل عددها اللازم لمراقبة الشبكة بالكامل.وقد تم التحقق من فعالية الطريقة المقترحة من خلال محاكاة الأنظمة IEEE14-bus.

كلمات مفتاحيه : شبكة الكهرباء ، نظام الحماية ، المرشح الرقمي ، وحدة إدارة المشروع ، التنسيب ، تحسين التعلم التعليمي ، الشبكات الذكية ، إمكانية الملاحظة ، أنظمة قياس الواسعة ، أنظمة IEEE-bus.

Résumé

De nos jours, les unités de mesure Phasor (PMU) peuvent être utilisées pour améliorer la protection du réseau électrique en raison de leurs propriétés de flexibilité, de sécurité et de fiabilité. La décision du relais de protection numérique dépend fortement du filtrage numérique des signaux pour le calcule des phaseurs fondamentaux des tensions et des courants de ligne. Cependant, pendant un régime transitoire, le courant et la tension de ligne peuvent inclure des composants indésirables tels que la composante DC décroissance exponentiellement, harmoniques et aux sous-harmoniques, en particulier dans les réseaux intelligents. Les algorithmes numériques utilisés ont toujours besoin de quelques cycles pour obtenir avec la précision requise les phaseurs fondamentaux. Ceci engendre par conséquent un temps de retard au traitement de l'information non souhaitable dans le domaine de la protection. La première approche proposée dans ce travail de recherche est le développement d'un algorithme fiable pour l'estimation des phaseurs en supprimant les signaux de perturbation à l'aide d'un filtre numérique optimisé (ODF) et d'un

algorithme DFT. L'algorithme d'extraction des phaseurs ainsi obtenu possède les caractéristiques requises pour éliminer la composante DC et atténuer les composantes harmoniques ainsi que les sous-harmoniques des signaux acquis par les circuits de mesure. Les performances du relais numérique développé sont testées en utilisant des signaux de test de perturbation estimés ou par application de signaux générés obtenus à partir d'un simulateur de réseau compensé par condensateur commuté commandé par thyristor (TCSC) qui a été développé à cet effet. Dans cette thèse de recherche, l'analyse des causes principales basée sur l'analyse des arbres de défaillances est utilisée pour identifier les perturbations en premier lieu et en second lieu de trouver la cause derrière les faux déclenchements des relais de protection qui peut conduire à une cascade de pannes et l'arrêt total du réseau. Une fois les causes critiques identifiées, des mesures d'atténuation conventionnelles ont d'abord été utilisées, puis des fonctions de blocage et de déblocage et des filtres numériques en vue d'accroître la fiabilité du système de protection considéré sont proposés.

Le placement d'unités de mesure de phaseurs (PMU) dans les systèmes de transmission électrique a également beaucoup attiré l'attention des spécialistes pour améliorer le contrôle ainsi que le système de protection. Dans ce travail de recherche, un algorithme d'apprentissage basé sur l'apprentissage binaire (BTLBO) pour le placement optimal des unités de mesure de phaseurs (PMU) est proposé. Le problème de positionnement optimal du PMU est formulé pour minimiser le nombre d'installations de PMU en vue d'une observabilité totale des bus du réseau. L'efficacité de la méthode proposée est vérifiée par simulation sur les systèmes IEEE 14 bus.

Mots clés: Réseau électrique, Système de protection, filtre numérique, PMU, Placement, Optimisation de l'apprentissage de l'enseignement, réseaux intelligents, observabilité, phaseurs, systèmes de mesure étendus, systèmes de bus IEEE.

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Thesis outline

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List of Acronyms and Symbols

ADC	Analog/Digital Converter
BS	Blocking Scheme
CB	Circuit Breaker
CT	Current Transformer
D	Dependability
DAC	Data Acquisition Card
DFT	Discrete Fourier Transform
DSP	Digital Signal Processing
FACTS	Flexible Alternating Current Transmission System
FCDFT	Full Cycle DFT
HCDFT	Half Cycle DFT
HRC	High Rupturing Capacity
HV	High Voltage
I_{2h}	Second harmonics of the operating current,
I_{3h}	Third harmonic of the operating current
I_{mpu}	Minimum pickup current
I_{op}	the fundamental component of the operating current
I_{rt}	unfiltered restraint current
k_1, k_2	constant coefficients
N_e	total number of events of disturbances
N_f	Number of Failures to operate
N_i	Number of incorrect trips (false trip),
NSC	Negative Sequence Compound
N_t	total number of trips
ODF	Optimized Digital Filter

OLTC	Over Load Tap Changer
PDC	Phasor Data Concentrator
PDT	Probability of occurrence of disturbances leading to tripping
PF	Post Fault
P_{ft}	False trips causes' probability
P_{in}	Input power
PLC	Programmable Logic Controller
PMU	Phasor Measurement Unit
P_{out}	Output Power
PQA	power quality analyzer
PS	Power Swing
PS	Power System
PSB	Power Swing Block
PT	Potential Transformer
P_{un}	Probability of occurrence of disturbances leading to unnecessary tripping
R	Reliability
ROCOF	Rate of Change Of Frequency
RS	Relay System
RTU	Remote Terminal Unit
RWG	Relay Working Group
S	security
S_e	existing security
SEL	Schweitzer Engineering Laboratories, Inc.
SLP	Slop
S_n	new security
SOA	Spiral optimization Algorithm
TCR	Thyristor Controlled
TCSC	Thyristor Controlled Switched Capacitor

TT	Grounding system Type
TVE	Total vector error
UBS	Un-Blocking Scheme
Φ_M	Steady state Flux, Wb
UP	Unknown Phenomenon
Φ_M	Steady state Flux, Wb
Φ_R	reminisce Flux, Wb

Chapter 1

Introduction

1.1 Context

In latest years, electrical power technology throughout the world is quickly developed, which leads to smart power grid where some modern components may be used such as the thyristor-controlled switched capacitor (TCSC) compensated lines [1]. However, some transient disturbances may be produced in a transmission line, such as a DC offset, harmonics and sub-harmonics. These transient disturbances may cause negative effects on the measurement of currents and voltages and hence on the control and protection schemes in the power grid. Since there is a much likelihood that some failures may occur due to disturbances neither evaluated by simulation nor field tested under unforeseen measurement conditions of the system. This may occur in particular in a smart power grid that is interconnected with different types of energy sources, including new type of flexible alternating current transmission (FACT) devices having nonlinear elements and complex controlling functions. Improvement in measurement reliability for non predicted disturbance having a requested accuracy in digital relaying and control systems can be obtained through designing a band-pass filter to reject undesired signal components. One of approaches proposed in this research work for reliable phasor estimation algorithm first removes disturbance signals using designed digital filter then use HCDFT or FCDFT algorithm to compute phasors with required accuracy and convergence speed. The digital filtering design issue based on optimization approach is aimed to achieve different perspectives. The first point of view is to develop a unified accurate phasor measurement algorithm that immunes nearly all disturbances in power grid, (including other type of FACT devices) by introducing considerable and different kind of waveform distortions affecting on both line voltage and current signals, simultaneously with required speed of convergence. However, only the line current waveform distortion

filtering is of concern and considered in this work. The second point focuses on reducing the computational resources and algorithm complexity through designing recursive digital filter with reduced order.

Since the functional security of the power system depends upon the successful operation of the thousands of relays that may be used in these schemes for preventing the power grids from cascading abnormal operations and failures. The failure of one relay of these systems to operate as intended may jeopardize the stability of the entire power grid and hence it may lead the whole blackout. In fact, major power system failures after a transient disturbance appearance are more likely to be caused by unnecessary protective relay tripping rather than by the failure of a relay to take action. In other words, the performance of protective relay or system is measured by several criteria including reliability, selectivity, speed of operation, etc. However, reliability which has two aspects: dependability and security is very important especially in smart power grid. Dependability is a degree of certainty that the protective relay will operate correctly when there is a fault in the power system. However, security relates to the degree of certainty that the protective relay or scheme will operate unnecessary when there is transient distribution in the power grid. Thus, appropriate relay testing provides a first defense against relay mal-operations and hence improve power grid stability and prevent catastrophic bulk power system failures. Relay testing can help to validate the design of relay logic, compare the performance of different relays, verify relay settings, identify system conditions that might cause unintended relay operation, and carry out post-event analysis to understand the causes of unintended or incorrect relay actions. Relay testing system improvements need to continue because of the use of relays in smart power grids where the conditions that are not the same as in the conventional power system.

Placing the PMU at every substation would certainly provide all the necessary real-time voltage magnitudes and angles for full system observability. However, by knowing a bus's voltage magnitude and angle, all current phasors, and the connecting line parameters, then all connecting bus voltages and angles can be calculated. This significantly reduces the number of PMUs (and therefore cost) needed for complete observability.

Engineers and mathematicians have developed many algorithms to determine the best PMU locations for observability of the whole power system. To be practical, a PMU strategy should aim for full observability (depends on the nature of power system topology and system configuration). Research work [2,3] estimated that for a real system, PMUs are required to be on a minimum of 1/5th-1/4th (20-30%) buses to achieve full system observability.

1.2 Importance of measurement in protective relays enhancement

An accurate and fast measurement of the phasors of the fundamental components (current and voltage) and frequency may be required in an intelligent, flexibly controllable power grid. This high quality of measurement may be obtained using of a Phasor measurement unit (PMU) that is very important in modern power grid instrumentations/meters, digital relays, control apparatus, and power quality analyzer (PQA). In such PMU instrumentation or digital relay, Discrete Fourier Transform (DFT) is the most widely used filtering algorithm [4, 5] for computing the fundamental components and frequency. However, lines currents disturbances in a transmission line may contain a dc offset which decays exponentially, and/or a large number of unwanted significant harmonics and sub-harmonics. Besides, the thyristor-controlled switched capacitor (TCSC), which may be used to enhance and optimize the use of the transmission network facilities, may generate this decaying dc components and harmonics [6]. This latter always needs few cycles (10– 20 cycles) for obtaining accurate fundamental phasors by DFT algorithm. Such waveform distortion caused by the insertion of TCSC, may affect the reliability of digital protective relays and may cause relays to operate improperly. In most cases, the waveform distortion of the load current has little effect on the lines current disturbances. However, for low magnitude disturbances, the load may consist of a large part of the load current and distortion can become a significant factor. Since the relay must function properly even with distorted load currents [7]. This underlines the importance of a good quality measurement. Moreover, protective relays must easily discriminate among fault, normal and transient abnormal conditions when power quality is good. When power quality is poor in such grid including TCSC, the threshold between normal and transient fault conditions becomes imprecise. In the relaying application, engineers can no longer rely on the performance of the relay under conventional normal system conditions. However, under conditions of poor power quality especially in the smart grid case, they have improved the relay performance by designing

filters which in turn make the relay more secure and dependable. In several cases, transmission line protective relays have undesirably operated in response to harmonics or dc offset in the power grid.

1.3 Reliability Analysis and Testing System for Protection Enhancement

A Cigré study found that 27 % of bulk power system failure (blackout) resulted from false trips of protection system. Besides, an analysis of 17 years data provided in NERC reports revealed that 63% of major disturbances are protection related protective relaying which suffers from two types of problem: false trip (unnecessary tripping) and fail to operate [8-10].

The mal-operation of this relay is generally due to not only unnecessary tripping during power swing that reduces the security of protection system and hence its reliability but also unnecessary blocking when symmetrical fault occurs accompanying a power swing [11]. This latter action may affect the dependability of the relay and hence its reliability. Many techniques have been developed to unblock the operation of the relay during power swing associated with a fault condition such as a negative sequence current magnitude and a derivative of current angle [12], and a combination of waveform of swing center's voltage (WSCV) and synthetic negative vector [13]. A more advanced new blocking and unblocking function based on power swing detector using Phasor Measurement Units (PMUs) has been proposed [11,14,15]. In addition to the local phasors information, the proposed scheme uses remote phasors information from different locations for power swing detection, which can be provided at high speed by PMUs. These measurements are used for calculating the apparent power absorbed by power line and the difference in phase angles of voltages that may be used for detecting power swings and faults. Hence, the proposed scheme blocks tripping signal during the power swing and unblocks it during fault condition.

Major power system disturbances are more likely to be caused by unnecessary tripping rather than by the failure of a relay to take action [10]. In fact, a major cause of power system instability is due to the relative long time delay for fault clearance of zone three backup relays. In order to overcome the drawbacks of these relaying systems, many techniques have been developed such as a blinder that blocks the relay to operate during the power swing [11].

1.3.1 Reliability Analysis

In this research work, Root Cause Analysis based on fault tree analysis is used to identify disturbances first and root cause of false trips of a protective relay which may lead in cascading to blackout. Once the critical root causes are identified, conventional mitigation measures have been used first and then blocking and unblocking functions and digital filters in view of increasing the reliability of the considered protection system are proposed. Previous works [1, 16] proposed some efficient solutions (based mainly on using digital filters) to obtain accurate and disturbance-free phasor measurements. As a result, the reliability of the measuring block of the protection system has been significantly improved. However, this improvement concerns the reliability of one part (the phasor measurement block) of the protection system. In the present work the reliability of the global protection system is considered. This new approach has many advantages compared to those published in previous works as it allows obtaining an important quantitative figure (security). This permits to selectively reinforce the elements of the protecting system which are most likely apt to failure and hence the impact on the overall system's cost is significant. Another main advantage is that unlike former works, our approach takes also into account the reliability of the software part of the system which is considered to have a significant contribution in the overall reliability of the protecting system.

1.3.2 Protective Relays Testing Systems

Appropriate relay testing is very important to reduce relay false-tripping rate. Relay testing can aid to confirm the design of relay, compare the performance of different relays, verify relay settings, classify system conditions that might cause unplanned relay operation, and carry out post-event analysis to understand the causes of unintentional or incorrect relay actions. Relay tester enhancements need to continue because of the use of relays in smart power grids where the conditions that are not the same as in the conventional one. A Relay Tester should be able to emulate in laboratory most of disturbances that may appear in real operating conditions.

Disturbances include transient distortion in the voltage due to post fault, potential transformer saturation or compensator switching may affect on transmission line relays and relaying systems in various ways. The mal-operation of this relay is generally unnecessary tripping during post fault or compensator connection which produces DC offset and harmonics. This may reduce the security of protection system and hence its reliability.

This part focuses mainly on the design and the implementation of the Class D amplifier which is the amplification part of the testing system. The Class D amplifier has been used in this work to amplify the simulated disturbances that are generated by Simulink power system model to be then injected to the protective relay and monitor its response. Labview has been used for developing the graphical user interface and controlling the NI 7851Board

We have used new technology that allow designing an enhanced relay testing system which in turn can be used for improving the performance of protective relay. In order to test both security and dependability and hence the reliability, this work propose a new frame work of tester based on FPGA associated with a NI (National Instruments) acquisition card.

1.4 PMU placement Optimization

Installing PMUs for full system observability is a large investment. The strategy used needs to be practical, adaptable, and cover the entire process from preparation to installation schedule. Three steps such as placement model, placement algorithm, and phased installation in order to cover the entire process.

-The placement algorithms such Spanning Tree based on graph theory developed by Reynaldo Nuqui [2] and Integer Programming developed by Ali-Abur [3] require a list of busses, a list of branches or incidence matrix, and a list of which busses have injection. The placement algorithms do not take into account physical locations, component states, or the number of transformers in a substation. Thus the person running the placement algorithm must interpret the real system into a very simplified format, determining what exactly qualifies as a bus and how to modify existing models for certain situations.

-The integer programming method can work very well and fast. The amount of result variance and run time will depend on the specific algorithm used by the optimization toolbox.

-Installation Schedule: In reality however, fully observable placement sets may not be immediately attainable or even necessary at all. By preparing an implementation schedule that takes observability into account, the PMU planner can make the most of the available PMUs long before full observability is reached.

Even when the goal is to attain full observability, it is unlikely that a system owner will purchase and install all the PMUs at once. This large investment will likely be spread out over several years by installing a subset of the PMUs each year in steps or phases. How to choose which PMU locations selected in each step should depend on the operator's most urgent need and gradually increasing the overall observability with each phase.

In this research work, a binary teaching learning based optimization (BTLBO) algorithm for the optimal placement of phasor measurement units (PMUs) is proposed. The optimal PMU placement problem is formulated to minimize the number of PMUs installation subject to full network observability at the power system buses. The effectiveness of the proposed method is verified by the simulation of IEEE14-bus.

1.5 Research objectives

The first objective of this research is to develop an approach for reliable phasor estimation algorithm for removing disturbance signals using optimized digital filter (ODF) and DFT algorithm. The developed phasor algorithm may have the required characteristics to remove the dc component and dump the harmonic as well as sub-harmonic components. The performance of the developed digital relay may be tested using estimated disturbance test signals or generated signal obtained from the simulator of thyristor-controlled switched capacitor (TCSC) compensated power system network that has been developed for this purpose. An optimization technique is used for the design of digital filter with simultaneous objective functions. The discrete time transfer function of the desired recursive digital filter is first developed. The second step of the design, an error function between the desired ideal response and the desired filter transfer function is formulated. A norm of the error function is minimized by changing the practical filter coefficients considered as optimization design

variable. A compromise or a trade-off between the different objective function must be made to satisfy filter design. The combined optimized digital filter (ODF) and DFT algorithm are therefore successfully used to quickly and accurately calculate the phasors. Moreover, the obtained phasor algorithm has the required characteristics to remove the dc component and dump the sub-harmonic as well as harmonic components. The phasor filter dynamic performances are tested using either data obtained from simulated network faults and specific test signals including undesired components. To assess the phasor Measurement filter, several indices have been used to evaluate the performances of the designed filter.

The second objective of this research thesis is first to perform Root Cause Analysis based on fault tree analysis for identifying disturbances first and then to study root cause of false trips of a protective relay which may lead in cascading to blackout. Once the critical root causes are identified, conventional mitigation measures have been used first and then blocking and unblocking functions and digital filters in view of increasing the reliability of the considered protection system are proposed.

The third objective of the research work is the placement of phasor measurement units (PMUs) in electric transmission systems for enhancing the protection scheme. In this research work, a binary teaching learning based optimization (BTLBO) algorithm for the optimal placement of phasor measurement units (PMUs) is proposed. The optimal PMU placement problem is formulated to minimize the number of PMUs installation subject to full network observability at the power system buses. The effectiveness of the proposed method is verified by the simulation of IEEE14-bus.

1.6 Thesis Organization

The outlines of this thesis may be organized as follows. Chapter 2 deals with an extensive literature review of related research, especially in the areas of smart power grid, causes of disturbances and their effects on the measurement quality, measurement system based on digital filters and protection system based on synchronized phasor measurement. The study of the reliability of protective system is presented in Chapter 3 through the analysis of the power network with digital filters. The testing system that may be used for reliability evaluation is discussed in chapter 4. Chapter 5 presents the importance of the PMU placement optimization in power system is emphasized by a brief review. In addition, the

optimization techniques such as the teaching learning based optimization (TLBO) that is used for optimal PMU placement is discussed. A summary of the contributions, implications, and limitations of the study and future research directions is given in Chapter 6.

1.7 Publications List

The thesis is developed from the peer-reviewed journal and conference papers which are listed below.

1. H Bentarzi, A **Zitouni**, « Field-Programmable Gate Array Based Tester for Protective Relay », *International Journal of Electrical, Computer, Energetic, Electronic and Communication Eng**ineering*, **Vol.11, N°7, pp. 791-796, WASET, 2017.**
2. **Abdelkader Zitouni**, Abderrahmane Ouadi, Hamid Bentarzi, Mahfoud Chafai , "Distance relay reliability enhancement using false trip root cause analysis », Springer International Journal of System Assurance Engineering and Management, pp.1-9 , 2018.
3. H. Bentarzi, A. **Zitouni**, "FPGA Based Tester for Protective Relay", 19th International Conference on Power Electronics and Power Engineering, ICPEPE Istanbul 2017.
4. Abdelkader **Zitouni**, Mahfoud Chafai; Hamid Bentarzi, Abderrahmane Ouadi, False Trip Root Cause Analysis and Mitigation in Electrical Power System Protection, International Conference on Production, Energy & Reliability (ICPER2016), 15 - 17 August 2016; Kuala Lumpur, Malaysia.
5. H.Bentarzi, Abdelkader **Zitouni**, Ayache Mati, Abderrahmane Ouadi, Dependability and Security Enhancement of Distance Relay in Power System; International Conference on Production, Energy & Reliability (ICPER2016), 15 - 17 August 2016; Kuala Lumpur, Malaysia. http://www.utp.edu.my/icper2016
6. A. **Zitouni**, A. Ouadi, and H. Bentarzi, (2015) "Measurement Quality Enhancement using Digital Filter in Power Grid integrating TCSC", EPE2015, Kouty nad Desnou, Czech Republic, May 20 – 22 2015, (IEEE explorer) DOI: 10.1109/EPE.2015.7161175..
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Chapter 2

Disturbances Effects on Measurement and Protection

Measurements of the instantaneous amplitude and phase angle of the fundamental current or voltage components and frequency that may be needed in three-phase power grid instrumentations/meters and relays may be affected by several encountering disturbances. These disturbances may be due to an abrupt heavy load changes and post-faults resulting in frequency deviation, DC offsets decaying, and harmonics especially in the power grid including TCSC devices. To study these effects on the quality of measurements, this research work presents a new approach using the data generated by Simulink/MATLAB software. The obtained simulation results show that the unwanted DC offset and harmonics as well as sub-harmonics cannot be removed completely by conventional filters such as anti-aliasing and DFT filtering but they can be eliminated by inserting before DFT algorithm a digital filter.

2.1 Introduction

Power systems are the largest manmade dynamic system. They are highly nonlinear and involve complicated electromagnetic and electromechanical phenomena. To operate the system reliably and economically, system conditions may be monitored using voltages and currents phasors. So, an accurate and fast measurement of these phasors of the fundamental components (current and voltage) and frequency may be required in a power grid such as one. This high quality of measurement may be investigated through the use of a Phasor measurement unit (PMU) that is very important in an intelligent, flexibly controllable modern power system (smart grid) instrumentations/meters, digital relays, control apparatus, and power quality analyzer (PQA). In such PMU instrumentation or digital relay, Discrete Fourier Transform (DFT) is the most widely used filtering algorithm [4,5] for computing the fundamental components and frequency. However, lines currents disturbances in a transmission line may contain a dc offset which decays exponentially, and/or a large number of unwanted significant harmonics and sub-harmonics. Besides, the thyristor-controlled switched capacitor (TCSC), which may be used to enhance and optimize the use of the transmission network facilities, may generate this decaying dc components and harmonics [6]. This latter always needs few cycles (10– 20 cycles) for obtaining accurate fundamental phasors by DFT algorithm. Such waveform distortion caused by the insertion of TCSC, may affect the reliability of digital protective relays and may cause relays to operate improperly. In most cases, the waveform distortion of the load current has little effect on the lines current disturbances. However, for low magnitude disturbances, the load may consist of a large part of the load current and distortion can become a significant factor. Furthermore, the relay must function properly even with distorted load currents [5]. This can be achieved only by a good quality measurement. Moreover, protective relays can easily discriminate between fault and non-fault conditions when power quality is good. When power quality is poor, the threshold between normal and fault conditions becomes imprecise. In the relaying application, engineers can no longer rely on the performance of the relay under conventional normal system conditions. However, under conditions of poor power quality especially in the smart grid case, they have improved the relay performance by designing filters which in turn make the relay more secure and dependable. In several cases, transmission line protective relays have undesirably operated in response to harmonics or dc offset in the power grid.

From the obtained evaluation using the ideal network [6], the DC offset may have an effective impact on the Fourier algorithm and if no correction is taken on, the relative error of the real amplitude from the Fourier algorithm may attain 20%, which is mainly caused by this decaying dc offset. In SCADA and protection applications, such large relative error is not permissible. The performances of these techniques employed directly establish the functions of these systems and affect their behaviors under various service conditions. Hence, the real-time accurate phasor measurement of the fundamental component and/or symmetrical components is essential and crucial to the safe and economic running of smart electric power grid [5, 7, 8].

For an ac input signal that is associated with an exponentially decaying dc offset component, some authors [12] propose a modified Fourier filter algorithm using a data window of one cycle plus two samples to compute and perform compensation to remove the unwanted dc offset [9]. The idea behind this algorithm is that the decaying DC component can be completely removed from the original signal once its parameters are determined. The weakness of the previous algorithms is that more calculation is needed to eliminate the dc offset. Many other works can be found in the literature [10-14] devoted to remove the DC-component and associated unwanted signals.

Conventionally, static state estimation has been used to estimate the steady-state power and voltage magnitudes. However, for dynamic applications, measurements are time-skewed without a time reference. Digital computer based measurements; protection and control have become common features of electric power substations. These systems use sampled data to compute various quantities such as voltage and current phasors.

The advent of satellite-based time-keeping system, such as high accurate atomic clocks used in global position system (GPS), with lowest cost GPS receiver providing high precision timing sources, measurements are made with a common time reference, usually GPS clock. The advances of computer, synchronization and communication technologies have made synchronized phasor measurement in power system applications such as protective relay and phasor measurement unit (PMU) within 1μs. Even the measurements accomplished at various sites, are synchronized to each other using the same common time base. Synchronized phasors measurement set provides a vastly improved method for tracking power system dynamic phenomena. They facilitate a number of wide area applications including wide area

measurement systems. (WAMS), a power system protection, monitoring and control applications such as wide-area measurement protection and control system (WAMPAC) which utilizes these measurements.

Stand alone phasor measurement units (PMU) have been used on critical systems, for providing synchronized phasor measurement data. They are only in developed countries because they are relatively expensive, this has conveyed some manufacturers to design modern protective relay includes phasor measurement function and capabilities. The addition of synchrophasor measurement in a protective relay results in increased power system reliability and provides easier disturbance analysis, protection, and control capabilities.

For phasor measurement, the discrete Fourier transform (DFT) algorithm is used to calculate the phasors providing the phasor magnitude and angle estimation. When the power system frequency is at off nominal frequency, the DFT phasors estimators are no longer accurate, and the frequency compensation algorithm based on the smart DFT algorithm is used to correct the phasors. The power system frequency is accurately estimated by using the least square algorithm based on instantaneous angles and frequency measurements obtained by the SDFT algorithm.

The phasor measurement is tested under different power system disturbances. This is due to the fact that power system voltage and current waveforms are not steady state sinusoids, particularly during system disturbances. They frequently contain sustained harmonic and non-harmonic components. In addition, because of faults and other switching action transients, there may be step changes in the magnitude and phase angles of the waveforms. Other disturbances are the relatively slow changes in phase angles and magnitudes due to oscillations of machine rotors during electromechanical disturbances. This chapter includes general background information about disturbances causes and their effects on measurements, synchro-phasor measurements technology and how to mitigate the harmonics and sub-harmonics that may be initiated in the smart grid.

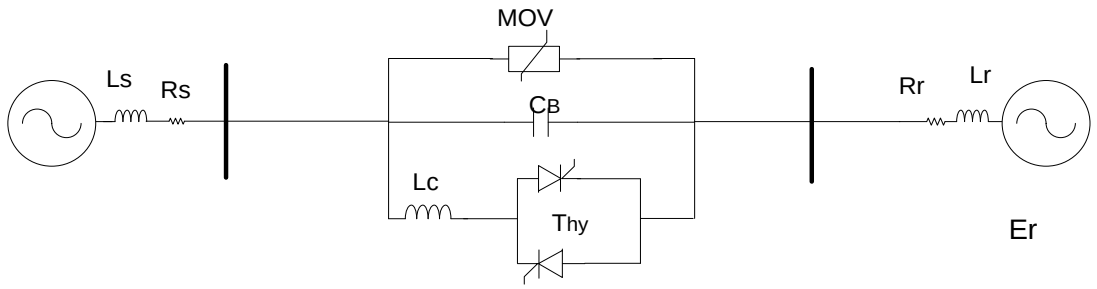
2.2 Disturbances

A Power transmission network plays a very important role in transporting and delivering power over a wide geographical area. Due to the rapidly increasing power demand and in order to drive the high voltage transmission lines up to the optimum limits, new

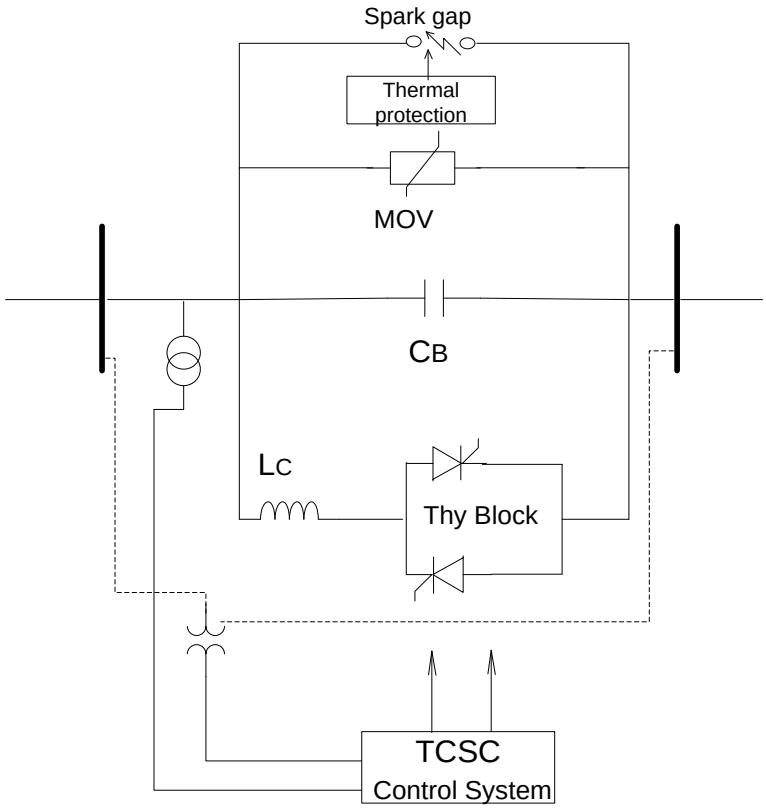
methods have been developed to improve transmission line capacity. Transmission lines are included with FACT series compensated devices to increase the power transfer capability. However these FACT devices introduce nonlinearities in the power system transmission network and particularly during power system disturbances where the occurrences of faults are more likely and security of the supply became a critical issue. Therefore, it is necessary to study effects of FACTS devices on the power systems measurement quality in protective devices and PMUs during disturbances. Both voltage and current may contain a considerable exponentially decaying DC component, and significant harmonics in line voltages and sub-harmonic in line currents components. This causes significant error in voltage and current phasor determination as has been studied by many authors [12], [20-23] for a power system transmission line fault analysis.

2.2.1 Series Compensator

Among the actually known FACT devices are series compensated devices, which have been used successfully for many years to enhance stability and load capability for HV and EHV transmission networks. They work by inserting capacitive voltage to compensate for the inductive voltage drop in the line, i.e they reduce the effective reactance of the transmission line. Series compensation can be classified into switched capacitor systems and thyristor controlled switched capacitor (TCSC) systems. The Capacitors bank is installed in series with the transmission line as shown in Fig.2.1a, for a single phase diagram. On the same installation platform, the main capacitor is located together with TCSC controller. TCSC compensated scheme consists of controlled reactors in parallel with sections of capacitor banks, as illustrated in Fig.2.1b. A metal-oxide varistor (MOV) is connected across the capacitor to prevent capacitor overvoltage. Further, a bypass switch in parallel with gap automatically closes the abnormal circuit condition that causes prolonged current flow through the gap. A snuber circuit connected in series is used to limit the current that may flow through the air-gap switch. Also connected is an air-type induction with a thyristor which can be used to short-up or bypass the capacitor when a fault occurs. The TCSC can operate in two modes when a fault occurs.



(a)



(b)

Fig.2.1 Series compensated scheme used in transmission network:
(a) Single circuit diagram of a capacitor bank used in transmission network, (b) TCSC compensated scheme.

a) Blocking mode: The TCSC will operate in blocking mode, where the thyristors are not triggered and the thyristors remain in non-conducting state. Line current passes through the capacitor bank only.

A primary overvoltage protection typically involves non-linear metal-oxide varistors, a spark gap with a snuber circuit. In this mode the MOV will conduct to limit the capacitor over voltage during the fault. If the overvoltage is frequently repeated, the energy dissipated by MOV grows and when reaching a certain threshold a spark gap, a fast switch, is activated to bypass the MOV and hence protect the MOV from overheating. During this mode, the power transmission network can be modeled as an RLC circuit, as shown in Fig.2.2-a, for short line consideration.

b) Bypass mode (Fig.2.2-b): During severe short circuit or high current, the thyristor controlled (TCR) reactor is connected by continuously triggering the thyristor switch that bypass the capacitor for conducting fault currents. The TCSC will behave like a parallel connection of the series capacitor bank and the inductor of the thyristor switch branch. The inductor whose purpose is to limit the rate of rise of current through the thyristor and to prevent resonance with the network (normally 6% with respect to Xc). The capacitor may be switched with a minimum of transients if the thyristor is turned on at the instant when the capacitor voltage and the network voltage have the same value. In this mode, the capacitor voltage is much lower than in the blocking mode.

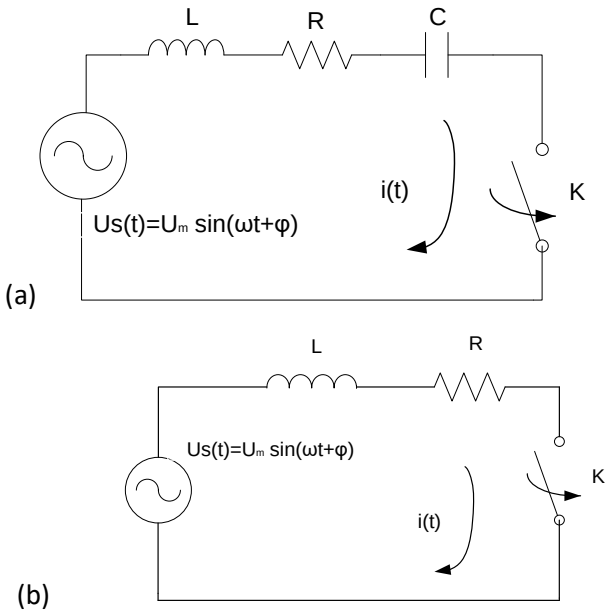


Fig.2.2 Equivalent power transmission network model using TCSC: (a)- switched capacitor bank connected, (b)- switched capacitor bank bypassed by TCR

2.2.2Fault Analysis

During a severe fault, the power system transmission can be modeled using the ideal network shown in Fig.2.2.b. It can be used to reveal how the source of the decaying DC offset that is induced in the current. In the network, the L or R is variable according to the power system operation conditions as well as the fault. If the switch k is closed at t=0, and through the use of the Kirchhof voltage law it leads to the following differential equation:

$$V_m \sin(\omega t + \varphi) = Ri + L\frac{di}{dt} \tag{2.1}$$

By solving Eq.(2.1), the fault current i(t)is given as follows:

$$i(t) = -\frac{V_m e^{-\frac{R}{L}t}}{\sqrt{R^2+(L\omega)^2}} \sin\left[\varphi - \tan^{-1}\left(\frac{L\omega}{R}\right)\right] + \frac{V_m}{\sqrt{R^2+(L\omega)^2}} \sin\left[\omega t + \varphi - \tan^{-1}\left(\frac{L\omega}{R}\right)\right] \tag{2.2}$$

The DC component needs 0.5 to 5 cycles for decaying. In the case where a relatively high short resistance, between phase and ground, the capacitor bank model takes place and the ideal network includes a series capacitor C, in addition to the RL model, as shown in Fig.2.2.a. This model can be used for the purpose of determining the power flow transfer, but also to analyze the transient switching for some fault, which is considered at once. During this mode, when a relatively high fault resistor ranging between 10Ω and 200 Ω, a slow decaying with sub-synchronous frequency will appear in transient fault current. This can be modeled by the following differential equation as:

$$U_s(t) = Ri + L\frac{di}{dt} + u_c(t) \tag{2.3}$$

For a heavily short circuits the capacitor are shorted, so the following are added to Eq.(2.3)

$$u_c(t) = 0, \quad i_c(t) = 0 \tag{2.4}$$

The solution will be the same as given in Eq.(2.2). When the short is not severe, the capacitors bank are not bypassed, in addition to Eq.(2.3), the capacitor voltage should include following additional equation with initial condition as:

$$\begin{cases} u_c(t) = \frac{1}{C}\int_{t_o}^{t_n} i_c(t)dt + u_c(t_o) \\ i_c(t) = c\frac{du_c(t)}{dt} \end{cases} \quad (2.5)$$

By solving Eqs. (2.3) and (2.5) simultaneously, the fault current i(t) will be as follows:

$$i(t) = \frac{V_m}{\sqrt{R^2+\left(L\omega-\frac{1}{C\omega}\right)^2}} e^{-\frac{R}{2L}t} \sin\left(\omega_n t + \varphi - \tan^{-1}\left(\frac{R}{L\omega_n}\right)\right) + \frac{V_m}{\sqrt{R^2+\left(L\omega-\frac{1}{C\omega}\right)^2}} \sin\left(\omega t + \varphi - \tan -1 L\omega R\right) \quad (2.6)$$

Where, $\omega_n = 1/\sqrt{LC}$.

During this mode, when a relatively high fault resistor ranging between 10Ω and 200Ω a slow decaying with sub-synchronous frequency will appear in transient fault current.

In Eqs.(2.2) and (2.6), the first term is a transient decaying DC offset component that depends on the parameters R, L,ω,φ and Vm. The effect of this term has been evaluated and concluded that the DC offset may have a severe impact on the Fourier algorithm [7]. The relative error of the amplitude from the Fourier algorithm may reach 20% due to this decaying DC offset.

2.2.3 Simulink Model of Electrical Network integrating TCSC

The power transmission lines circuit to be simulated as shown in Fig.2.3 with a base voltage of 400kV, and 50Hz frequency for a 300km distance compensated of 40% at the receiving end of the line. The PSB with Simulink simulator is used to simulate the power system components including a series capacitor compensator (TCSC) placed in the right end of the power line, as previously modeled, to evaluate and generate voltages and current before and after the fault. The related parameters of the simulation are given in table 2.I.

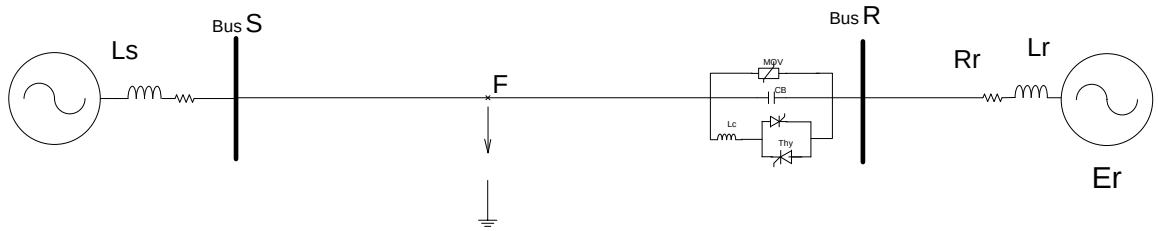


Fig.2.3 Studied Power system transmission including switched capacitor

TABLE 2.I DIFFERENT ELEMENTS PARAMETERS OF POWER NETWORK

Elements	Parameters	Values
Sources	**Resistance** **Inductance** **Frequency**	**1.31 (Ω)** **0.3008 (H)** **50 (Hz)**
T.L.	**R0 and R1** **L0 and L1** **C0 and C1**	**0.0275 and 0.0275Ω/km** **3.3 and 0.1591 (mH/km)** **8.5 and 13 (nF/km)**
Receiver	**R0 and R1** **L0 and L1**	**2.33 and 1.31 (Ω)** **0.0477 and 0.0847 (H)**
Series Cap.	**Reference voltage** **Reference current**	**300 kV** **2 kA**

The power transmission network shown in Fig.2.3 includes a power transmission line connecting two generators at two busses S and R, and a TCSC line compensation system at the receiving end. A MATLAB/SIMULINK simulator associated with power system block set (PSB), are used to perform a time domain simulation of this power system network. The main components of the TCSC are modeled in this section, as required by the SIMULINK time domain solver, as follows: - the spark gap, and hence both the capacitor bank and the MOV, is protected when any unwanted spark over the spark gap. This is performed by measuring spark gap current continuously. This in turn is compared to a maximum current that the spark gap can withstand.

Figure 2.4 shows a simulation model of one phase compensator with protection block subsystem and its typical protection functions including the main protective elements and their appropriate models that have impact on transient behavior of the TCSC in its conventional operation. Several other protections functions are not considered to facilitate the simulation modeling, but they are essential for a correct operation of a hole TCSC as capacitor unbalance protection, line current supervision, MOV high temperature protection, MOV failure protection, flash over to platform protection, trigger circuit supervision, bypass breaker failure protection, thyristor overvoltage protection, thyristor thermal overload protection etc.

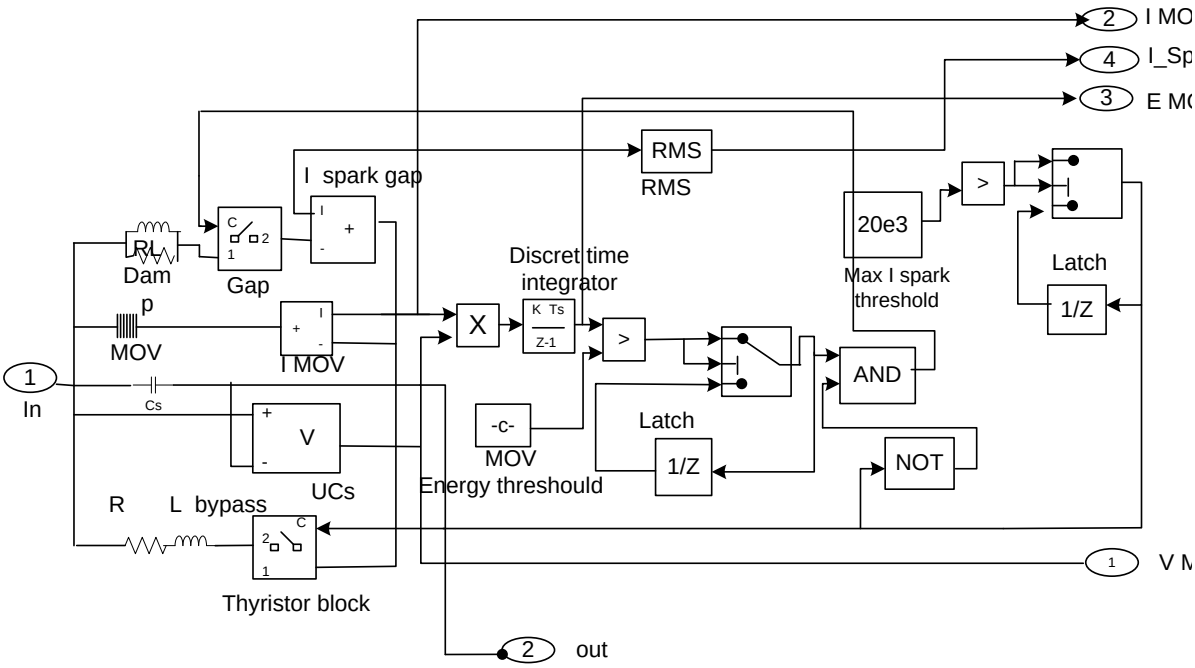


Fig.2.4 TCSC compensator-protection SIMULINK block component for one phase

(from Simulink Power System Blockset documentation)

2.2.4 Fault Simulation of the Power Network Integrating TCSC

Two fault resistances are simulated as shown in Fig.2.5. The simulation results show that the faulted signals are associated with DC decaying signals, harmonic and sub-harmonic components. The voltage waveform is corrupted by harmonic components and fast decaying DC components for small resistance faults. The current waveform may be significantly affected, depending on the inception angle, by decaying DC components for small resistance faults. Besides, the sub-harmonic component may also be added in the case of the series compensated transmission line associated with relatively

A line-to-ground fault is applied on phases A, B and C at t = 100ms. The sampling time Ts= 5.556 10^{-6} s is used in the power system simulation (3600 samples per cycle) so that a down sampling process generates a 36 sample per cycle. The Simulink time domain solver generates the different voltage and current waveforms at the corresponding bus.

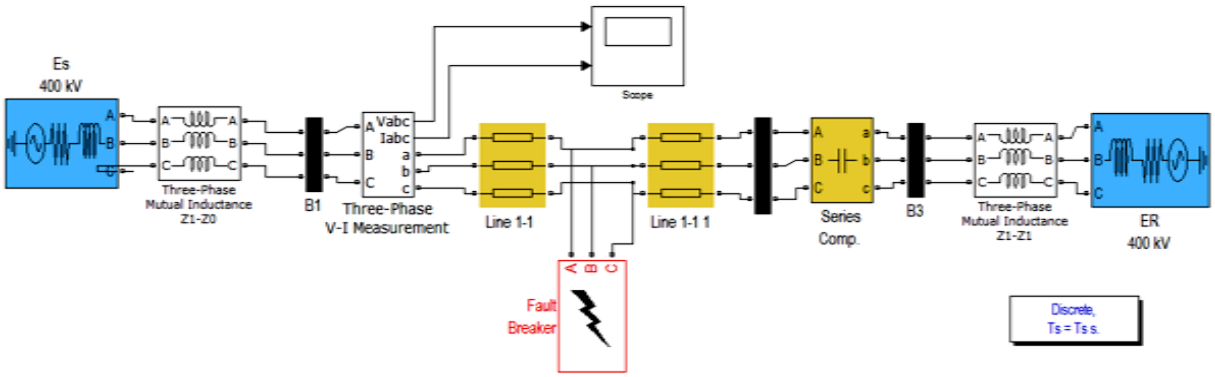


Fig.2.5 Simulink model of power network with TCSC

In order to show the DC decaying and the sub-harmonics waveform components, two fault resistances are simulated. For a severe short-circuit (R-short is nearly zero) condition initiates the state of the TCSC in bypass mode where the capacitor is shorted by an inductor, and induce the transient DC decaying waveform that is added to the lines current, whose magnitude also depends on the inception angle as stated in Eq.(2.4). When the short-circuit resistance R-short is relatively high, the TCSC is operating in the blocking mode where the capacitors bank are connected, and causes an additive decaying sub-harmonic component to the fundamental one. As stated in Eq.(2.5), the magnitude of the sub-harmonics component depends on the inception angle, its frequency is related to the capacitor bank and the distance to the fault, while its decaying time is two times the one of the severe short circuit [11].. These facts are illustrated and confirmed by the simulation results as shown in Figs 2.6-2.9.

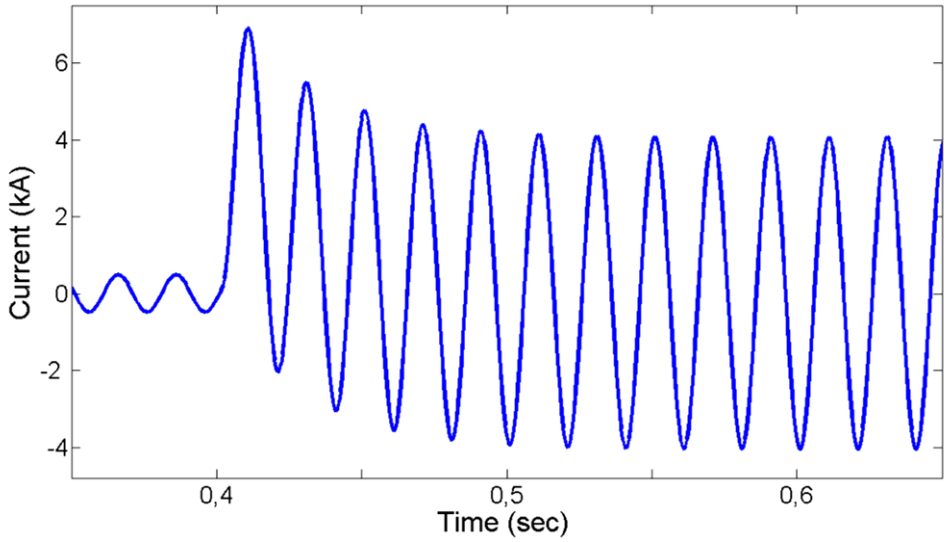


Fig.2.6 Current phasor for solid short circuit

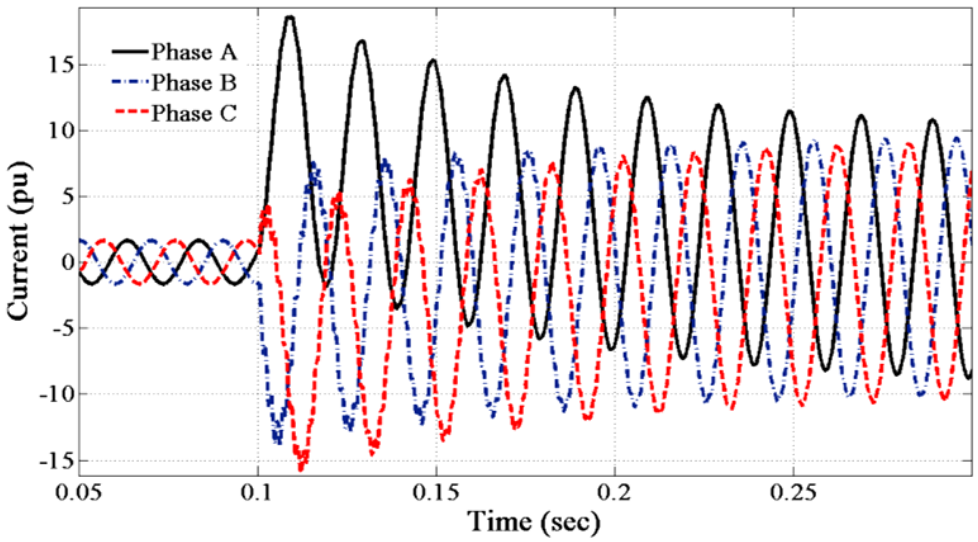


Fig.2.7 Current transient waveforms in pu for three phase to ground faults (Rs=0.01Ω)

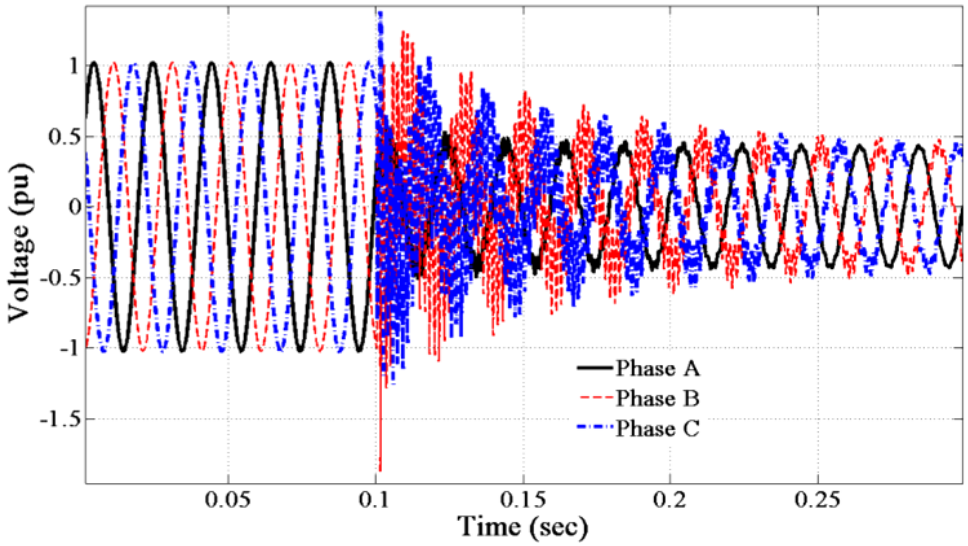


Fig.2.8 Voltage transient waveforms in pu for three phase to ground faults (Rs=0.01Ω)

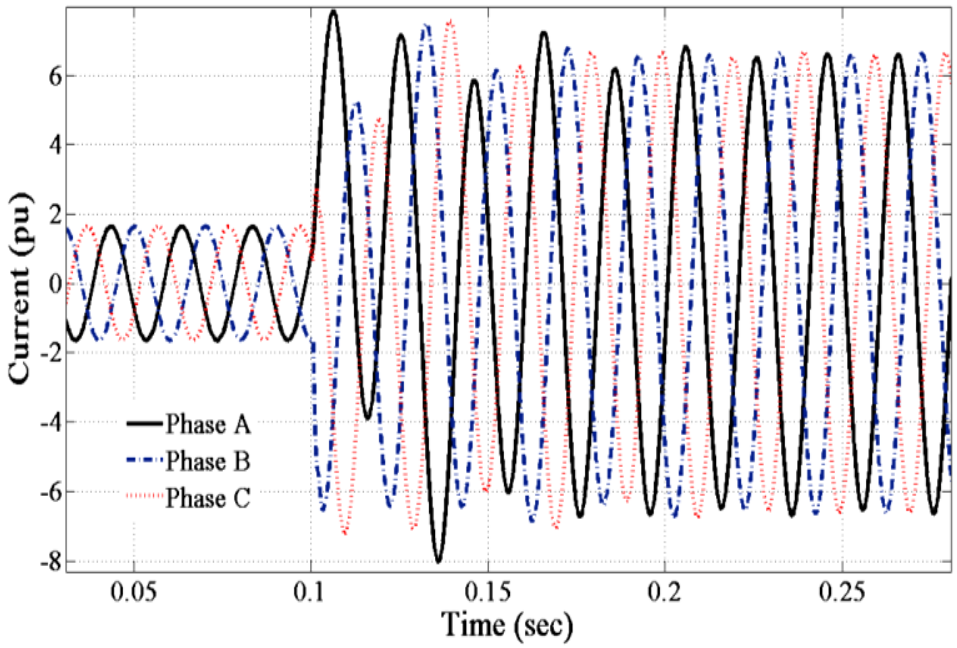


Fig.2.9 Current in pu after fault for short circuits Rs=100 Ω.

The obtained simulation results show that the faulted signals are associated with DC decaying signals, harmonic and sub-harmonic components. The voltage waveform is corrupted by harmonic components and fast decaying DC components for small resistance faults. The current waveform may be significantly affected, depending on the inception angle, by decaying DC components for small resistance faults. Besides, the sub-harmonic component may also be added in the case of the series compensated transmission line

associated with relatively high fault resistance. The DFT algorithm may induce significant errors if it is directly used for phasors computation of these generated signals [33]. To eliminate these unwanted components, many efforts have been developed using different approaches to mitigate the effect of these components on phasor computations.

2.3 Synchrophasor Measurements

During steady state in an electric power system, the voltage and current signals are virtually sinusoidal waveforms. A phasor is a vector consisting of magnitude and angle that represents a sinusoidal waveform as illustrated in Fig2.10. The phasor of a signal can be derived using Fourier transforms utilizing the data samples of the signal within a selected time window. For a steady state signal, the magnitude is a constant, while the value of the angle depends on the starting point of samples. The angle is a relative quantity and a reference has to be selected.

A pure sinusoidal waveform can be represented by a unique complex number known as a phasor. Consider a sinusoidal signal:

$$x(t) = X_m \cos(\omega t + \varphi) \tag{2.7}$$

Where, X_m : maximum value of the input signal,

f_0: the nominal frequency,

Δf:the frequency offset,

φ : the initial phase angle of the input signal.

The phasor representation of this sinusoidal is given by:

$$x(t) = \frac{X_m}{\sqrt{2}} e^{j\varphi} = \frac{X_m}{\sqrt{2}} (\cos\varphi + j\sin\varphi) \tag{2.8}$$

The signal frequency ω is not explicitly stated in the phasor representation.The term $e^{j\omega}$ is customary suppressed in the expression above, with the understanding that the frequency is ω.The magnitude of the phasor is the rms value of the sinusoid $\frac{\mathrm{Xm}}{\sqrt{2}}$ and its phase angle is φ,the phase angle of the signal in Eq.2.7. The sinusoidal signal and its phasor representation given by Eq.2.7 and Eq.2.8 are illustrated in Fig. 2.11.

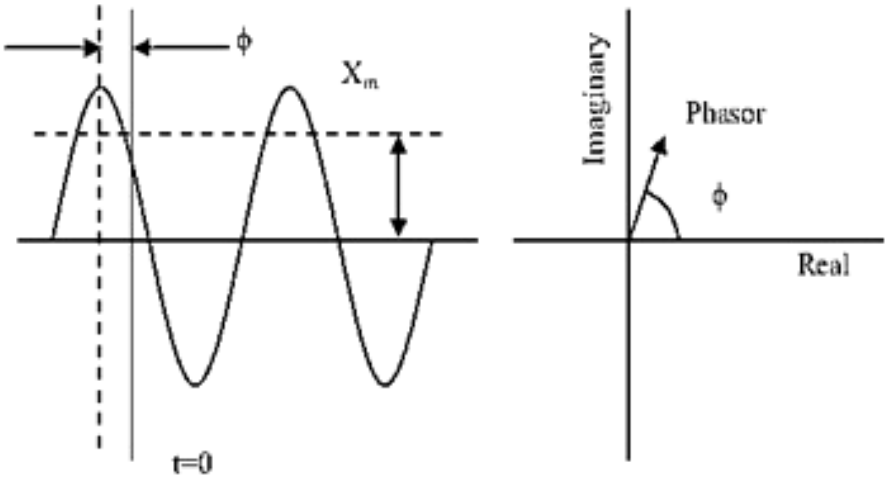


Figure 2.10 Phasor representation of a Sinusoidal signal

(left) Sinusoidal signal, (right) Phasor representation.

Measurement devices are placed at different locations in a power grid to capture voltage and current waveforms, from which phasors can be calculated. If the samples obtained by the measurement devices are not synchronized to a common timing reference, the angles of the phasors computed at different locations will not be comparable.

This may delay the understanding and analysis of certain power system phenomena and hence the development of certain power system applications. To remove this barrier, phasors measured across the power grid should have a common timing reference such that direct comparison is feasible.

A synchrophasor is defined according the IEEE standard C37.118 as “A phasor calculated from data samples using a standard time signal as the reference for the measurement; however, synchronized phasors from remote sites have a defined common phase relationship.” (C37.118-2005, March 2006.) Thus, synchrophasors measured across an interconnected power grid will have a common timing reference and thus can be compared directly as illustrated in Fig.2.12.

According to the same standard, a synchronizing source that provides the common timing reference may be local or global. The synchronizing signal may be distributed by broadcast or direct connection, and shall be referenced to Coordinated Universal Time (UTC). One commonly utilized synchronizing signal is the satellite signal broadcast from the Global Positioning System (GPS).

The definition of a real-time or synchronized Phasor provided in the IEEE Standard 1344-1995 [2] (1344-1995, 2001) corresponds to the conventional definition described earlier, at least at rated frequency (50 Hz or 60 Hz). With real-time waveforms, it is necessary to define a time reference to measure phase angles synchronously [3]. The IEEE Standard 1344-1995 [2] (1344-1995, 2001) defines the start of the second as the time reference for establishing the phasor phase angle value. The synchronized phasor measurement convention is shown in Fig.2.12.

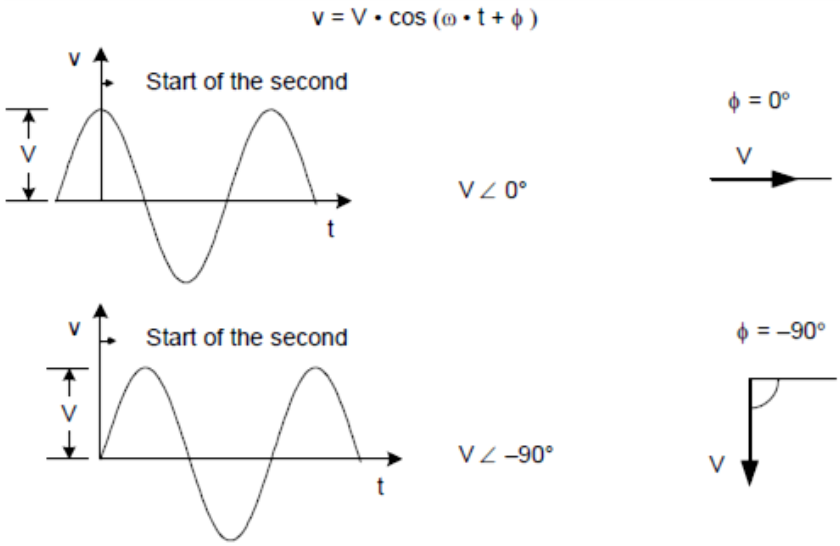


Figure 2.12 Synchrophasor measurement conventions with respect to time.

The instantaneous phase angle measurement remains constant at rated frequency when using the start of the second phase reference. If the signal is at off-nominal frequency, the instantaneous phase varies with time. It can be seen later that the choice of this reference has an impact on the phasor phase angle measurement at off-nominal frequency.

2.3.1 Phasor measurement principle

A PMU is a standalone device that measures 50/60 Hz AC voltage and current signals and provides them in phasor form with their frequency. The analog AC waveforms are digitized by an analog to digital converter for each phase and a phase-lock oscillator and a GPS reference time source, often called pulse per second (PPS) provides high-speed time synchronized sampling as illustrated in Fig.2.13. A PMU calculates line frequency, as well as voltage and current phasors at a high sampling rate and streams those data, along with the associated GPS time stamp, via networked communication lines. The synchrophasors can be phase or symmetrical component values.

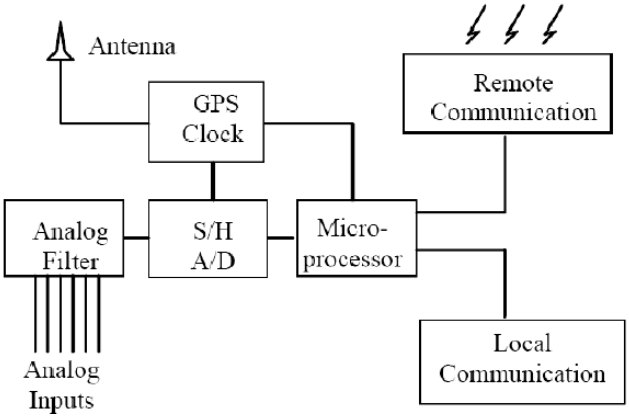


Figure 2.13 PMU block diagram.

At present, phasor measurement units (PMUs) are the most accurate and advanced synchronized phasor measurement equipment. It measures 50/60 Hz sinusoidal waveforms of voltages and currents at a high sampling rate, up to 1200 samples per second and with high accuracy. From the voltage and current samples, the magnitudes and phase angles of the voltage and current signals are calculated in the phasor microprocessor of the PMU. As the PMUs use the clock signal of the Global Positioning System (GPS) to provide synchronized phase angle measurements at all their measurement points, the measured phasors are often referred to assynchrophasors.

Fig 2.13 illustrates a functional block diagram of a typical PMU. The GPS receiver provides the 1 pulse-per-second (pps) signal, and a time tag consisting of the year, day, hour, minute, and second. The l-pps signal is usually divided by a phase-locked oscillator into the number of pulses per second required for the sampling of the analogue signals. The analog signals are derived from three-phase voltage and current transformers with appropriate anti-aliasing filtering. The microprocessor calculates the positive sequence voltage and current

phasors, and determines the timing message from the GPS, along with the sample number at the beginning of a window.

2.3.2 Phasor measurement algorithm

Synchrophasor finds wide use in wide area measurements, while the actual trends are increasingly considered in power system protection applications. During power system electromechanical disturbances and electromagnetic transient faults, the protective devices must have shorter response time for making a decision. This requires lower overshoot/under shoot measurement response.

The actual need in such application is designing phasor measurement and filtering algorithms suitable for protection applications while satisfying all the steady state and dynamic performance criteria of the IEEE standard c37.118.2011 [14]. The motivation of the work is presenting the synchrophasor estimation algorithm based on the DFT filter and introducing improvement that makes it suitable for both phasor measurement unit and protective devices.

2.3.3 Different Phasor Measurement Techniques

In the power system phasor, amplitude, phase angle and frequency are variables which may be critical and used by many power system control and protection applications. The fast and accurate measurements of these variables are still considered in a contemporary topic of research interest. Many phasor estimation algorithms as the Newton method [49], Kalman filtering[50] and level tracking[51], least square algorithm techniques have also been proposed for synchro-phasor computations in[52], a raised cosine filter (RCF) is used to compute phasors during power oscillations and dynamics. The RCF filter needs a comparatively large (4cycles) computational time windows. This algorithm has a very slow time response.

Discrete Fourier Transform (DFT) is widely used as phasor estimation algorithm of fundamental frequency [91, 92]. Due to their good harmonic rejection property conventional DFT algorithm achieve excellent performance when the signal contains only fundamental frequency and integer harmonic frequency components.

2.3.4 DFT Measurement technique

Assuming that the signal x(t) is sampled N times per fundamental period (50Hz or 60Hz) waveform to generate the sample set:

$$x_k = X_m \cos\left(\frac{2\pi}{Nf_o}k + \varphi_i\right) \tag{2.9}$$

The phasor $\overline{X}$ is given by:

$$\overline{X} = \frac{\sqrt{2}}{N}(X_c - jX_s) \tag{2.10}$$

Where:

$$X_c = \sum_{k=1}^{N} x_k \cos\left(\frac{2\pi}{N}k\right) \tag{2.11}$$

And

$$X_s = \sum_{k=1}^{N} x_k \sin\left(\frac{2\pi}{N}k\right) \tag{2.12}$$

Fig.2.15 shows a signal processing steps performed for generating the synchronized phasors provided that the power system frequency is operating at nominal frequency. This is based on the fixed frequency sampling synchronized to an absolute time reference, followed by multiplication of the cosine and sine nominal frequency carrier.

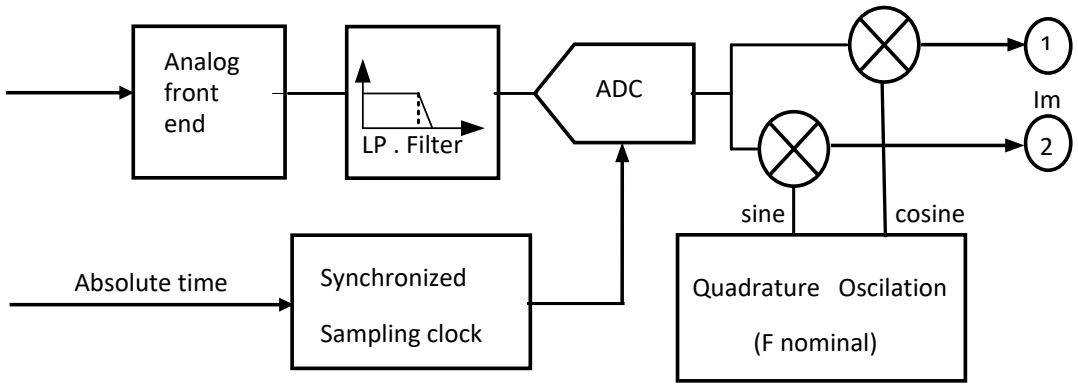


Figure 2.15 PMU Phasor signal processing model.

The conventional phasor representation of a sinusoidal signal is related to the fundamental component by its DFT as follows:

$$\overline{X} = \frac{1}{\sqrt{2}}(X_s - jX_c) \tag{2.13}$$

Eqs.2.10-2.12 represents a phasor measurement using the DFT algorithm for a period of a fixed data window (a set of N samples). This DFT procedure provides the phasor computation for a fixed-length data window, but These equations represent a non recursive calculations which are repeated for each data window as shown in Fig2.16. Evidently the procedure described by Eqs.(2.10-2.12) is non-recursive, and requires 2N multiplications and (N-l) additions to produce the phasor $\bar{X}$. It may be noted that in progressing from one data window to the next, only one sample (x_0) is discarded and only one sample (x_N) is added to the data set. Therefore, it is advantageous to develop a technique which retains 2(N-1) multiplications and 2(N-1) sums corresponding to that portion of the data which is common to the old and new data windows.

Let$\overline{X}_r$ be the phasor corresponding to the data set $x_k\{k = r, r+1, \dots, N+r-1\}$ and let a new data sample be obtained to produce a new data set x_k $\{k = r+1, r+2, \dots, N+r\}$. The Phasor corresponding to the new data window $\overline{X}_{r+1}$is then given by:

$$\overline{X}_{r+1} = \overline{X}_r + \frac{\sqrt{2}}{N}(x_{N+r} - x_r)\, e^{-j\frac{2\pi}{N}r} \tag{2. 14}$$

The difference between the recursive and non-recursive Phasor calculations is illustrated in Fig.2.16. The non-recursive Phasor rotates in counter-clockwise direction by an angle $\frac{2\pi}{N}$ as the sample time advances, whereas the recursive phasor remains stationary. More importantly, the computations implied in the recursive formula involves only two samples:x_{N+r} and x_r, whereas the non-recursive formula implies computations with N samples. Now, all phasor measurement systems use the recursive form of phasor calculations.

Unlike Eqs.(2.10-2.12), Eq.(2.14) with the recursive procedure only two multiplications are needed at each new sample time; making this a very efficient computational algorithm. It is interesting that when the input signal is a pure sine wave of fundamental frequency, $\overline{X}_{N+r} = \overline{X}_r$ for all r as shown in Fig.2.6 (c); and consequently for this case, Eq.(2.2.) becomes,

$$\overline{X}_{r+1} = \overline{X}_r \tag{2.15}$$

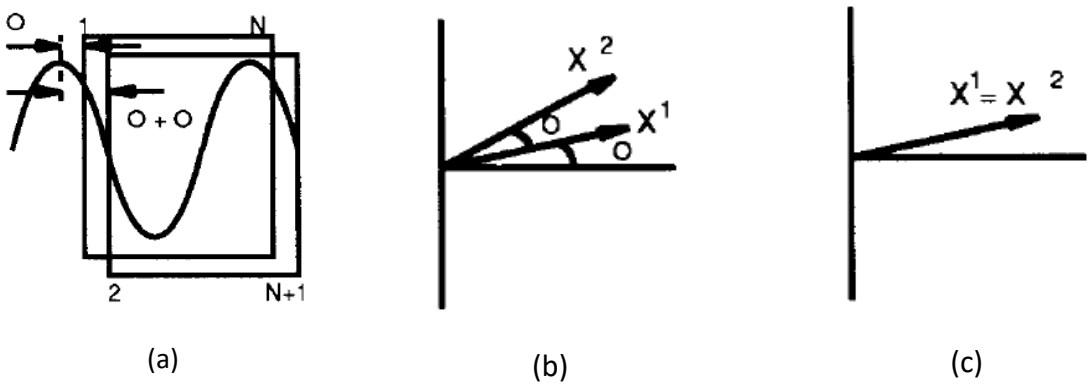


Figure 2.16. Phasors from sampled data. (a) Moving window. (b) Non-recursive. and (c) Recursive computation.

Equation (2.15) shows that when a recursive computation is used to calculate phasors, it leads to stationary phasors in the complex plane when the input signal is a pure sine wave of fundamental frequency. Recall that non-recursive phasor computation leads to phasors which rotate in the complex plane with an angular velocityω_0.

The phasor computation can be performed using FFT (Fast Fourier Transform) algorithm implemented on Digital Signal Processing (DSP) chips which are custom built for this function. A common form of the FFT requires that there will be 2^n samples in the data window, eg.8,16, 32 etc. whereas, the recursive DFT algorithms can be used for any number of samples in a window. The FFT computes harmonic components up to the Nyquist limit. If the window is taken as (60 Hz) cycle, then, 32 samples per cycle allows calculation up to the 15th harmonic for each variable. It is unlikely that any relay application will require higher harmonics than this harmonic order. The recent developed DSPs can calculate an FFT for ten input variables in a sampling interval of (1/32x60) second.

If we concentrate on the fundamental components coming from, say, one set of three-phase variables, the microprocessor can calculate the sequence components and make them available for use in a number of functions internal to the station. If the sampling frequency and the frequency of the measurands are not synchronously related, then, they will produce errors in the phasor calculations and the positive sequence voltage will not remain stationary. The latter fact is used to measure the line frequency and to adjust the sampling frequency for making the phasor stationary (phase locked loop) in some relays. The errors in the phasors are small providing the frequency variation is small. By combining the three phase voltages, any oscillating component in the individual phase voltage phasors tends to be canceling out [9].

The window length of one60Hz (50Hz) cycle is about optimum for relaying purposes, however, consecutive Phasor estimates can be averaged over several m cycles if higher precision is required for metering or control purposes, and a slow response is acceptable. Whether one uses the recursive DFT, or the angle-compensated FFT described previously, this leads to the measurement of a stationary phasor at steady state network conditions if the sampling rate is fixed to N times the network frequency.

If the network frequency undergoes a change characterized by a frequency offset Δf, it has been shown in [10] that for a small if the positive sequence phasor will undergo the following change, at each r'th sampling interval,

$$X^r(f_0+\Delta f) = Xe^{-j(N-1)\pi\Delta f\Delta t}\left\{\frac{\sin N\Delta f\Delta t}{\mathrm{N}\sin \Delta f\Delta t}\right\}e^{j2\pi\Delta f\Delta t} \tag{2.16}$$

Where f_0 is the power system nominal frequency.

To simplify the computing algorithm, an efficient recursive DFT algorithm can be used as follows:

$$\overline{\mathrm{X}}_{\mathrm{r}} = \overline{\mathrm{X}}_{\mathrm{r}-1} + \frac{\sqrt{2}}{\mathrm{N}}(\mathrm{x}_{\mathrm{N}+\mathrm{r}-1} - \mathrm{x}_{\mathrm{r}})\,\mathrm{e}^{-\mathrm{j}\frac{2\pi}{\mathrm{N}}(\mathrm{r}-1)} \tag{2.17}$$

2.3.5 Wide area monitoring, protection and control

Wide Area Monitoring, Protection, and Control (WAMPAC) involves the use of wide area synchronized measurements, reliable and high bandwidth communication networks and advanced centralized protection and control schemes. Synchronized Measurement Technology SMT and related applications are the essential element, and enabler, of WAMPAC. Presently, Phasor Measurement Units (PMUs) are the most accurate and advanced synchronized measurement technology available. They provide voltage and current phasors and frequency information synchronized with high precision to a common time reference, the Global Positioning System (GPS). The measurement functions of a PMU are based on numerical algorithms. These algorithms must be both computationally efficient and suitable for real-time applications, particularly when the measurements are used to support dynamic-response applications.

Figure 2.17 shows the main components and structure of a generalized WAMPAC system. In this system, the necessary synchronized voltage and current phasors are produced by PMUs. The measurement data from these PMUs is transmitted through a Wide-Area Network (WAN) and aggregated at one, or more Data Concentrators (DCs).

The aggregate data is then stored locally in the DC before being transmitted to the various Application Software or Servers (ASS) of the different utilities. The main task performed by the DCs is alignment of the received PMU data; however, the opportunity also exists to perform additional pre-processing tasks before forwarding the data to ASS.

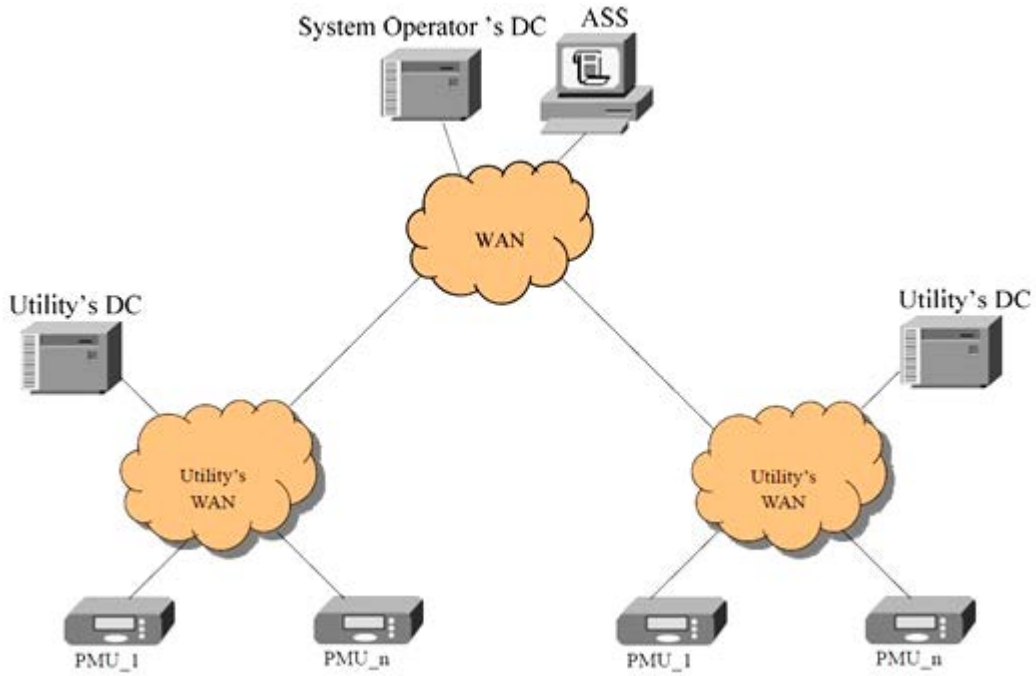


Fig. 2.17 A Generalized WAMPAC system

2.3.6 Phasor Sequence Quantities

Even though a three-phase system is balanced most of time, it is important to develop an estimator that can accomplish accurate estimations under unbalanced condition. In practice, machine-oscillating modes can be determined by measuring the phase angle of the positive-sequence voltage phasor at the machine terminals. According to Fortescue's theorem, any three phase asymmetric (unbalanced) system can be decomposed into a set of a balanced three phase direct component (1: positive sequence), a balanced three phase inverse component (2: negative sequence) and a balanced three phase homopolar (0: zero sequence) component. The

abcthree phase (X_a, X_b, X_c) sinusoidal system can be expressed in terms of the symmetrical components (X_0, X_1, X_2)as:

$$\begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha^2 & \alpha \\ 1 & \alpha & \alpha^2 \end{bmatrix} \begin{bmatrix} X_0 \\ X_1 \\ X_2 \end{bmatrix} \quad (2.18)$$

Or the symmetrical components in terms of the phase sequences can be expressed as:

$$\begin{bmatrix} X_0 \\ X_1 \\ X_2 \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha & \alpha^2 \\ 1 & \alpha^2 & \alpha \end{bmatrix} \begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix} \quad (2.19)$$

Where $\alpha = e^{j\frac{2\pi}{3}}$ and X may be a voltage or current variable

The recursive relation for the positive sequence voltage is:

$$\overline{X}_r = \overline{X}_{r-1} + \frac{\sqrt{2}}{N}\frac{1}{3}\left[\begin{array}{c} \left(x_{a,N+r-1} - x_{a,r}\right) e^{-j\frac{2\pi}{N}(r-1)} + \alpha.\left(x_{b,N+r-1} - x_{b,r}\right) e^{-j\frac{2\pi}{N}(r-1)} \\ +\alpha^2.\left(x_{c,N+r-1} - x_{c,r}\right) e^{-j\frac{2\pi}{N}(r-1)} \end{array}\right] \quad (2.20)$$

Other symmetrical components of voltages and currents are calculated in a similar manner [4, 6, 7]. Measurements of system frequency and time deviation of frequency can be done using the positive sequence voltage. Since the phase angle of this voltage, used here, is measured using narrow-band filtering performed by the DFT algorithm. These measurements provide excellent rejection of the effects of harmonics, noise and dc offsets. Using the positive-sequence voltage corresponds closely to the actual state of the system, as compared to measurements made on a single phase only. Of course, single-phase measurement of frequency and time of variation is also possible where system requirements dictate its use.

2.3.7 PMU Implementation in Protection System and Field Installation

The PMUs which provide synchronized measurements have been integrated in the modern digital protective relays as well as smart digital meters and digital fault recorders.

Additional processing requirements are associated for the relay to measure, communicate and record the PMU data in addition to their core protection functionality. All this raises potential concerns with respect to integrating PMU functions in protective relays. This new platform commonly deployed data acquisition system of a relay in order to accommodate synchrophasors measurements, local recording and digital communication using transmission

protocols. This relates to internal architectures, time synchronization, metering accuracy, communication capabilities, and processing power required to comply with the C37.118 requirements. The data acquisition methods discussed earlier provide solutions suitable for both synchronized phasor (synchrophasors) measurement applications and line distance protection applications, which require sampling referenced to an absolute time reference. Figure 2.18 shows data acquisition and data processing suitable for both kinds of applications as described hereafter.

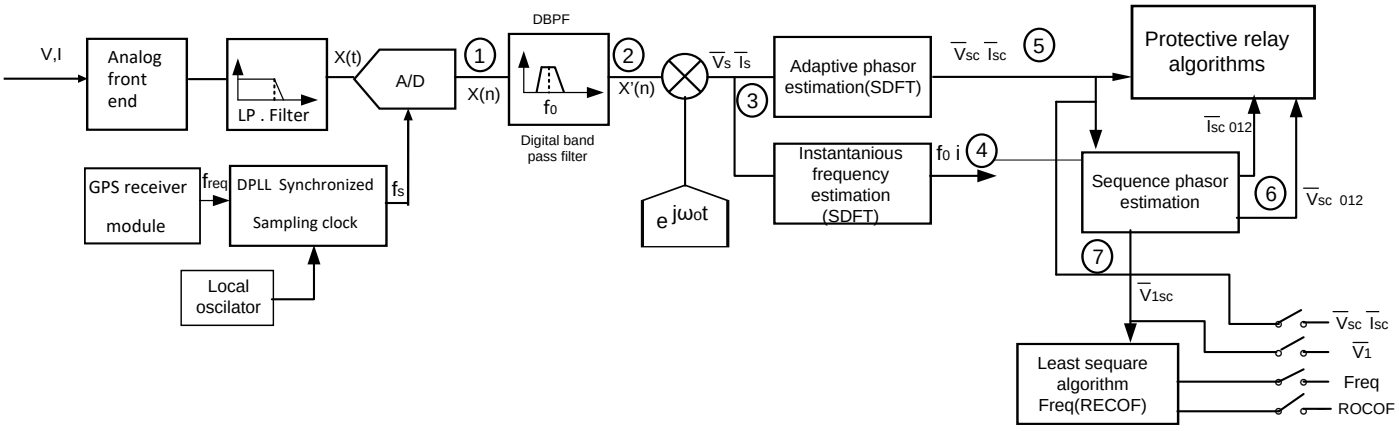


Figure 2.18 Signals processing for synchronized phasor measurement and line distance protection.

The multiple applications device acquires data at fixed time intervals Ts; the sampling frequency (f_S) obtained from a digital phase locked loop by controlling precise free running clock and locking it to a reference clock signal (GPS receiver) and provides an absolute time for tagging information. For synchronized phasor measurement applications, the device uses the GPS clock reference. After the A/D converter acquires the data①, which are available at a high sampling rate(e.g. f_S =1.8 kSPS).

These data are suitable for synchronized phasor measurements, oscillography, and harmonic analysis applications. The high sampling rate data pass through a digital band-pass filter (DBPF)②before estimating the phasors. The filter data outputs pass to a classical DFT filter③ for frequency estimation. One of the voltage phasor outputs is introduced to the instantaneous operating frequency estimator f_{i0} block using the SDFT algorithm④. After calculating this instantaneous frequency, an adaptive phasor filter estimator (SDFT algorithm) is used to correct the synchronized phasors while down-sampling to 12 corrected phasor ⑤.

These synchronized and corrected data pass to a phase sequence calculator to provide the positive, negative and zero sequence balanced phasors⑥. The correct synchronized phasors ⑤and sequence phasors⑥ are prepared for protective relay functions. The positive sequence voltage phasor data⑦, having a down sample number of corrected phasors, are input to the least square filter algorithm for estimating an averaged (during 3 or 4 cycles) operating frequency f_{req} and the rate of change of the frequency (ROCOF) power system data used with phasor measurement unit.

2.3.8 PMU Field installation

The synchrophasor measurement functionality needs not be the sole function or purpose of a device; for instance, many digital relays have PMU functionality but their primary purpose is to serve as a relay rather than as a PMU. Any device that incorporates this functionality — such as digital fault recorders (DFRs) and digital relays — is considered a PMU supported device, i.e. PMU- supported IED. Other unrelated functions of the device must be shown not to affect the performance of the PMU component, and equally importantly the PMU functions must not affect the other functions of the device. The main components of a PMU or PMU-supported IED include analog input signal interface, data acquisition system, phasor estimation module and post-processing module for output data.

PMUs and PMU-supported IEDs are typically installed in a substation or at a power plant. Each phasor requires three separate electrical connections (one for each phase), to either measure a current (from a line or power transformer bank) or a voltage (from either line or bus PTs). A typical PMU installation is shown in Fig.2.19.

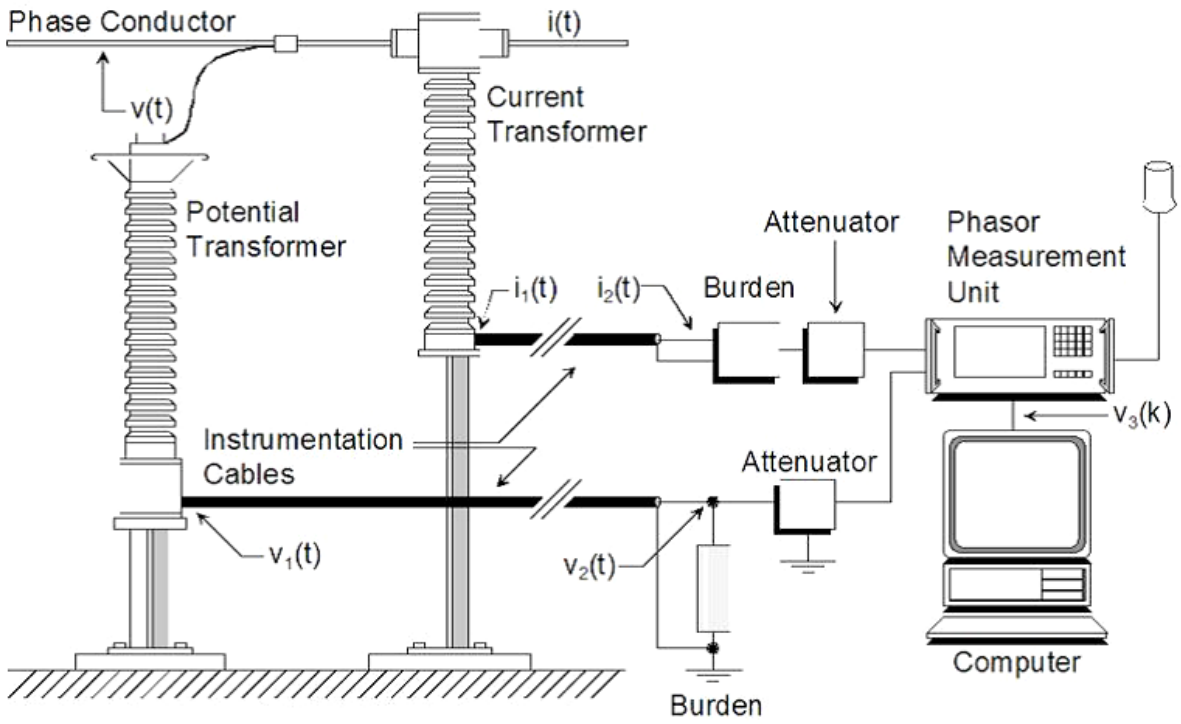


Figure 2.19 A typical PMU installation [6]

2.4 Disturbances Effects on Protection

The digital protective relay uses the measured synchrophasor and executes the implemented protective algorithms which are considered the core of any protective relay. The protection algorithms themselves are usually a sequence of computations of some features of input signals as Root mean square (RMS), impedance, active and reactive power, phasor shifts, etc. These quantities enable to recognize whether a protected element is faulty or in abnormal state and make the primary decision and generate a tripping signal for isolating the faulted section. The multifunction protection unit can be distinguished mainly by three different basic protection principles which are:

Over current protection: This technique is based on measuring the current amplitude in which the over-current due to short-circuit may be used for tripping decision and isolating the faulted elements. The over-current relay usually measures the amplitude of the fundamental current (synchronized current phasor) or obtained from direct RMS calculations.

Differential protection: This technique is based on instantaneous values of current measured at each terminal of a protected element. The differential signals represent a decision variable

beyond which a certain setting value generates a tripping signal. This protection is used for protecting power transformers, generators, bus bars and transmission lines.

Distance protection: This technique is used for protecting transmission lines, generators, and bus bars. It is based on calculating the positive sequence impedance in three phase system obtained from real-time measurements of synchrophasor voltages and currents.

For transmission lines, its positive sequence impedance varies with its length. Using this basis, the measured impedance is compared with the transmission impedance to be protected beyond which is considered as a fault. Thus, the measured impedance indicates whether or not a protected element suffers an internal fault. However, transient behavior of current (dc-decaying) and voltage may induce disturbance in the measured impedance if not well filtered.

The microcomputer unit must also manage a number of interfaces enabling communication with:

- Local keyboard and display,
- Host computer for parameterizing functions,
- Remote relays and phasor data concentrators through communication modules.

Finally, a software part considered as self-monitoring is used for checking the safe operating state of the IED system. This has benefit to improve the reliability of the overall hardware/ software of the IED devices, reducing the number potential hidden failures.

2.5 Disturbances Mitigation Techniques

2.5.1 Anti-aliasing Analog Low Pass Filter

The generated transient signals before and after the fault are passed through an anti-aliasing fourth order Butterworth analog low pass filter, having the following transfer function:

$$H(s) = \frac{1}{(1+1.8478\ s+s^2)(1+0.7654\ s+s^2)} \tag{2.21}$$

Because of its quasi linearity property (Butterworth filter) or constant delay, its amplitude time response is a delayed amplitude, where for the final phasor is corrected by a phase shift linearly dependant of the actual fundamental frequency of the phasor. This filter having a cut-

off frequency 430 Hz is considered to avoid aliasing the higher harmonic components generated during faults simulation of a power transmission network with TCSC.

The DC decaying and the sub-harmonics waveform components, for two fault resistances cases cannot totally be removed as confirmed by the simulation results as shown in Figs 2.20, 2.21 and 2.22. This result agrees with those published in literature see reference [11].

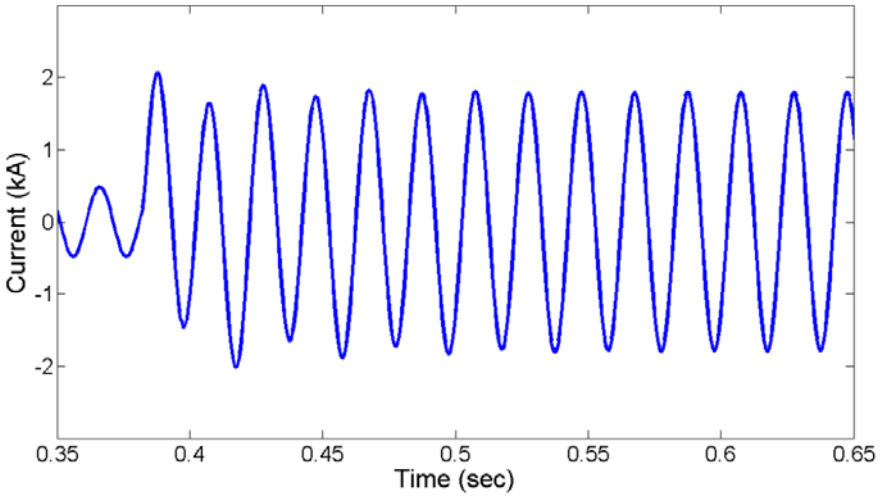


Fig.2.20 Current phasor for soft short after anti aliasing filter

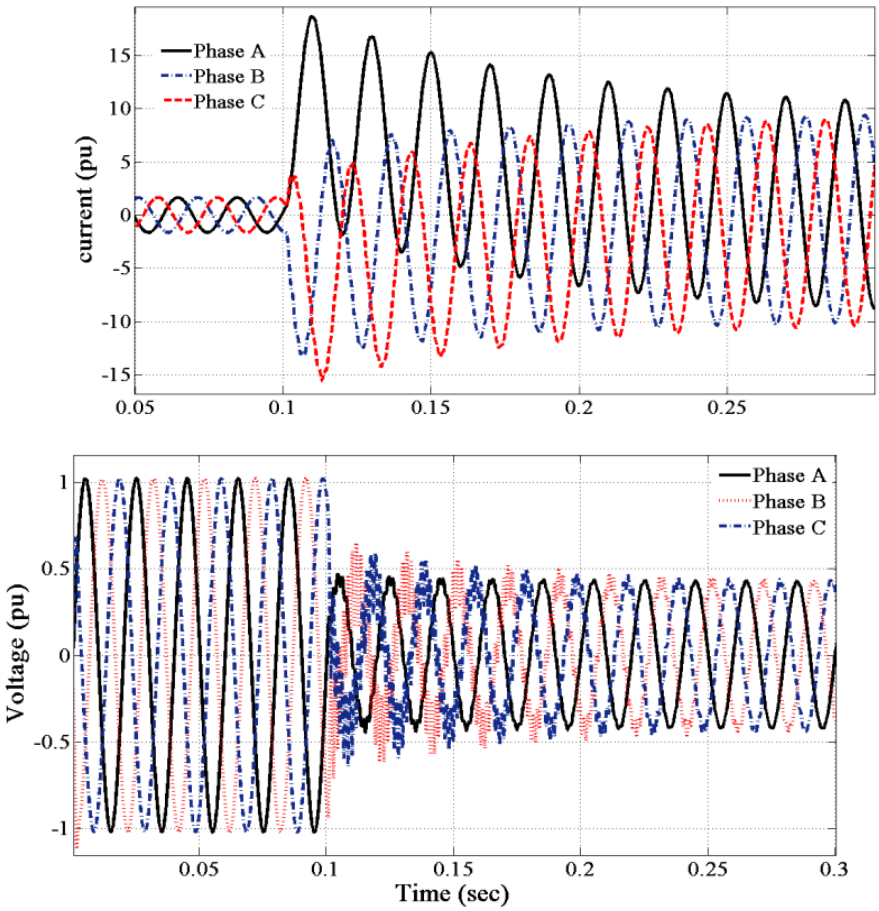
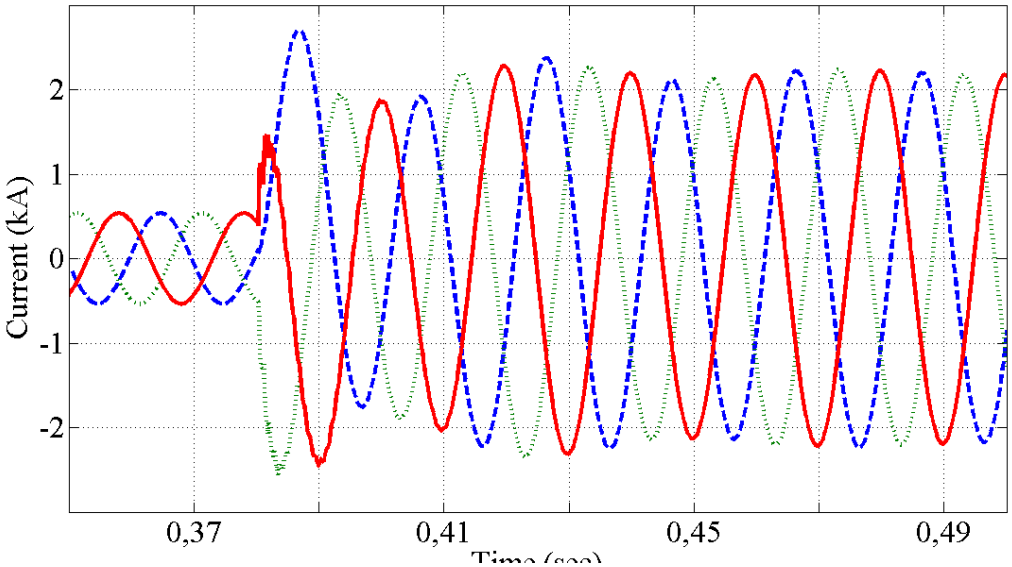
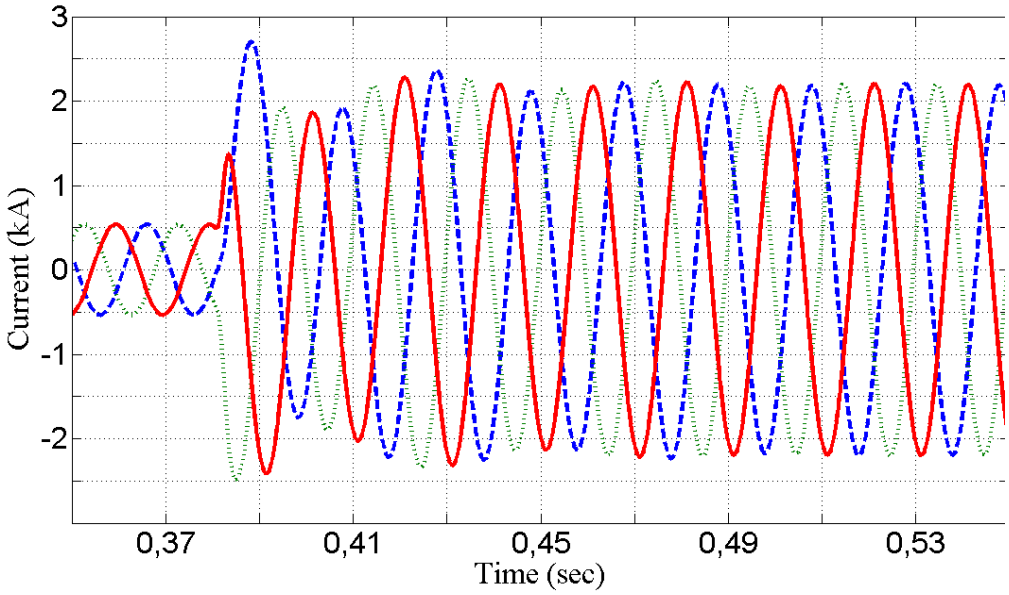


Fig.2.21 Current and Voltage transient waveforms in pu for three phase to ground faults (Rs=0.01Ω): (a) current waveform of anti-aliasing filter output (b) voltage waveforms of anti-aliasing filter output.



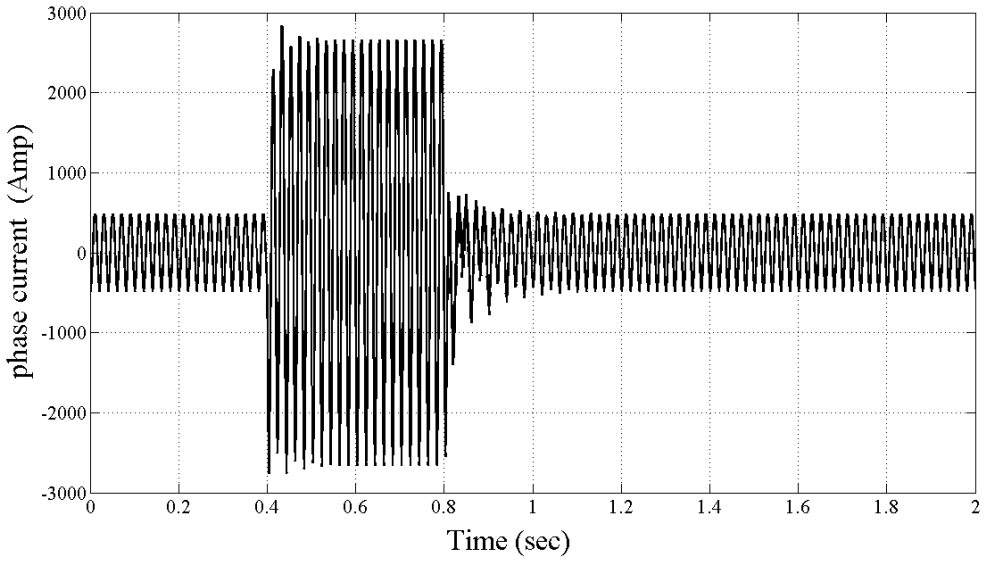
(a)



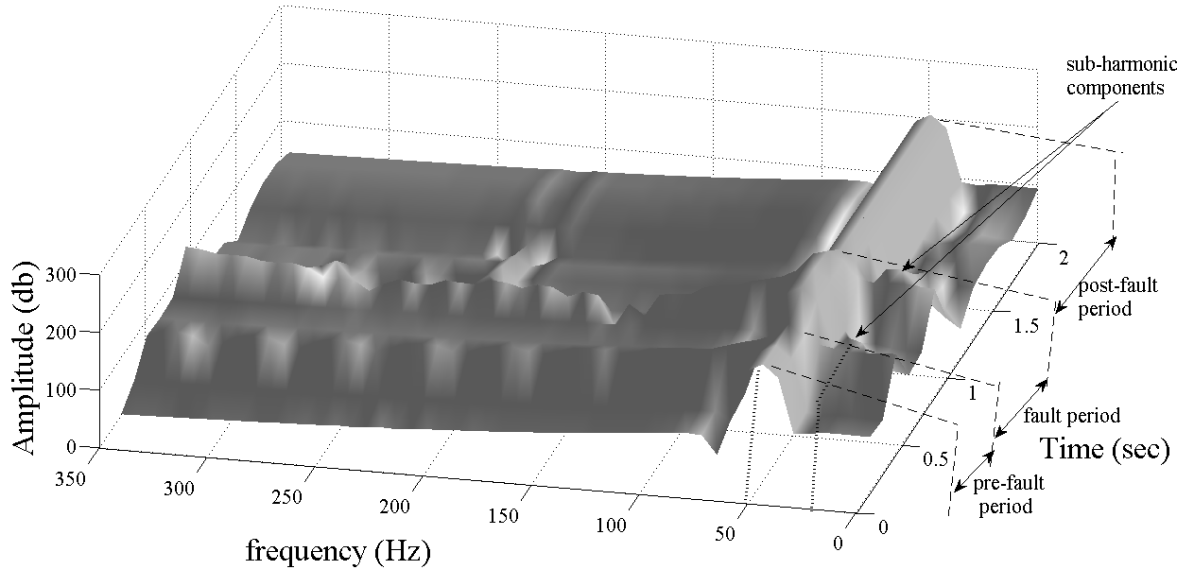
(b)

Fig.2.22 Current in pu after fault for short circuits Rs=100 Ω: (a) without filter (b) with anti-aliasing filter.

On figure 2.23 is presented a soft short line current simulation. On figure (b), the current amplitude FFT shows the existence of both harmonic and sub-harmonic components.



(a)



(b)

Fig.2.23 soft short line fault Ron = 30 ohm, Rg=0.1ohm, line1=100km, line2=200km (a) phase current wave form, (b)Current amplitude FFT for window size of 256 samples, with a hamming filtering window.

The simulation results show that the faulted signals are associated with DC decaying signals, harmonic and sub-harmonic components. The voltage waveform is corrupted by

harmonic components and fast decaying DC components for small resistance faults. The current waveform may be significantly affected, depending on the inception angle, by decaying DC components for small resistance faults. Besides, the sub-harmonic component may also be added in the case of the series compensated transmission line associated with relatively high fault resistance. The DFT algorithm may induce significant errors if it is directly used for phasors computation of these generated signals [33]. To eliminate these unwanted components, many efforts have been developed using different approaches to mitigate the effect of these components on phasor computations.

2.5.2 DFT Measurement Filter

Consider a waveform signal x(t) having a fundamental frequency ω0 and sampled at uniform and distinct time intervals x(k)for discrete computation. The sampling frequency is N times the fundamental frequency ωs=N. ω_0, and obviously the sampling period $T_s = \frac{T_0}{N}$ ($T_0 = \frac{2\pi}{\omega_0}$). Assuming that the signal x(t) is corrupted with dc decaying having sub-harmonic component and M harmonic components, which can be expressed as:

$$x(t) = A_0 e^{-t/\tau}\cos(\omega_{sh} t + \theta_{sh}) + \sum_{n=1}^{M+1} A_n \cos(n\omega_0 t + \theta_n) \quad (2.22)$$

Where A_0 and τ are the amplitude and time constant of dc decaying component, ω_{sh} and θ_{sh} are the frequency and arbitrary phase of the sub-harmonic component, $A_1$and θ_1 are amplitude and arbitrary phase angleof the fundamental component and A_n and θ_n are amplitudes and arbitrary phase angles of the harmonic components.

The signal can be represented in discrete form by:

$$x(k) = A_0 e^{-k.T_s}\cos(\omega_{sh}.k.T_s + \theta_{sh}) + \sum_{n=2}^{M+1} A_n \cos\left(\frac{2\pi n}{N}k + \theta_n\right) \quad (2.23)$$

The full cycle DFT filters, which are among the most popular in relaying, are used to compute fundamental phasor of this signal x(k). The fundamental DFT components of this discretized signal x(k) is provided by[15]:

$$X(k) = \frac{2}{L}\sum_{k=1}^{L} x(k).e^{-j\frac{2\pi}{N}k} = X_r + j\,X_i \quad (2.24)$$

WhereX_r and X_i are real and imaginary part of X(k) and L is the window length of the DFT, for L=N case the full cycle DFT computation is considered. The ideal fundamental DFT of x(t) in equation 2.22 may be calculated for a full cycle as :

$$X_r = \frac{2}{N}\sum_{k=1}^{N} A_1 \cos\left(\frac{2\pi}{N}k + \theta_1\right).\cos\left(\frac{2\pi}{N}k\right) \quad (2.25a)$$

$$X_i = -\frac{2}{N}\sum_{k=1}^{N} A_1 \cos\left(\frac{2\pi}{N}k + \theta_1\right).\sin\left(\frac{2\pi}{N}k\right) \quad (2.25b)$$

The fundamental phasor can be represented in polar form, magnitude and angle, as:

$$A = \sqrt[2]{X_r^2 + X_i^2} \quad (2.26a)$$

$$\theta = \tan^{-1}\left(\frac{X_r}{X_i}\right) \quad (2.26b)$$

2.6 Phasor algorithm using Fourier filter evaluation

The line current signals pass first through an anti-aliasing filter (low pass 4th order Butterworth filter) are sampled by an A/D converters. These samples then are used to compute the phasors depending on whether a half cycle or a full cycle of data samples are considered. In order to evaluate the phasor estimation algorithm, both static and dynamic tests of system response are used. To this end, first the frequency domain and time domain responses are considered to assess this phasor measurement algorithm using specific test signals. Then the algorithm is further tested using data obtained from fault simulation of series compensated power transmission network.

2.6.1 Frequency domain analysis

The actual measuring algorithm is used to estimate the phasors at only the fundamental frequency of the power system. The measuring algorithm must filter and reject all other frequencies located outside the desired or ideal frequency range of measurement. This ideal measurement algorithm is desired to provide phasors inside a narrow bandwidth centered at the fundamental frequency. The magnitude response of this phasor algorithm is presented in Fig.2.25 for the FCDFT filter and HCDFT filter. Also, the cosine filter magnitude response is provided for comparison purposes, since its properties are very well known having unity gain at rate frequency, excellent immunity to dc offset and rejection of harmonic components.

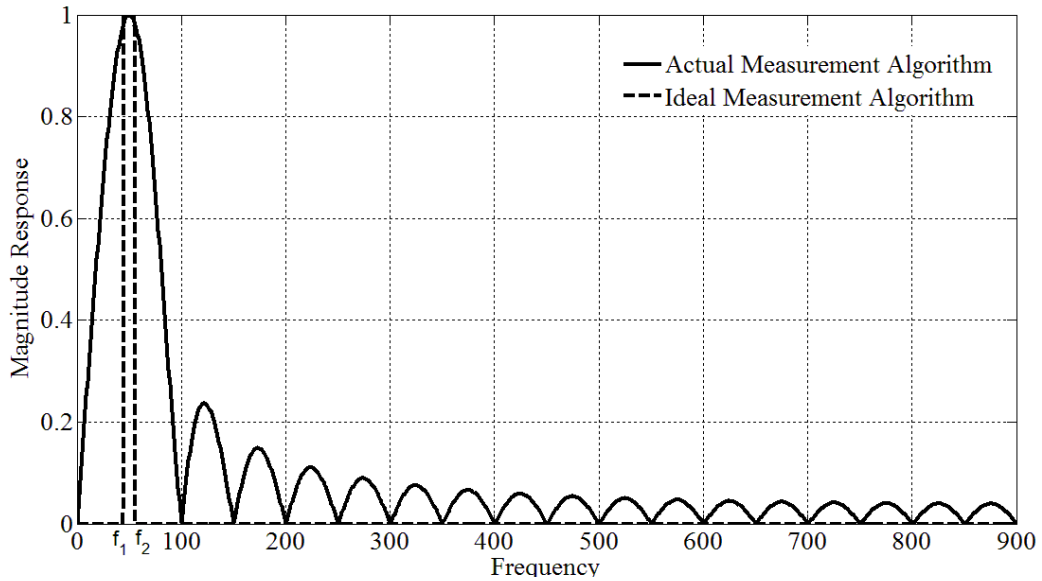


Fig.2.24 Gain frequency response of phasor measurement filters

The measuring algorithm used in the present application is to estimate the phasors at only the fundamental frequency of the power system. This means that the measuring algorithm must filter and reject all other frequencies located besides the desired or ideal frequency range of measurements. The DFT filter and the ideal measurement algorithms are presented in Fig. 2.24 for a 50Hz power system fundamental frequency and at sampling frequency F_s of 1800Hz.

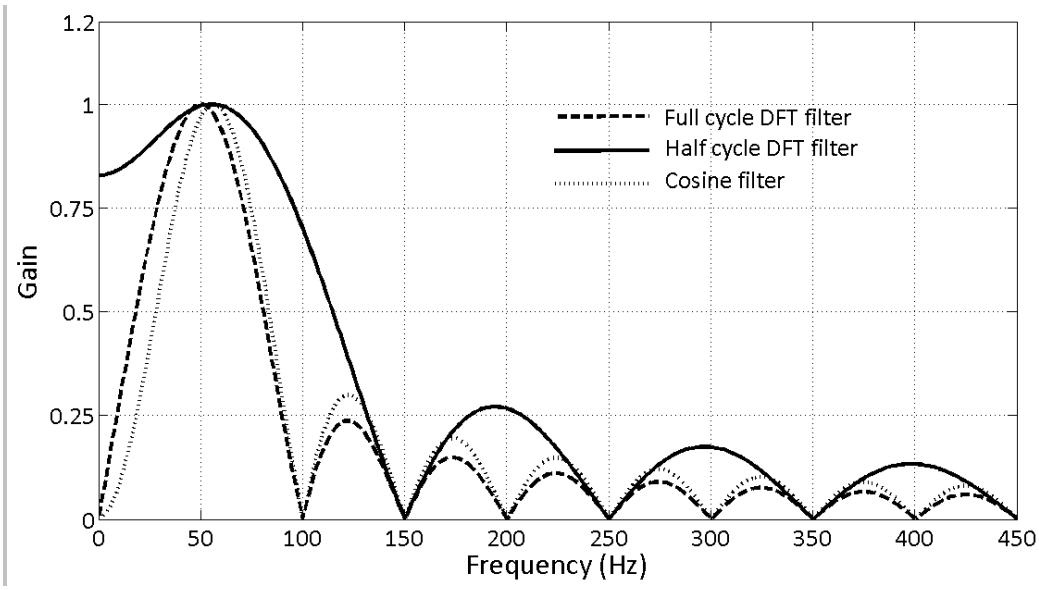


Fig.2.25 Normalized gain response of DFT and cosine filters

A filtering quality may be assessed by evaluating the Magnitude error ε(f) obtained from the absolute difference of the actual and the ideal algorithm. A performance index in frequency domain may be defined as the mean value $\bar{E}_f$ of the absolute error |ε(f)| in the considered frequency range (f_{min} , f_{max}), which can be calculated by

$$\bar{E}_f = \frac{1}{f_{max} - f_{min}} \int_{f_{min}}^{f_{max}} |\varepsilon(f)| df \qquad (2.27)$$

For the ideal selective filter f_{min} = 0 Hz, f_{max} =F_s, f_1= 45 Hz and f_2 = 55 Hz.

The smaller the mean error $\bar{E}_f$, the better the measuring algorithm to reject the undesired components (outside the frequency measurement range) and thus discard or mitigate the effect of the disturbance on the measurement accuracy.

2.6.2 Time domain analysis

In order to evaluate the accuracy and speed of phasors measurement algorithms, the system response error e(t) defined as the difference between the reference or the ideal response and the actual or designed system response. The system response provides many system characteristics as settling time, speed of convergence and accuracy of the measurement system. Figure 2.26 shows a typical measurement algorithm system output response and desired reference response. It illustrates the trade-off between speed and accuracy of measurement.

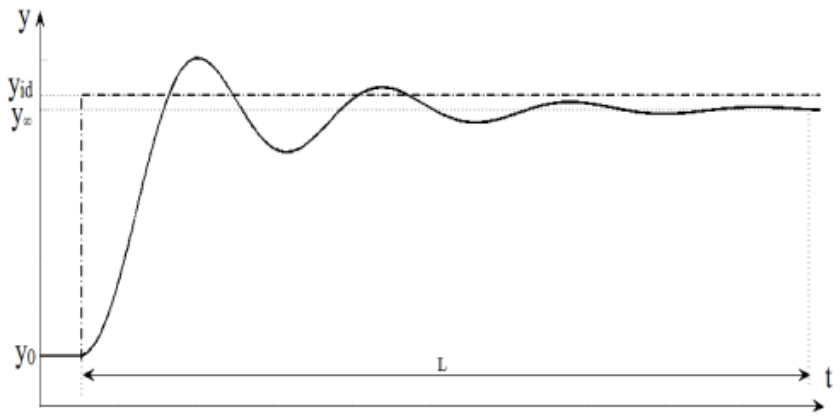


Fig.2.26 Typical system step measurement response

The DFT algorithm has been utilized to compute the phasors of voltage and current phases. But a considerable error may be incurred for the faulted current and voltage phasors due to the DC decaying, harmonics and sub-harmonics components. Thus, the insertion of the digital Filter is necessary before the DFT algorithm for suppressing the harmonics and DC offset decaying components.

2.6.3 Digital Filters

A digital filter based solution is proposed [15] to remove unwanted disturbances using digital filter design techniques. The filter time response must be included in the requirements. The present filtering application imposes different kind of specifications. On one hand, the time domain requirement where both a high speed and accurate system response are needed. On the other hand, the frequency domain requirements (DC, sub-synchronous and harmonic components elimination) which are the magnitude response within small bandwidth including sharp frequency edges as well as an approximately constant group delay in this band are required too. Usually the best optimum value of all the objective functions of this filter design can be obtained for some values of design variables. A compromise or a trade-off between the objective functions must be made to achieve a satisfactory filter design.

The considered recursive digital filter must satisfy: a desired magnitude response specification; a minimum time response or settling time. However, this proposed filter satisfies the former not the latter.

Filter transfer functions

In the general case an IIR filter can be described by its discrete-time difference equation[15] as:

$$y[n] + \sum_{i=1}^{2N-1} c_i\, y[n-1] = \sum_{j=0}^{2M} d_j\, x[n-j] \tag{2.28}$$

Where $x[n]$ and $y[n]$are discrete-time input and output signals. Equation (2.27) can be transformed into the Z-domain and assuming c_i and d_j are real coefficients a second order

form transfer function can be obtained, having 2M conjugate zeros and 2N conjugate poles; called hereafter second order sections (SOS), as:

$$H(x,z) = H_0 \frac{\prod_{j=1}^{2M}(a_{0j} + a_{1j}Z + Z^2}{\prod_{j=1}^{2N}(b_{0j} + b_{1j}Z + Z^2} \tag{2.29}$$

Where a_{ij} and b_{ij} are real coefficients and H_0 is a positive multiplier constant. The polar formulation is also useful and is written as:

$$H(z) = H_0 \frac{\prod_{j=1}^{2M}\left(z - r_{aj}e^{j\theta_{aj}}\right)\left(z - r_{aj}e^{-j\theta_{aj}}\right)}{\prod_{j=1}^{2N}\left(z - r_{bj}e^{j\theta_{bj}}\right)\left(z - r_{bj}e^{-j\theta_{bj}}\right)} \tag{2.30}$$

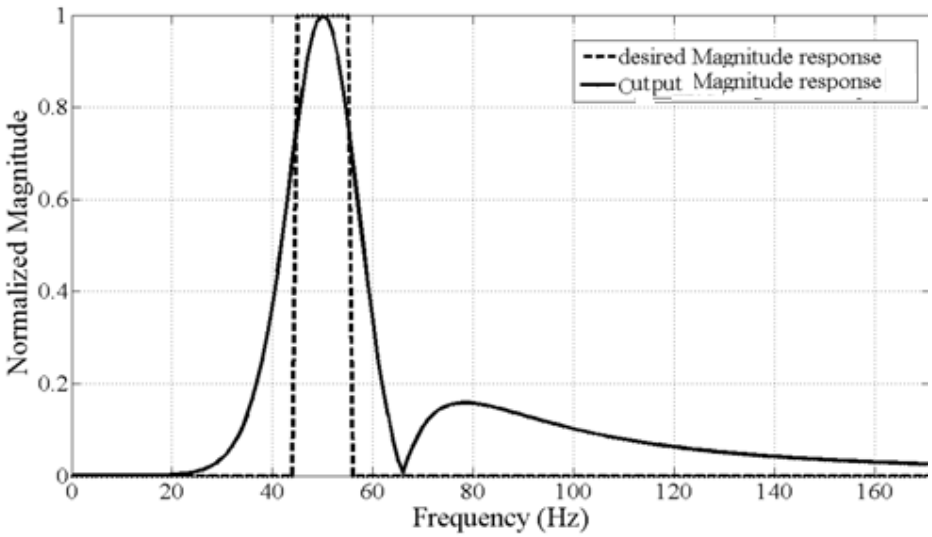
Where a_{ij} , θa_{ij} and rb_{ij} , θb_{ij} are the radii and angles of the zeros and poles, respectively.

The amplitude and the phase responses of a recursive filter is given by

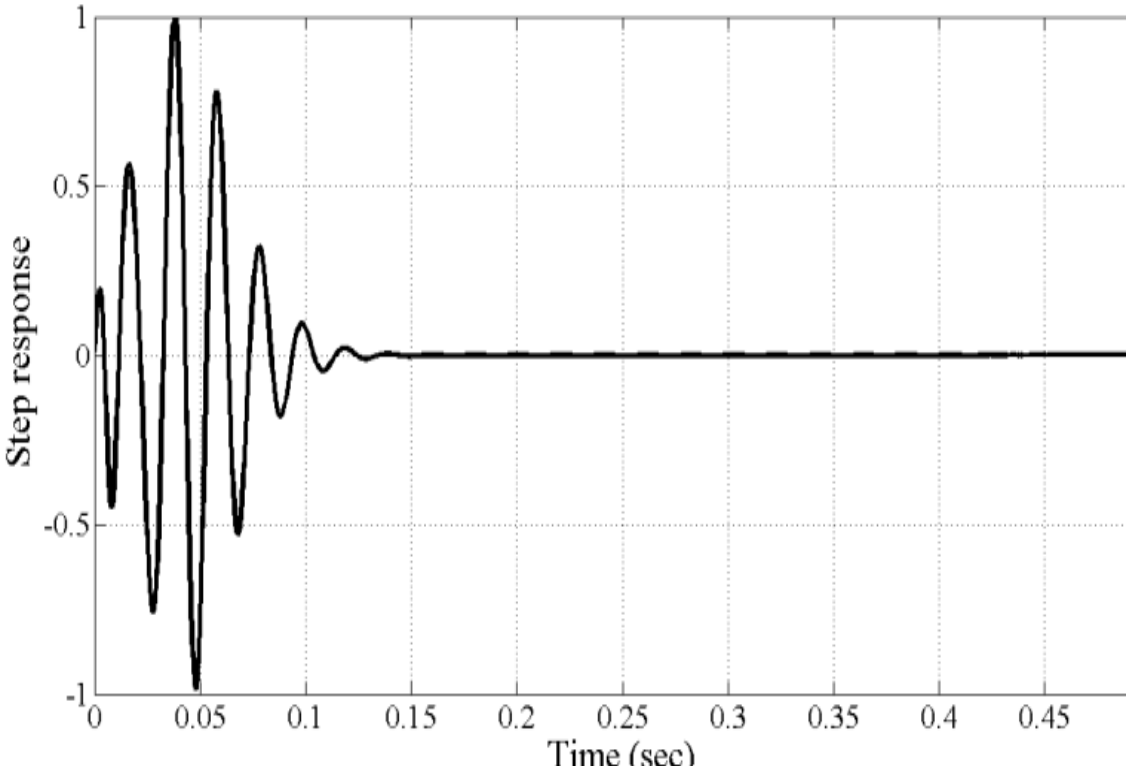
$$A(x,\omega) = \left|H\left(e^{j\omega T}\right)\right| \quad , \quad \phi(x,\omega) = \arg\left(H\left(e^{j\omega T}\right)\right) \tag{2.31}$$

Where ω is the frequency and x is a column vector with 2M+2N+1elements.

Figure 2.27 shows both the desired and the magnitude response of the digital filter. It can be noted that the filter has good performance in the sense that it fulfills the requirements of magnitude response. Indeed, the filter response falls exactly within the desired response and it attenuates all other frequencies as the overall Side-lobe level does not exceed -16dB.



2.27 Magnitude filter response (SOOF)[18]



2.28 Impulse response of the filter and time delay (about 100 ms) (SOOF)[18].

However, the digital filter is not of practical use as it suffers from drawbacks in the dynamic properties. First, as shown in Fig.2.27, the time delay is in the order of 100 ms which is not suitable in the present applications as the requirements specify that the time delay should not exceed one cycle (20 ms). The results are summarized in table I where are presented the filter SOS coefficients and SOS gains.

TABLE 2.2. SINGLE-OBJECTIVE OPTIMIZED FILTER (SOOF) SOS COEFFICIENTS AND GAINS[15]

Section	**Numerator Coefficients a0 and a1**		**Denominator Coefficients b0 and b1**		**Gain**
1	**−1.952033526**	**0.9999998**	**−1.8473812327**	**0.8836**	**$8.977\ 10^{-4}$**
2	**−1.9999996**	**0.9999998**	**−1.9999996**	**0.9999998**	**1**
3	**−1.9999996**	**0.9999998**	**−1.8473812327**	**0.8836**	**1**
4	**−1.8851094580**	**0.9999998**	**−1.8473812327**	**0.8836**	**1**
5	**1.9999998**	**0.9999998**	**−1.8473812327**	**0.8836**	**1**

The proposed phasor estimation algorithms performances are evaluated using specific test signals, generated to emulate the different kind of power system faults. For comparison purposes, the known cosine filter algorithm is considered due to its superior capability of removing the low frequency and harmonic components. The performance indices are computed for various input kind signals with different parameters.

2.6.4 Performance indexes

Three performance indices [3, 8, 13, 65, 68, 69] are considered to evaluate the phasor measurement systems. The first performance index Pi_1 is the normalized mean square index defined as:

$$PI_1 = \frac{1}{N_{ps}(y_\infty - y_0)} \sqrt{\sum_{k=L}^{L+N_{ps}} (y(k) - y_{id})^2}^{\,2} \tag{2.32}$$

Where N_{ps} is considered as the number of post-faults samples (bounding the system output response for a certain arbitrary instant of time). y_{id} , y_∞ are the ideal (without disturbance) and infinite response respectively (actual system response) and L is the sample number at which the fault occurs and y_o is the previous initial or pre-fault value . This index given by Eq.(2.31) is computed for a fixed window (N_{ps} samples) starting from the L-th sample, where the fixed window is considered for one cycle, since the desired relay steady-state output is expected to be within the first cycle or less after the fault incidence. It is associated to either, the transient error energy giving more importance to larger errors and less importance to small errors, and the speed of convergence of the output response to the steady-state. When PI_1 index is closeor equal to zero, it can be concluded that the disturbance has no effect on the measuring filter output, and the system output response has a very small settling time.

Important information is also needed after the first cycle following time the fault is induced; the filter output starts to oscillate around the steady state output level. Thus another performing index (PI_2) is used to indicate if the filter output is free of oscillation around the steady state regime, and is defined as:

$$PI_2 = \frac{1}{M}^{2} \sqrt{\sum_{k=L_1}^{L_1+M} \left(\frac{y(k)}{y_{id}} - 1\right)^2} \tag{2.33}$$

Where M is the considered number of post-steady state samples (M=3xN) and L_1 is the sample number taken atN_{ps}, considered as the steady state starting sample taken one cycle after fault event.

A third performance index (PI_3) is used to indicate the percentage maximum overshoot in the magnitude output and is defined as follows:

$$PI_3 = \frac{Max\,(y(k) - y_{id})}{y_{id}} \times 100\% \tag{2.34}$$

This PI_3 factor may be related to the relay maximum overreach.

2.7 Conclusion

The study of disturbance effects on the measurement quality has been investigated during the faults in 400kV overhead long transmission line with series TCSC compensator. A power system simulator based on MATLAB/Simulink associated with PSB has been used to generate voltage and current signals for different locations and inception angles of faults. Also the DFT algorithm has been utilized to compute the phasors of voltage and current phases. The considerable error has been incurred for the faulted current and voltage phasors due to the DC decaying, harmonics and sub-harmonics components. The insertion of the filter is necessary before the DFT algorithm for suppressing the harmonics and DC offset decaying components but it is always associated with time delay.

Chapter 3

Protection System Reliability Analysis

A distance relay, which is widely used for protecting a power transmission line as the primary as well as remote backup device, may be affected by the power disturbances such as power swings and post-faults. Consequently, false trips of protection system may be resulted. Root cause analysis based on fault tree analysis has been used to identify disturbances which may lead to false trips. Once the critical root causes have been identified, conventional mitigation measures are used and then, new blocking function and digital filters are proposed to enhance the security of the system. The quantitative analysis of the improved model shows an increase of about 3% of the security which implies an appreciable enhancement of the reliability of the considered protection system.

3.1 Introduction

A protection system is a vital part of any electric power system and plays an incredible role in maintaining high degree of availability required in present day. The failure of one relay of the protective scheme to operate as intended may place at risk the stability of the whole power grid and hence may lead to blackout.

A Cigré study found that 27 % of bulk power system failure (blackout) resulted from false trips of protection system. Besides, an analysis of 17 years data provided in NERC reports revealed that 63% of major disturbances are protection related protective relaying which suffers from two types of problem: false trip (unnecessary tripping) and fail to operate [19-21].

Major power system disturbances are more likely to be caused by unnecessary tripping rather than by the failure of a relay to take action [21]. In fact, a major cause of power system instability is due to the relative long time delay for fault clearance of zone three backup relays. In order to overcome the drawbacks of these relaying systems, many techniques have been developed such as a blinder that blocks the relay to operate during the power swing [22].

The mal-operation of this relay is generally due to not only unnecessary tripping during power swing that reduces the security of protection system and hence its reliability but also unnecessary blocking when symmetrical fault occurs accompanying a power swing [23]. This latter action may affect on a dependability of the relay and hence its reliability. Many techniques have been developed to unblock the operation of the relay during power swing associated with a fault condition such as a negative sequence current magnitude and a derivative of current angle [24], and a combination of waveform of swing center's voltage (WSCV) and synthetic negative vector [25]. A more advanced new blocking and unblocking function based on power swing detector using Phasor Measurement Units (PMUs) has been proposed [23,26,27]. In addition to the local phasors information, the proposed scheme uses remote phasors information from different locations for power swing detection, which can be provided at high speed by PMUs. These measurements are used for calculating the apparent power absorbed by power line and the difference in phase angles of voltages that may be used for detecting power swings and faults. Hence, the proposed scheme blocks tripping signal during the power swing and unblocks it during fault condition.

Moreover, protective relays can easily discriminate between fault and non-fault conditions when power quality is good. When power quality is poor, the threshold between normal and fault conditions becomes imprecise. In the relaying application, engineers can no longer rely on the performance of the relay under conventional normal system conditions. However, under conditions of poor power quality especially in the smart power grid including TCSC, they have improved the relay performance by designing digital filters which in turn make the relay more secure and dependable. In several cases, transmission line protective relays have undesirably operated in response to harmonics or dc offset in the power grid [28]. From the obtained evaluation using the ideal network, the DC offset may have an effective impact on the Fourier algorithm and if no correction is taken on, the relative error of the real amplitude from the Fourier algorithm may attain 20%, which is mainly caused by this decaying dc offset. In protection applications, such large relative error is not permissible. The performances of these techniques employed directly establish the measurements of these protection systems and affect their reliability. Hence, the real-time accurate phasor measurement of the fundamental component and/or symmetrical components is essential and crucial to the safe operations of protection system [29, 30].

In this study, Root Cause Analysis based on fault tree analysis is used to identify disturbances first and root cause of false trips of a protective relay which may lead in cascading to blackout. Once the critical root causes are identified, conventional mitigation measures have been used first and then blocking and unblocking functions and digital filters in view of increasing the reliability of the considered protection system are proposed. Previous works [31-33] proposed some efficient solutions (based mainly on using digital filters) to obtain accurate and disturbance-free phasor measurements. As a result, the reliability of the measuring block of the protection system has been significantly improved. However, this improvement concerns the reliability of one part (the phasor measurement block) of the protection system. In the present work the reliability of the global protection system is considered. This new approach has many advantages compared to those published in previous works as it allows obtaining an important quantitative figure (security). This permits to selectively reinforce the elements of the protecting system which are most likely apt to failure and hence the impact on the overall system's cost is significant. Another main advantage is that unlike former works, our approach takes also into account the reliability of the software

part of the system which is considered to have a significant contribution in the overall reliability of the protecting system.

A protective system should be designed to recognize certain system abnormalities which, if undetected, could lead to damage equipments or extended loss of service. The design and specification of the system components is an important part of the protective strategies and power system are designed to withstand the usual operating contingencies that accompany load changes and line switching operation. There is several design consideration that must be weighed against cost in devising a protection strategy, the following fundamental requirements that are considered in designing the protective systems with a good performance of a relay are [19-21]:

Reliability: it is the ability of the relay system to operate under the predetermine condition. Without reliability, the protection will be rendered largely ineffective and could even become a liability. The reliability of a relay is directly in correspondence with the concepts of dependability and security. A relay is said to be dependable when it operates in the occurrence of a fault relevant to its protection zone. In other words, dependability is a measure of the relay ability to operate when it is supposed to operate. Security is defined as “the degree of certainties that a relay or relay system will not operate incorrectly”. Security is reached either when the relay will not operate for a fault outside its operating zone, or when the system is in a healthy state.

Selectivity: is the ability of the protective system to select correctly that part of the system in trouble and disconnect the faulty part with disturbing the rest of the system.

Selectivity discrimination can be achieved by time grading or by unit protection. Selectivity by time grading means that different zones of operation are graded by time and that in the occurrence of a fault, although a number of protections equipment respond, only those relevant to the faulty zone complete the tripping function. Selectivity by unit protection means that the relay will only operate under certain fault conditions occurring within a clearly defined zone.

Speed: the relay system should disconnect the faulty section as fast as possible for the following reasons. In the occurrence of a fault, the greater the time in which the fault is affecting the power system, the greater is the risk that the power system falls into an unstable operation point. Relays are therefore required to clear the fault as quickly as possible.

1. Electrical apparatus may be damaged if they are made to carry the fault current for a long time.
2. A failure on the system leads to a great reduction in the system voltage. If the faulty section isn't disconnected quickly, then the low voltage created by the fault may shut down the customers' motors and the generations on the system may be unstable.
3. The high speed relay system decreases the possibility of development of one type of fault into more sever types.

***Sensitivity*:** it is the ability of the relay system to operate with low value of actuating quantity. In other words, the relay is said to be sensitive if the relay operates to the minimum value of faulted input signals.

Simplicity: the relaying system should be simple so that it can be easily maintained. Reliability is closely related to simplicity. The simpler the protection schema the greater will be its reliability.

Economy: the most important factor in the choice of a particular protection scheme is the economic aspect. Sometimes it is economically unjustified to use an ideal schema of protection and compromise methods have to be adopted. As a rule, the protective gear should not cost more than 5% of total cost. However, when the apparatus to be protected is of utmost importance, economics considerations are often subordinate to reliability.

The relay application for protection of power system date back nearly 100 years ago. Since then, the technology employed to construct relays have improved dramatically relay size, weight, cost and functionality. Based on the technology employed for their construction, relays can be classified as follows:

Electromechanical relays: The first relays employed in the electric industry were electromechanical devices. These relays worked based on creating a mechanical force to operate the relay contacts in response to a fault situation. The mechanical force was established by the flow of a current that reflected the fault current through windings mounted in magnetic cores. Due to the nature of its principle of operation, electromechanical relays are relatively heavier and bulkier than relays constructed with other technologies. Besides, the burden of these relays can be extremely high, affecting protection purposes. However, electromechanical relays were so largely employed, tested and known that even modern relays

employ their principle of operation, and still represent a good choice for certain conditions of application.

Solid-state relays: With the advances on electronics, the electromechanical technology presented in the relays of the first generation started to be replaced by static relays in the early 60's. Static relays defined the operating characteristic based in analog circuitry rather than in the action of windings and coils. The advantages that static relays showed over electromechanical relays were a reduced size, weight and electrical burden. However, static relays showed some disadvantages since analog circuitry is extremely affected by electromagnetic interference and the ranges of current and voltages values are strongly restricted in analog circuits, affecting the sensitivity of the relay.

Digital relays: Incorporating microprocessor into the architecture of relay to implement relay and logic functions started happening in the 80's. Digital relays incorporated analog-to-digital converter (ADC) to sample the analog signals incoming from instrument transformers, and used microprocessor to define the logic of the relay. Digital relays presented an improvement in accuracy and control over incoming signals, and the use of more complexes relay algorithms, extra relay functions and complementary task.

Numerical relays: The difference between numerical relays and digital relays lies in the kind of microprocessor used. Numerical relays use digital signal processors (DSP) cards, which contain dedicated microprocessors especially designed to perform digital signal processing.

3.2 Distance relay

Distance relay may be used in the power grid protection. The basic principle governing the operation of a distance relay is the impedance Z at the relaying point as shown in Fig.3.1. Then, the measured impedance is compared to the set impedance, and if this impedance is within the reach of the relay then it operates.

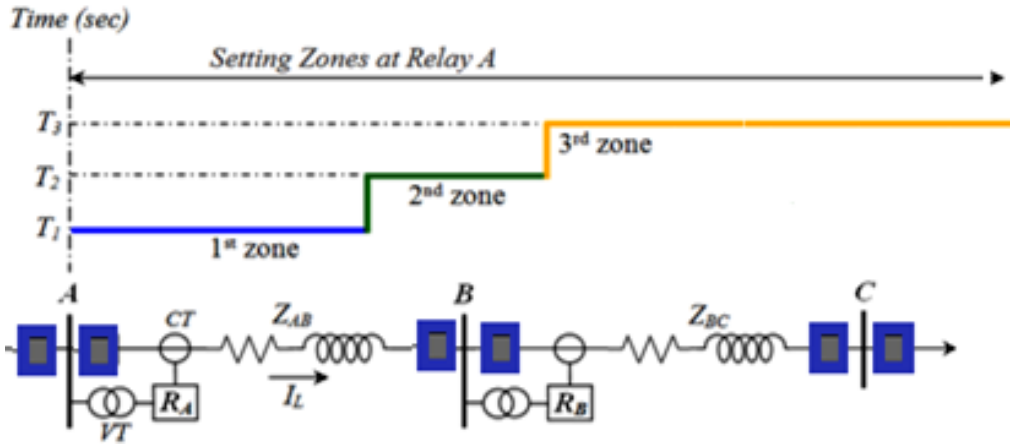


Fig.3.1 A typical single line AC connection of a protective distance relays.

Distance relay can be implemented through the use of phase comparators of two input quantities for obtaining the operating characteristics which may be circles when plotted on an R-X diagram. For the impedance elements of the distance relay, the two quantities being compared are the voltage and current measured by the relay.

The signals S1 and S2 that may be introduced to the phase comparator are in the following form:

$$S_1 = -KI + K_1|V|\angle(\theta - \varphi) \quad (3.1)$$

$$S_2 = KI + K_2|V|\angle(\theta - \varphi) \quad (3.2)$$

The general equation of phase comparator at threshold condition can be obtained as follows:

$$-K^2I^2 + \left[\begin{matrix}-KK_2\cos(\theta - \varphi) + K_1K\cos(\theta - \varphi)VI \\ +K_1K_2V^2\end{matrix}\right] = 0 \quad (3.3)$$

Letting $Z = V/I$, we get:

$$-K^2 + K_1K_2Z^2 + K\,Z\,(K_1 - K_2)\cos(\theta - \varphi) = 0 \quad (3.4)$$

Replacing Z^2 by $R^2 + X^2$ and after some Algebraic manipulations, we finally obtain:

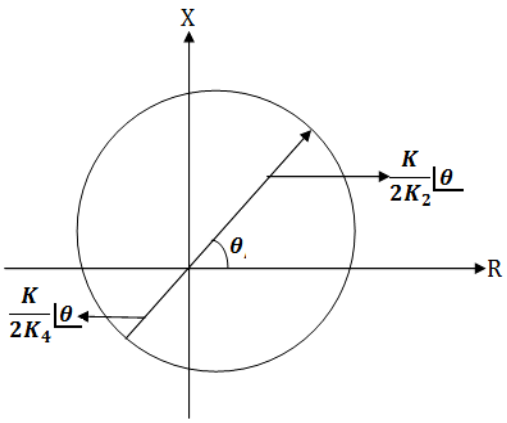


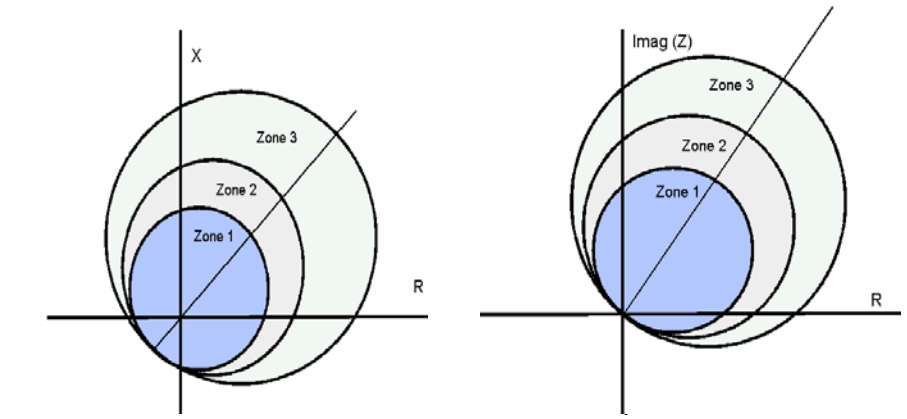
Fig.3.2 The characteristic of the offset mho relay.

$$\left(R-\frac{K'(K_1-K_2)}{2K_1K_2}\cos\theta\right)^2+\left(X-\frac{K(K_1-K_2)}{2K_1K_2}\sin\theta\right)^2=\left(\frac{K(K1+K_2)}{2K_1K_2}\right)^2 \quad (3.5)$$

This equation represents a circle with a radius of $\left(\frac{K}{2K_2}+\frac{K}{2K_1}\right)$ and centered at $\frac{K(K_1-K_2)}{2K_1K_2}\angle\theta$ on the R-X plan. Figure 2 shows the characteristic of the offset MHO relay.

The distance relay can be set to protect different zones of a transmission line either in forward direction (MHO characteristic) or in both forward and backward direction (Offset MHO characteristic). Figure 3 shows characteristics of a Mho relay.

The zone 1 protection for the MHO relay should never fall outside of the line to be protected as shown in Fig.3.1. Normally it is protecting up to 80-90 % of the line. Therefore, the remote transmission line end is not protected by zone 1 relays. Zone 2 relays protect the entire transmission line section and a half of the next section but for coordination purpose a time delay may be introduced. Zone 3 relay is normally a backup protection for an adjacent transmission line sections associated with longest time delay.



(a) (b)

Fig.3.3. (a) Offset Mho and (b) Mho relays characteristics.

3.3 Root Cause Analysis

Root cause analysis is a step by step approach that leads to identify a disturbance's first or root cause. There are specific successions of events (disturbances) that lead to a failure such as false trip. A root cause analysis investigation follows the cause and the effect path from the final outcome back to the root cause [31]. In this case, a Fault Tree is constructed to determine all possible causes that can lead to the undesirable top event that is false trip.

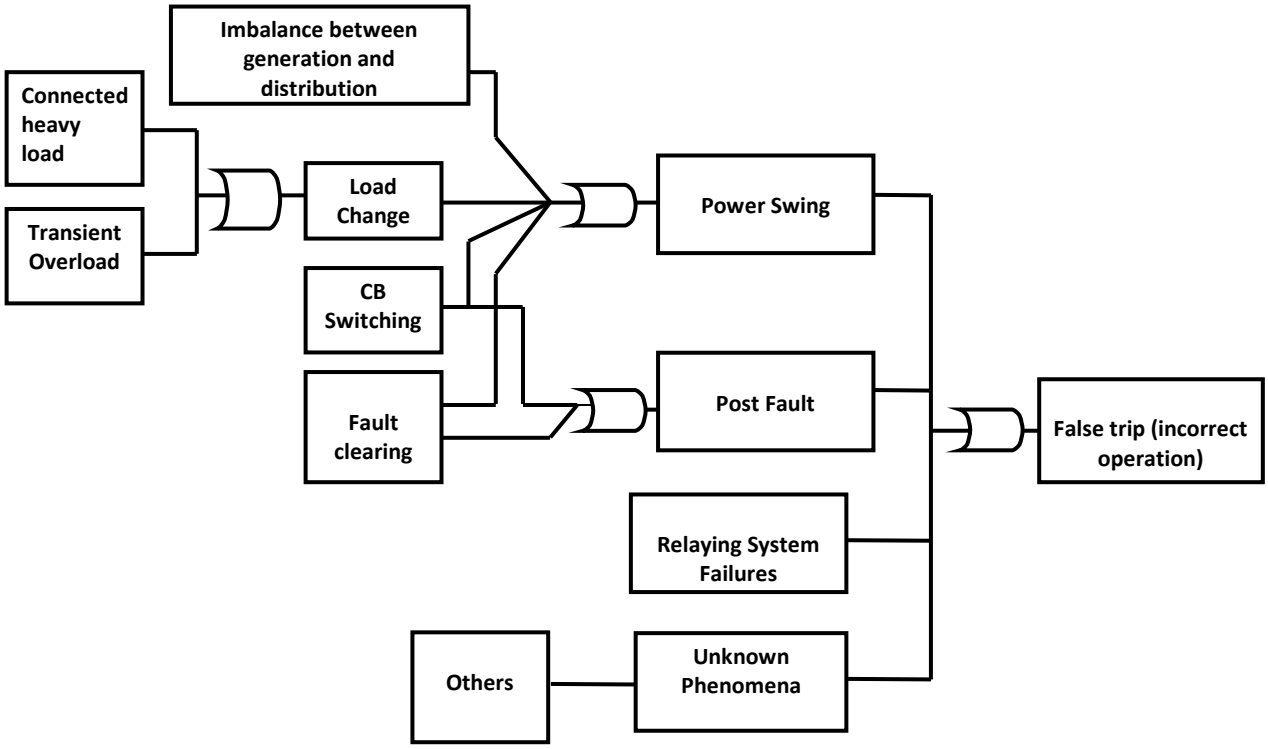


Fig.3.4 Root cause Analysis based on FTA of false trip.

Table 3.1 Disturbances causes with their weights (proportions).

Disturbances	Abbreviation	Causes	W (%)
Power swing	PS	Power generation unbalance and load change.	30
Post-fault	PF	Switching actions	30
Relaying system	RS	Self technical failures in hardware or software parts and or incorrect setting, current transformer saturation	20
Others	UP	Unknown phenomena	20

A small power system integrating one source and three busses with three zones relays at each bus can be considered in this research paper as shown in Fig.3.1.

From field data, false trips may generally be caused by stable power swings, post-faults, the relay system failures or other unknown phenomena as given in Table 3.1 [35, 36]. These

phenomena may include harmonics, DC offset and sub-harmonics generated by power electronic devices in the modern power grid. The fault tree diagram of the false trips (incorrect operations) has been illustrated in Fig.3.4.

3.4 Relaying System Reliability

A reliable relaying system can be achieved by redundancy i.e. duplicating the relaying system. Obviously redundancy can be a costly proposal. However, it is important to realize that back-up protection for safe operation of relaying system. Redundancy in protection also depends upon the criticality of the power apparatus to be protected.

A quantitative measure for reliability is defined as follows:

$$R = \frac{N_c}{N_d + N_i} \tag{3.6}$$

Where, Nc : Number of corrected trips, Nd: Number of desired trips, Ni : Number of incorrect operations (false trip).

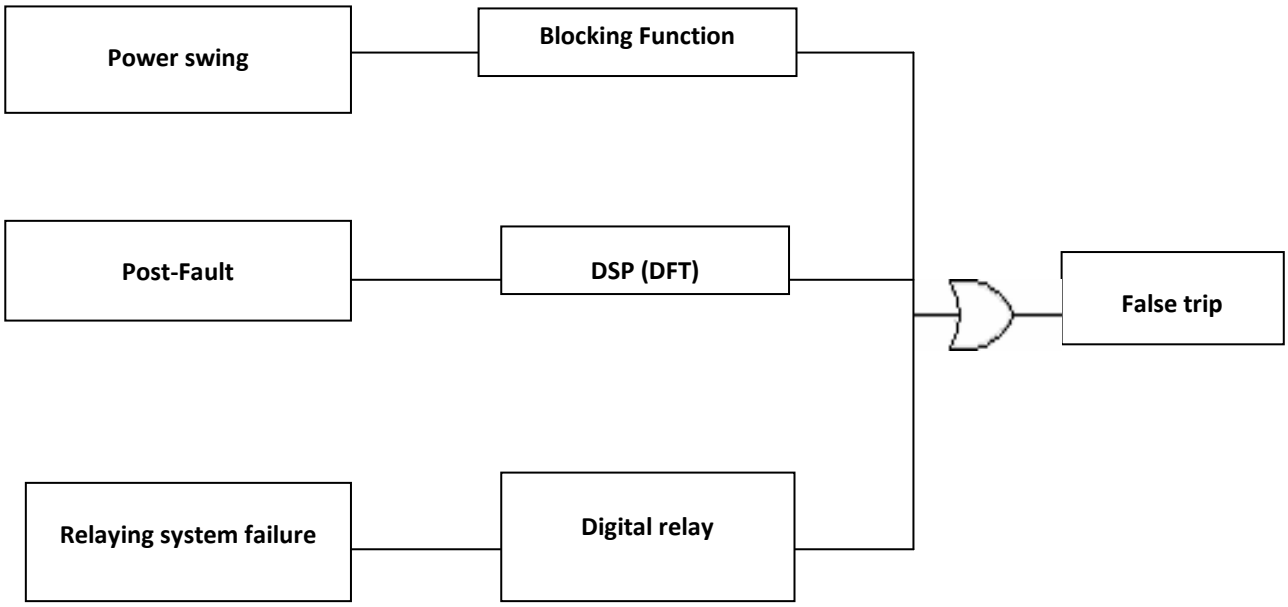
Protection system reliability is characterized by following two important terms: 1-Dependability, and 2-Security.

3.4.1 Dependability

A relay is said to be dependable if it trips only when it is expected to trip. This happens either when the fault is in its primary control (primary protection) or when it is called upon to ensure the back-up protection. However, false tripping of relay due to faults that are either not within its jurisdiction or within its purview may lead to power system instability. Power system may get unnecessarily stressed or else there can lose its service. Dependability (D) is the degree of certainty that the relay will operate correctly:

$$D = \frac{N_c}{N_d} \tag{3.7}$$

Fig.3.5. Root cause (FTA) of false trip after providing barriers.



3.4.2 Security

On the other hand, security is a property used to characterize false tripping of the relays. A relay is said to be secure if it does not trip when it is not expected to trip. It is the degree of certainty that the relay will not operate incorrectly during a given time interval according to the IEEE/PSRC Working Group [37].

$$S = 1 - \frac{N_i}{N_t} \tag{3.8}$$

Where S: security, and Nt =Nc+Ni: total number of trips.

3.4.3 Software Reliability Model

In software engineering, most of failures are due to errors, 'Bugs' or defect built into software from the beginning at design stage or exploitation and this may cause malfunction or halt in digital relaying system.

Assuming that an error is eliminated without causing any new errors, the simplest model that takes this into account is the following; let the number of errors N initially equal to No and let each has the same probability of detection p (and hence elimination) per unit time, then the failure rate is expressed as follows [38] :

$$\lambda(t) = pN(t) = pNo\exp(-pt) \tag{3.9}$$

In this model, the failure rate is decreasing with time in exponential fashion with the essential tasks of debugging in order to eliminate the errors. The expression for reliability growth is given as follows:

$$Rs = \exp(+N) = \exp[\exp(-pt)] \tag{3.10}$$

3. 5. Distance Relay Reliability (Security)

Subsequent to the identification of potential root cause of false trips (incorrect trips), the preventive mitigation (barriers) for enhancing the security and hence reliability of the relay has been proposed.

The weighted important factor of the disturbance cause, obtained previously, will provide the priority on mitigations and barriers which can be provided first against fast power swing, post fault and relaying system failures as shown in Fig.3.5.

Traditional impedance-based techniques for detecting power swings in the transmission network as shown in Fig.3.1, involve measuring apparent impedance and introducing a time delay between two measuring elements. The impedance measurement is typically a phase-phase impedance, where all three phase-phase loops are required for operation, or it is positive-sequence impedance.

A timer is started when the apparent impedance enters the characteristic as illustrated in Fig.3.6. If the apparent impedance remains between the inner and outer characteristics for the set time delay, the Power Swing Block (PSB) element operates and selected distance element zones are blocked from operation for a period of time. A timer determines if the change in impedance is due to a fault or a power swing. If it is an unstable power swing, then one can select tripping on the way into the characteristic or on the way out of the characteristic. Selection of tripping on the way in or on the way out is determined from numerous stability studies and the ability of the circuit breakers to isolate the circuit with a significant voltage angle across the breaker [25].

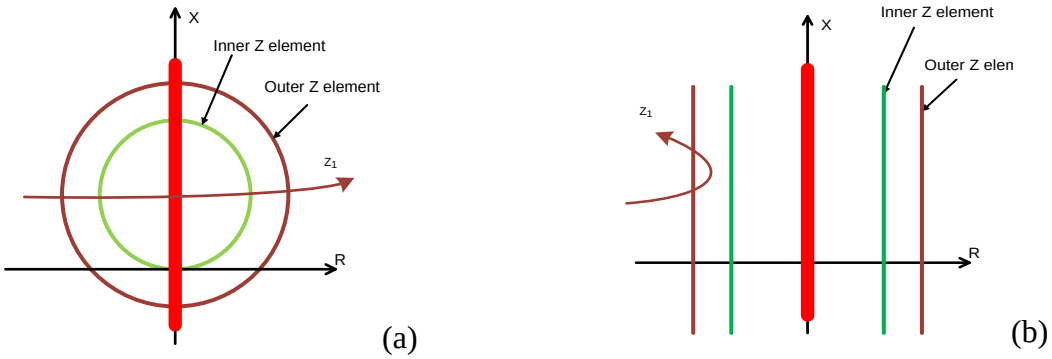


Fig.3.6. Different power swing protection schemes: (a) Double blinder, power swing characteristic, (b) Offset mho, power swing characteristic.

Lines currents disturbances in a transmission line which contain a dc offset which decays exponentially, and/or a large number of unwanted significant harmonics due to switching actions may cause false trip of the relay. In digital relay, Discrete Fourier Transform (DFT) is the most widely used filtering algorithm [39-40] for computing the fundamental components and illuminating these disturbances.

These false trips may be produced from power swing, post-fault or switching actions. They do not just create trouble. They can even compromise system security. One way to categorize the data from the chosen utilities' relay operations is as follows: Over (Ne=1425) total events or disturbances per year we have the following data indicated in table 2 [37, 41].

The probability of occurrence of power system disturbances leading to false tripping relative to the total number of disturbances or events can be evaluated as follows:

$$PDT= Ni /Ne \tag{3.11}$$

The average value of disturbances leading to incorrect tripping is evaluated 4.6 for a given time interval. Then, the probability of occurrence of each cited disturbance leading to the false trip can be obtained as follows:

$$Pft=PDT*w \tag{3.12}$$

The quantitative evaluations associated with the weight values are given in table 3.3 [38].

Table 3.2 Statistics for different operations

Operations	Symbole	value
Corrected trips	Nc	1346
incorrect operations (False Trips)	Ni	66
Desired trips	Nd	1359
Failure to operate	Nf	13

Table 3.3 False trips causes' probability.

Disturbance	W (%)	False trips causes' probability	False trips causes' probability
PS	30	PPS	0.0138
PF	30	PRF	0.0138
RS	20	PRS	0.0092

The total probability of occurrence of the known disturbance leading (with the assumption of independency) to unnecessary tripping is evaluated as follows:

$$Pun=Pps\ U\ PPFU\ PRS \tag{3.13}$$

$$Pun \approx \Sigma Pft = 0.0368 \tag{3.14}$$

Hence, the security value is deduced as the complement of the previous probability:

$$S = 1- Pun= 1-0.0368=0.9632 \tag{3.15}$$

The existing security for the given protective system can be obtained using Eq. (3.8) which is Se=0.9632 or through the use of Eq.(3.15). It can be noted that they are approximately equals.

3.6. Distance Relay Reliability Enhancement

After identifying a root cause of false trips (incorrect trips), the previous preventive mitigation has been used. However, for further enhancing the reliability of the relay, recent developed techniques used as barriers have been proposed.

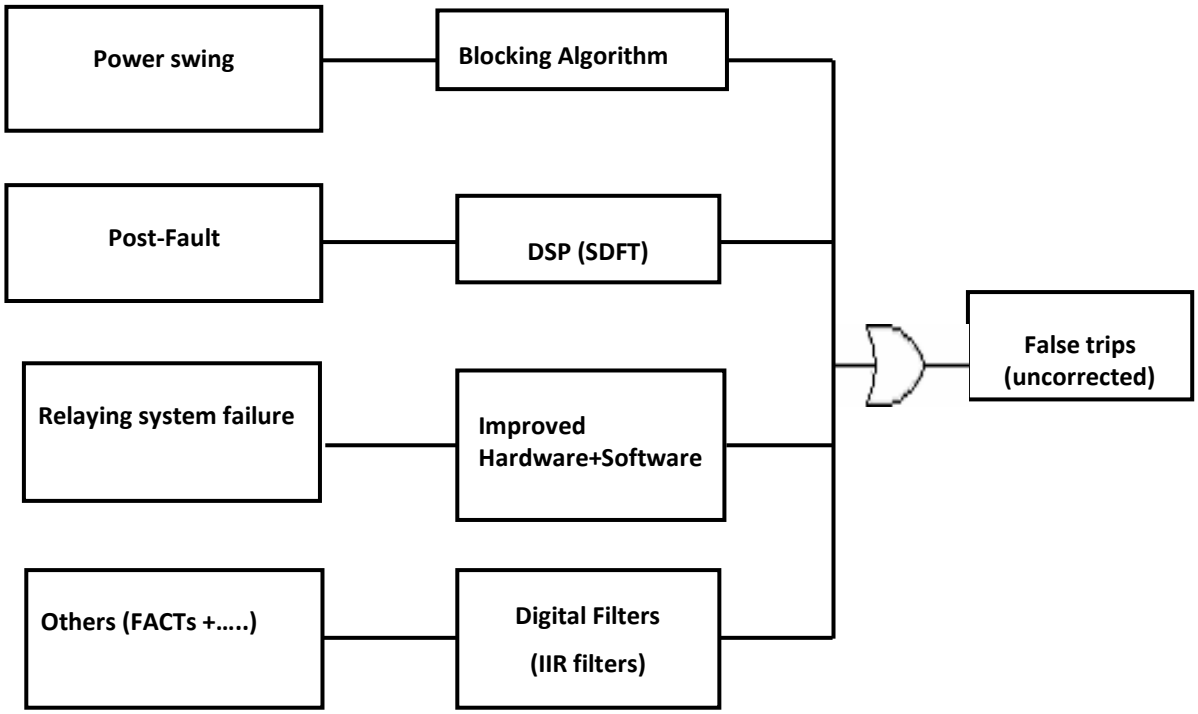


Fig.3.7. Root cause (FTA) of false trip after improving barriers.

Recently a new approach has been proposed by integrating software measurement algorithm that will detect the power swing to enable and to give order to block or unblock the relay trips [23]. In that research work, two PMUs may be used for measuring phase-currents and phase-voltages at both ends of the transmission line. These values can be received every 20ms. On the base of these measurements, an angle δ and apparent power S absorbed by power line are calculated and used in developed algorithm for detecting and distinguishing the power swing from the fault. The algorithm is implemented as a set of Matlab routines and its performance is successfully tested by simulation.

The thyristor-controlled switched capacitor (TCSC), which may be used to enhance and optimize the use of the transmission network facilities, may also generate these DC

components and harmonics [28]. This latter always needs few cycles (10– 20 cycles) for obtaining accurate fundamental phasors by DFT algorithm. Such waveform distortion caused by the insertion of TCSC, may affect the reliability of the protective relays and may cause relays false trips.

The weaknesses of the previous algorithms have been overcome by many other research works [23, 26, 28]. For removing the DC-components and associated unwanted signals, digital filters such as IIR filters have been proposed.

Using the model illustrated in Fig.3.7, assuming in each case the probability of success in removing the disturbances leading to false trip in each barrier is given in table 3.4.

Then, the new probability after improving the barrier will be:

$$Pn= PD*Pr = PD (1-Ps) \quad (3.17)$$

The overall probability of occurrence of disturbance leading to unnecessary trips (false trips) is approximated as the sum of Pni:

$$Po= \sum Pni=0.00989 \quad (3.18)$$

Table 3.4 Probability of success

Disturbance (False trip)	Probability of success Ps	Probability Residual Pr	Poccurence Pni
Power Swing (PS)	0.70	0.30	0.00414
Post Fault (PF)	0.85	0.15	0,00207
Relaying System (RS)	0.90	0.10	0.00092
UP (FACTs)	0.70	0.30	0.00276

The ratio of the obtained result with the initial is given:

$$R= Pno/Pun=0.26875\sim1/4 \quad (3.19)$$

Comparing the results: the Pnu has been reduced by approximately 4 times.

And hence the new security will be evaluated as follows:

$$Sn=1- Pno= 1-0.00989 =0.99011 \quad (3.20)$$

Then, the new Security Sn has been substantially improved with respect to the existing one (Se = 0.9609).

3.7 Conclusion

In this chapter, Root Cause Analysis (RCA) based on fault tree analysis has been used to identify root cause of false trips of distance relay. Once the critical root causes have been identified and their weights quantified, barriers such as blocking functions and DSP Algorithms have been introduced. By applying recent developed techniques to the barriers, a considerable increase in the security and hence reliability has been noticed. One of the main advantages of the RCA is to make possible to perform quantitative analysis on the protection system before and after using improved barriers. Thus, the overall cost of the system may be significantly optimized, since it is possible to selectively reinforce the elements of the protecting system which are most likely apt to failure and hence avoid the use of unnecessary redundancy.

A relaying system has to be reliable. Reliability can be achieved by redundancy i.e. duplicating the relaying system. Obviously redundancy can be a costly proposition. Another way to improve reliability is to ask an existing relay say, protecting an apparatus A to backup protection of apparatus B. Both the approaches are used (simultaneously) in practice. However, it is important to realize that back-up protection must be provided for safe operation of relaying system. Redundancy in protection also depends upon the criticality of the power apparatus.

Chapter 4

Protective Relay Testing System

The reliability of the power grid depends on the successful operation of thousands of protective relays. The failure of one relay to operate as intended may lead the entire power grid to blackout. In fact, major power system failures during transient disturbances may be caused by unnecessary protective relay tripping rather than by the failure of a relay to operate. Adequate relay testing provides a first defense against false trips of the relay and hence improves power grid stability and prevents catastrophic bulk power system failures.

One of the main objectives of this research project is to design and enhance the relay tester using new technology such as FPGA card NI 7851. A new PC based tester framework has been developed using Simulink power system model for generating signals under different conditions (faults or transient disturbances) and Labview for developing the graphical user interface and configuring the FPGA. Besides, the interface system has been developed for outputting and amplifying the signals without distortion. These signals should be like the generated ones by the real power system and large enough for testing the relay's functionality. The signals generated that have been displayed on the scope are satisfactory. Furthermore, the proposed testing system can be used for improving the performance of protective relay

4.1 Introduction

The reliability of the power system depends upon the performance of the thousands of relays that may be used in protective and control system. The failure of a relay to operate as intended may jeopardize the stability of the entire system and its bulk elements. In fact, major system failures during a disturbance are more likely to be caused by unintended relay operation rather than by the failure of a relay to take an action. Reliability has two aspects: dependability and security. Dependability is known as the degree of certainty that a relay system will operate correctly as intended. Security is the degree of certainty that a relay will operate unnecessary during any transient disturbance [42].

Appropriate relay testing provides first guard against relay false-triping. Relay testing can aid to confirm the design of relay, compare the performance of different relays, verify relay settings, classify system conditions that might cause unplanned relay operation, and carry out post-event analysis to understand the causes of unintentional or incorrect relay actions. Relay tester enhancements need to continue because of the use of relays in smart power grids where the conditions that are not the same as in the conventional one. This leads to new relay technologies [43].

Disturbances include transient distortion in the voltage due to post fault, potential transformer saturation or compensator switching may affect on transmission line relays and relaying systems in various ways. The mal-operation of this relay is generally unnecessary tripping during post fault or compensator connection which produces DC offset and harmonics. This may reduce the security of protection system and hence its reliability.

This work focuses mainly on the design and the implementation of the Class D amplifier which is the amplification part of the testing system. The Class D amplifier has been used in this work to amplify the simulated disturbances that are generated by Simulink power system model to be then injected to the protective relay and monitor its response. Labview has been used for developing the graphical user interface and controlling NI 7851Board

In this research work, we have used new technology that allow designing an enhanced relay testing system which in turn can be used for improving the performance of protective relay. In order to test both security and dependability and hence the reliability, this work propose sa new frame work of tester based on FPGA associated with acquisition card NI.

4.2 Testability

Protection System Reliability and Testability require in part that the protection system be designed for high functional reliability and in-service testability commensurate with the safety function to be performed. They also require a design that permits on-line periodic testing of the functioning of the protective system.

The testing of protection schemes faces many problems. Since the main function of protection equipment is taken into consideration under operation during system fault conditions, and it cannot readily be tested under normal conditions [44]. This situation is aggravated by increasing the complexity of protection schemes and use of relays containing software.

Type tests are required to prove that a relay meets the published specification and complies with all relevant standards. Since the principle function of the protection relay is to operate correctly under abnormal power conditions, it is essential that the performance be assessed under such conditions. Comprehensive type tests simulating the operational conditions are therefore conducted at the manufacturer's works during the development and certification of the equipment.

Different testings that can be carried out by the developed testing system are as follows [45]:

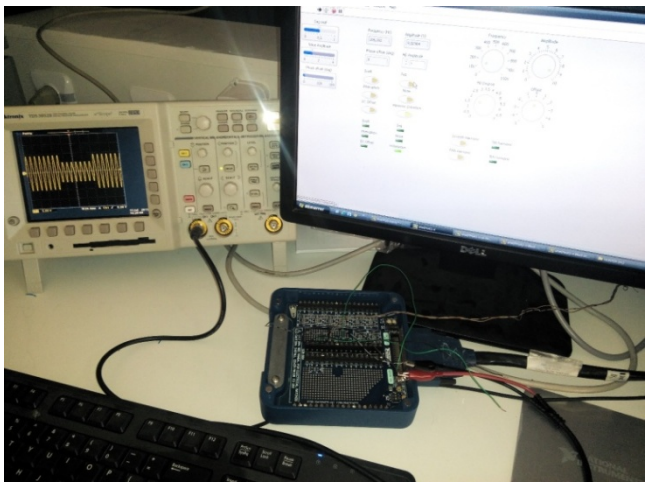


Fig.4.1 FPGA based tester

4.2.1 Steady State test [4]

Usually steady state test is used for the examination of the relay setting by injecting current and voltage at predetermined values for time longer than the setting time of relay. Then, the signal is varied slowly at a rate much smaller than resolution of relay, whichever manually turning a knob or by an automatic system[45]. This type is of less use in commissioning, due to the signal does not represent the real power system signal during faults or abnormal condition.

4.2.2 Dynamic state test

Dynamic state test is inspected by simultaneously applying fundamental frequency components of voltage & current which represent power system states of pre-fault, fault and post fault [45]. Time for relay operation is measured. This type of test can be used in commissioning and troubleshooting.

4.2.3 Transient Test

Transient testing may be investigated by applying simultaneously fundamental and non-fundamental frequency components of voltage and current those represent real power system conditions. This type of test may be used for testing a security of the protective relay.

The signal that may be used in this type for testing may be obtained from digital fault recorders (DFR) real-time Simulator using Simulink/Matlab [46].

The increasing use of digital technology in devices such as protection, measurement, and control apparatus in electric power substations has created the potential for accumulating large numbers of digital recording of power system transient events. In addition to these sources of digital data, real-time system simulators may be used to generate digital data. The users of these data are faced the problem of how to convert it to real-time signal by amplifying it without distortion as the signals outputted from instrument transformers.

4.3 Tester Implementation

FPGA based tester has been implemented using the acquisition card NI as shown in Fig.4.1. It consists of three main parts which are computer, NI 7851 board and amplifier.

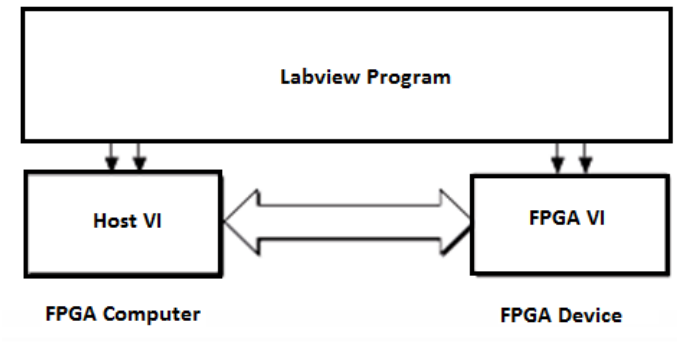


Fig. 4.2 Using a Host VI to Communicate with the FPGA Target

4.3.1 Software Part:

Application development for relays tester has been investigated using SIMULINK and Labview as development tools and driver of NI7851 board [47].

The NI LabVIEW FPGA Module allows the user to graphically implement digital circuits within an FPGA chip using LabVIEW to create VIs and functions that control the I/O, timing, and logic of the device, PCIe 7851, in our case, to generate the desired output [48]. Interactive Front Panel Communication has been used to communicate directly with the FPGA board using an FPGA VI, but the communication is limited in the number of functions and operations that can be performed and lacks real times updating as shown in Fig.2. So a separate HOST VI running simultaneously that references the FPGA VI, has been used to interact with it in real time and provide the user with more control over the inputs of the FPGA, Host Vis are used to send information between the host computer and the FPGA target for the following reasons: - Doing more data processing than you can fit on the FPGA,

- Performing operations not available on the FPGA target,
- Controlling the timing and sequencing of data transfer.

The Host VI takes advantage of a limited number of LabVIEW's inbuilt functions and relies on the FPGA interface functions like Open FPGA VI Reference, Close FPGA VI Reference to establish a connection between the FPGA VI and the Host VI and close it when needed, Read/Write Control to read a value from or write a value to a control or indicator in the FPGAVI.Using the Read/Write block. Figures 3and 4 show the Front Panel and the Block Diagram Host VI.

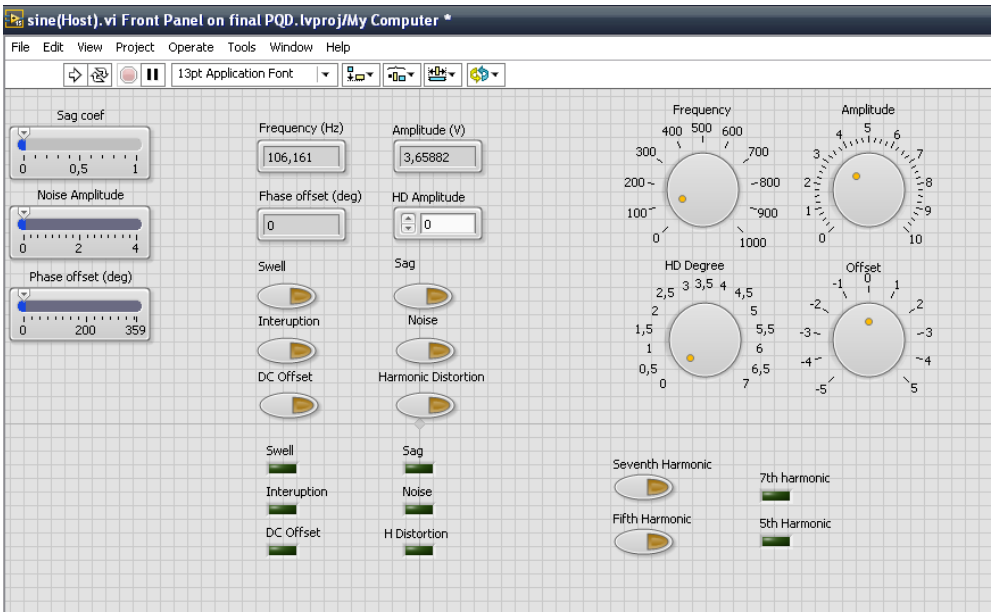


Fig.4.3 Host VI Front Panel of Tester

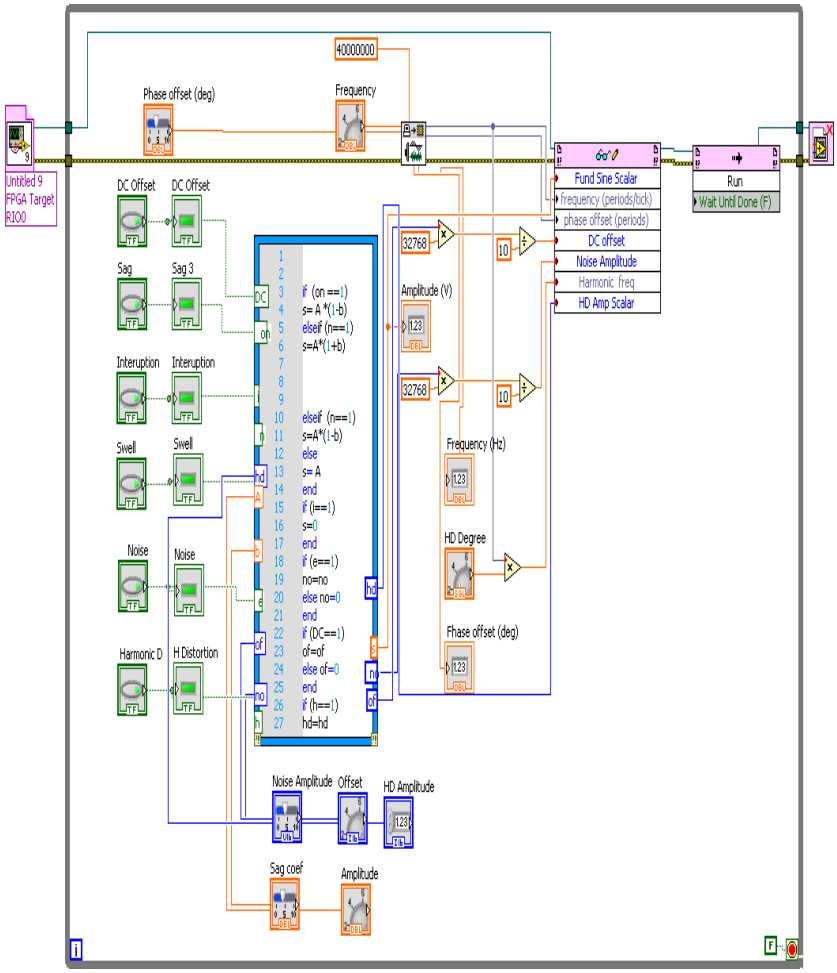


Fig. 4.4 Host VI Block Diagram of tester.

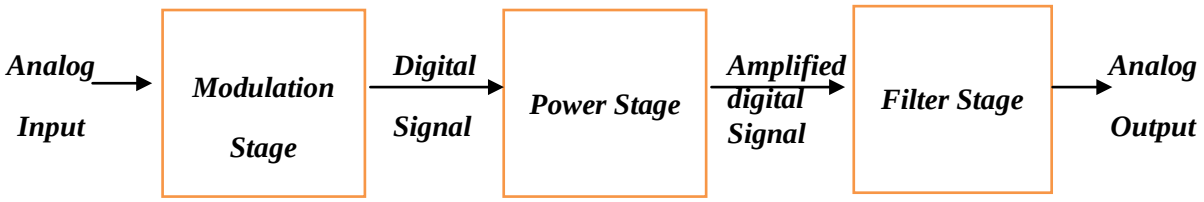


Fig. 4.5 Block diagram of class D amplifier.

4.4 Hardware Part

PC outputs the signals generated by simulator via the card NI7851, where the DAC converts the data to analog form, and then to the relay under test using the amplifier [46].

Figure 5 shows a block diagram of the (class D) amplifier [48]. First the signal that will be injected to the amplifier is sampled by an analogue-to-digital converter up sampled version of the 24-bit digital input signal in the considered Bandwidth (0-5Khz). The produced signal is as input to a digital filter which drives a digital PWM. The power circuit, which can be a half-bridge converter, is followed by a low pass filter to recover the original analog signal [49].

Amplifier development

The final circuit design of this class D amplifier is shown in Figure 4.6. The first stage of this class D amplifier is the control circuit where the PWM signal generator is fed to the two gate drives that have as main role to create dead-time for avoiding shoot-through current that can damage the output stage. Then, the power stage which consists of H-Bridge and low pass filter is the final stage. The implementation of the circuit is shown in figure 4.6.

This circuit first was implemented on proto board in order test it. After that it will be implemented on the PCB. The control circuit should be well isolated using opto-couplers from the power circuit.

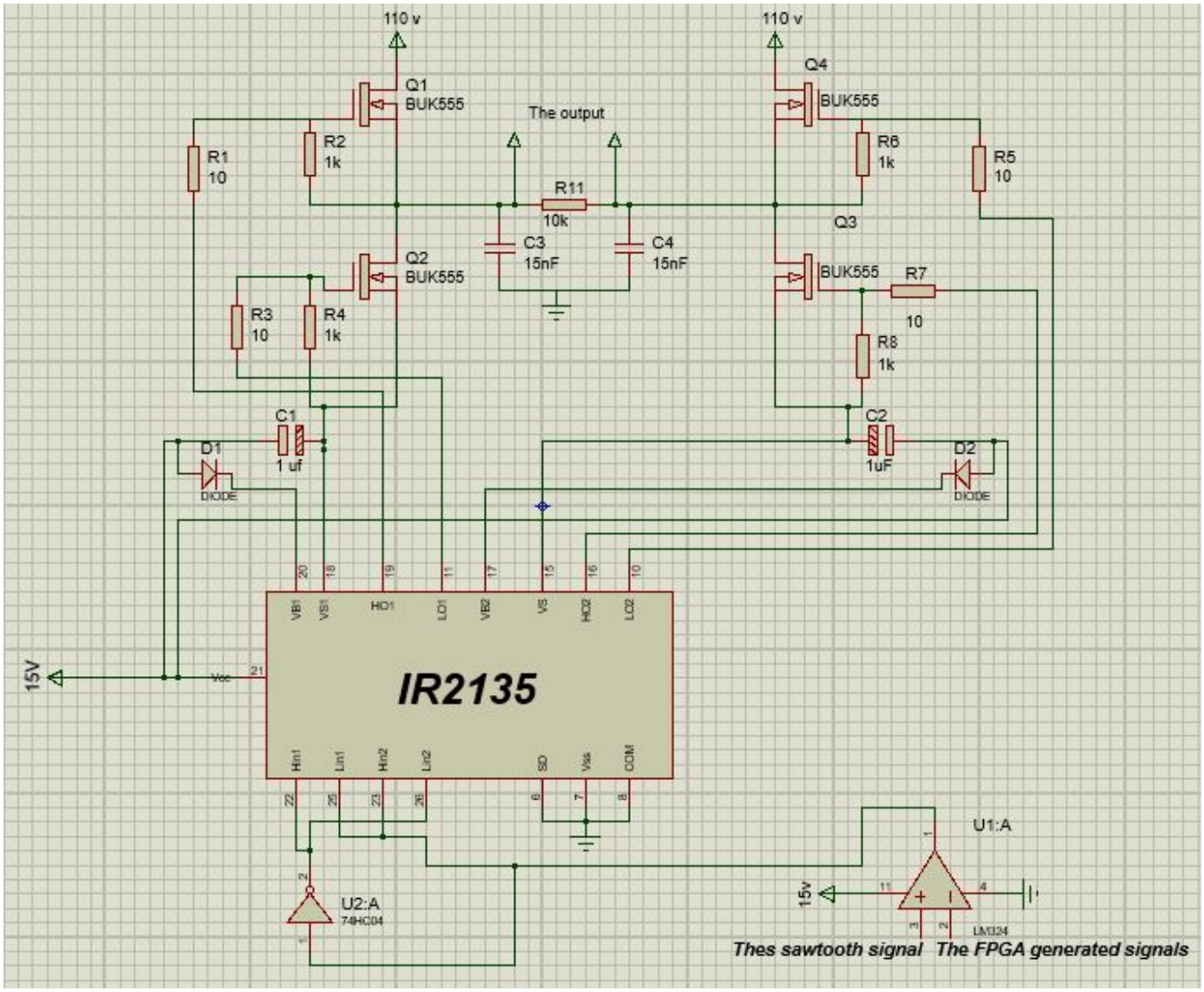


Fig.4.6 Class D Amplifier circuit

4.5. Performance Evaluation of the Tester

The signal of the PWM is supplied to H-bridge.The output PWM signal of the H-bridge before the using the low passive filter is shown in Fig. 4.8 where the H-bridge is fed with 12V.

The output signal of the H-Bridge fed with 18.73V and a load of 100Ω is shown in figures 3.9 and 4.10, the input signal is a sine wave of 10V peek to peek and frequency of 50Hz.

This signal has been taken and injected to the Class D amplifier but the voltage of the H-bridge has been changed to 38.8V and the probes were changed to X10 to decrease the scale of the oscilloscope so that each division is 20V. The amplified output signal is 110V peak to peak and a frequency of 50 Hz the efficiency is approximately 100%. However, in Fig.4.11 some distortions are appearing in the output amplified signal, these distortions are not due to the class D amplifier, they are part of the disturbance input signal.

The theoretical efficiency of a Class D amplifier is 100% but this is unachievable in practice. However, this efficiency can approach significantly this value by making a good design to minimize switching losses that lead to high power loss.

The formula to calculate the efficiency is:

$$\eta = \frac{P_{OUT}}{P_{in}} * 100 \qquad (4.1)$$

The efficiency and the gain are calculated with respect to a sine wave input of 10V and the voltage of the source that feed the H-bridge has efficiency is $\eta = 92.4\%$.

The total harmonic distortion (THD) is very important parameter to evaluate the performance of the Class D amplifier to have a clean signal, we don't have the proper means to do the calculation to have the exact value but it appears that the THD is less than 1%.

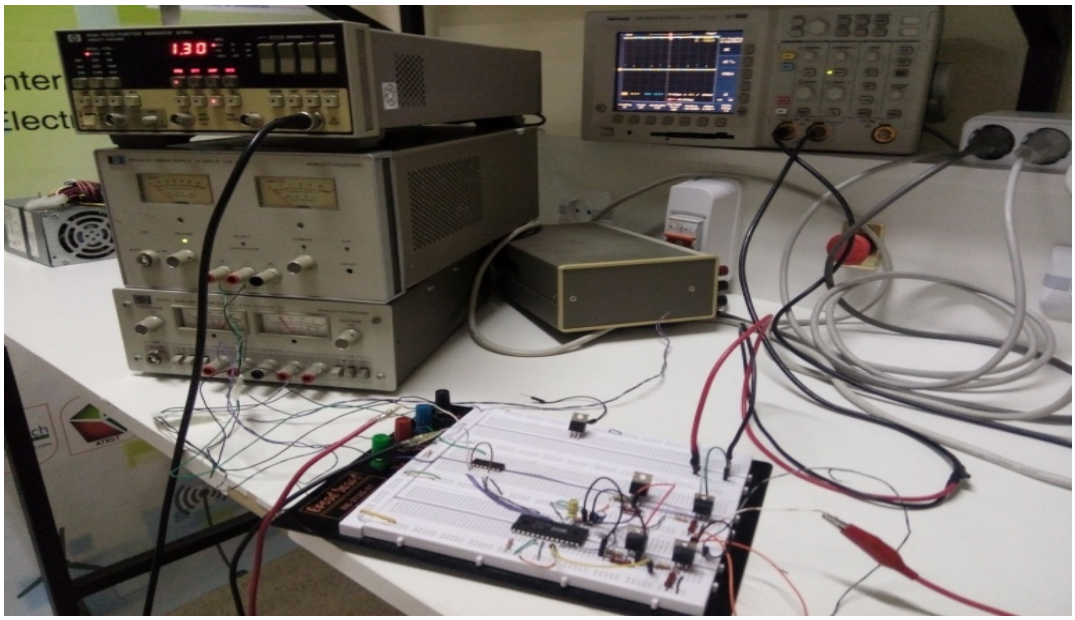


Fig.4.7 Class D amplifier circuit

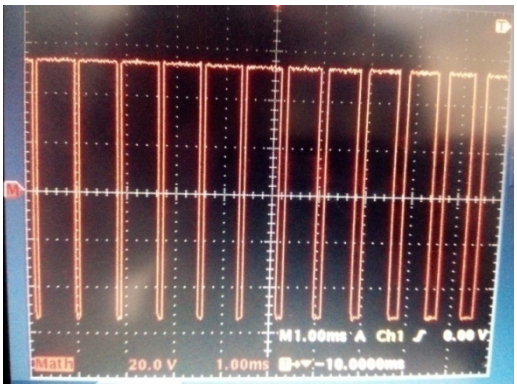


Fig.4.8 H-bridge output PWM signal

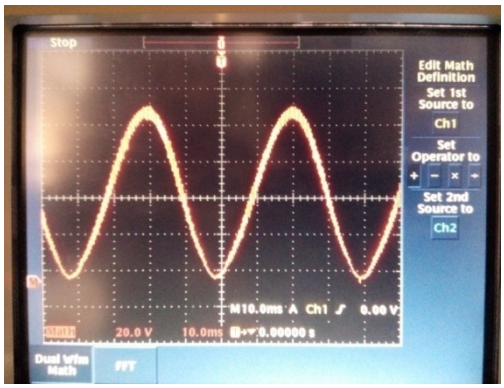


Fig.4.9 Output signal of class D amplifier

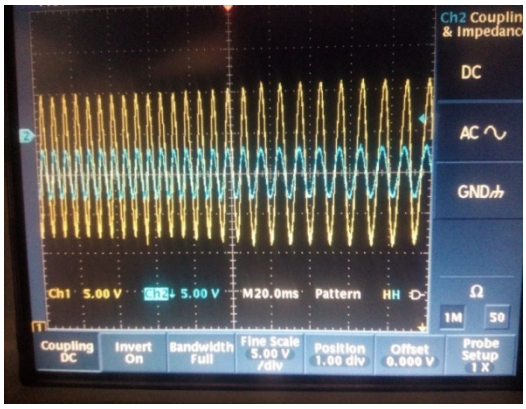


Fig.4.10 Amplified sine wave using Class D amplifier

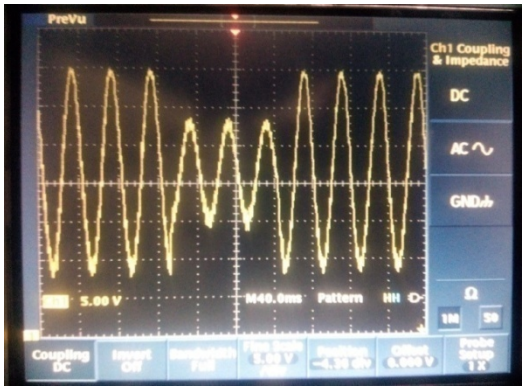


Fig.4.11 Voltage sag generated from Disturbances generator

4.6 Conclusion

The FPGA based tester has been successfully designed and implemented. Our emulating circuit can be used to generate the three phase voltages and currents to represent the actual power grid events mainly the fault and other abnormal conditions to check the relay settings. In fact, a PC has been used to generate these events signals and inject them to the relay under test via the NI7851 cquisition card.

User Interface (GUI) has been developed to include some parameters of the relay, to control the generated data of waveform signals and to display the generated signals.

The Class D amplifier has been selected in this circuit to amplify the simulated disturbances signals. Design and implementation of the Class D amplifier which is the amplification part of the testing system have been investigated in this work.

The test results and performance of this tester are very satisfying. This is clearly proven by its high efficiency and very low THD. The Class D amplifier that has been used can amplify any disturbance signal with the same performance results even if the frequency of these disturbances is changing. This ability is possible because the cut-off frequency of its filter can attain 1.1 kHz.

Chapter 5

PMU Placement Optimization

The placement of phasor measurement units (PMUs) in electric transmission systems has also gained much attention for enhancing the control as well as the protection scheme. In this research work, a binary teaching learning based optimization (BTLBO) algorithm for the optimal placement of phasor measurement units (PMUs) is proposed. The optimal PMU placement problem is formulated to minimize the number of PMUs installation subject to full network observability of the power system buses under fault conditions. The effectiveness of the proposed method is verified by the simulation of IEEE 14-bus benchmark system.

5.1. Introduction

In order to make the electrical power systems more reliable, stable, and controllable; state estimation of the transmission network is necessary [50-56]. The Phasor Measurement Unit (PMU) is a tool for measuring the voltage and current which are synchronized by using the global positioning system (GPS) satellite. Integrated with the GPS receiver [50], the power station including the Phasor Data Concentrator (PDC), which is used for analyzing the PMU data, can receive the synchronous data from each PMU in real time [57].

State estimation of power network may allow the scheduling generation and interchange; monitoring outages and scheduling alternatives; supervising scheduled outages; scheduling frequency and time corrections; coordinating bias settings; and emergency restoration of system [58]. This can be achieved either by state estimation algorithms [59] or by means of PMUs with extreme precision, time synchronization, and excellent performance. Measuring state estimation is achieved through complex bus voltages [60] that enable the estimation of the neighborhood bus voltage magnitudes and angles by using the line flow measurement (both real and reactive power). The static and dynamic behaviors of the power grid may be obtained from the information gathered by PMUs.

Faults that occur in the transmission line may be either permanent or temporary [61, 62]. Permanent fault may lead to a broken transmission line or a power generator malfunction; this causes different signals during the pre-fault and post-fault. This can be easily detected and located. However, the temporary fault may cause insulator flashover, which may lead to full insulator breakdown if it occurs frequently. This emphasizes the importance of PMU-based fault location technique [63-65].

Nowadays, Wide Area Monitoring System (WAMS) that is considered the most advanced system to detect disturbances and avoid a bulk blackout is based on the PMUs . It aims to maintain the dynamic stability in the whole power network [65]. This is implemented by synchronizing and recording the acquired data from systems in distributed locations through new computing and communication technologies. Upon their delivery to the central control station, these data are measured and analyzed from any point of the power network. In addition to its ability to monitor the static stability of the network (as traditional SCADA), WAMS enables the controllers to recognize unusual activities within the power network such as instability in the network voltage, to analyze the network oscillation, and to detect fault localization. Thus, using the data provided by PMUs installed in some appropriate buses of a power grid, one can construct a new type of measuring system to improve the observability and the precision of the power system state estimator. The observability depends on the type, the number and the geographic distribution of measurements [66]. Several methods [67-73] were considered when formulating the optimal placement of monitoring devices for fault location.

In this research work, a binary teaching learning based optimization (BTLBO) algorithm [74-78] for the optimal placement of phasor measurement units (PMUs) is proposed. The optimal PMU placement problem is formulated to minimize the number of PMUs installation subject to full network observability at the power system buses during the fault. The effectiveness of the proposed method is verified by the simulation of IEEE14-bus.

5.2. Fault Analysis Using PMU

PMU-based fault location technique is achieved through monitoring the synchronized fault voltages, calculating the line currents between these buses, and forming bus injection currents at two terminals of the faulted line. Thus, calculation of fault locations can be indirectly investigated.

A PMU placed at a given bus of the network can measure both the phasor voltages and phasor currents of all lines incident to that bus. Thus, the entire parameters of a bus can be made observable by placing judiciously PMUs at specific buses of the network. As shown in Fig.5.1, most power transmission networks may consist in general of five different sub-network configurations or types [79]. In this figure, for each of the five sub-networks, the placed PMUs obey to what is called the “one bus spaced deployment strategy”.

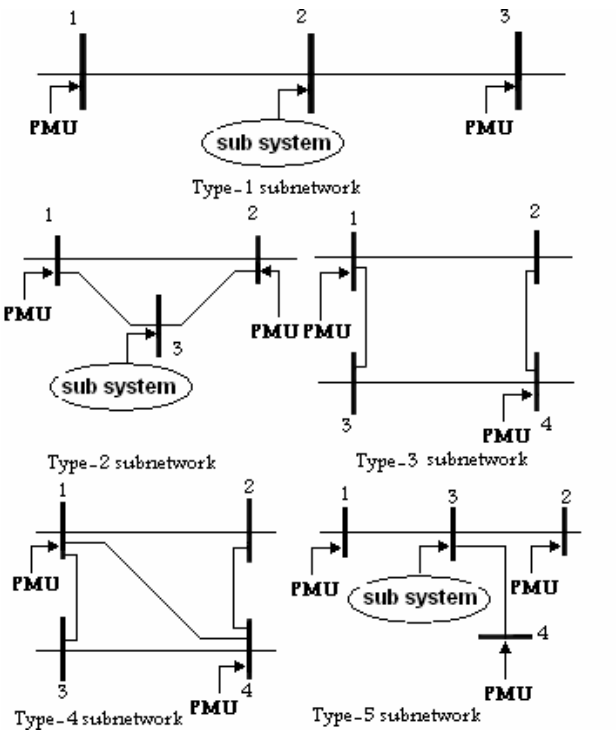


Fig.5.1 The five possible sub-network configurations

Whatever is the considered sub-network type, it is always possible to make the fault location problem of that sub-network similar to the fault location problem of type-1 sub-network [80]. A faulty type-1 sub-network is shown on Fig.5.2. In this figure, a fault occurs in line jk between bus j and bus k. The fault location problem consists thus, of finding the parameter D_k.

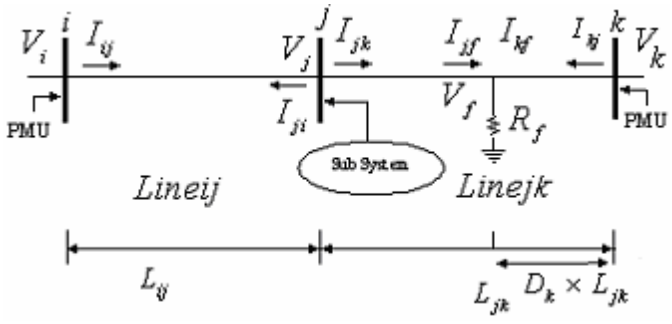


Fig.5.2. Faulty type-1 sub-network

By using the voltage phasor of bus i and the parameters of line ij, the voltage phasor of bus j will be determined as:

$$V_j = V_i - (I_{ij} - V_i - L_{ij}\ Y_{ij}/2)\ L_{ij}\ Z_{ij} \tag{5.1}$$

In addition,

$$I_f = I_{kf} + I_{jf} \tag{5.2}$$

Where the line parameters Z_{ij} and Y_{ij} are relative to the Π line model. Current phasor I_{jk} however, cannot be deduced with the similar way as no PMU is connected at bus j. Therefore, the problem consists of finding two unknown variables I_{jk} and D_k. Using the basic electrical networks theory and assumption constraints, the two sets of equations of the two unknown variables can be derived:

- Network equations, derived from equations (5.1) and (5.2)

  $F_1(I_{jk}, D_k, \theta) = 0$

- Constraints equations, assuming pure resistance fault impedance or $Arg(I_f) = Arg\ (V_f)$

  $F_2(I_{jk}, D_k, \theta) = 0$

Where θ represents the known variables, such as V_i, V_j, V_k, etc.

In Table 5.1 the two groups of equations for fault location detection of three phase faults are summarized.

Table 5.1: Summary of the two groups of equations for fault location detection

Group 1: Network equation (n=0,1,2,)	
$V_{fn} = V_{kn} - (I_{kjn} - V_{kn} \times Y_{kfn} / 2) \times Z_{nfn}$ $I_{jkn} = (V_{jn} - V_{fn}) / Z_{jfn} + V_{jn} \times Y_{jfn} / 2$ $I_{fn} = (V_{kn} - V_{fn}) / Z_{kfn} - V_{fn} \times Y_{kfn} / 2 +$ $(V_{jn} - V_{fn}) / Z_{jfn} - V_{fn} \times Y_{jfn} / 2$	
Group 2: Constraint equation	
a-g fault	$Re(I_{f0} + I_{f1} + I_{f2}) \times Im(V_{f0} + V_{f1} + V_{f2}) =$ $Im(I_{f0} + I_{f1} + I_{f2}) \times Re(V_{f0} + V_{f1} + V_{f2})$
b-c-s fault	$Re(I_{f1} - I_{f2}) \times Im(V_{f1} - V_{f2}) =$ $Im(I_{f1} - I_{f2}) \times Re(V_{f1} - V_{f2})$
b-c-g fault	$V_{f1} = V_{f2}$
a-b-c-g fault	$Re(I_{f1}) \times Im(V_{f1}) = Im(I_{f1}) \times Re(V_{f1})$

Solving numerically these sets of equations leads to the unknown parameter D_k, that is the location of the fault on the line between bus j and bus k.

It is not economical to install a PMU at each bus of a wide-area power network. Thus, the problem of optimal PMU placement (OPP) concerns with where and how many PMUs should be implemented in a power system to achieve full observability at minimum number of PMUs [81-88].

For an n-bus system, the PMU placement problem can be formulated as follows:

$$\begin{aligned} &\textit{Objective function: } J = Min \sum_{i=1}^{n} x_i \\ &\text{such that: } f(X) \geq \hat{i} \end{aligned} \tag{5.3}$$

Where X is a binary decision variable vector, whose entries are defined as:

$$x_i = \begin{cases} 1 & if\ Bus\ i\ has\ a\ PMU \\ 0 & otherwise \end{cases} \tag{5.4}$$

f (X) is a vector function, whose entries are non-zero if the corresponding bus voltage is solvable using the given measurement set and zero otherwise.

î is a vector whose entries are all equal to two or more.

Constraints

In order to form the constraint set, the binary connectivity matrix A, whose entries are defined as below, will be formed first.

$$A_{k,m} = \begin{cases} 1 & if \quad k = m \\ 1 & if \quad k \text{ and } m \text{ are connected} \\ 0 & if \quad otherwise \end{cases} \tag{5.5}$$

Based on the acknowledgement that by placing a PMU on one bus, the voltage phasors of this bus and its neighboring buses can be calculated, we can get

$$\mathbf{f} = \mathbf{A} \times \mathbf{X} \tag{5.6}$$

Constraint functions defined by equations ensure full network fault observability while minimizing the total number of the PMUs.

The procedure for building the constraint equations (vector function f (X)) will be presented for four possible cases:

- No PMU measurements or conventional (flow and injection) measurements exist,
- Only flow measurements exist,
- Both flow and injection measurements (they may be zero injections or measured injections) exist or PMU measurements and conventional flow or injection measurements exist.

To verify the effectiveness of the proposed method, IEEE 14-bus system is taken as test system shown in Fig.5.3.

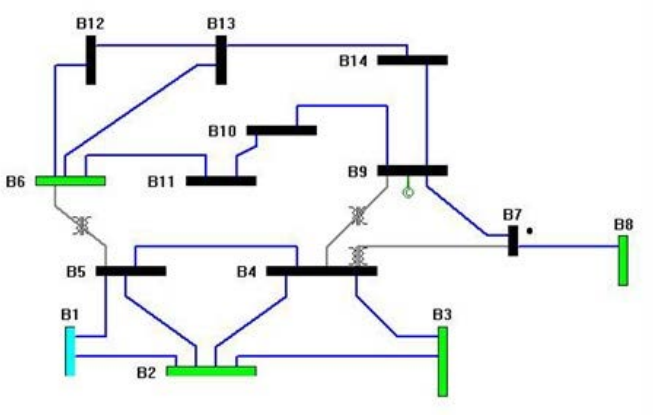


Fig. 5.3. IEEE 14-bus system

5.3. BTLBO Optimization Algorithm

A binary version of TLBO that is a new method has been proposed [89]. The algorithm in binary can be explained as follows:

Step 0: define the optimization problem, the objective function:

Minimize (objective function) $y=f(x_1,x_2,\ldots,x_{n-1},x_n)$ such that: $x_1,x_2,\ldots,x_{n-1},x_n$ can take only two values: either a "1" or a "0".

Decide how many students will be used or the population size, elite size and the number of generation. We consider a minimization problem; the maximization is similar.

Step 1: initialization: suggest a population (that will be developed to reach the final solution) or students randomly according to the following equation:

$$x_{(i,j)}^{1} = randi([0,1],1) \tag{5.7}$$

i: refer to student number, so there are i^{th} student, i=1, 2, …,P

j:refer to the course number, $x_{(i,j)}$ is the level of the i^{th} student at the j^{th} course, j=1, 2,…,D

The small number 1 refers to the generation number that is the first generation.

After manipulating the above equation $P \times D$ times we obtain a $P \times D$ matrix which represents our population:

$$population^1 = \begin{bmatrix} x^1_{(1,1)} & \cdots & x^1_{(1,D)} \\ x^1_{(2,1)} & \ddots & x^1_{(2,D)} \\ \vdots & \ddots & \vdots \\ x^1_{(P,1)} & \cdots\theta & x^1_{(P,D)} \end{bmatrix} \tag{5.8}$$

Choose the teacher: the best student is the one which has the minimum fitness function.

Step 2: teacher phase

As in real version each student tries to be like his teacher, so he makes his design variables as those of the teacher, of course not all of them otherwise he will be exactly as his teacher, so the student copies some components of teacher and replace his components by those copied ones. The number of copied components depends on the ability of teacher and the student; that is represented by one random number h that is between 0 and D. The corresponding formula is:

$$h = randi(D,1) \tag{5.9}$$

This number determines how many courses that student i will learn from his teacher.

The location of those courses in the teacher vector can be specified according to the equation below:

$$Course = randi(h,[1,h]) \tag{5.10}$$

These randomly selected courses are now ready to be transmitted from teacher to student:

$$\begin{aligned} &X_{i,new} = X_i \\ &X_{i,new}(course) = X_{teacher}(course) \\ &if\ f(X_{i,new}) < f(X_i) \text{ then } X_i = X_{i,new} \text{ else do nothing} \end{aligned} \tag{5.11}$$

Executing may produce duplicate solutions; therefore an additional step is needed.

Step 3: remove duplicate solutions by mutation on randomly selected dimensions.

Step 4: learner phase

The interaction between students in binary interpretation will be as follows:

choose for a student i another one j, if j is better than i then i will learn from j by trying to change components that are different from those of j, in order to be like him; otherwise he will change some components that are similar to those of j. This can be done as follows:

For i = 1: P do

Choose another student j and record where they are similar and where they are different in a vector ,

$$q = [q_1\ q_2\ \ldots\ldots\ldots q_D] \text{such that } q_k = 1 \text{ if } x_{i,k}^g = x_{j,k}^g \text{else } q_k = 0; \quad k = 1, \ldots, D$$

The vector $h = \text{randi}(D, 1)$ specifies how many courses will student i learn from j if he is better than him or change them in other case.

The vector $\text{course} = \text{randi}(h, [1, h])$ specifies the location of courses which will be learnt or changed.

Now the learning process can be implemented:

$X_{i,new} = X_i$ The new student is the old with some modifications.

$$\begin{aligned} &if\ f(X_i^g) < f(X_j^g) \text{ then } X_{i,new}(course) = X_j(course) \times not(q(course)) \\ &else\ if\ f(X_i^g) \geq f(X_j^g) \text{ then } X_{i,new}(course) = not(X_j(course)) \times q(course) \end{aligned} \tag{5.12}$$

Equation (5.12) indicates that some components where i and j differ will be copied from j (the highest learned one between the two) to i otherwise (j is worse than i) some of similar component in i will be changed from 0 to 1 or 1 to 0. Now, check if the new student is better than the old:

$$if\ f(X_{i,new}) < f(X_i) \text{ then } X_i = X_{i,new} \text{ else do nothing} \tag{5.13}$$

After completing the process for all the population, a new teacher will be determined.

Step 5:-Remove duplicate solutions.

-replace bad solutions by elite solutions and again remove duplicate solutions.

Step 6: if $g \neq$ number of generation go to step2 else stop.

Using the binary teaching learning based optimization explained previously which is based on the problem formulation pointed out in previous sections; an algorithm for the optimal placement problem is shown below:

1. Build the binary connectivity matrix using the one line diagram and constraint modification when injection, flow measurements or already installed PMUs.
2. Define the optimization parameters; the population size (pop_size), the design variables (N_buses), and the number of generation (N_gen), the (elite size).
3. Generate random solutions within boundaries of the system.
4. Check that random solutions satisfy the inequality constraint of buses $f(x)=(A*X) \geq$ î

5. Modify those not satisfying the constraints.
6. Calculate the fitness of each solution based on the objective function of expression.
7. Set the best solution as teacher of the population.
8. For each student apply teacher phase, replace x by x_{new} if it gives better fitness function (less) otherwise keep the old one.
9. If the duplicate solutions exist then it is necessary to modify the duplicate solutions in order to avoid trapping in the local optima. In the present work, duplicate solutions are modified by mutation on randomly selected dimensions of the duplicate solutions before executing the next generation without losing the observability.
10. For each student apply learner phase, replace x by x_{new} if it gives better fitness function (less) otherwise keep the old one.
11. Again, remove duplicate solutions keeping the constrained satisfied (observability).
12. Replace (elite_size) bad solutions by (elite_size) elite solutions.
13. Again, remove duplicate solutions keeping the constrained satisfied (observability), then determine the teacher.
14. Repeat from step 7 for maximum number of iterations.
15. Set the best solution $x_{teacher}$ as the final solutions.

The flowchart for the optimal placement algorithm is shown in Figs.5.4 and 5.5.

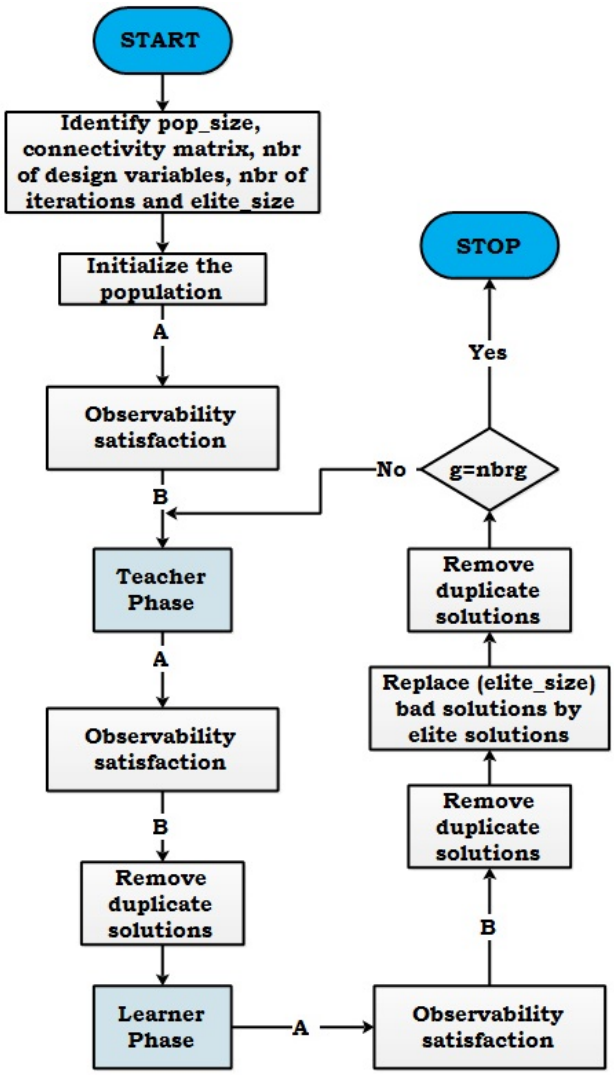


Fig. 5.4 Flow chart of BTLBO algorithm applied to the optimal PMU placement

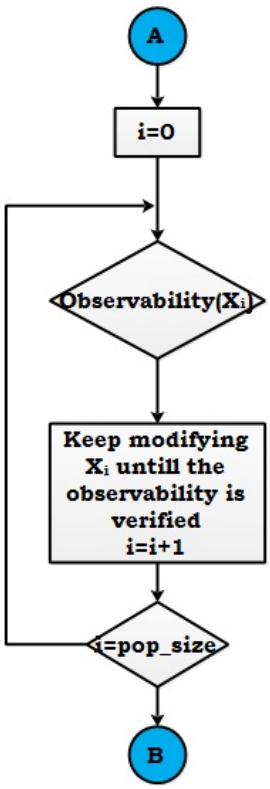


Fig. 5.5 Observability subroutine

5.4. Simulation Results and Discussion

The PMU placement optimization algorithm presented in the preceding sections was implemented in MATLAB® on the IEEE 14-bus system. Network data for this system is in public domain as given in Table 5.2. The parameters used in the optimization are: The maximum iteration number in BTLBO is selected to be 1000 with the population size of 100. In the simulations presented in this research work, the best solution of the binary TLBO is concluded after 20 runs of the algorithm. The simulations are carried out on an Intel i5 (2.40 GHz) with 4 GB RAM. It should be mentioned that the corresponding configuration of the required number of PMUs is not necessarily unique. Since heuristic algorithms, such as TLBO, are based on a random search in the search space of the problem, and the result of

each execution of these algorithms might be different from another one. Therefore, they must be run several times to ensure that the optimal point of the problem is found. However, from the observability point of view, there is no difference between different configurations with the same number of PMUs, so only one configuration is presented.

Two sets of simulations are carried out on the IEEE 14- bus system, which are initially assumed to have no flow measurements and no previously existed PMUs. In the first set of simulations, zero injection is simply ignored while in the second set, it is used as existing measurement.

The IEEE 14 bus test system has got only one zero-injection bus. The output of the BTLBO algorithm is 8 PMUs. The information of the system and zero injections are given in the Table.5.2.

The global solution is obtained with only a small number of iterations (between 5 and 10) and population size (10). Seven PMUs can be deployed to observe the IEEE14 bus system. Here, when ignoring injection, different configuration of PMUs is obtained, whereas, considering injection give only one set (1, 2, 4, 6, 9, 10 and 13). It is observed that the number of PMUs required for system observability reduces by 1, if the system observability is to be maintained after considering zero injections buses.

Table 5.2 System information of IEEE 14-bus system

System	Num. of branches	Num. of zero injections	Zero injection buses
IEEE 14-bus	20	1	7

The number of PMUs calculated by the proposed approach is given in Table 5.3. The number of PMUs that guarantees 100% of observability of power system during any failure that can occur by guaranteeing that each bus is observable by at least two PMUs.

Table 5.3 Optimum number and location of PMU

System	Num. of PMUs	Location of PMUs
IEEE 14-bus with Zero injection buses	7	1,2,4,6,9,10,13
IEEE 14-bus with injection buses	8	1,2,4,6,9,10,13, 14

The obtained results using our approach is in good agreements with those published in literature using other techniques of optimization [90] as shown in Table 5.4.

Table 5.4 Optimal PMUs number using various optimization techniques for the IEEE 14-bus test system.

Optimization Technique	Optimal PMU number
BTLBO algorithm	**7**
Fuzzy based procedure	7
CPLEX	8
Single shot N-1 security	8
Multistage procedure	7
BILP	9
BPSO	7
BICA	7
Integer programming based procedure	7
Binary search algorithm	7
Modified GA	7

5.5 CONCLUSION

The obtained simulation results are in agreement with the previous research work results [81-86, 90]. Moreover, the results show that full network observability can be met under fault conditions using more than 50% PMUs installation; however, under normal conditions, approximately 30% PMUs installation is required.

Finally, the proposed work represents a potential tool to monitor power systems, and will give valuable help the operators in a smart grid environment.

Chapter 6

Conclusions

In this research project, we have presented a new approach allowing the reliability improvement of distance protective relay that can be used for a modern smart power system which has a great amount of harmonic components using optimized digital filters. Besides, we have reviewed the developments .of different techniques of the phasor measurement unit PMU as a new technology in advanced power system protection applications. It is clearly noticed that PMU plays a very important role for improving the reliability of the power system protection.

The placement of phasor measurement units (PMUs) in electric transmission systems has also gained much attention for enhancing the protection scheme. In this research work, a binary teaching learning based optimization (BTLBO) algorithm for the optimal placement of phasor measurement units (PMUs) has been proposed. The optimal PMU placement problem has been formulated to minimize the number of PMUs installation subject to full network observability at the power system buses. The effectiveness of the proposed method has been verified by the simulation of IEEE14-bus.

In Chapter 2, The study of disturbance effects on the measurement quality has been investigated during the faults in 400kV overhead long transmission line with series TCSC compensator. A power system simulator based on MATLAB/Simulink associated with PSB has been used to generate voltage and current signals for different locations and inception angles of faults. Also the DFT algorithm has been utilized to compute the phasors of voltage

and current phases. The considerable error has been incurred for the faulted current and voltage phasors due to the DC decaying, harmonics and sub-harmonics components. The insertion of the filter is necessary before the DFT algorithm for suppressing the harmonics and DC offset decaying components but it is always associated with time delay.

In chapter 3, Root Cause Analysis (RCA) based on fault tree analysis has been used to identify root cause of false trips of distance relay. Once the critical root causes have been identified and their weights quantified, barriers such as blocking functions and DSP Algorithms have been introduced. By applying recent developed techniques to the barriers, a considerable increase in the security and hence reliability has been noticed. One of the main advantages of the RCA is to make possible to perform quantitative analysis on the protection system before and after using improved barriers. Thus, the overall cost of the system may be significantly optimized, since it is possible to selectively reinforce the elements of the protecting system which are most likely apt to failure and hence avoid the use of unnecessary redundancy.

In chapter 4, The FPGA based tester has beensuccessfully designed and implemented.Simulator is used to generate three phase voltages andcurrents presented the actual power grid eventsmainly the fault and other abnormal conditions to check the relay settings. In fact, a PC has been used to generate these events signals and inject them to the relay under test via the acquisition card NI7851.

User Interface (GUI) has been developed to include some parameters of the relay, to control the generated data of waveform signals and to display the generated signals.

The Class D amplifier has been selected in this circuit to amplify the simulated disturbances signals. Design and implementation of the Class D amplifier which is the amplification part of the testing system have been investigated in this work.

The test results and performance of this tester are very satisfying. This is clearly proven by its high efficiency and very low THD. The Class D amplifier that has been used can amplify any disturbance signal with the same performance results even if the frequency of these disturbances is changing. This ability is possible because the cut-off frequency of its filter can attain 1.1 kHz.

Chapter 5 has presented a binary teaching learning based optimization method is developed for determining optimal locations for PMUs; various scenarios are considered where the system is first assumed to be observed by PMUs only. Next, the placement problem is considered for a system with existing measurements, some of which may be PMUs.

The work reported in this thesis shows that the objectives have been fulfilled successfully. Specifically, the project has made the following contributions:

- An exhausting review which resumes the main highlights in distance protective relay's developments and trends.

- An enhanced algorithm based on the theory of digital filter and analysis to remove all harmonics created during the switching of the power circuit breaker. The simulation results of the proposed approach gave very satisfactory results in term of performance as well as in term of reliability (security).

- A new approach allowing the reliability improvement of distance protective relay when it is used for a modern smart power system which has a great amount harmonic and sub-harmonic components has been verified using the reliability analysis.
- A PC-based power system simulator prototype has been developed in this work, where we have implemented the algorithm using the Simulink/Matlab and interfaced with the real world via a data acquisition card. This card is used to allow generate real time signals, which will be injected in the distance relay under test.

After testing, it can be noticed that the obtained results verify the enhancement of numerical distance relay and its characteristics using optimized digital filters.

The above discussion implicitly assumes that all PMUs are free of defects and their failure is not considered as a possibility. In practice, this assumption may not always hold true due to unexpected failures in these devices or gross errors introduced by the noise in the communication system. Therefore, it might be prudent as future challenge to consider the case of PMUs failure as a possible contingency in the formulation and solution of the PMU placement problem.

Moreover as future scope, it is intended to implement the procedure of PMU placement on a real world grid. The power system has to be first modeled such as to cast the IEEE bus systems. Next, a topological analysis is done in a similar manner as the work presented in this chapter. Further, the optimization algorithm will be dealt with to enhance its convergence and speed of execution. This is done by hybridizing it with classical local minimizers.

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