Deep analysis of the Geometric Component in Charge Pumping of Polysilicon Thin-Film Transistors

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Abstract- In this article, we model the geometric component in charge pumping technique (*CP*) of polysilicon thin film transistors (poly-Si TFT). This model is based on both remaining carrier types when the device transit from accumulation to inversion and vice versa. Therefore, it depends on gate length (*L*) and width (*W*) as well as on gate signal rise (t_f) and fall (t_f) time. The proposed model shows a good agreement with the experimental data. We have shown that the geometric component due to the remaining carriers, when poly-Si TFT transits from inversion to accumulation, is very small compared to that due to the transition from accumulation to inversion. Consequently, a new analytic CP model, depending on gate width, is developed for n-channel poly-Si TFT.

***Index Terms*—Charge pumping (CP), geometric current (I_{Geo}), polycrystalline Silicon thin-film transistors (poly-Si TFTs).**

I. Introduction

The geometric component (I_{Geo}) in charge pumping (CP) technique is well known as the parasitic and undesirable effect causing the overestimation of interface trap density [1-3]. In conventional metal- oxide -silicon field effect transistors (MOSFETs), this component arises from recombination of remaining inversion-layer carriers, which not have enough time to flow back to the source and drain regions, with the substrate majority carriers, when the device is witched from inversion to accumulation. Therefore, in conventional MOSFETs I_{Geo} is inversion-layer carriers- transport limited and depends on the gate length and the gate signal time (t_f) in N-MOSFET (gate signal rise time, t_r, in P-MOSFET). These issues have been modeled in our previous work [4].

The poly-silicon thin film transistors (poly-Si TFT) have recently attracted research interest, due to their application in integrated active matrix display [5-6]. Some authors investigated I_{Geo} in CP technique of poly-Si TFT [7-8]. They reported that I_{Geo} is somewhat different from that of the conventional MOSFET. For an n-channel poly-Si TFT, during t_r of the CP gate signal, the device is switched from the accumulation regime to the inversion regime, the accumulated holes and the trap emitted holes return from the channel to the side contact laterally through the active area along the channel *width* (*W*) direction. If t_r is sufficiently short, some holes have not enough time to flow back to the substrate side contact, they will subsequently recombine with electrons coming from the Source/Drain when the channel is switched to the inversion, resulting in the geometric component. Hence, contrary to the conventional MOSFET, I_{Geo} in n-channel poly-Si TFTs depends on *W* and t_r, and is hole-transport (substrate carrier) limited [8]. However, in those above-sited works the effect of the gate length *L* on I_{Geo} is not investigated and is unclear. In addition, recently, Wang et *al* [8] proposed an interesting method to extract and separate I_{Geo} in CP measurement of n-channel poly-Si TFTs. However, this method is based on the empirical equation with undefined fit parameters (without physical meaning). In this work, using the semiconductors theory the I_{Geo} in CP of poly-Si TFTs is modeled in two dimensions (by taking into account both inversion-layer and substrate carriers transport). Consequently,

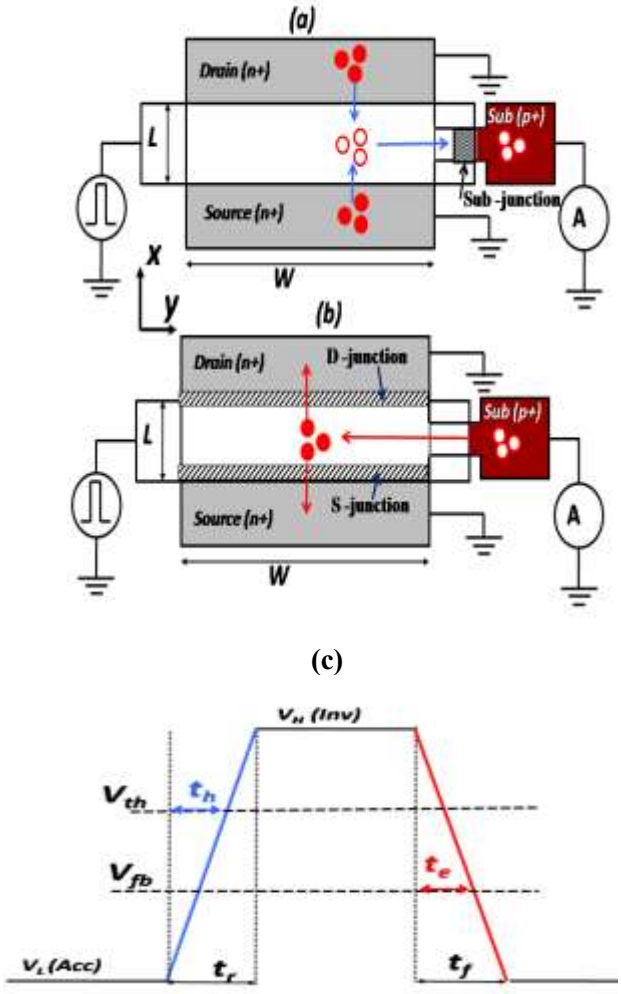

Fig.1 Illustrative schematic of the contribution mechanisms to the geometric component at different time of gate signal in n channel poly-Si TFT. (a) Recombination of remaining accumulation holes with the electrons inversion layer during the rise time of the gate signal (t_r), (b) remaining electrons of the inversion layer which recombine with the incoming substrate holes during the gate signal fall time (this geometric component is similar to that occuring in conventional MOSFETs), (c) definition of CP gate signal parameters.

a new analytic physical-based CP model is established for poly-Si TFTs.

II. Geometric Component in Poly- Si TFT

The geometric component model, developed in this paper is based on both amount of remaining inversion-layer carriers (electrons in the case of n-channel poly- Si TFT) transferred to the poly-Si TFT substrate after the switching off and remaining accumulated carriers (holes) after the switching on. Since, it holds that the remaining inversion-layer (accumulated) carrier density n_s (p_s) is lower than the majority substrate (inversion-layer) carriers, it is reasonable to assume that all remaining carriers recombine with incoming substrate majority (inversion-layer) carriers (see fig.1). Hence, I_{Geo} can be expressed by the contribution of two components I_{Geo_n} and I_{Geo_p} due to remaining electrons and holes, respectively:

$$\begin{aligned} I_{Geo} &= I_{Geo\_n} + I_{Geo\_p} \\ &= q\, f\, [n_s(L)W + p_s(W)L] \end{aligned} \tag{1}$$

where q is the electron charge, f is the gate signal frequency, L and W are the gate length and width, respectively. n_s (p_s) is the total number of remaining electrons (holes) under the gate given by:

$$n_s(L) = 2\int_0^{\frac{L}{2}} g(x)dx \tag{2}$$

$$p_s(W) = \int_0^{W} g(y)dy \tag{3}$$

g(x) and g(y) (cm^{-2}) are the remaining carriers concentration after transition from inversion to accumulation and from accumulation to inversion, respectively. *g(x) [g(y)]* depends on gate length (width) and gate fall (rise) times as well as on the following mechanisms (see fig.1):
During the rise time, the accumulated holes are first evacuated at the side substrate contact by the self induced field [9]. Then, as soon as the hole are evacuated the self induced field decreases and the holes evacuation is caused by the combination of the fringing field (due to substrate-contact side depletion zone, Sub Junction) and the thermal diffusion, see fig.1 (a). However, during the fall time (t_f), the electrons of the inversion layer are evacuated in the same manner as in the conventional MOSFET, see fig.1 (b), the detail can be found in ref [4,9].

III. Model Derivation

During the gate rise time, the holes drift back to p+ contact laterally thought the active area along the channel width. However, during the gate fall time, the electrons move only from the middle of the channel to the source/drain due to CP configuration (the source-substrate and drain-substrate are biased to the same potential). In our previous work [4], we have modeled the remaining carriers in n-channel transistor by using the continuity equation, the current carrier density equation, and the evacuation processes by both the electric field and the thermal diffusion, which are generally the most case encounters in experimental CP. We have demonstrated that the total number of remaining carriers in conventional NMOSFETis given by [4]:

$$n_s(L,t) = 2\left(\frac{C_{ox}(V_H - V_{th})}{q}\right)\left[\left(\frac{\mu_n\beta}{v_n} EXP\left(\frac{v_n}{\mu_n\beta}\frac{L}{2}\right) - \frac{\mu_n\beta}{v_n} - \frac{L}{2}\right)\right] EXP\left(-\frac{t_e}{\tau_L}\right) \tag{4}$$

Using the same method as in [4] for the evacuation of hole during the gate rise time and keeping in mind that in poly-Si TFT the holes move laterally thought the active area along the channel width, it will be easy to find the fallowing expression:

$$p_s(W,t) = \left(\frac{C_{ox}(V_L - V_{fb})}{q}\right)\left[\left(\frac{\mu_p\beta}{v_p} EXP\left(\frac{v_p}{\mu_p\beta}W\right) - \frac{\mu_p\beta}{v_p} - W\right)\right] EXP\left(-\frac{t_h}{\tau_W}\right) \tag{5}$$

where C_{ox} is the gate capacitance par unit area, $\mu_{n(p)}$ is the electron (hole) mobility, $v_{n(p)}$ is the drift electron (hole) velocity β is the thermal voltage, V_L (V_H) is the low (high)-level of the gate signal, V_{th} (V_{fb}) is the threshold (flat band) voltage, τ_L (τ_W) is the exponential decay constant associated with the influence of the electric field and the thermal diffusion in x (y) direction, see fig.1. t_e and t_h are the time of electron and hole drift, respectively, given by :

$$t_e = \frac{|V_H - V_{fb}|}{\Delta V_G} t_f \tag{6}$$

and

$$t_h = \frac{|V_L - V_{th}|}{\Delta V_G} t_r \tag{7}$$

where ΔV_G is the gate signal magnitude.

Therefore, using (1), (4) and (5) the geometric component can be expressed by:

$$\begin{aligned} I_{Geo}(L,W,t) &= I_{Geo\_n}(L,W,t) + I_{Geo\_p}(L,W,t) \\ &= qW f\left[\left(\frac{2\mu_n\beta}{v_n} EXP\left(\frac{v_n}{\mu_n\beta}\frac{L}{2}\right)\right) - L - \frac{2\mu_n\beta}{v_n}\right] X \\ &\left(\frac{(C_{ox}(V_H - V_{th}))EXP\left(-\frac{t_e}{\tau_L}\right)}{q}\right) + qLf\left[\left(\frac{\mu_p\beta}{v_p} EXP\left(\frac{v_p}{\mu_p\beta}W\right)\right) - W - \frac{\mu_p\beta}{v_p}\right] X \\ &\left(\frac{(C_{ox}(V_L - V_{fb}))EXP\left(-\frac{t_h}{\tau_W}\right)}{q}\right) \end{aligned} \tag{8}$$

By adding the expression of the geometric component given by (8) to the pure CP current $I_{CP\text{-}Pure}$ given by [2]:

$$I_{CP\_Pure} = 2kTqfD_{it}LWLn\left[\frac{v_{th}n_i\left(\sqrt{\sigma_n\sigma_p}t_f t_r\right)}{\Delta V}\left|V_{th}-V_{fb}\right|\right] \quad (9)$$

where σ_n/σ_P , $v_{th,}$ n_i, D_{it} , k and T are, respectively, the electron/hole capture cross section, the carrier thermal velocity, intrinsic carrier density, the density of state within the band gap, the Boltzmann constant and temperature.
Therefore, the modeled CP current (I_{CP_Mod}) can be expressed as :

$$\begin{aligned} I_{CP\_Mod}(L,W,t) &= I_{CP\_Pure} + I_{Geo} \\ &= 2kTqfD_{it}LWLn\left[\frac{v_{th}n_i\left(\sqrt{\sigma_n\sigma_p}t_f t_r\right)}{\Delta V}\left|V_{th}-V_{fb}\right|\right] + \\ &qWf\left[\left(\frac{2\mu_n\beta}{v_n}EXP\left(\frac{v_n}{\mu_n\beta}\frac{L}{2}\right)\right)-L-\frac{2\mu_n\beta}{v_n}\right]X \\ &\left(\frac{(C_{ox}(V_H-V_{th}))EXP\left(-\frac{t_e}{\tau_L}\right)}{q}\right)+qLf\left[\left(\frac{\mu_p\beta}{v_E}EXP\left(\frac{v_p}{\mu_p\beta}W\right)\right)-W-\frac{\mu_p\beta}{v_p}\right]X \\ &\left(\frac{(C_{ox}(V_L-V_{fb}))EXP\left(-\frac{t_h}{\tau_W}\right)}{q}\right) \end{aligned} \quad (10)$$

The terms $\frac{2\mu_n\beta}{v_n}$ and $\frac{\mu_p\beta}{v_p}$ present the gate length and width below which the $I_{CP\ Mod}$ is linearly depending on L and W, respectively. In other words, they present the gate length and width below which the geometric component can be negligible.

For $L<\frac{2\mu_n\beta}{v_n}$ and $W<\frac{\mu_p\beta}{v_p}$, the geometric component is reduced in x and y direction, thus (10) can be rewrites as:

$$\begin{aligned} I_{CP\_Mod}(L,W,t) &= qfWL \\ &X\left(N_{it}-\frac{(C_{ox}(V_H-V_{th}))EXP\left(-\frac{t_e}{\tau_L}\right)}{q}-\frac{(C_{ox}(V_L-V_{fb}))EXP\left(-\frac{t_h}{\tau_W}\right)}{q}\right) \end{aligned} \quad (11)$$

where N_{it} is the density of state par unity area ($N_{it}=Dit*\Delta E$, where ΔE is the scan energy band gap interval by the CP, given by $\Delta E = 2kTLn\left[\frac{v_{th}n_i\left(\sqrt{\sigma_n\sigma_p}t_f t_r\right)}{\Delta V}\left|V_{th}-V_{fb}\right|\right]$.

Therefore:

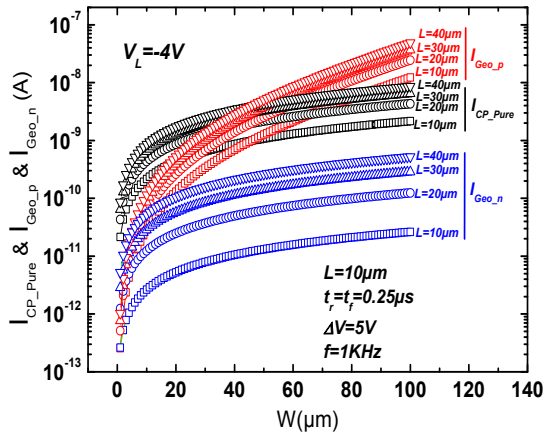

Fig.2 Calculated pure charge pumping current (I_{CP_Pure}), the geometric component in x direction (I_{Geo_n}) ,and y direction (I_{Geo_p}) as a function of the gate width (W) for different gate lengths (L). The used parameters are: V_L=-4, ΔV_G=5V , t_f=t_r=0.25 µs , ,C_{ox}=9.667 10^{-8} F/cm^2, V_{th}=0 and V_{fb}=-2V, ni=1.5$10^{10}$cm^{-3}, σ_p= σ_n=2.027 10^{-16} cm^2, D_{it}= 2.01410^{12} cm^{-2} eV^{-1}, v_{th}=10^7cm/s, μ_p=40cm/Vs[8], μ_n=80 cm/Vs, v_p=v_n=400 cm/s.

$$\frac{d^2 I_{CP\_Mod}(L,W,t)}{dLdW} = 0$$

$$N_{it} = \frac{(C_{ox}(V_H-V_{th}))EXP\left(-\frac{t_e}{\tau_L}\right)}{q}+\frac{(C_{ox}(V_L-V_{fb}))EXP\left(-\frac{t_h}{\tau_W}\right)}{q} \quad (12)$$

The last equation relies the exponential decay constants evacuation (τ_e and τ_h) with the transistors and gate signal parameters. It will be used later, in section-IV to experimentally extraction of τ_e and τ_h.

IV. MODEL VALIDATION

In the fallowing, to validate our proposed model we used the literature CP experimental data of n-channel poly-Si TFT as well as their parameters reported by Lu et al [7] and Wang et al[8].
First, we used equation (12) and the following parameters: t_f=t_r=0.25 µs , ΔV =5V ,C_{ox}=9.667 10^{-8} F/cm^2, V_{th}=0, V_{fb}=-2V, and N_{it}= 1.3 10^{12} cm^{-2} to extract the exponential decay constants τ_W and τ_L along the gate width (y direction) and length (x direction), respectively, using two low voltage CP gate signal a round the CP maximum current (V_L=-4V and V_L=-3.5V). τ_W and τ_L are found around of 6.58 10^{-7} s and 5.4 10^{-7} s, respectively. Then, we have computed I_{CP_Pure}, I_{Geo_n} and I_{Geo_p} as function of gate width for different gate lengths (L=10-40µm), using the first, the second and the third term of equation (10). The results of the calculation are given in fig.2. These results show that I_{Geo_n} is lower compared to I_{Geo_p} and I_{CP_Pure} for all used gate length.

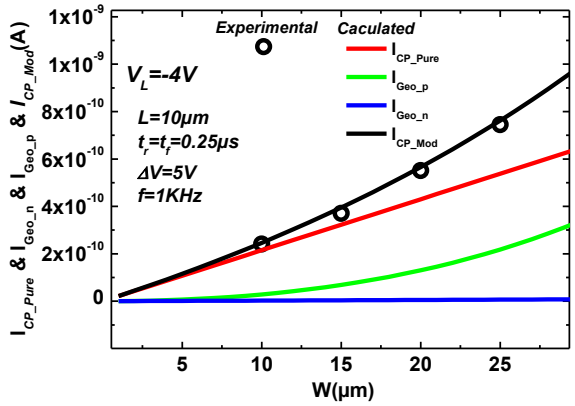

Fig.3 Comparison between the calculated $I_{CP\text{-}Mod}$ using the proposed model and the CP experimental data for gate length fixed at 10μm and varied gate width ,reported in[8]. The same parameters as in fig .1 are used for the calculation.

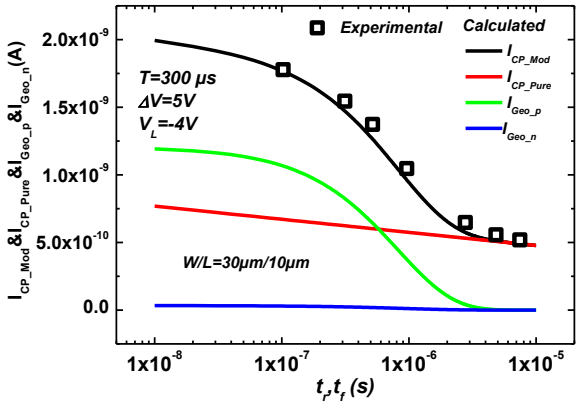

Fig.4 Comparison between the experimental CP data reported by Lu et al and the calculated I_{CP_Mod} using the proposed model as a function of transition gate signal time (t_f=t_r).

This behavior is not surprising, since it is clear that for conventional n-channel poly-Si TFT the electron evacuation during fall time could be much faster than that of (evacuation) hole during the rise time, because the electrons can be quickly drift along the low resistance of inversion channel, while the hole must drift through the substrate (of high resistance due to grain boundaries) to side contact. In addition due to CP configuration the electrons move back only from the middle of the channel to the source/drain. Contrary, to the hole which drift along the gate width to the side contact. Finally, the mobility of holes is smaller than that of electrons. According to the above analysis, one can plausibly think that the geometric component in n-channel poly-Si TFT (under certain condition t_f and t_f) is dominated by the remaining hole when the transistor transits from accumulation to inversion and depend on t_r and W. Indeed, the same behavior is experimentally reported in [7] and [8] for the same parameters as used in our calculation. In those works, it has been demonstrated that, I_{Geo} is hole transport limited and for typical $t_f > 0.1\mu s$ the sheet density of remaining hole in the channel is independent of the channel length but depends on channel width. Furthermore, fig.3 shows a good agreement between the CP experimental data and calculated I_{CP_Mod} (black curve), which is the sum of I_{CP_Pure} *(red curve)*, I_{Geo_p} (green curve) and I_{Geo_n}*(blue curve)*, as a function of the gate width using the same experimental conditions and devices parameters as those used in [8]. We should note that the evacuation velocity carriers (v_p=v_n), is the only adjustable parameter to fit the experimental data. The comparison un between the experimental CP data reported by *Lu* et al [7] and the computed I_{CP_Mod} , using equation (10) as a function of $t_{f,r}$ (t_f=t_r) is presented in fig.4 for n-channel poly-Si TFT with W/L=30/10. In this figure, we also presented the calculated I_{CP_Pure}, I_{Geo_p} and I_{Geo_n}. It is clear, from fig.4, that the CP experimental data is well fitted by computed I_{CP_Mod} using the proposed model (equation (10)). I_{CP_Mod} increases with decreasing $t_{f,r}$ and fallow the pure CP current (I_{CP_Pure}) as described in [2]. However, an additional increase can be observed when $t_{f,r} < 1\mu s$ and I_{CP_Mod} diverges rapidly from I_{CP_Pure} . This is due to the geometric component increase caused by $t_{f,r}$ decrease, which is principally dominated by I_{Geo_p} (green curve), whereas I_{Geo_n} is negligible. According to this comparison, our proposed model not anly fit well the experimental CP data but captures all experimental observations reported in [7] and [8] such as the disappearance of the geometric component for the transition time $t_{f,r}>1\mu s$ and the dependence of the geometric component on gate width and not on gate length. Thus, our developed model could be powerful tool to predict the geometric component and charge pumping in poly-Si TFT devices.

In addition, as we have reported above, the I_{Geo_n} is negligible. Therefore, we can use equation (10) to establish CP empirical relationship reported by Wang et al [8] and identify their empirical parameters as follow:

$I_{Geo\_n}(L,W,t) \approx 0$, if we put:

$$\lambda = \frac{\beta \mu_p}{v_p} \tag{13}$$

and

$$\alpha = qfW\lambda f\left(\frac{(C_{ox}(V_L - V_{fb}))EXP\left(-\frac{t_h}{\tau_W}\right)}{q}\right) \tag{14}$$

we can express (8) as

$$I_{Geo} = \frac{\alpha}{\lambda}\left(\lambda EXP\left(\frac{W}{\lambda}\right) - W - \lambda\right) \tag{15}$$

Equation (15) corresponds to the empirical model of the geometric component developed in [8]. Where fitting parameters α and λ are well defined as function of device and experimental conditions, and they have now a physical meaning in CP as a function of *W*. Note that the equation (15) is also used by Tahi et al [10] to extract the geometric

component in CP current of MOSFET, excepting using *L* instead of W, because in MOSFET the geometric component is L-controlled effect.

In addition, in the absence of I_{Geo_n}, equation (12) can be expressed as:

$$N_{it} = \frac{\left(C_{ox}\left(V_L - V_{fb}\right)\right)EXP\left(-\frac{t_h}{\tau_W}\right)}{q} \tag{16}$$

Therefore using (14), (15) and (16), the CP current given by (10) can be expressed as:

$$I_{CP\_Mod} = -\alpha + \alpha EXP\left(\frac{W}{\lambda}\right) \tag{15}$$

This equation is used by Wang et al [8] to fit their experimental CP data, where the empirical parameter λ and α are not physically explained, but in this work they are well established and given by (13) and (14), respectively.

V. CONCLUSION

Based in our understanding of the physical mechanisms behind the geometric component in charge pumping of polycrystalline thin film transistors, we have proposed an analytic model for this component. The developed model seems to be in good agreement with the experimental data and can capture all the experimental behaviours reported in the literature for polycrystalline thin film transistor, In addition, based on this geometric component model developed in this work, we have fixed the parameters of CP empirical equation previously reported elsewhere. Thus a new expression of CP current with geometric current is established.

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