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MASTER

In **Power Engineering**

Title:

A Single Phase Active Power Factor Correction Using Interleaved Boost Converter

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Abstract

DC power supplies are extensively used inside most of electrical and electronic appliances such as in computers, televisions, audio sets and others. And the electrical energy available in the utility grid is not suitable for direct use. So in particular, applications requiring DC source must involve an interface device between the AC power line and the load requiring the DC voltage. Conventional AC/DC conversion involves diode rectifiers with large capacitor to reduce DC voltage ripple. The filter capacitor reduces the ripple present in the output voltage but draws non sinusoidal line current which reduces the power factor. Therefore, power factor correction (PFC) techniques are gaining increasing attention.

This project introduces one of the most popular topologies for active PFC which use a boost converter to draw a continuous input current. This input current can be manipulated by average current mode control technique. But there is ripple in the input current due to inductor of boost converter, this can be minimized by using two phase interleaved boost converter. This project applied the average current mode technique to control two channels interleaved boost converter in continuous conduction mode using PI controller. The simulation results show that the applied topology provides high power factor and low THD.

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List of abbreviations

AC	Alternative Current
ACMC	Average Current-Mode Control
APFC	Active Power Factor Correction
CCM	Continuous Conduction Mode
CICM	Continuous Inductor Current Mode
DC	Direct Current
DCM	Discontinuous Conduction Mode
DICM	Discontinuous Inductor Current Mode
DSP	Digital Signal Processor
DPS	Distributed Power System
EMI	Electromagnetic Interference
HVDC	High Voltage Direct Current
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronic Engineers
LF	Low-Frequency
LPF	Low-Pass Filter
MOSFET	Metal Oxide Semi-conductor Field Effect Transistor
PCC	Point of Common Coupling
PF	power factor
PFC	Power Factor Correction
PID	Proportional-Integral-Derivative
PI	Proportional-Integral
PQ	Power Quality
PU	Per Unit
SMPS	Switch Mode Power Supplies
TDD	Total Demand Distortion
THD	Total Harmonic Distortion

General Introduction

The extensive use of DC power supplies inside most of electrical and electronic appliances lead to an increasing demand of DC power. So, for obtaining this DC power, an interface must be provided between the AC power line and the load requiring DC voltage.

Generally, this conversion from AC to DC is done by single phase diode rectifiers. These classical converters rectify the input AC line voltage to obtain DC output voltage, but this DC voltage oscillates between zero to peak. To reduce this ripple from DC voltage a filter capacitor is used, and that is where the problem of power factor and total harmonics distortion (THD) arises. The capacitor maintains the DC voltage at a constant value but it draws non sinusoidal current from the supply. It draws current from the supply only at the line voltage peaks. Hence, the input current becomes pulsating which results in poor power factor and high THD. So, the power factor correction techniques are gaining attention.

There are two types of power factor correction techniques, passive power factor correction and active power factor correction. Better power factor cannot be obtained by passive power factor correction techniques, and the output voltage also cannot be controlled. As a result, active power factor correction technique is used for satisfactory result. In active power factor correction most popular is boost converter for its continuous input current. The boost converter is widely used as active power factor corrector [1] because it draws continuous input current from the supply. This input current can be controlled to follow a sinusoidal reference using current mode control techniques. There are different current mode control techniques [2], but best result can be obtained from average current mode control technique [3] due to its various advantages.

In this thesis , power factor correction and THD minimization is done by two phase interleaved boost converter [4] whose input current is controlled by average current mode control technique. In this interleaved boost converter, there are two boost converters operating in 180˚ out of phase. Therefore, the ripple present in the current of boost converter gets almost eliminated and that is the main advantage of the interleaved boost converter. Here for average current mode control, PI controllers are used. The simulation of interleaved boost converter with PI controller is shown here to show that interleaved boost converter with PI controller provides good input current with high power factor and low THD. All the simulation is done by MATLAB-Simulink.

This project is mainly divided into 3 chapters, the first chapter is an overview of power quality issues and power factor correction and the second is about a Modeling and control of active power factor correction, the simulations and results are discussed in the last chapter.

Chapter I

Overview of power quality issues and power factor correction

1.1 Introduction

The distortion normal electric current waveform due to the nonlinear loads creates harmonics in AC distribution systems. Nonlinear loads arise for variable resistance i.e. resistance varies for each sine wave of the applied voltage, causing in a series of positive and negative pulses. In AC-DC system, the connected equipment to the distributed power system (DPS) desires some kind of power conditioning, rectification in general, which creates a non-sinusoidal line current because of the non-linear input characteristic.

The focus of this chapter is to introduce power factor and harmonics power quality problems caused by rectifiers and non-linear loads and provide a general idea on the classification methods that can be used to fix it in single phase system.

1.2 Non-sinusoidal systems

In earlier time's rectification used to be a much simpler concern covering circuits such as the peak-detection and inductor-input rectifiers, the phase-controlled bridge, poly-phase transformer connections, and perhaps some multiplier circuits. But recently, rectifiers have become much more sophisticated, and now complicated systems rather than mere circuits. They include pulse-width modulated converters such as the boost converter, with control systems that regulate the AC input current waveform. The reason for this trend is the undesirable AC line current harmonics, and low power factors, of conventional rectifier circuits such as peak-detection and phase-controlled rectifiers. The adverse effects of power system harmonics are well recognized and include: unsafe neutral current magnitudes in three-phase systems, heating and reduction of life in transformers and induction motors, degradation of system voltage waveforms, unsafe currents in power-factor-correction capacitors, malfunctioning of certain power system protection elements. In a real sense, conventional rectifiers are harmonic polluters of the AC power distribution system. With the widespread deployment of electronic equipment in our society, rectifier harmonics have become significant and measurable problems. Thus, there is a need for high-quality rectifiers, which operate with high power factor, high efficiency, and reduced generation of harmonics. Several international standards now exist that specifically limit the magnitudes of harmonics currents, for both high-power equipment such as industrial motor drives, and low-power equipment such as electronic ballasts for fluorescent lamps and power supplies for office equipment [1].

1.3 Power quality

Power quality is an important concept in the design and analysis of AC-DC converters, and is the primary motivation behind this Project. In this section, an overview of Power quality issues, total harmonic distortion (THD) and power factor (PF) is presented.

In addition, the relationship between THD and power factor, as well as the negative effects of low power factor on power systems are shown [5].

1.3.1 Power quality issues

Power quality issues are defined as any power problem manifested in voltage, current, or frequency deviations that results in failure or miss-operation of customer equipment. Power quality problems can be categorized mainly into: Overvoltage, Under-voltage, Sags, Swells, Transients, Harmonics and Noise [5].

- **Overvoltage:** is an increase in the RMS voltage greater than 1.1 P_u at the power frequency for a duration longer than 1 min.
- **Under-voltage:** is a decrease in the RMS voltage to less than 0.9 P_u at the power frequency for a duration longer than 1 min. **Fig.1.1** shows overvoltage and under-voltage events.

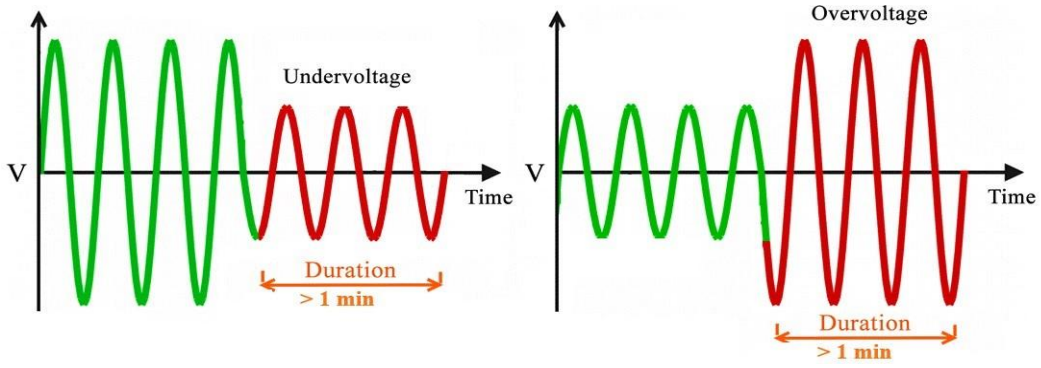


Fig.1.1 *Waveform shape during Under-voltage and Overvoltage events*

- **Sag:** is a decrease in RMS voltage or current at the power frequency for duration from 0.5 cycle to 1 min.
- **Swell:** is an increase in RMS voltage or current at the power frequency for durations from 0.5 cycle to 1 min. **Fig.1.2** shows sag and swell events.

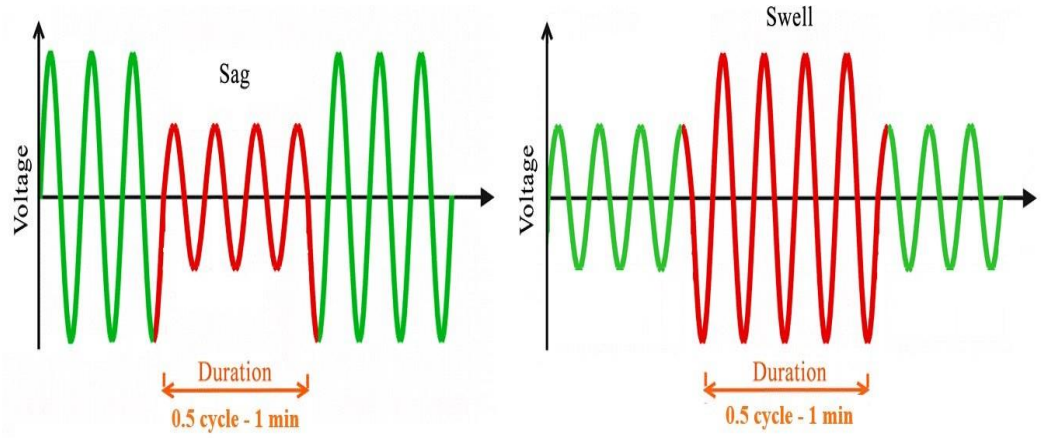


Fig.1.2 *Waveform shape during voltage Sag and Swell events*

- **Transients:** are power quality disturbances that involve destructive high magnitudes of current and voltage or even both as shown in **Fig1.3**. It may reach thousands of volts and amps even in low voltage systems. However, such phenomena only exist in a very short duration from less than 50 nanoseconds to as long as 50 milliseconds. This is the shortest among PQ problems, hence, its name. Transients usually include abnormal frequencies, which could reach to as high as 5 MH_Z. In addition, transients are also known as surge. According to IEEE 100, surge is a transient wave of voltage, current or power in an electric circuit [1].

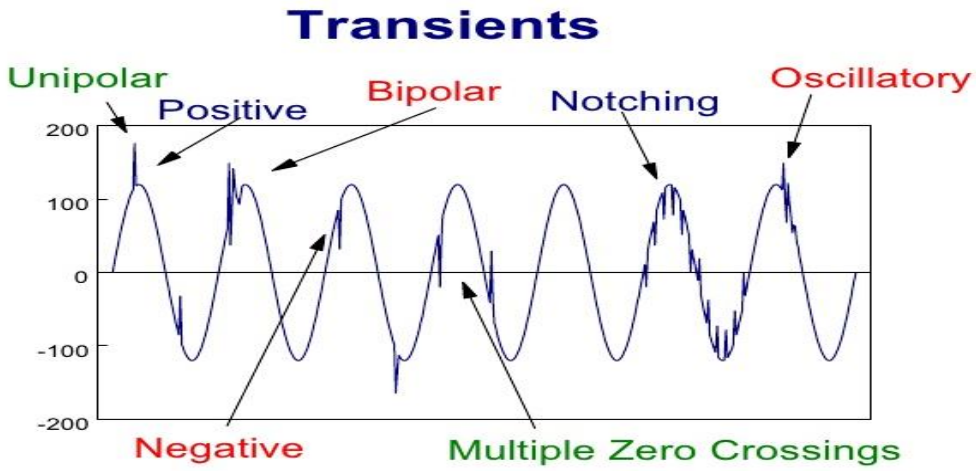


Fig.1.3 *Waveform shape during different transient events*

- **Harmonics:** are sinusoidal voltages or currents having frequencies that are integer multiples of the fundamental frequency as shown in **Fig.1.4**, if the multiples are not integers, they are called inter harmonics. They are created when a non-linear load is connected to the system. Harmonics will be discussed in further details in the next section [1].

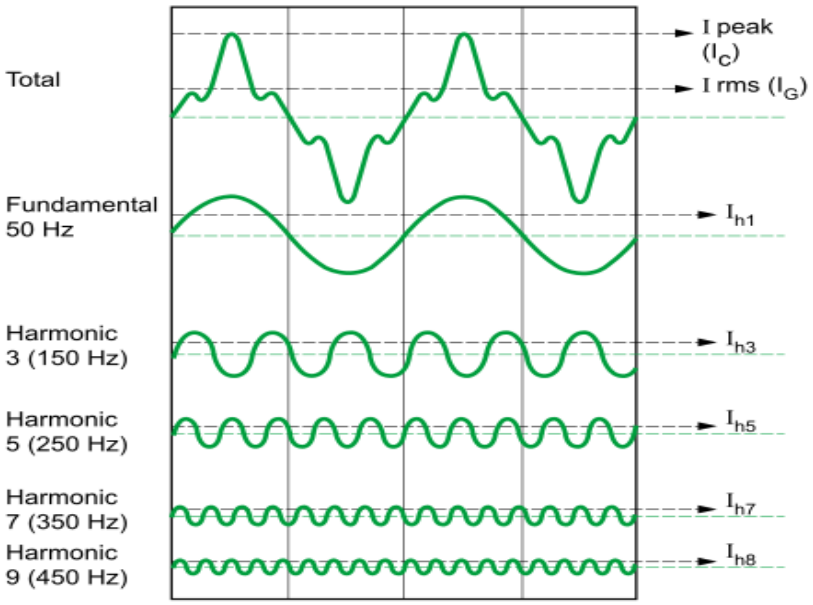


Fig.1.4 *Distorted current waveform with fundamental and harmonic frequencies*

- **Noise:** are unwanted electrical signals that produce undesirable effects in the circuits of the control systems in which they occur. **Fig.1.5** is an example of a noisy signal.

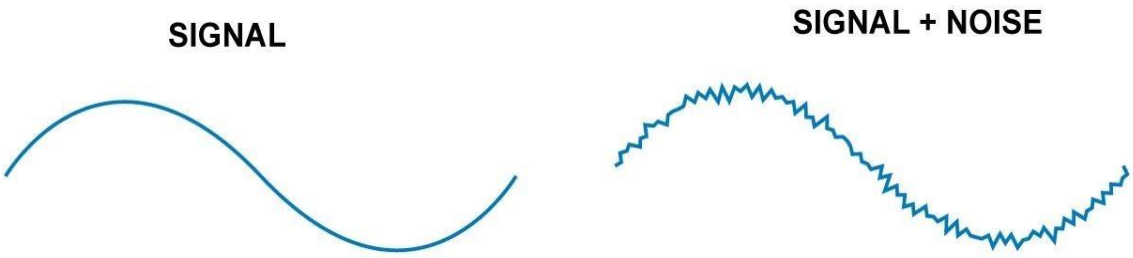


Fig.1.5 *Waveform shape of a signal with and without noise*

It should be noted that the previous classification is very brief and generalized. Standards like IEEE and IEC provide more detailed classifications of power quality problems. Other terms that

may be encountered when describing power quality issues include: voltage fluctuations, flicker, notching and interruptions…etc.[6]. Power quality issues are discussed in further detail in **Appendix A**.

1.3.2 Definition of Power Factor and Total Harmonic Distortion

Total harmonic distortion (THD) is a measurement that tells you how much of the distortion of a voltage or current is due to harmonics in the signal. THD is an important aspect in audio, communications, and power systems and should typically, but not always, be as low as possible[5].

A voltage or current that is purely sinusoidal has no harmonic distortion because it is a signal consisting of a single frequency. A voltage or current that is periodic but not purely sinusoidal will have higher frequency components in it contributing to the harmonic distortion of the signal. In general, the less that a periodic signal looks like a sine wave, the stronger the harmonic components are and the more harmonic distortion it will have[6].

The power factor *PF* gives information about the distortion of a line voltage, a line current and a phase shift between them. Simultaneously, it gives information about the real power utilization in the power system. The **Fig.1.6** illustrates relations between an apparent, a real and a reactive power in linear systems. The **Fig.1.7** outlines relations between an apparent, real, displacement reactive power, and distortion reactive power in non-linear systems[5],[6].

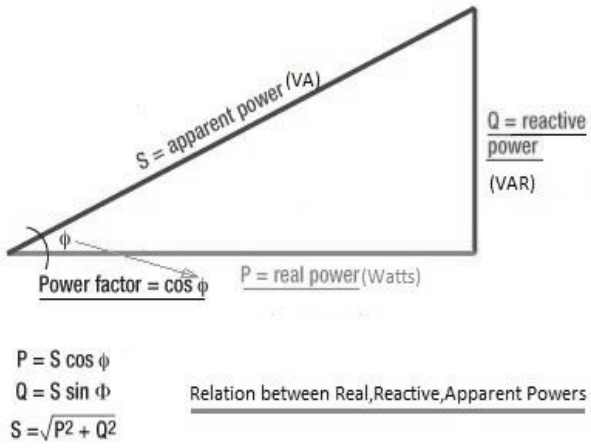


Fig.1.6 *Relations in linear systems.*

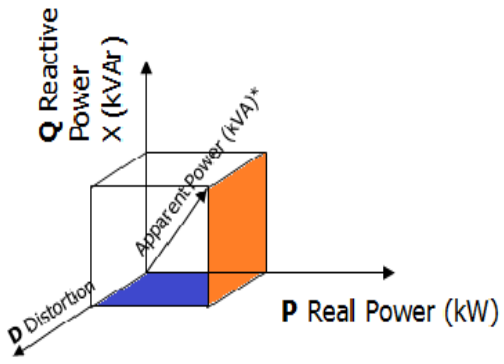


Fig.1.7 *Relations in non-linear systems*

$$PF = \frac{P}{S} \tag{1.1}$$

$$PF = \frac{V_{RMS} \cdot I_{RMS} \cdot \cos\theta}{V_{RMS} \cdot I_{RMS}} \tag{1.2}$$

Where $\mathbf{I_{RMS}}$ and $\mathbf{V_{RMS}}$ are line voltage and line current, θ is phase shift between them. Therefore the power factor in linear systems equals to a cosine of the phase shift, However, in power electronic systems due to non-linear behavior of the power devices the power factor representation is not valid. The non-linear loads cause a typical distorted line current. The **Fig.1.9** illustrates this situation.

shall be used Fourier representation of line voltage and current [5],[6]

$$i(t) = I_{DC} + \sum_{n=1}^{\infty} I_{mn}\sin(n\omega t + \theta_n) \tag{1.3}$$

$$i(t) = I_{DC} + I_{m1}\sin(\omega t + \theta_1) + \sum_{n=2}^{\infty} I_{mn}\sin(n\omega t + \theta_n) \tag{1.4}$$

$$v(t) = V_{DC} + \sum_{n=1}^{\infty} V_{mn}\sin(n\omega t + \theta_n) \tag{1.5}$$

$$v(t) = V_{DC} + V_{m1}\sin(\omega t + \theta_1) + \sum_{n=2}^{\infty} V_{mn}\sin(n\omega t + \theta_n) \tag{1.6}$$

Inserting (1.4) and (1.6) into a definition of the power factor (1.2), it is obtained a representation of the power factor for non-linear systems

$$PF = \frac{\sum_{n=1}^{\infty} V_{RMS,n}\cdot I_{RMS,n}\sin\theta_n}{V_{RMS}\cdot I_{RMS}} = \frac{\sum_{n=1}^{\infty} V_{RMS,n}\cdot I_{RMS,n}\sin\theta_n}{\sqrt{\sum_{n=1}^{\infty} V_{RMS,n}^2}\cdot\sqrt{\sum_{n=1}^{\infty} I_{RMS,n}^2}} \tag{1.7}$$

Where V_{RMS},n and $I_{RMS,n}$ are RMS values of the nth harmonics of the voltage and current, and θ_n is phase shift between nth harmonics of the current and voltage. Generally, the most of power electronic systems have their input voltage from stable line voltage sources. Consequently, the equations can be written as ((1.8) and (1.9)), assuming that the line voltage is a pure sinus and the current is distorted (non-sinusoidal) [5].

$$v(t) = V\sin\omega t \tag{1.8}$$

$$i(t) = \sum_{n=1}^{\infty} I_{mn}\sin(n\omega t + \theta_n) \tag{1.9}$$

In the general cases the real power equals to:

$$P = \sqrt{P_{DC}^2 + P_1^2 + P_2^2 + P_3^2 + \cdots} \quad (1.10)$$

Due to an absence of the other voltage harmonics except the first one, the total real power can be computed by the following equation (1.11)

$$\mathrm{P} = \mathrm{V_{RMS,1}} \cdot \mathrm{I_{RMS,1}} \cdot \cos\theta_1 \quad (1.11)$$

$$PF = \frac{P}{S} = \frac{V_{RMS,1} \cdot I_{RMS,1} \cdot \cos\theta_1}{V_{RMS,1} \cdot \sqrt{\sum_{n=1}^{\infty} I_{RMS,n}^2}} \quad (1.12)$$

If the equation (1.12) is simplified, it is obtained the following expression (1.13). The equation is composed of two factors k_{dist} and k_{disp}

$$PF = \frac{I_{RMS,1}}{I_{RMS}} \cdot \cos\theta_1 = k_{dist} \cdot k_{disp} \quad (1.13)$$

Where θ_1 is a phase shift between a voltage and a fundamental component of the line current. $\mathrm{I_{RMS}}.1$ is a RMS value of the fundamental component of the line current, $\mathrm{I_{RMS}}$ is a RMS value of the total line current [5].

k_{dist} is a distortion factor which is defined as a fraction of the fundamental component of the line current and the total line current (contains all harmonics).

$$k_{dist} = \frac{\mathrm{I_{RMS,1}}}{\mathrm{I_{RMS}}} = \text{ distortion factor} \quad (1.14)$$

k_{disp} : factor describes an angle between the line voltage and the fundamental component of the line current.

$$k_{\text{disp}} = \cos\theta_1 = \text{ displacement factor} \tag{1.15}$$

A further important parameter is a total harmonic distortion of the line current $\mathbf{THD_i}$, which is defined as follows:

$$\text{THD} = \sqrt{\frac{\sum_{n=2}^{\infty} I_{RMS,n}^2}{I_{RMS,1}^2}} = \sqrt{\frac{1}{k_{dist}^2} - 1} \tag{1.16}$$

Conventional Switch Mode Power Supplies (SMPSs) use a rectifier with a bulky capacitor. As result the line current is characterized by a high pulsation 1.3. $\mathbf{THD_i}$ comes over 70% and PF is poor, it does not exceed 0,67. The equations (1.14) and (1.16) demonstrate that the power factor and total harmonic distortion are connected together. If the power factor is near unity, the total harmonic distortion is very small[5].

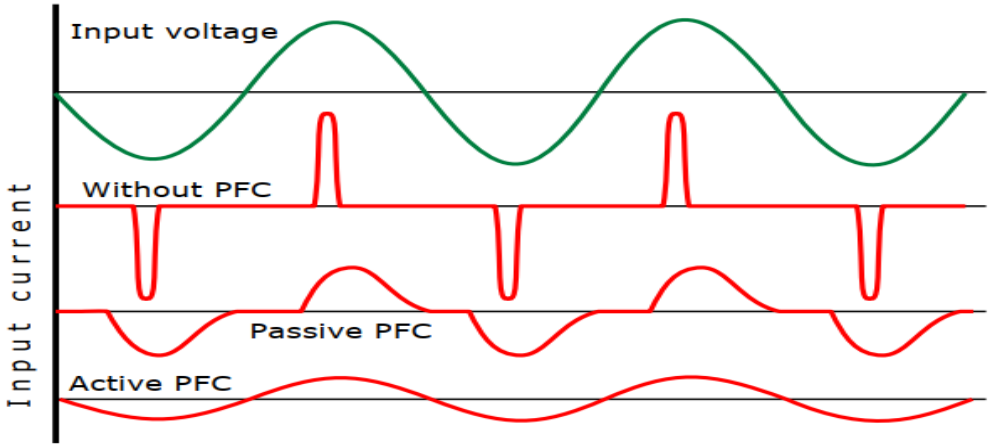


Fig.1.8 *Voltage and current waveforms*

1.3.3 Sources of harmonics

The main source of the harmonics is any non-linear loads that produce the voltage harmonics and current harmonics. This occurs because the resistance of the device is not a constant. The resistance in fact, changes during each sine wave, as shown in **Fig.1.9** nonlinear systems is one in which the current is not proportional to the applied voltage[7].

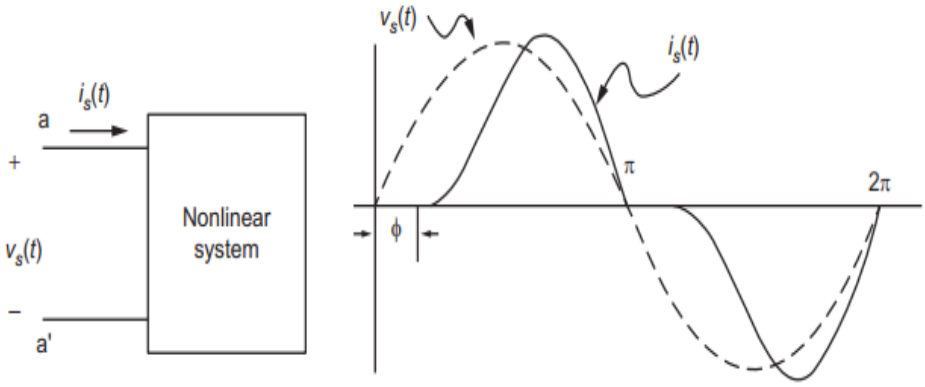


Fig.1.3 *Nonlinear load draws distorted line current*

Source of harmonics can be classified into three main sources: electronic devices, arcing devices and saturated magnetic devices.

- Power electronic devices create harmonics by drawing power only during parts of the voltage cycle. Electronic devices such as AC/DC converters, are found in many domestic and industrial applications, e.g. televisions, personal computers, speed controllers for motors, battery chargers…etc.[7].
- Arcing equipment like arc furnaces, welders, lighting (mercury vapor, fluorescent) generate harmonics due to the nonlinear characteristics of the arc itself [7].
- When magnetic devices such as power generators and transformers are operated close to magnetic saturation region (nonlinear B-H region of hysteresis curve), the voltage-current characteristics become greatly distorted and generate harmonics[7].

1.3.4 Effects of harmonics

The presence of harmonics has harmful effects on the power system's equipment as well as on its functioning reliability. The main negative impacts of harmonics are listed below [8]:

- **Decreased power factor:** harmonics increase the apparent power (S) required by the system, while the effective real power at the fundamental frequency does not benefit from that. This signifies that higher current is drawn, so added wire section and higher rating protection and distribution circuits are required[8].
- **Conductor losses:** obviously, additional current drawn apart from the needed at the fundamental frequency yields to additional cable losses at the conductors.

- **Skin effect**: the higher the frequency of the current passing through the wire, the higher its resistance losses.
- **Tripled harmonics and neutral conductor:** zero sequence harmonics (3^{rd}, 6^{th}, 9^{th}, …etc.) also known as tripled harmonics circulate between phases and neutral. The presence of significant components of these harmonics can cause overheating. Unless the neutral is sufficiently oversized, a fire hazard may occur[8].
- **Resonance:** inductances and capacitors in the power system form resonant circuits. If this resonance is close to one of the harmonic frequencies injected, large current and voltage will be induced. This issue is especially related to capacitors bank installations for power factor correction[8].
- **Motors and generators:** the high impedance of generators will easily transfer current harmonic distortion into voltage harmonic distortion affecting other loads supplied from that source. The excessive shaft voltages and relevant bearing currents in motors fed from distorted supplies can cause bearing damage. Also, negative sequence harmonics tend to exert a force against torque rotation causing vibration, added heat and derating of motors. extra core and copper losses are common effects of harmonics for both generators and motors[8].
- **Transformers:** the same effect of core losses and copper losses appear in transformers. Tripled harmonics in the neutral conductor of transformers can dangerously overheat them. There is also a potential risk of resonance between transformer inductance and supplied capacitive loads at some harmonic frequencies. Additionally, laminated transformers cores can vibrate at certain harmonic frequencies, causing audible noise and overheat[8].
- **Circuit breakers and fuses:** since tripping mechanism in circuit breakers and fuses responds to RMS current, a highly distorted current signal can cause false tripping and fusing and thus the need to oversize them which affects the sensitivity of the protection system[8].

Other effects of harmonics can be:

- Digital circuits can be affected by misinterpretation of logical values in the presence of harmonics.
- Reduced service life of components and equipment under continuously distorted supply voltage.
- Malfunction of information technology equipment (computers, printers, monitors…) such as memory losses and turn offs.

- Telecommunication system operate at high frequencies; high frequency harmonics can create interference in communication circuits sharing a common path.

1.4 Uncontrolled AC-to-DC converters

Electric power conversion stands for converting electrical energy from one form to another (AC/AC; AC/DC; DC/DC; DC/AC). Devices that are used for this purpose are called power converters. Rectifiers among those power converters, are circuits that convert AC signal into DC signal. Their extensive use in nowadays applications made them the most contributing source of harmonics generation in power systems. They are classified as the following[5]:

- Uncontrolled rectifiers.
- Half wave rectifier
- Full wave rectifier (Bridge rectifier, center-tap rectifier)

The next figure summarizes the previous classification:

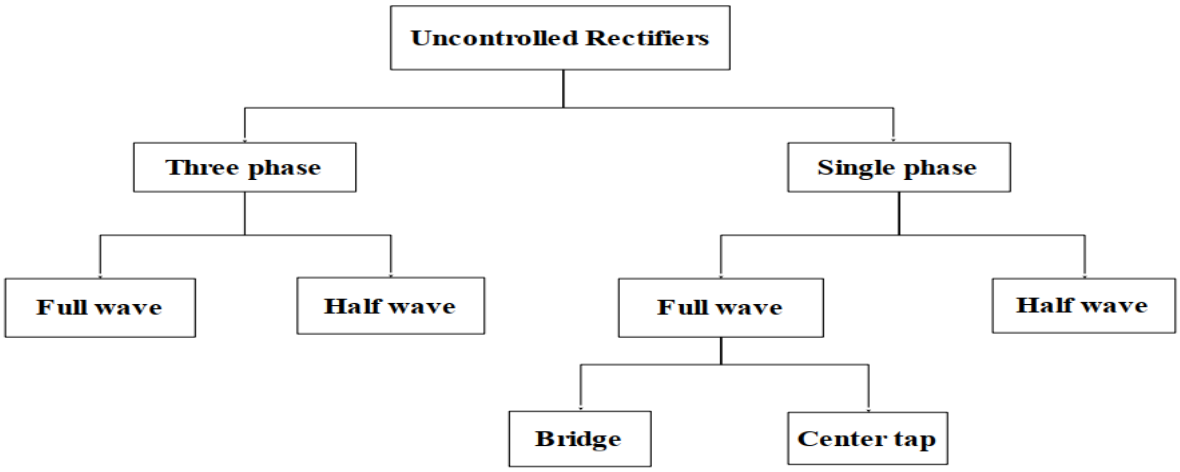


Fig.1.4 *Classification of uncontrolled rectifier*

1.5 Perturbations caused by rectifiers

The most severe perturbation caused by rectifiers affects the line current's power quality; The signal is discontinuous, periodic but far from sinusoidal, meaning it contains a large number of harmonics. The harmonic currents are reactive in nature which means that they decrease the power factor of the system[5].

The output is not pure DC and contains undesired ripples, adding a capacitor in parallel with the load can significantly reduce these ripples. Rectifiers are also responsible for voltage notching

when commutated from one phase to another, resulting in a momentary short circuit between the lines.

For single phase low voltage applications, the voltage drops of the diodes due to forward biasing and their internal resistance distorts the voltage waveform and decreases the efficiency of the system[5].

1.6 THD standards:

Engineering standards and recommendations are employed to set limits to the permissible amount of harmonic distortion introduced at the point of common coupling (PCC), often expressed by $\mathbf{THD_{max}}$ for voltage and $\mathbf{TDD_{max}}$ for current. The next tables represent limits of voltage and current harmonic distortions according to IEEE 519 (USA) for the year of 2014.

Table.1.1 *IEEE STD 519-2014 voltage distortion limits*

Bus voltage V at PCC	**Individual harmonic (%)**	**Total harmonic distortion THD (%)**
V ≤ 1.0 kV	5.0	8.0
1 kV < V ≤ 69 kV	3.0	5.0
69 kV < V ≤ 161 kV	1.5	2.5
161 kV < V	1.0	1.5
A high-voltage system can have up to 2.0% THD where the cause is an HVDC terminal whose effects will have attenuated at points in the network where future users may be connected.		

Table.1.2 *IEEE STD 519-2014 current distortion limits for systems rated 120 V - 69 kV*

Maximum harmonic current distortion in percent of I_L						
Individual harmonic order (odd harmonics)						
I_{sc}/I_L	3≤ h <11	11≤ h <17	17≤ h <23	23≤ h <35	35 ≤ h <50	TDD
<20	4.0	2.0	1.5	0.6	0.3	5.0
20<50	7.0	3.5	2.5	1.0	0.5	8.0
50<100	10.0	4.5	4.0	1.5	0.7	12.0
100<1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0
I_{sc}: maximum short-circuit at PCC. I_L: maximum demand load current (fundamental frequency component) at PCC under normal load operating conditions.						

1.7 Power Factor Correction

It is a technique of counteracting the undesirable effects of electric loads that create a power factor less th0an 1.

When an electric load has a PF lower than 1, the apparent power delivered to the load is greater than the real power which the load consumes.

Only the real power is capable of doing work, but the apparent power determines the amount of power that flows into the load, combining both active and reactive components.

The purpose of the power factor correction circuit is to minimize the input current waveform distortion and make it in phase with the voltage one. Most of the research on PFC for nonlinear loads is actually related to the reduction of the harmonic content of the line current[9].

1.8 Power Factor Correction Circuits Types

There are several methodologies to achieve PFC in single-phase systems, depending on whether active switches (controllable by an external control input) are used or not, they can be categorized as "*Passive*" or "*Active*".

The classification of single-phase PFC topologies is shown in **Fig.1.11** [9]:

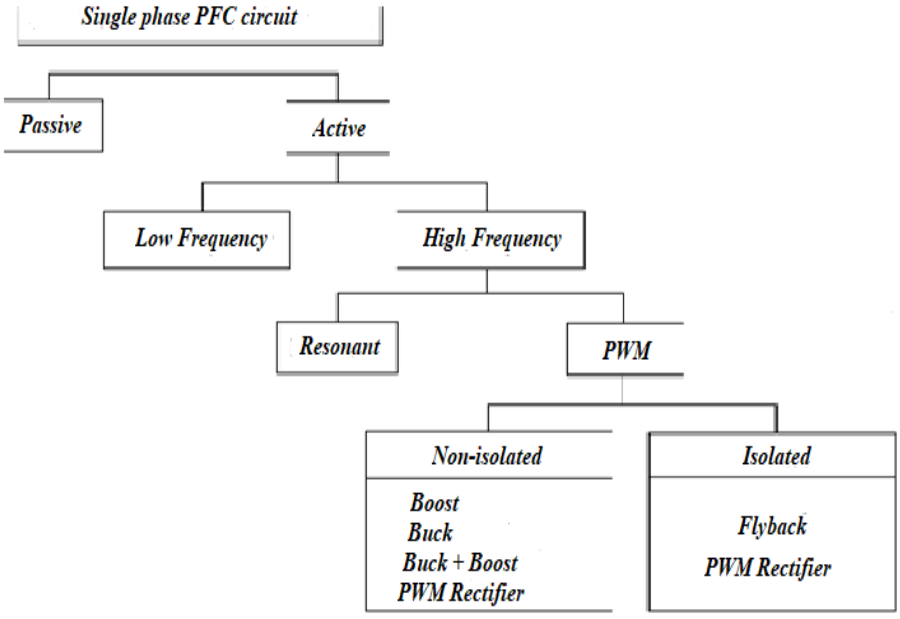


Fig.1.5 *Various Single-Phase PFC topologies*

1.8.1 Passive PFC:

In this circuit type, only the passive elements are being used along with diode bridge rectifier in order to improve the power factor and shape of the input line current. Using this PFC circuit type, input power factor of the system can be increased from the value of 0.7 to 0.8 nearly. The size of the PFC circuit and its cost will increase according to the increase in the input supply-voltage. The main objective of the PFC is filtering the input current harmonics in line current. These current harmonics can be filtered using LPF by only allowing the fundamental component to pass and blocking all the other harmonics to improve the power factor. Using the passive PFC, current harmonics can only be decreased to a certain limit and the power factor cannot reach a value near unity. The output voltage cannot be controlled in this PFC type [10].

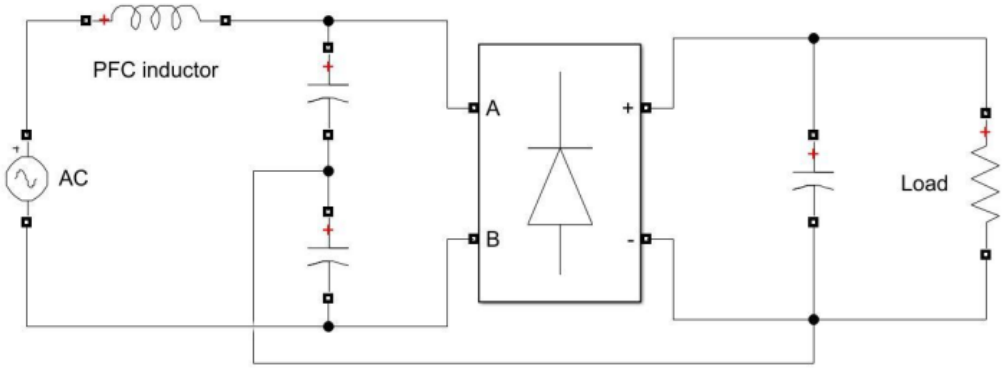


Fig.1.6 *Passive PFC circuit*

- **Advantages**
  - Simple in structure.
  - More reliable and rugged.
  - Equipment's used in passive PFC will not generate high frequency EMI [11].
  - The cost required to process this method is very low.
  - High frequency switching losses are not present in this method and it is insensitive to noise and surges.
- **Disadvantages**
  - Bigger filter size.
  - Dynamic response of the system is very low.
  - Output voltage control is difficult and it is not possible.

- As inductors and capacitors are present in the circuit, there will be a chance of interaction between the elements in the circuit.
- With the use of filters in this method, harmonics can be decreased but the fundamental component of the line current will shift its phase from the original one [10].
- load connected to the system decides the shape of the input line current.

1.8.2 Active PFC

In recent years, using the switched-mode topologies, many circuits and control methods are developed up to date to comply with certain standard (such as IEEE Std 519 and IEC1000-3-2).

To achieve this, high-frequency switching techniques have been used to shape the input current waveform successfully [12]. Basically, the active PF correctors that are used to accomplish the PFC function in single-phase power supply are based on the well-known basic converter topologies or their developed versions, the active PFC solution can be divided into two classes[13].

1.8.2.1 Active Low Frequency PFC:

Active low-frequency (LF) PFC circuits operate at a switching frequency of twice the line frequency, 100 or 120 Hz, and in synchronism with it. This method uses an active switch, a LF inductor, and a control circuit to perform PFC [14].

1.8.2.2 Active High Frequency PFC:

In this class of circuits, switching frequency is greater than the line-frequency, 20kHz to 200 kHz [15]. The power factor value obtained in this circuit is more than 0.9. And further, the value of power factor can be increased to a higher value to reach unity, this can be achieved by adding some filtering elements to the circuit [16]. With the active PFC circuit, the size of the circuit is smaller comparing to a passive one. Harmonics in this case are decreased to the lower values.

- **Advantages**
  - Power factor ≥ 95.
  - Small system size and power factor value can reach approximately unity.
  - Decreases the harmonics to lower values.
  - Wide range of input voltages.
  - Greater flexibility and control.

- **Disadvantages**
    - Design of this system is more complex than the passive PFC.
    - Higher overall cost [17].

1.9 Basic Circuit Topologies of Active Power Factor Correctors

There are many kinds of topologies of APFC, the typical topologies of APFC are Boost, Buck, Boost-Buck and flyback converters. Boost converter is the most used because it has several advantages against other APFC circuits. Boost and Buck converters have the most basic topology structures among all APFC circuits and other structures are developed from these two structures. Now we simply talk about the features of Boost, Buck, Boost-Buck and flyback converters.

The buck-converter topology in **Fig.1.13** works in a way that it decreases the output voltage compared to the input voltage. Due to the criteria of having an input voltage greater than the output voltage to work properly, this makes the buck-topology a bad choice for a pre-regulator because of the inability to work in the skirts of the half input sine wave having V_{in} less than V_{out}. On the other hand, having a buck converter connected after for example a boost pre-regulatormakes it agreat choice forlowering the" "constantDC voltage or providing a current limiting feature [18].

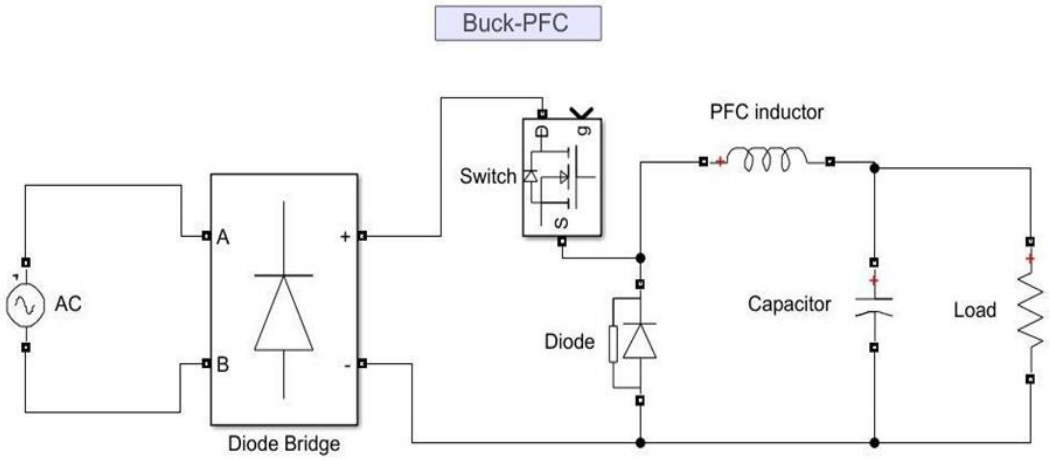


Fig.1.7 *Buck PFC converter circuit*

Compared to the buck converter, the boost converter in **Fig.1.14** boosts the output voltage compared to the input voltage. The Boost-PFC topology is the most used and preferred topology in PFC circuits and one of the reasons to this is the ability to control the input current.Criteria's for makinga boost converter work in a convenient way is that the output voltage is higher than

the input voltage. If the circuit is constructed in such a way that the output voltage exceeds the maximum peak of the input voltage it will be able to work in the full range from zero to max peak value. Due to the ability to work at high power levels and the possibility to use current mode control to program the input current half sine wave, it makes the boost topology a popular choice. If the converter works in Continuous Conduction Mode (CCM), the inductor and input current will always be continuous, helping to reduce input current harmonics. If there is a need to have lower voltage levels it is often popular to have a buck converter connected in series with the boost to make this transformation instead of having a buck right from the start. The only drawback of the boost topology is that it does not have a switch in series between the input and output, therefore it is unable to limit the input current. This means overloads and/or startup currents cannot be controlled. Also, if the input voltage surpasses that of the output voltage the converter is unable to control the current as the diode will be forward biased and the current will flow continuously [19].

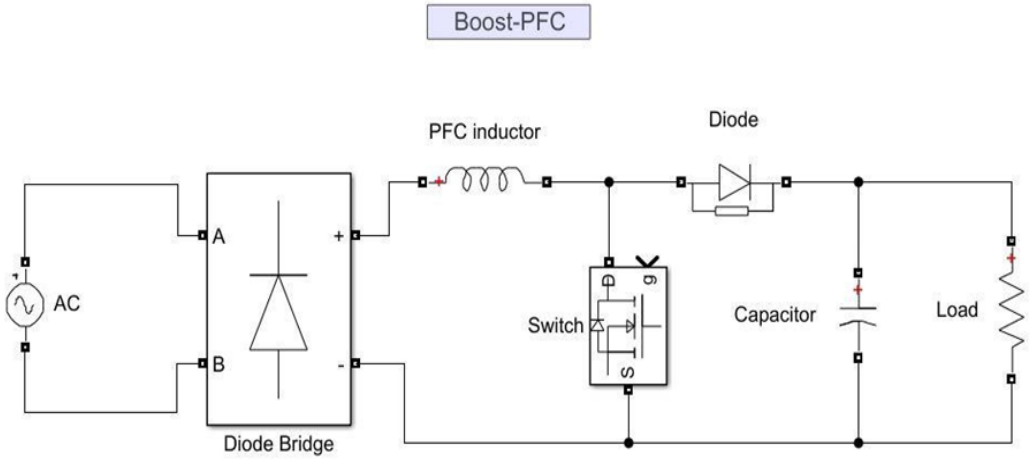


Fig.1.8 *Boost PFC converter circuit*

When it comes to the feature of being able to create either a higher or a lower output voltage compared to the input voltage, there are some different converters that can be used. This can come in handy when there is a special need for the circuit to be able to do both conversions without using two different converters connected in series. Two common converters are the buck/boost converter and the flyback converter. The mentioned features make these topologies viable choices compared to only a buck or boost. The basic concept of the two is the same but they are constructed in two different ways that will be described further down. Examples of simple schematics that are most common for the converters are shown in **Fig.1.15** and **Fig1.16**

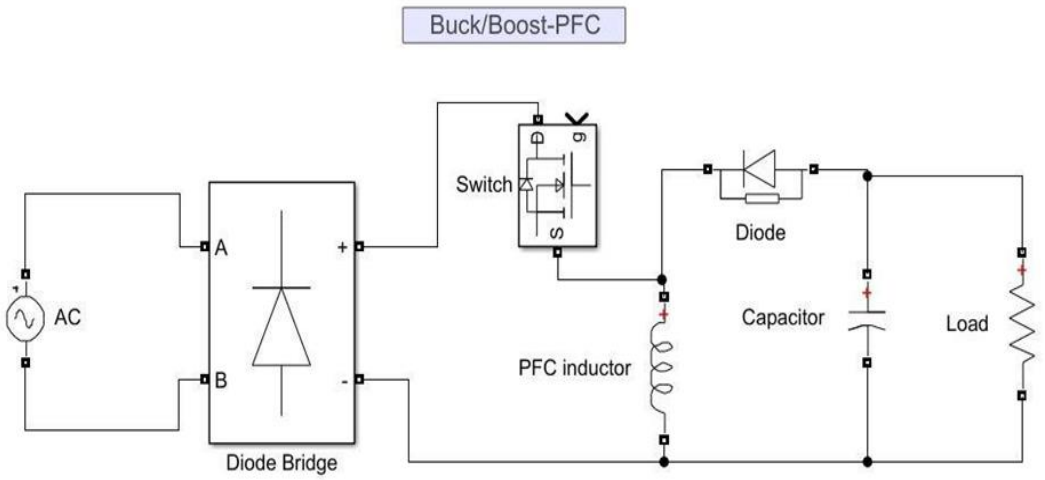


Fig.1.9 *Buck/Boost PFC converter circuit*

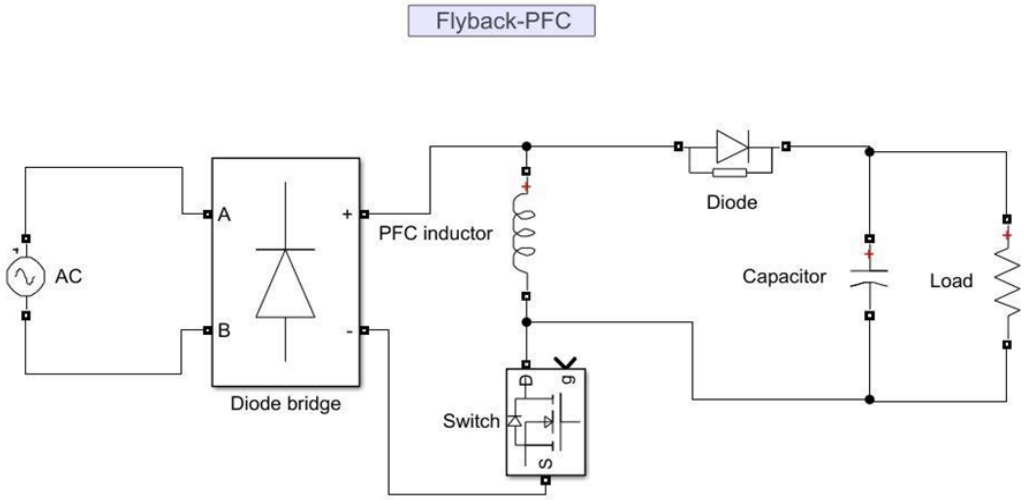


Fig.1.10 *Flyback PFC converter circuit*

Several different approaches are possible when constructing buck/boost and flyback converters. In the buck/boost case, there are versions where two switches are used instead of the conventional single-switch topology, there are also some topologies involving magnetic isolation, i.e. there is a galvanic isolation between the input and output sides. Also, flyback converters have the advantage of having low cost and galvanic isolation of the voltage. It is also able to both regulate the output voltage both up and down as mentioned making it a competitive choice when choosing converter topologies for power factor correction. While working under optimal conditions, flyback converters have high efficiency, and that is when power levels$< 500\ W$. For applications using higher power levels, it is required to use parallel devices. To achieve this, there

is also a need to use the right control algorithms, the optimal controller to drive this circuit is the DSP [20].

The buck, buck/boost and flyback topologies have discontinuous input current due to the fact that there are switches in series with the power line. However, the boost topology can have an input current in both CCM and DCM. The ability to operate in CCM makes the boost-topology the most viable option of the mentioned topologies for high performance power factor correction circuits.

1.10 Conclusion

This chapter surveyed some power quality theories, PFC types and basic circuit topologies of Active Power Factor Correctors briefly.

The next chapter will give an analysis with more details about the system configuration (full wave bridge rectifier, single channel boost converter, two channels interleaved boost converter) and also several control techniques used in APFC, in addition to mathematical modeling (small-signal model) of the interleaved boost PFC.

Chapter II

Modeling and control of active power factor correction

2.1 Introduction

The basic idea of PFC is using power conversion of high frequency switching mode to make the shape of input current close to sinusoidal wave. One of the popular ways is to have a value which is in proportion to the input voltage to be the reference of the current. For this way, we just assume that the harmonic of the input voltage is small and can't affect the control of harmonic current. In most cases, the correction of power factor is achieved by an independent part which is called PFC (power factor corrector). The input of the PFC is usually power grid, and the output is usually a DC voltage. The DC voltage will be the input of DC-DC converter or DC-AC current and provides a stable output for the next converter, making the DC-DC converter or DC-AC converter becomes an optimal design.

This chapter will describe theoretically the main power topology structure of Boost APFC and analyze its control strategy.

2.2 System configuration of Boost APFC

The general block diagram of the proposed system of the boost APFC is as shown in **Fig.2.1**, the system consists of bridge full wave rectifier, boost converter (Two channels interleaved boost converter) and a control block.

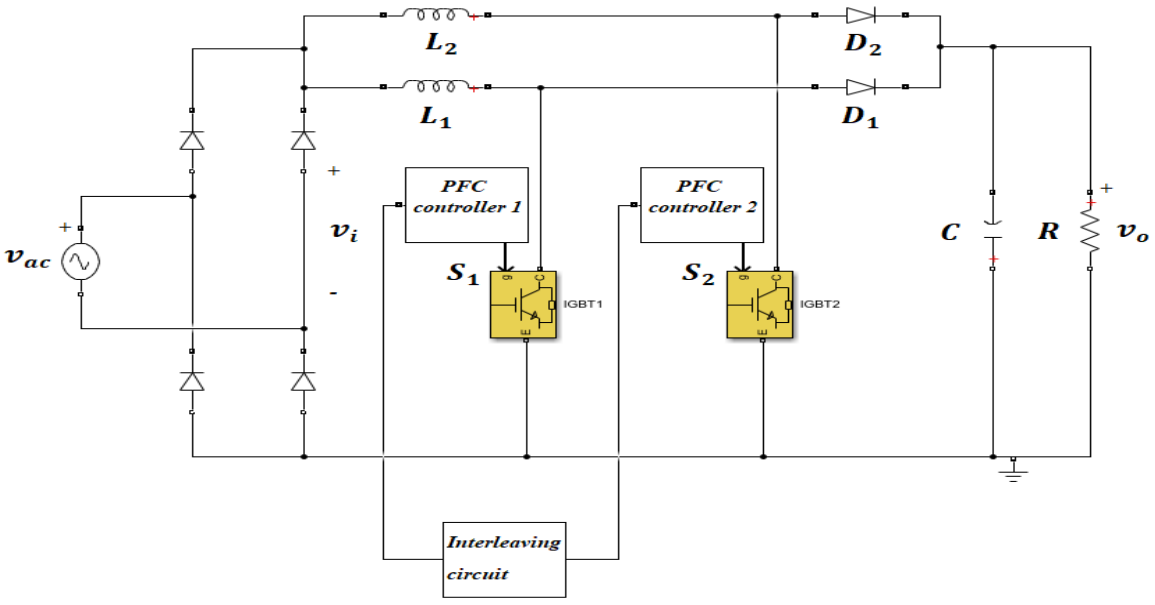


Fig.2.1 *The general block diagram of interleaved APFC*

2.2.1 Single phase full-wave rectifiers

The objective of a full-wave rectifier is to produce a voltage or current that is, purely DC or has some specified dc component, full wave rectifiers have some fundamental advantages. The average current in the AC source is zero in the full-wave rectifier, thus avoiding problems associated with nonzero average source currents, particularly in transformers. The output of the full-wave rectifier has inherently less ripple compared to half-wave rectifier[21].

There are two types of single-phase full-wave rectifier, namely, full-wave rectifiers with center-tapped transformer and full wave bridge rectifier. In this system, full wave bridge rectifier is used. For the bridge rectifier of **Fig.2.2**, Diodes *D1* and *D4* conduct together for positive half wave, and *D2* and *D3* conduct together for negative half wave[21].

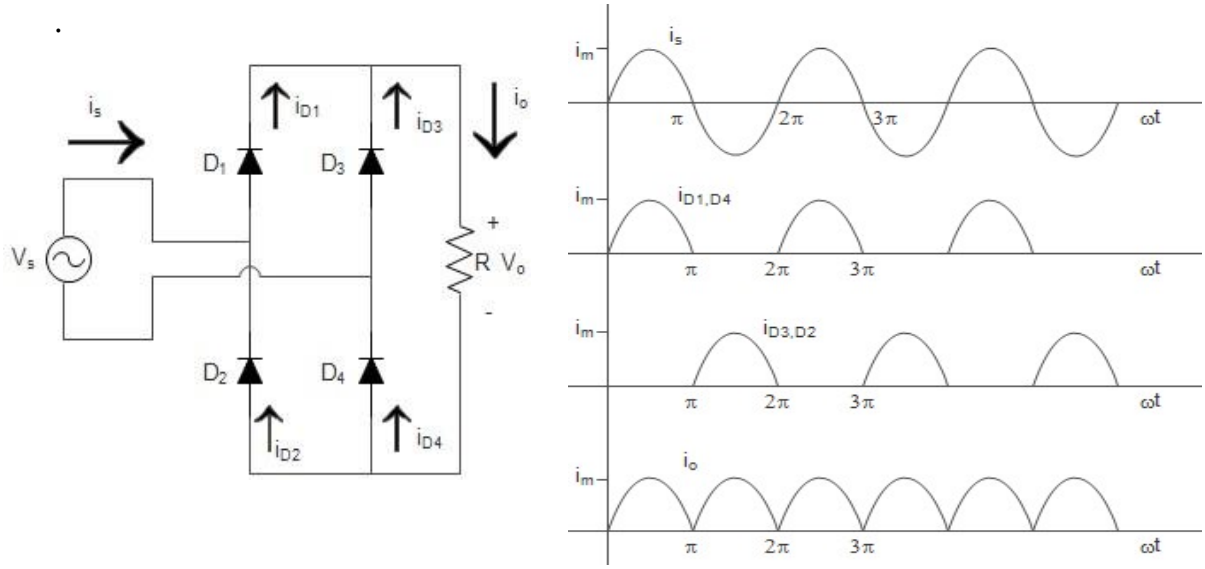


Fig.2.2 *Bridge FWR circuit and its output*

The DC component and rms values of the output voltage and current across a resistive load are:

$$\mathrm{V_{dc}} = \frac{1}{\pi}\int_0^{\pi} \mathrm{Vm}\sin(\omega \mathrm{t})d\omega t$$

$$\mathrm{V_{dc}} = \frac{2Vm}{\pi} \quad (2.1)$$

$$\mathrm{V_{rms}} = \left[\frac{1}{\pi}\int_0^{\pi} [\mathrm{Vm}\sin(\omega \mathrm{t})]^2 d\omega t\right]^{1/2}$$

$$\mathrm{V_{rms}} = \frac{Vm}{\sqrt{2}} \quad (2.2)$$

$$I_{dc} = \frac{V_{dc}}{R} \quad (2.3)$$

$$I_{rms} = \frac{V_{rms}}{R} \quad (2.4)$$

2.2.2 DC-DC Converters

Power electronic converters are essentially required when we need to convert electricity from one form to other. They form an interface between the source and load side.

In the last several years, the massive use of single-phase power converters has increased, that leads to several problems of power quality in electrical systems.

High-frequency active PFC circuits are preferred for power factor correction. Any DC-DC converters can be used for this purpose, if a suitable control method is used to shape its input current or if it has inherent PFC properties.

The DC-DC converters can operate in Continuous Inductor Current Mode – CICM, where the inductor current never reaches zero during one switching cycle or Discontinuous Inductor Current Mode - DICM, where the inductor current is zero during intervals of the switching cycle.

2.2.2.1 Single channel Boost Converter

A boost converter is a power converter with an output *DC* voltage greater than its input *DC* voltage. A typical circuit diagram for the single-channel boost converter is shown in **Fig.2.3**. It is composed of a switch Sw_1, a diode D_1, a *DC* inductor L_1, and a filter capacitor *C*. It is assumed in the following analysis that (1) all the components in the converter are ideal (no power or voltage losses) and (2) the output filter capacitor *C* is very large and the output voltage of the converter is ripple free[22].

When switch Sw_1 is turned on, diode D_1 is reverse biased, and the output is isolated from the input. The input supplies energy to the inductor L_1. When the switch is turned off, diode D_1, is forward biased, and the energy stored in L_1 is released to the load through the diode. In this case, the output voltage v_o is the sum of the input voltage v_i and the inductor voltage v_{L1}, making the converter output voltage v_o higher than its input voltage v_i[22].

Depending on the continuity of the *DC* inductor current i_{L1} the operation of the converter can be divided into two operating modes: continuous-current mode (CCM) and discontinuous-current mode (DCM). When a boost converter operates in CCM, the inductor current i_{L1} never falls to zero. **Fig.2.4** shows the typical waveforms of currents and voltages in the boost converter operating in this mode[22].

In steady-state operation of the converter, the integral of the inductor voltage v_{L1} over time period T_S must be zero. This implies that the average voltage across the inductor L_1 over T_S is zero. Its graphical interpretation is that the area A_1 in **Fig.2.4**[22] must equal area A_2, that is:

$$V_i t_{\text{on}} = (V_o - V_i) t_{\text{off}} \tag{2.5}$$

From which

$$\frac{V_o}{V_i} = \frac{1}{1-D} \text{ for } 0 \leq D < 1 \tag{2.6}$$

Where D is duty cycle of the converter, defined by $D = t_{on} / T_S$, T_S is the switching period; and t_{on} and t_{off} are the turn-on and turn-off times of the switch Sw_1, respectively[22].

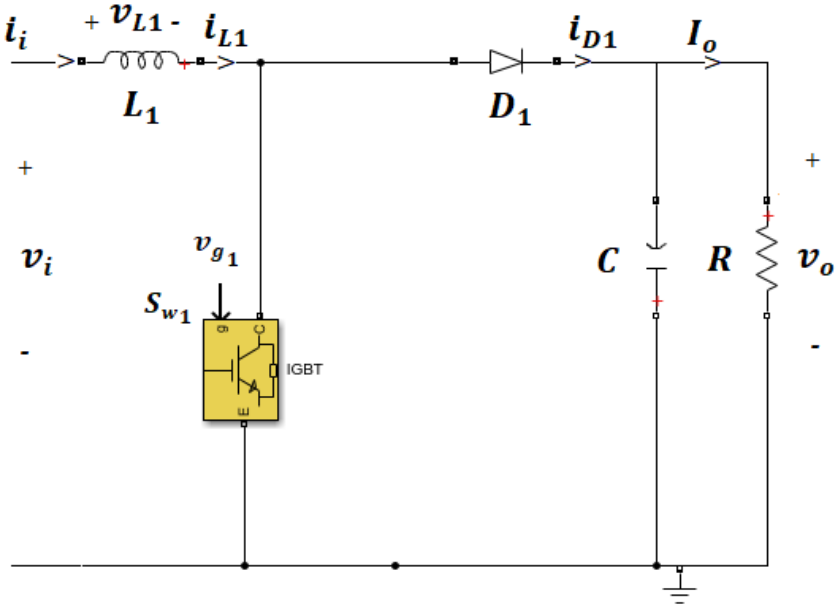


Fig.2.3 *Simplified circuit for single-channel boost converter*

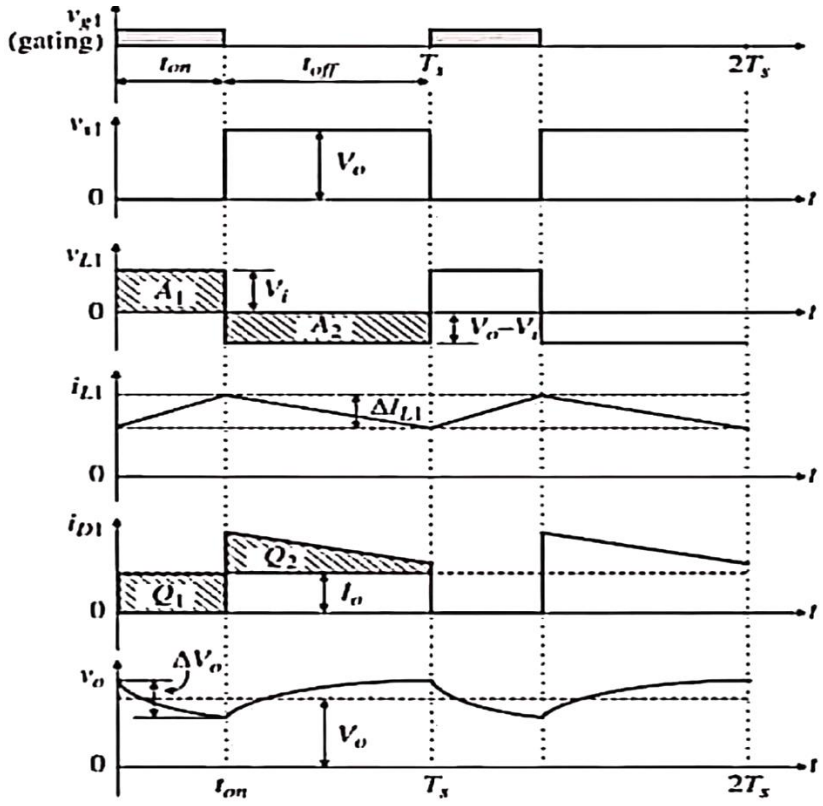


Fig.2.4 *Waveforms of single-boost converter operating in a continuous current mode.*

The above expression indicates that the output voltage of the converter is always higher than its input voltage. The relationship between the converter input current I_i and output current I_o can be derived from $V_i.I_i = V_o.I_o$. from which[22]:

$$\frac{I_o}{I_i} = 1 - D \quad \text{for} \quad 0 \le D < 1 \tag{2.7}$$

To calculate the ripple current in the inductor, differential equation $v_{L1} = L_1(di_{L1}/dt)$ can be replaced by a difference equation $\Delta v_{L1} = L_1(\Delta i_{L1}/\Delta t)$ since the inductor current changes linearly with time. For the t_{off} period in **Fig.2.4** , the inductor ripple current can be expressed by[22]:

$$\Delta i_{L1} = \frac{\Delta v_{L1}}{L_1}\Delta t = \frac{(V_o - V_i)}{L_1} t_{\text{off}} = D(1-D)\frac{V_o T_s}{L_1} \tag{2.8}$$

The maximum current ripple $\Delta I_{L1,max}$ for the single-channel boost converter occurs when the

duty cycle *D* is 0.5[2], at which:

$$\Delta I_{L1,max} = \frac{V_o T_s}{4L_1} \quad (2.9)$$

To calculate the output voltage ripple in the single-channel boost converter, we can look into the waveform of the current i_{D1} in the diode D_1 as shown in **Fig.2.4**[22]. Assuming that all the ripple current component in D_1 is absorbed by the large output capacitor *C*, the capacitor *C* is discharged to the load during the t_{on} period when the diode is turned off, and charged during the t_{off} period when *D1* is on. The amount of charges, *Q1* during ton and *Q2* during t_{off} represented by the shaded areas should be equal[22]. The peak-to-peak ripple voltage can then be calculated by

$$\Delta V_o = \frac{Q_1}{C} = \frac{I_o t_{\text{on}}}{C} = \frac{V_o D T_s}{RC} \quad (2.10)$$

From which:

$$\frac{\Delta V_o}{V} = \frac{DT_s}{RC} \quad (2.11)$$

For a given load resistance *R* and filter capacitor *C*, the ripple voltage ΔV_o increases with the duty cycle D[22].

2.2.2.2 Two-Channel Interleaved Boost Converter

The converter topology for a two-channel interleaved boost converter is shown in **Fig.2.5** [23]. There are two parallel converter channels in the circuit. The first channel is composed of inductor L_1 switch S_{w1} and diode D_1, whereas the second channel consists of L_2, S_2, and D_2. The two converter channels are essentially connected in parallel but operate in an interleaved mode. They share the same filter capacitor *C* at the output. It is assumed that the parameters of the two channels are identical[22].

The gating arrangement and the inductor current waveforms of the converter are shown in **Fig.2.6**[22].With the interleaving design, the gating signals v_{g1} and v_{g2} for Sw_1,

and Sw_2 are identical but shifted by 360°/N = 180°, where N is the number of parallel converter channels. The operation and waveforms of individual converter channels are the same as those for the single-channel converter and, therefore, are not repeated here[22].

Attention should be paid to the total input current i_i which is the sum of the two inductor currents i_{L1} and i_{L2}. The input current i_i has the following characteristics[22]:

- The average DC component of the input current (I_i) is twice that of the individual inductor $(I_i = I_{L1} + I_{L2})$ Since the input and output voltages for the parallel converters are the same, each channel handles only half of the total power of the load[22].
- The peak-to-peak input current ripple ΔI_i is smaller than that in the individual channels due to the use of the interleaved technique. This helps to reduce the volume of the input filter[22].
- The frequency of the input ripple current is twice that of the individual channels. In other words, the equivalent switching frequency of the interleaved converter is twice of that of each channel. For a given output voltage ripple, the capacitance of the output capacitor C can be reduced[22].

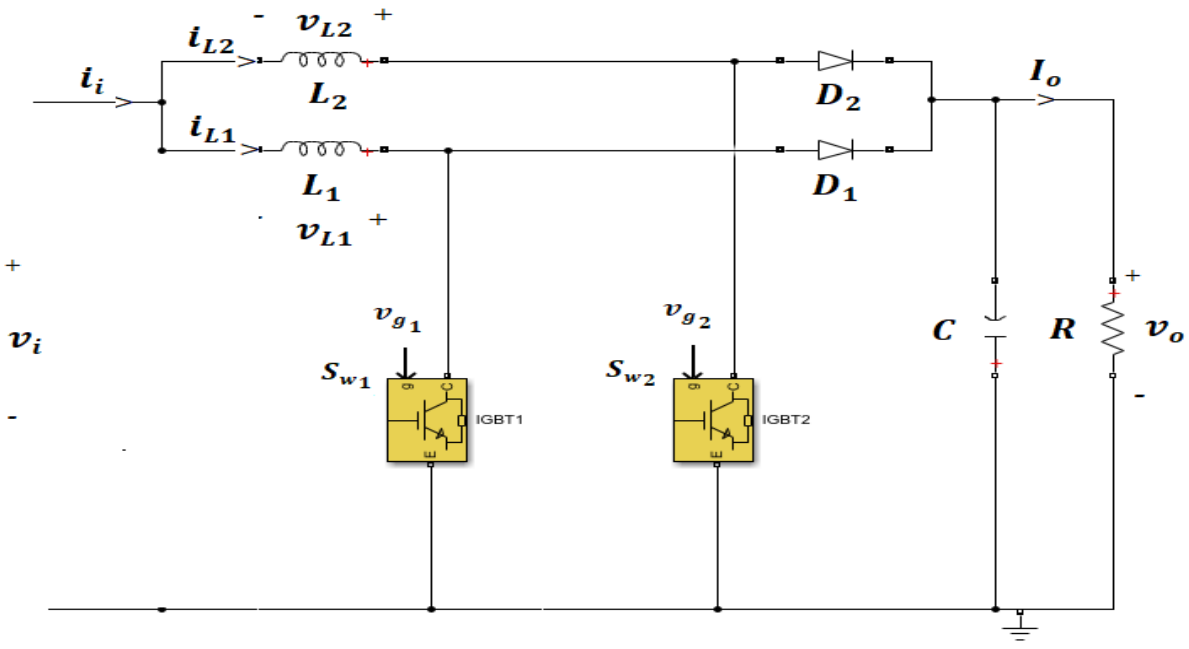


Fig.2.5 *Two-channel interleaved boost converter.*

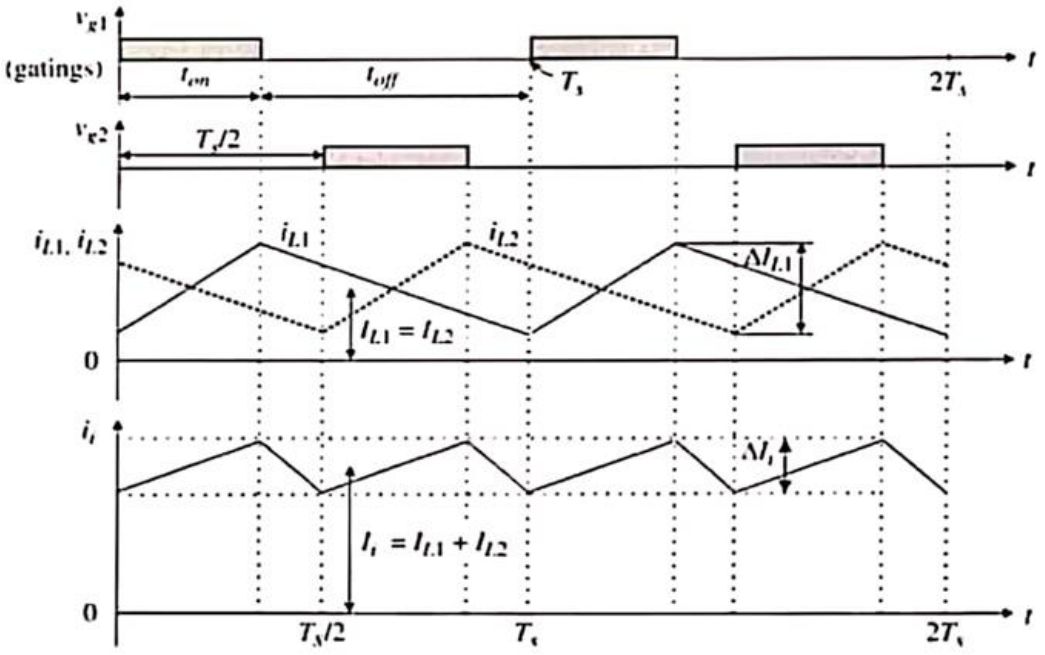


Fig.2.6 *Waveforms for the analysis of input current ripple in a two-channel interleaved converter (D < 0.5)*

Input Current Ripple; It is interesting to note that when the duty cycle *D* increases from about 0.35 in **Fig.2.6** to 0.5, the ripples in the two inductor currents i_{L1} and i_{L2} cancel each other and do not appear in i_i, that is, $\Delta I_i = 0$. The ripple current starts to increase when $D > 0.5$. Therefore, the analysis for the input current ripple can be carried out for the following two cases[22].

- **CASE1:** $0 < D \leq 0.5$ The waveforms in **Fig.2.6** can be utilized to analyze the input current ripple ΔI_i in the two-channel converter. It is more convenient to perform the analysis for the t_{on} period, during which the total input current i_i increases monotonously[22]. The input current ripple of the converter can be calculated by:

$$\Delta I_i = (K_1 - K_2)t_{on} = (K_1 - K_2)DT_s \tag{2.12}$$

Where $K_1 = \frac{di_{L1}}{dt}$ and $K_2 = \frac{di_{L2}}{dt}$, which are the slopes of the inductor currents i_{L1} and i_{L2} during charging and discharging process, respectively. Thus,

$$\Delta I_i = \left(\frac{V_i}{L} - \frac{V_o - V_i}{L}\right)\left(1 - \frac{V_i}{V_o}\right)T_s = (1 - 2D)D\frac{V_o T_s}{L} \quad (2.13)$$

Where L is the inductance of each converter channel, that is, $L = L_1 = L_2$.

The maximum input current ripple $\Delta I_{i,max}$ can be determined by differentiating the above equation with respect to V_i [22]:

$$\frac{\partial \Delta I_i}{\partial V_i} = \left(\frac{2V_i - V_o}{L}\right)\left(1 - \frac{V_i}{V_o}\right)T_s = 0 \quad (2.14)$$

From which

$$V_i = \frac{3}{4}V_o \text{ and } D = 0.25 \text{ for } \Delta I_i = \Delta I_{i,max} \quad (2.15)$$

The maximum current ripple can be found by substituting Equation (2.15) into Equation (2.14):

$$\Delta I_{i,max} = \frac{V_o T_s}{8L} \quad (2.16)$$

Compare the above equation with Equation (2.9) , where the maximum current ripple in the two-channel boost converter is half of the single-channel converter for $D \leq 0.5$.

- **CASE2:** $0.5 < D < 1$. The waveforms for the analysis of the input current ripple in the two-channel converter are shown in **Fig.2.7**, where the duty cycle D is 0.65.

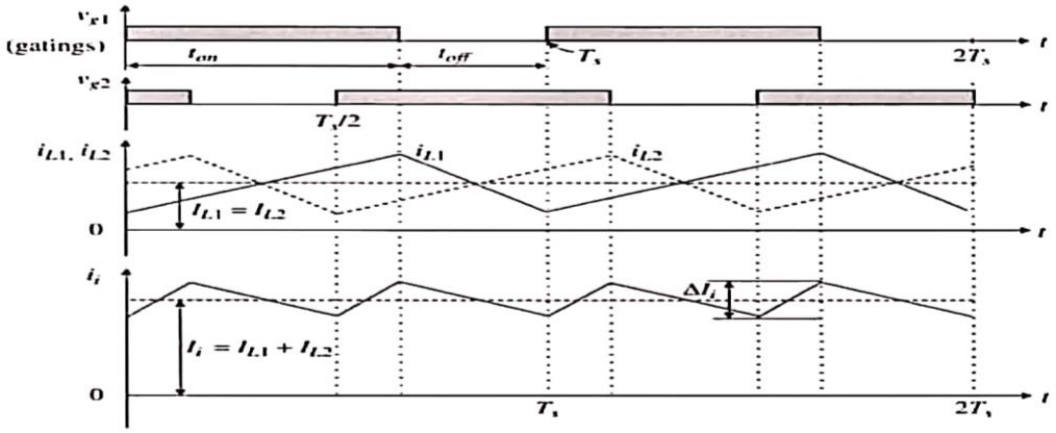


Fig.2.7 *Waveforms for analysis of input ripple current in a two-channel interleaved converter (D > 0.5).*

It is more convenient to perform the analysis for the t_{off} period, during which the input current i_i, decreases monotonously. The input current ripple can be determined by[22]:

$$\Delta I_i = (K_2 - K_1)t_{off} = (K_2 - K_1)(1 - D)T_s$$
$$= \left(\frac{V_o - V_i}{L} - \frac{V_i}{L}\right)\left(\frac{V_i}{V_o}\right)T_s = (2D - 1)(1 - D)\frac{V_o T_s}{L} \quad (2.17)$$

Following the same procedure, the maximum input current ripple ΔIL1.max can be determined, which is the same as that given in Equation (2.16) for the t_{off} period. Input ripple current for the two-channel converter is much lower than that in the single-channel converter[22].

Output Voltage Ripple; One of the benefits of the interleaved converters is the reduction of the output ripple in the two-channel converter, the two parallel converters share the same output capacitor C, which makes the analysis a little tedious. Computer simulation techniques can be used to determine the output voltage ripples. **Fig.2.8** shows the results for the relative output ripple voltage for the two-channel converter under the assumption that the converter operates in a continuous-current mode[23]. The relative output ripple voltage for the single-stage converter is also given in the figure. The two-channel converter produces much lower voltage ripple in comparison to the single-channel converter.

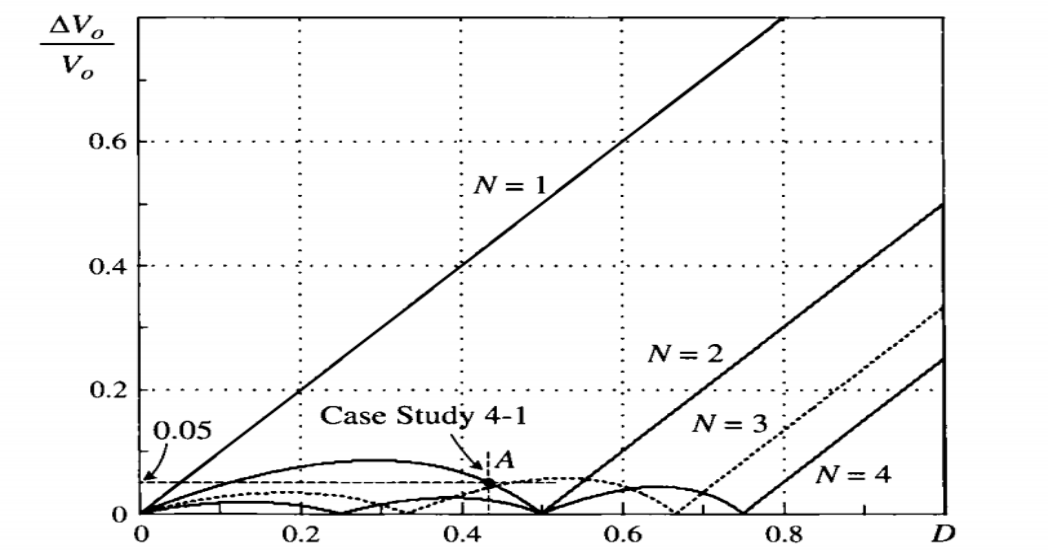


Fig.2.8 *Relative output ripple voltages versus duty cycle D for N channel boost converter*

2.2.3 Typical control strategy of APFC

In practical applications, we have different control strategies for different APFC topologies. No matter what APFC topology we use, in order to achieve PFC, we have to take control of two variables:

- Output voltage, that we have to make sure is stable DC voltage.
- Input current, that we have to make to follow the input voltage at the same frequency and the same phase, and make the input port to be pure resistance.

Therefore, for APFC, usually apply Voltage-Current double-loop feedback control Strategy is applied. In some cases, it will make the PFC circuit more complicated.

Because Boost converter has many advantages, like it is easy to control, and it has continuous input current and small ripple current, it is widely used in industry. So, we take two channels boost converter as an example to analyze the control strategy.

There are two goals we need to achieve for APFC strategy, which are stabling the output voltage and realizing unit input power factor. And there are many different control schemes presented by many scholars to fulfill the different requirements in different circumstance. We can divide APFC into two types according to whether the inductance current is continuous. One is DCM (Discontinuous Conduction Mode) and the other is CCM (Continuous Conduction Mode) and also CRM (Critical Conduction Mode) [24],[25]. In CCM, this system is concerned only with CCM mode. The **Fig.2.9**[26] shows the various APFC control techniques.

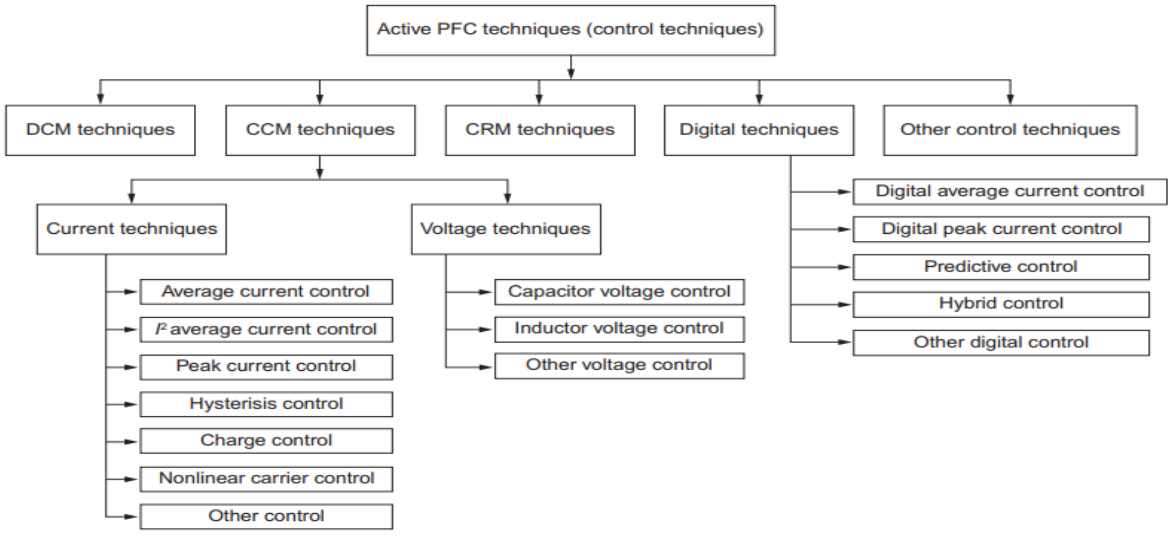


***Fig.2.9** Overview of (APFC) control techniques*

Now a day's average current control method is taken as a standard strategy in the industry for the boost AC-DC PFC converter, since it has merits of less THD with improved noise and easy to shape input current waveform[27],[28],[29],[30].
In this work, average current-mode control for interleaved boost converter is implemented.

2.2.3.1 Average Current Mode Control of Interleaved Boost Converter

Current sharing in paralleled converters can be ensured by adopting current-mode control techniques. Average current-mode control (ACMC) is well established and it has advantages of achieving higher bandwidths when compared to voltage mode control [31]. Average current-mode control is free from instability problems unlike peak current-mode control, which requires slope compensation to make it stable at duty ratio $D > 0.5$. Steady state gain and noise immunity are high in average current-mode control [32].

A detailed analysis on modeling and controller design are presented. The structure of interleaved boost converter with average current-mode control is shown in **Fig.2.10**. Interleaved boost converter consists of two inductors L_1, L_2 as shown in **Fig.2.10** and their average currents I_{L1}, I_{L2} are controlled using two independent current loops, whereas load voltage is regulated using outer voltage loop. Current reference to the two inner current loops is fed by the outer voltage loop. The output voltage v_o of the converter is sensed and fed to an error amplifier, through a voltage sensing element, which has a sensing gain of K_v. The error amplifier calculates the error between the feedback voltage v_{fb} and the reference voltage v_{ref}. This error is fed to the voltage loop compensator and multiplied with a rectified unity sine wave s_{in} to generate a sinusoidal reference current for the inductor currents.

Where

$$s_{in}(t) = \frac{|v_{in}(t)|}{V_{in,peak}} = |sin\, wt| \tag{2.18}$$

This current reference is tracked with the help of two inner current loops. Two independent current loops are required to ensure equal current sharing between the two inductors. Even both the switches in the converter are operated at same duty the average value of inductor currents i_{L1}, i_{L2} may not be equal due to the non-idealities present in the converter. Unequal on-state resistance

of the switches S_{w1} and S_{w2}, unequal forward voltage drops of diodes D_1 and D_2 can cause unequal voltages to be applied across the inductors, which in turn causes inequality in their average currents.

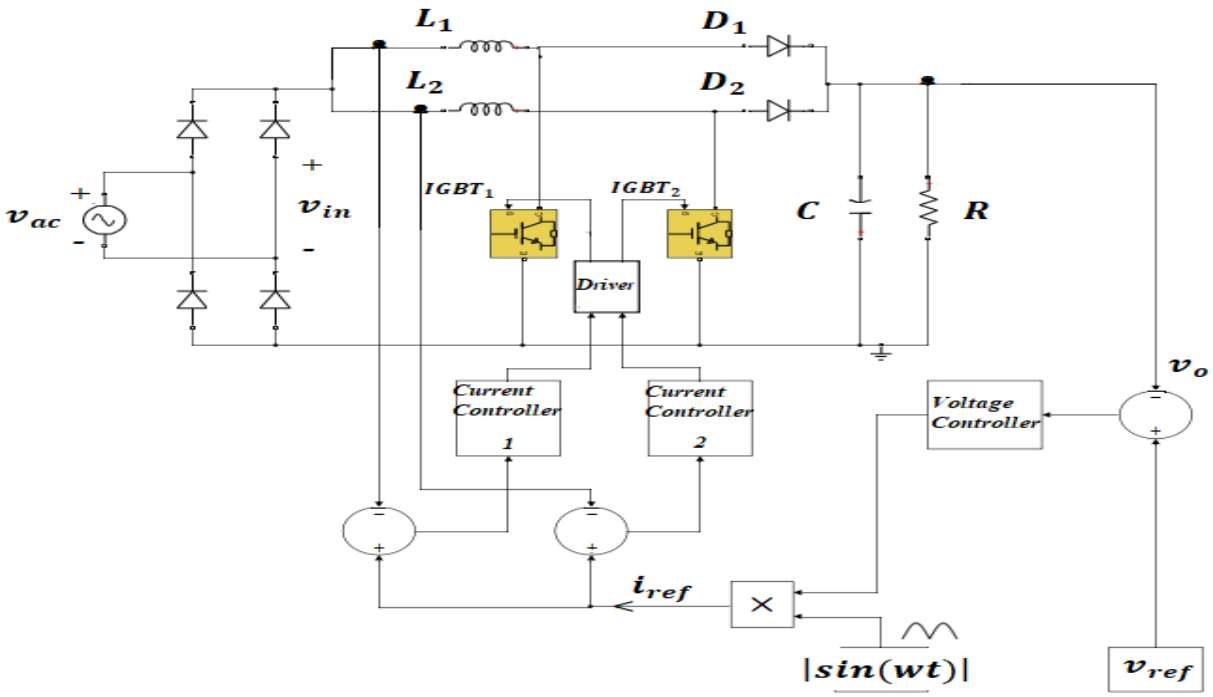


Fig.2.10 *Average current-mode control of interleaved boost converter with two inner current loops and one outer voltage loop*

The average current of each inductor is sensed by a current sensing element and fed to the inner current loops. Here the current sensing gain is denoted as K_{iL1} for the loop consisting inductor L_1 and as K_{iL2} for the loop consisting inductor L_2. Therefore $i_{L1,sen}$ and $i_{L2,sen}$ are the sensed inductor currents. The error between the sensed current and the current reference i_{ref} generated by the outer voltage loop is fed to the current loop compensator. Two current loop compensators H_{iL1}, H_{iL2} are required to control the two inductor currents individually. Output of each compensator is fed to a comparator, which compares it with a ramp signal to generate on-off commands for the switches. The ramp signals which are fed to two different comparators are phase shifted by 180°, so as to generate gate drive signals for the switches Sw_1 and Sw_2 with a 180° phase shift between them.

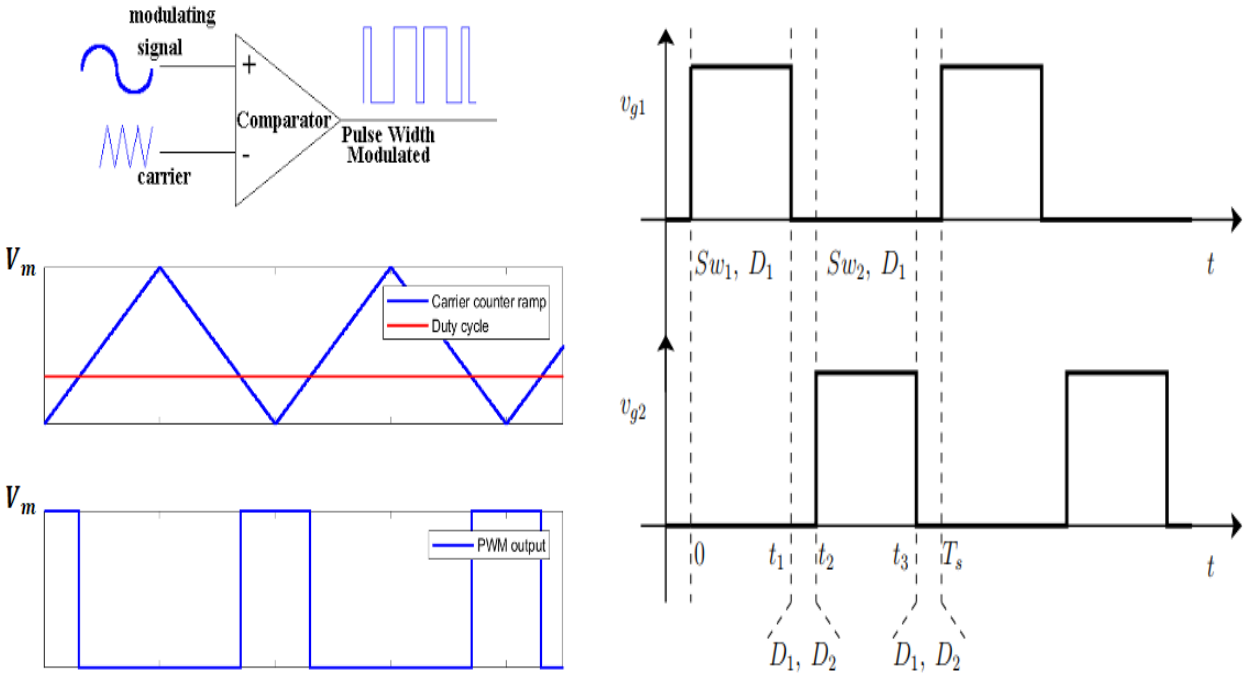
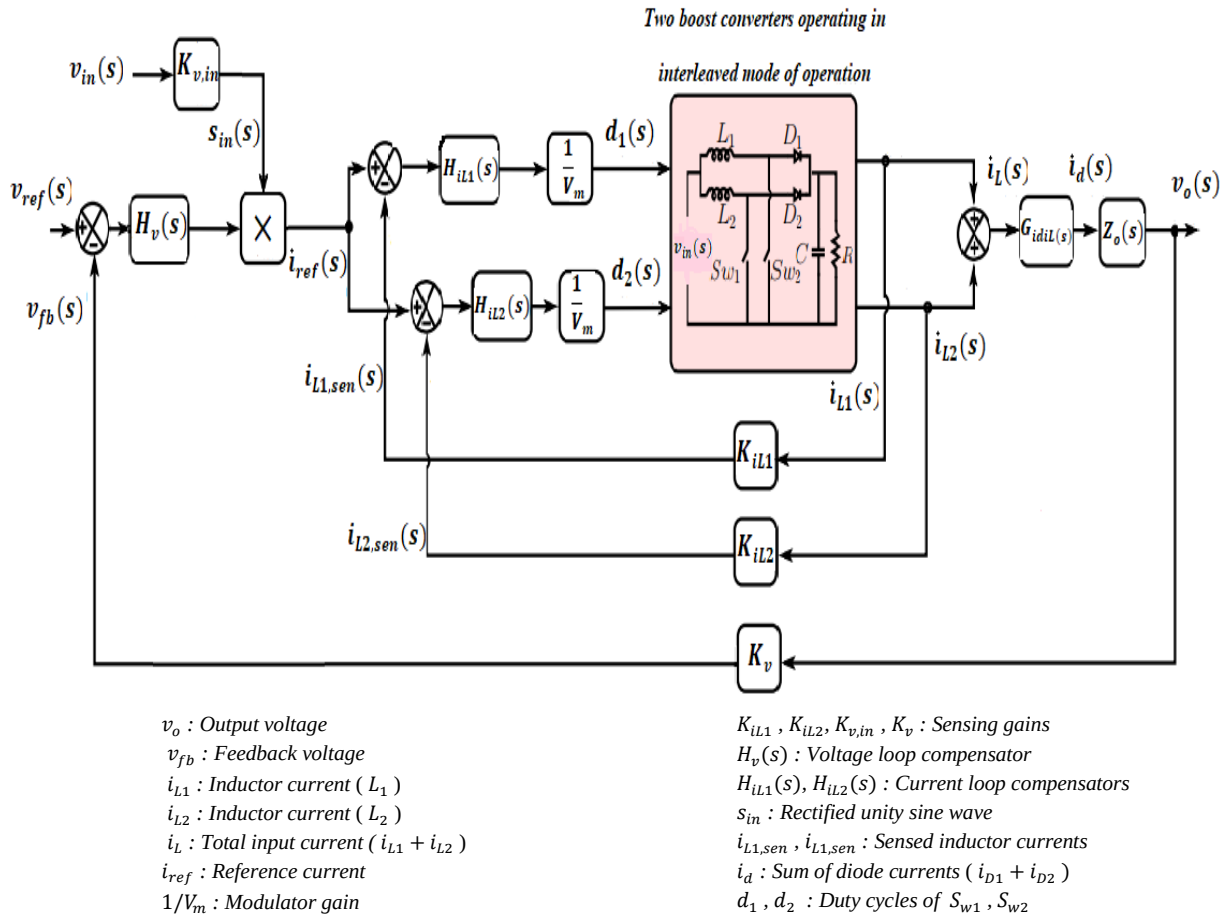


Fig.2.11 *Pulse width modulator and Gating pulse for Sw_1,Sw_2*

2.3 Modeling and control of the proposed system

The steps involved in mathematical modeling of average current-mode controlled interleaved boost converter are explained in this section. State space averaging method is used to obtain small signal model of the converter. The model is derived under the assumption that all the converter elements are ideal. The block diagram representation of average current-mode controlled interleaved boost converter is shown in **Fig.2.12**.



v_o : Output voltage
v_{fb} : Feedback voltage
i_{L1} : Inductor current (L_1)
i_{L2} : Inductor current (L_2)
i_L : Total input current ($i_{L1} + i_{L2}$)
i_{ref} : Reference current
$1/V_m$: Modulator gain

K_{iL1} , K_{iL2}, $K_{v,in}$, K_v : Sensing gains
$H_v(s)$: Voltage loop compensator
$H_{iL1}(s)$, $H_{iL2}(s)$: Current loop compensators
s_{in} : Rectified unity sine wave
$i_{L1,sen}$, $i_{L1,sen}$: Sensed inductor currents
i_d : Sum of diode currents ($i_{D1} + i_{D2}$)
d_1 , d_2 : Duty cycles of S_{w1} , S_{w2}

Fig.2.12 *Block diagram representation of ACMC for interleaved boost converter*

2.4 Open loop power stage transfer functions

Initial step is to model the converter in open loop to derive control to inductor current transfer function, which is used to design the inner current loop compensator. The state space averaging approach is used to model the converter in continuous conduction mode of operation (CCM). The basic steps of state space averaging are writing the state equations of the network and then averaging state vector matrices, this completes the averaging. After the parameters of the converter are perturbed by introducing small ac variations into them and then linearized about a quiescent operating point. This gives the small signal model of the converter.

The state space equation of the converter is given by (2.19)

$$\frac{dx(t)}{dt} = A_n x(t) + B_n u(t) \qquad (2.19)$$

Where x(t) is state vector matrix and is given (2.16), u(t) is the input vector defined as v_{in}(t) and n is the state.

$$x(t) = \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{Co}(t) \end{bmatrix} \tag{2.20}$$

The gating pulses for the switches Sw_1, Sw_2 are shown in **Fig.2.11**. The circuit conditions during turn on condition of the switch Sw_1 and diode D_2 in the interval $0 < t < t_1$, are shown in **Fig.2.13(a)**. The circuit conditions during turn on condition of the switch D_1 and diode D_2 in the interval $t_1 < t < t_2$, are shown in **Fig.2.13(b)**. The circuit conditions during turn on condition of the switch Sw_2 and diode D_1 in the interval $t_2 < t < t_3$, are shown in **Fig. 2.13(c)**. The circuit conditions during turn on condition of the switch D_1 and diode D_2 in the interval $t_3 < t < T_s$, are shown in **Fig.2.13(d).**

The node equation in state 1($t_0 < t < t_1$) can be expressed in the matrix form, is?

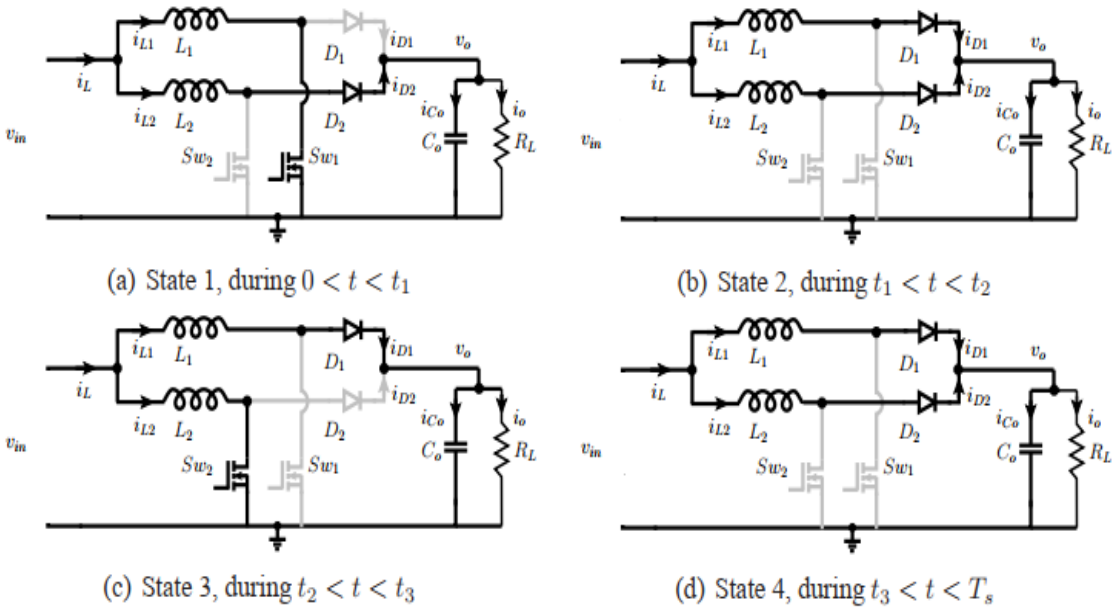


Fig.2.13 *Circuit conditions of interleaved boost converter*

given by equation (2.21).

$$\frac{d}{dt}\begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_o(t) \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{L_2} \\ 0 & \frac{1}{C_o} & -\frac{1}{R_L C_o} \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{Co}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ 0 \end{bmatrix} [v_{in}(t)] \quad (2.21)$$

The node equation in state 2($t_1 < t < t_2$) can be expressed in the matrix form, is given by equation (2.20).

$$\frac{d}{dt}\begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_o(t) \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1}{L_1} \\ 0 & 0 & -\frac{1}{L_2} \\ \frac{1}{C_o} & \frac{1}{C_o} & -\frac{1}{R_L C_o} \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{Co}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ 0 \end{bmatrix} [v_{in}(t)] \quad (2.22)$$

The node equation in state 3(t2 < t < t3) can be expressed in the matrix form, is given by equation (2.23).

$$\frac{d}{dt}\begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_o(t) \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1}{L_1} \\ 0 & 0 & 0 \\ \frac{1}{C_o} & 0 & -\frac{1}{R_L C_o} \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{Co}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ 0 \end{bmatrix} [v_{in}(t)] \quad (2.23)$$

The node equation in state 4(t3 < t < Ts) can be expressed in the matrix form, is given by equation(2.24).

$$\frac{d}{dt}\begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_o(t) \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1}{L_1} \\ 0 & 0 & -\frac{1}{L_2} \\ \frac{1}{C_o} & \frac{1}{C_o} & -\frac{1}{R_L C_o} \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{Co}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ 0 \end{bmatrix} [v_{in}(t)] \quad (2.24)$$

$$A_1 = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{L_2} \\ 0 & \frac{1}{C_o} & -\frac{1}{R_L C_o} \end{bmatrix}; A_2 = A_4 = \begin{bmatrix} 0 & 0 & -\frac{1}{L_1} \\ 0 & 0 & -\frac{1}{L_2} \\ \frac{1}{C_o} & \frac{1}{C_o} & -\frac{1}{R_L C_o} \end{bmatrix}; A_3 = \begin{bmatrix} 0 & 0 & -\frac{1}{L_1} \\ 0 & 0 & 0 \\ \frac{1}{C_o} & 0 & -\frac{1}{R_L C_o} \end{bmatrix} \quad (2.25)$$

$$B_1 = B_2 = B_3 = B_4 = \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ 0 \end{bmatrix} \quad (2.26)$$

The linear small signal dynamic model of the converter can be obtained using the state space averaged theory. By ignoring the second order nonlinear terms the small signal dynamic model of the converter is given by

$$\frac{d\hat{x}(t)}{dt} = \langle A \rangle \hat{x}(t) + \langle B \rangle \hat{u}(t) + \{(A_d)X + (B_d)U\}\hat{d}(t) \quad (2.27)$$

Where $$\langle A \rangle = A_1 D_1 + A_2 D_2 + A_3 D_3 + A_4 D_4 \quad (2.28)$$

$$\langle B \rangle = B_1 D_1 + B_2 D_2 + B_3 D_3 + B_4 D_4 \quad (2.29)$$

$$A_d = A_1 + A_3 - A_2 - A_4 \quad (2.30)$$

$$B_d = B_1 + B_3 - B_2 - B_4 \quad (2.31)$$

For simplified analysis it is assumed that

$$D_1 = D_3; D_2 = D_4$$

Where $D_1 + D_2 + D_3 + D_4 = 1$ and $D' = 1 - D$

Using equations (2.27) and (2.28), the averaged matrices $\langle A \rangle$ and $\langle B \rangle$ are given by

$$\langle A\rangle = \begin{bmatrix} 0 & 0 & -\frac{(1-D)}{L_1} \\ 0 & 0 & -\frac{(1-D)}{L_2} \\ \frac{(1-D)}{C_o} & \frac{(1-D)}{C_o} & -\frac{1}{R_L C_o} \end{bmatrix}; \langle B\rangle = \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ 0 \end{bmatrix} \tag{2.32}$$

Using equations (2.30) and (2.31), the matrices A_d and B_d are given by

$$A_d = \begin{bmatrix} 0 & 0 & -\frac{1}{L_1} \\ 0 & 0 & -\frac{1}{L_2} \\ \frac{1}{C_o} & \frac{1}{C_o} & 0 \end{bmatrix}; B_d = \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix} \tag{2.33}$$

Using the obtained matrices $\langle A\rangle$, $\langle B\rangle$, A_d and B_d, given by (2.32) and (2.33), the vectors in (2.20) are expressed in scalar form as follows:

$$L_1 \frac{d\hat{\imath}_{L1}(t)}{dt} = \hat{v}_g(t) - D'\hat{v}_o(t) + V_o\hat{d}(t) \tag{2.34}$$

$$L_2 \frac{d\hat{\imath}_{L2}(t)}{dt} = \hat{v}_g(t) - D'\hat{v}_o(t) + V_o\hat{d}(t) \tag{2.35}$$

$$C_o \frac{d\hat{v}_{Co}(t)}{dt} = D'[\hat{\imath}_{L1}(t) + \hat{\imath}_{L2}(t)] - \frac{\hat{v}_o(t)}{R_L} - [I_{L1} + I_{L2}]\hat{d}(t) \tag{2.36}$$

Using the equation given by (2.34), (2.35), (2.36) the small signal model of the converter is developed and is shown in the **Fig.2.14**. The duty ratio to total input current transfer

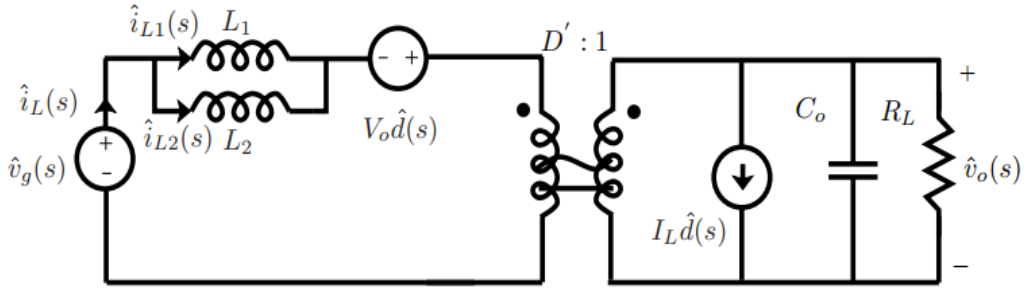


Fig.2.14 *Small signal AC equivalent circuit model of ideal interleaved boost converter*

function is given by

$$G_{i_L d}(s) = \frac{\hat{i_L}(s)}{\hat{d}(s)} = \frac{V_o}{R_L(1-D)^2} \frac{[2+sR_LC_o]}{1+s\frac{(L_1//L_2)}{R_L(1-D)^2}+s^2\frac{(L_1//L_2)C_o}{(1-D)^2}}$$

The combined duty to input current (i_{L1}+i_{L2}) transfer function is obtained as:

$$\hat{i_L}(s)\hat{d}(s) = \frac{\hat{i_{L_1}}(s)+\hat{i_{L_2}}(s)}{\hat{d}(s)};\ \hat{d} = \hat{d}_1 = \hat{d}_2$$

$$= \frac{\hat{i_{L_1}}(s)}{\hat{d}_1(s)} + \frac{\hat{i_{L_2}}(s)}{\hat{d}_2(s)} \quad (2.38)$$

The duty ratio to individual inductor current transfer function is given by equation (2.39)

$$G_{i_{Lx}} dx(s) = \frac{i_{Lx}(s)}{\hat{d}_x(s)} = \frac{V_o}{2R_L(1-D)^2} \frac{[2+sR_LC_o]}{1+s\frac{(L_1//L_2)}{R_L(1-D)^2}+s^2\frac{(L_1//L_2)C_o}{(1-D)^2}} \quad (2.39)$$

The duty ratio to output voltage transfer function is given by

$$G_{v_o d}(s) = \frac{\hat{v_o}(s)}{\hat{d}(s)} = \frac{V_o}{(1-D)} \frac{\left[1-s\frac{(L_1//L_2)}{R_L(1-D)^2}\right]}{1+s\frac{(L_1//L_2)}{R_L(1-D)^2}+s^2\frac{(L_1//L_2)C_o}{(1-D)^2}} \quad (2.40)$$

The total input current to output voltage transfer function is given by

$$G_{v_o i_L}(s) = \frac{\hat{v}_o(s)}{i_L(s)} = \frac{G_{v_o d}(s)}{G_{i_L d}(s)} = \frac{R_L(1-D)\left[1-s\frac{(L_1//L_2)}{R_L(1-D)^2}\right]}{2+sR_LC_o} \quad (2.41)$$

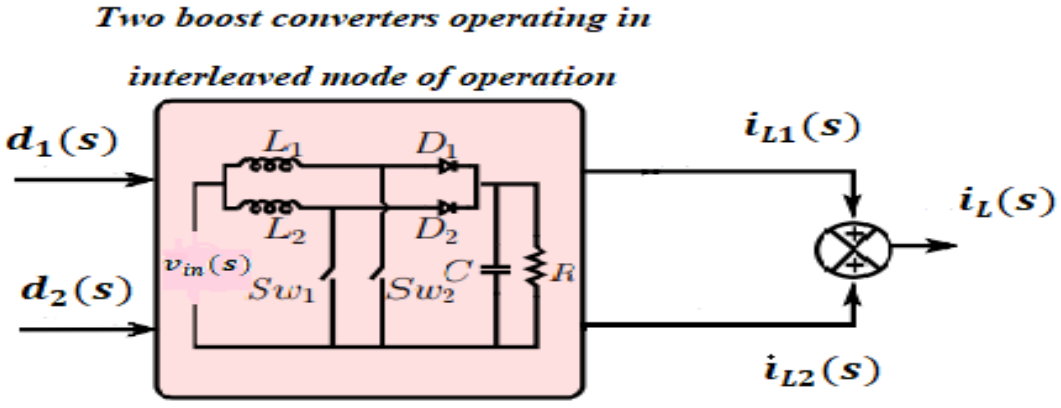


Fig.2.15 *Block diagram representation of interleaved boost converter*

2.2.3.2 Closed current loop transfer functions

The inner current loop block diagram is shown in **Fig. 2.16**. The transfer function of the inner Current loop with the current compensator is given by $\frac{\hat{\imath}_L}{\hat{\imath}_{ref}}$

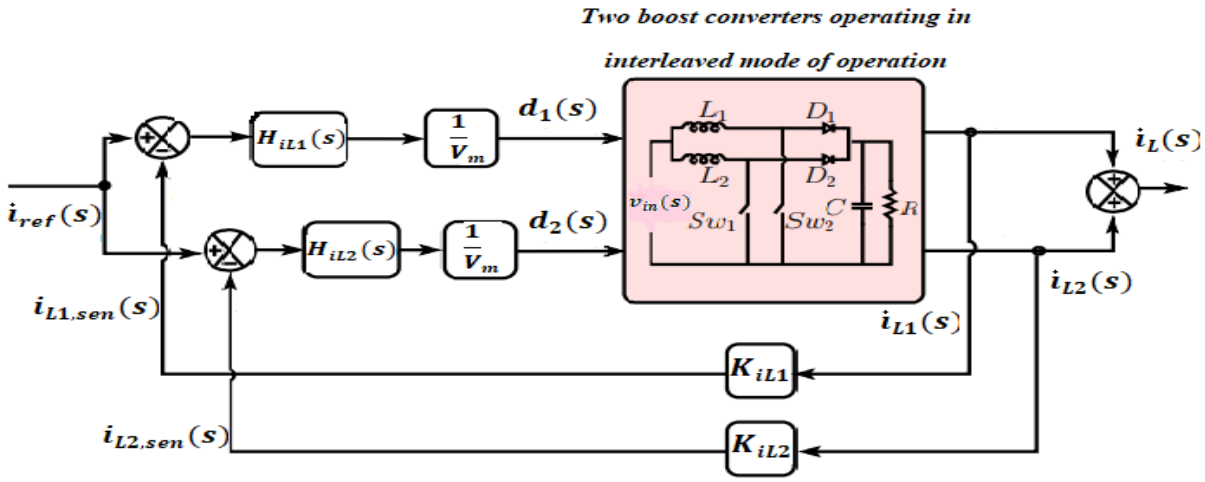


Fig.2.16 *Block diagram representation for The inner current loop of ACMC for interleaved boost converter*

The interleaved boost converter with closed current loop is modeled as $i_{ref}(s)$ to $\widehat{i_L}(s)$. This transfer function can be viewed as sum of individual transfer functions:

$$\frac{\widehat{i_L}(s)}{i_{ref}(s)} = \frac{i_{L1}(s)}{i_{ref}(s)} + \frac{i_{L2}(s)}{i_{ref}(s)} \tag{2.42}$$

Where:

$$\frac{i_{Lx}(s)}{i_{ref}(s)} = \frac{\frac{i_{Lx}(s)}{d_x(s)} \cdot H_{iLx}(s) \cdot \frac{1}{V_m}}{1+\frac{i_L(s)}{d_x(s)} \cdot H_{iLx}(s) \cdot K_{iLx} \cdot \frac{1}{V_m}} = \frac{1}{K_{iLx}} \cdot \frac{T_{iLx}(s)}{1+T_{iLx}(s)} \quad x: 1,2 \tag{2.43}$$

Here

$$\mathrm{T}_{iLx} = \left(\frac{\widehat{iL_1}(s)}{\hat{d}_1(s)} \cdot H_{iLx} \cdot K_{iLx} \cdot \frac{1}{V_m}\right) \tag{2.44}$$

T_{iLx} is individual current loop gain. From (2.17) and (2.25), the result is:

$$\frac{\widehat{\imath_L}(s)}{i_{ref}(s)} = \frac{1}{K_{iLx}} \cdot \frac{2 \cdot T_{iLx}(s)}{1+T_{iLx}(s)} \tag{2.45}$$

2.2.3.3 Closed voltage loop transfer function

For designing the H_v voltage compensator, we should derive $\frac{\widehat{v_o}(s)}{i_{ref}(s)}$:

$$\begin{aligned}\frac{\hat{v}_o(s)}{i_{ref}(s)} &= \frac{\widehat{v_o}(s)}{\widehat{\imath_L}(s)} \cdot \frac{\widehat{\imath_L}(s)}{i_{ref}(s)} \\ &= \frac{\widehat{v_o}(s)}{\widehat{\imath_d}(s)} \cdot \frac{\widehat{\imath_d}(s)}{\widehat{\imath_L}(s)} \cdot \frac{\widehat{\imath_L}(s)}{i_{ref}(s)}\end{aligned} \tag{2.46}$$

Where

$$\frac{\hat{v}_o(s)}{\widehat{\imath_d}(s)} = Z_o = R_o // \frac{1}{SC} = \frac{R}{1+SCR} \tag{2.47}$$

$$\frac{\hat{\imath}_d(s)}{\hat{\imath}_L(s)} = G_{idiL}(s) = (1-D) - \frac{I_L}{\widehat{\imath_L}(s)/\hat{d}(s)} \tag{2.48}$$

To find $G_{idiL}(s)$ in the boost converter the average diode current is given by:

$$\langle I_D \rangle = I_L(1-D) \tag{2.49}$$

Introducing small AC variations

$$\begin{aligned}&(I_D + \hat{\imath}_d) = (I_L + i_L)\left(D' - \hat{d}\right) \\ &\hat{\imath}_d = \hat{\imath}_L(1-D) - I_L\hat{d} \\ &\frac{\hat{\imath}_d}{\hat{\imath}_L} = (1-D) - \frac{I_L}{G_{ild}}\end{aligned} \tag{2.50}$$

Where

$$G_{ild} = \widehat{\imath_L}(s)/\hat{d}(s) \tag{2.51}$$

Therefore

$$\frac{\hat{v}_o(s)}{i_{ref}(s)} = Z_o \cdot G_{idiL}(s) \cdot \frac{\widehat{\imath_L}(s)}{i_{ref}(s)} \tag{2.52}$$

Finally, the total system transfer function $\frac{\hat{v}_o(s)}{v_{ref}(s)}$ with both current loop and voltage loop (as shown in **Fig. 2.12**) can be obtained as:

$$\frac{\hat{v}_o(s)}{v_{ref}(s)} = \frac{\left(\hat{v}_o(s)/i_{ref}(s)\right)\cdot H_v(s)\cdot s_{in}(s)}{1+\left(\hat{v}_o(s)/i_{ref}(s)\right)\cdot H_v(s)\cdot s_{in}(s)\cdot K_v} = \frac{1}{K_v}\cdot\frac{T_v(s)}{1+T_v(s)} \tag{2.53}$$

Where

$\left(\hat{v}_o(s)/i_{ref}(s)\right)$ is given in (2.46), $T_v(s) = \left(\hat{v}_o(s)/i_{ref}(s)\right)\cdot H_v(s)\cdot s_{in}(s)\cdot K_v$ And $s_{in}(s)$ is the Laplace transform of the absolute sine wave in one period, for getting the sinusoidal shape

2.2.3.4 Voltage and current controllers

In order to improve the system performance (avoid the unexpected behaviors), and keep the process variable for voltage loop and current loop close to the desired reference, it is necessary to redesign the system and add controllers (PID, PI).

To achieve optimum control results of inductor currents (i_1 *and* i_2) and the output voltage V_o, we select a three PI controllers structure that is suitable for our controlled system.

2.5 Conclusion

This chapter involves some details about the structure of the interleaved power factor correction. Also, several common APFC main circuit topologies are listed, the average current mode control is introduced with details and analyzed its principle of work.

The two-channel interleaved converter small signal state-space modeling has been provided to derive the system small signal transfer functions. Then, utilizing the transfer functions to study the system and design the suitable controllers.

In the next chapter MATLAB/Simulink software is used to build the system circuits and verify the control method in order to show the results and prove the performance of the system.

Chapter III
Simulation and Results

3.1 Introduction

In order to analyze the behavior of the PFC system, this chapter is divided into three mains parts, the first one shows the circuit behavior without any power factor correction, the second part presents the simulation results for the boost-based PFC, while the last one shows the interleaved boost-based PFC. The models presented are all done using MATLAB Simulink.

The power stage simulation parameters are listed in the **Table.3.1**

The following table show the different characteristics of the implemented system

Table.3.1 *The power stage simulation parameters*

Input Voltage	V_i =220V
PFC Output Voltage	V_O =360V
PFC Output Power	P_o =10.368KW
PFC Switching Frequency	F_s =10KHz
Output Filtering Capacitor	C =5Mf
Boost Inductor	L =0.56mh
Interleaved Boost Inductors	L_1 =0.25mH ; L_2 =0.25mH
Load Resistor	R =12.5Ω

3.2 Simulation and results for a single-phase diode rectifier

The MATLAB-Simulink model of single phase diode rectifier with filter capacitor is shown in **Fig.3.1**

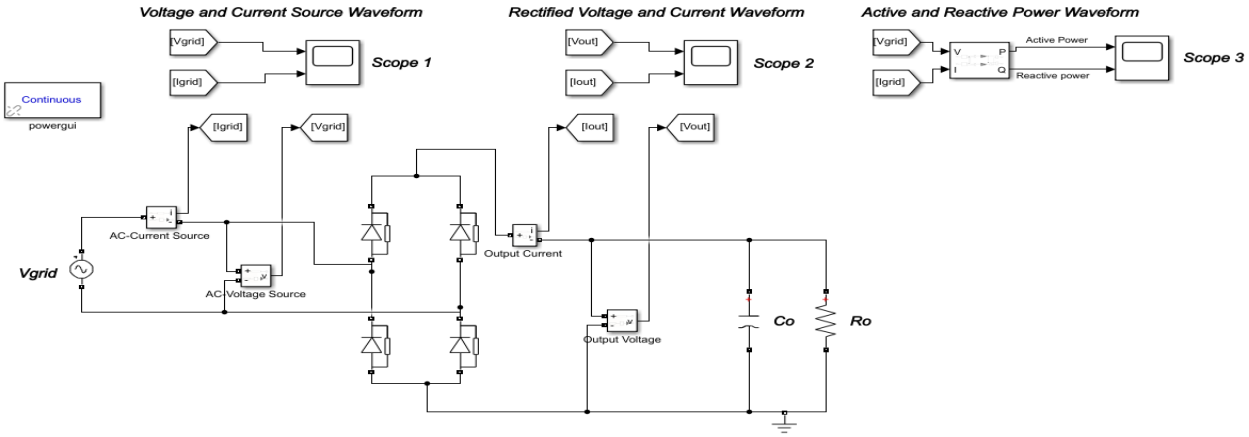


Fig.3.1 *Simulation diagram of single phase diode rectifier*

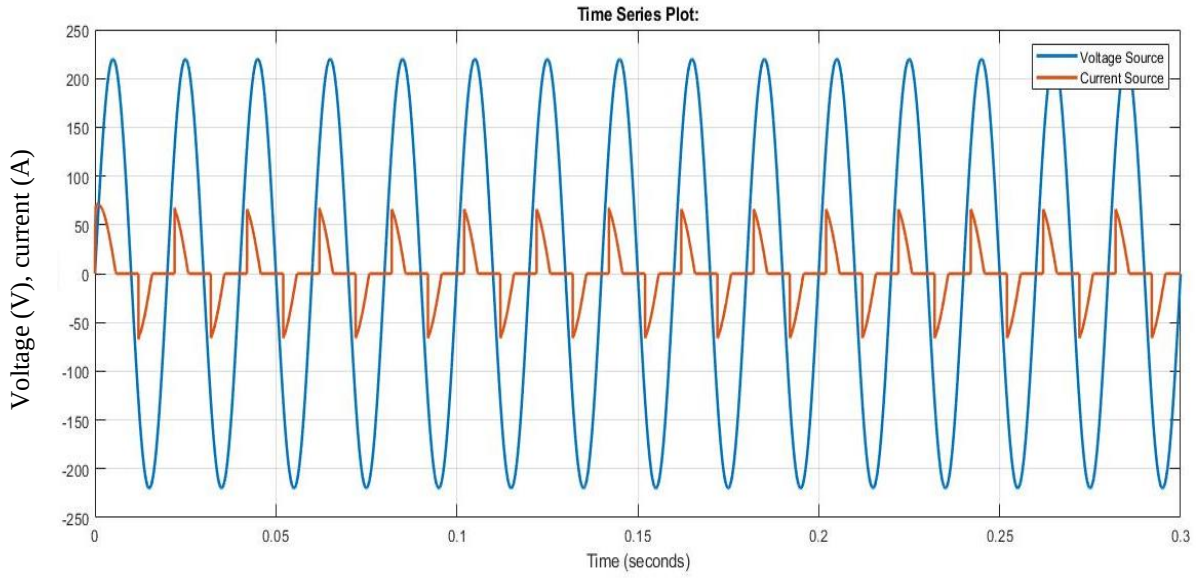


Fig.3.2 *Voltage source and current source waveform*

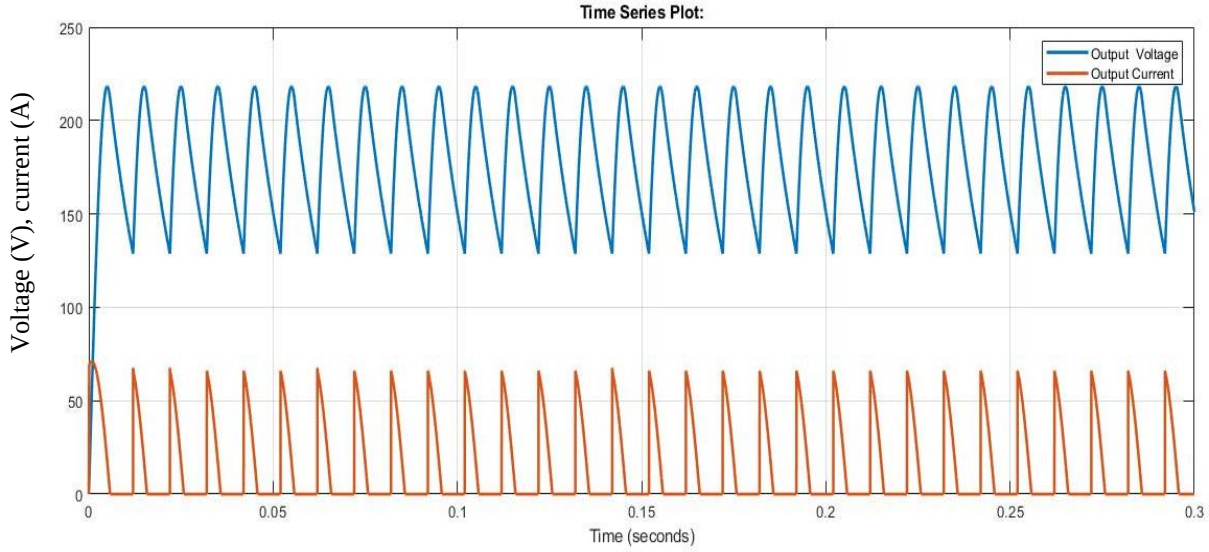


Fig.3.3 *Output voltage and output current waveform*

From **Fig.3.2**, it can be seen that the current source is discontinuous and pulsating. As a result, the power factor is poor. Moreover, the output voltage and current are depicted in **Fig.3.3,** where the high voltage ripple is so clear.

To decrease the ripple voltage and make the output voltage more smooth DC, a huge capacitor is needed, when the capacitor, C_o is increasing than the output voltages, *Vo* are becoming more pure DC but input current is distorting due to harmonics generated by the filter capacitor, C_o

That leads to a poor power factor and a high percentage of THD in the input current.

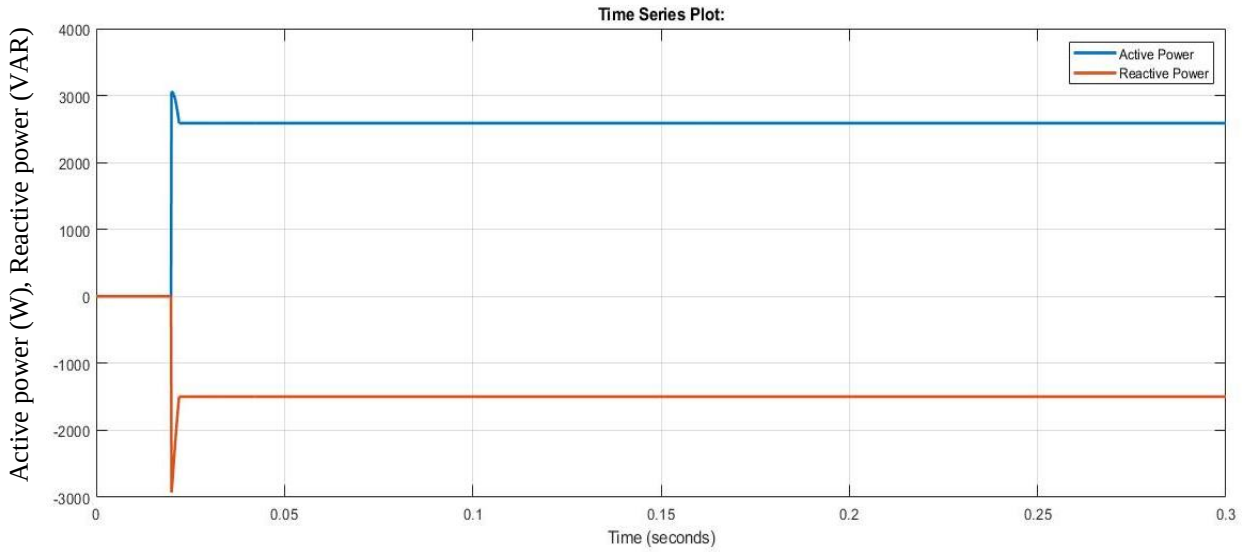


Fig.3.4 *Active and reactive power waveform*

Fig.3.4 below shows the active and reactive powers. The active power and reactive power are respectively obtained: P=**2589**W and Q=**-1489** VAR, therefore, the power factor is **0.86555596.**

The THD and the FFT spectrum of the current source is shown in **Fig 3.5.**

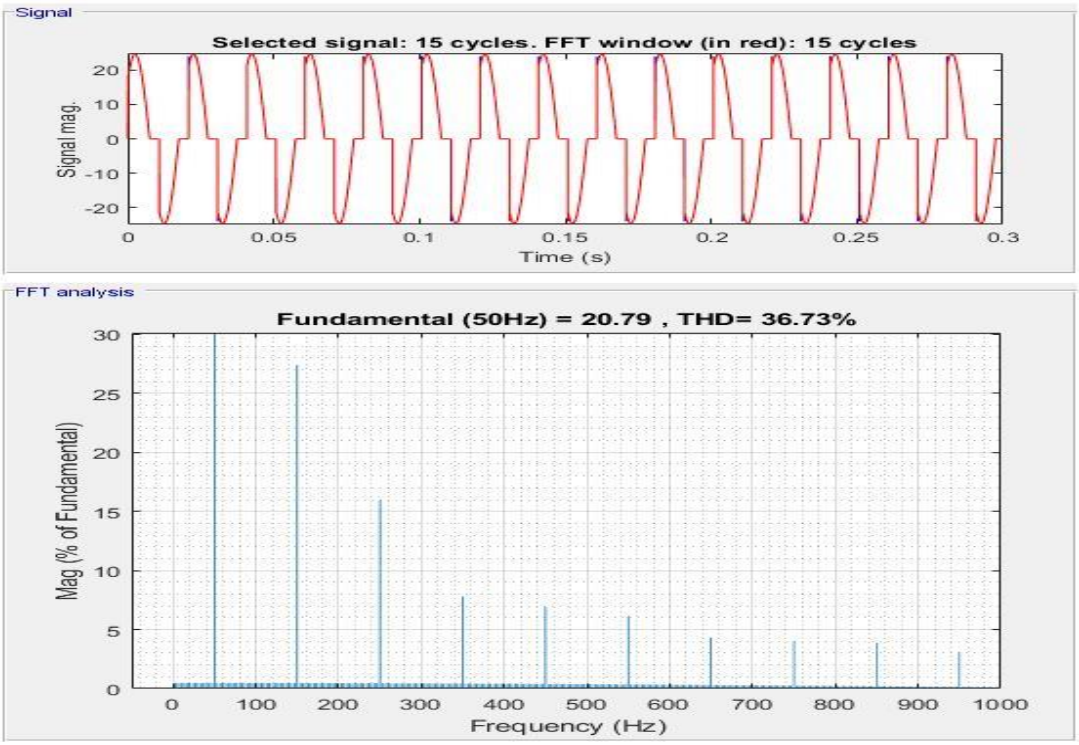


Fig.3.5 *THD of the input current of single phase rectifier*

It can be seen form **Fig.3.5** that the THD is very high (36.37%).

It can be deduced that the bridge rectifier the simplest form of AC to DC conversion, but the resulting current is discontinuous and pulsating, as shown in **Fig.3.2**, causing a high THD of about 36.37%which has an impact over the power factor (PF=0.865). Moreover, the ripple content of the output voltage is significantly high where it is found to be 85V peak to peak, shown in **Fig.3.3**, which means that power dissipation is very high due to the phase between input current and input voltage.

To overcome these problems, we use the single-phase boost PFC as shown in the following part.

3.3 Simulation and results for Boost Converter with PFC

The PFC boost converter was simulated in Simulink with a dynamic model to represent the dynamics of the boost PFC converter, specifically, to simulate the current shaping properties of this topology. The model was developed with the following assumptions and objectives.

- **Assumptions:**
  - The input voltage is a perfect sine wave which is held constant, meaning no sudden changes in amplitude or frequency. Only the fundamental of the voltage is included, so no harmonics exist at the voltage.
  - The system is assumed to be operating in steady state; thus, startup is not considered.
- **Objectives:**
  - The input inductor current shall follow the shape of the scaled rectified input voltage while having appropriate amplitude to keep the output voltage at the correct level.
  - Feed forward of the input voltage is not considered as this is more of a phenomenon during transients.
  - The output DC voltage shall be controlled to match the reference.

3.2.1 Boost PFC Simulation Results

The MATLAB-Simulink model using boost converter is shown in **Fig.3.6**

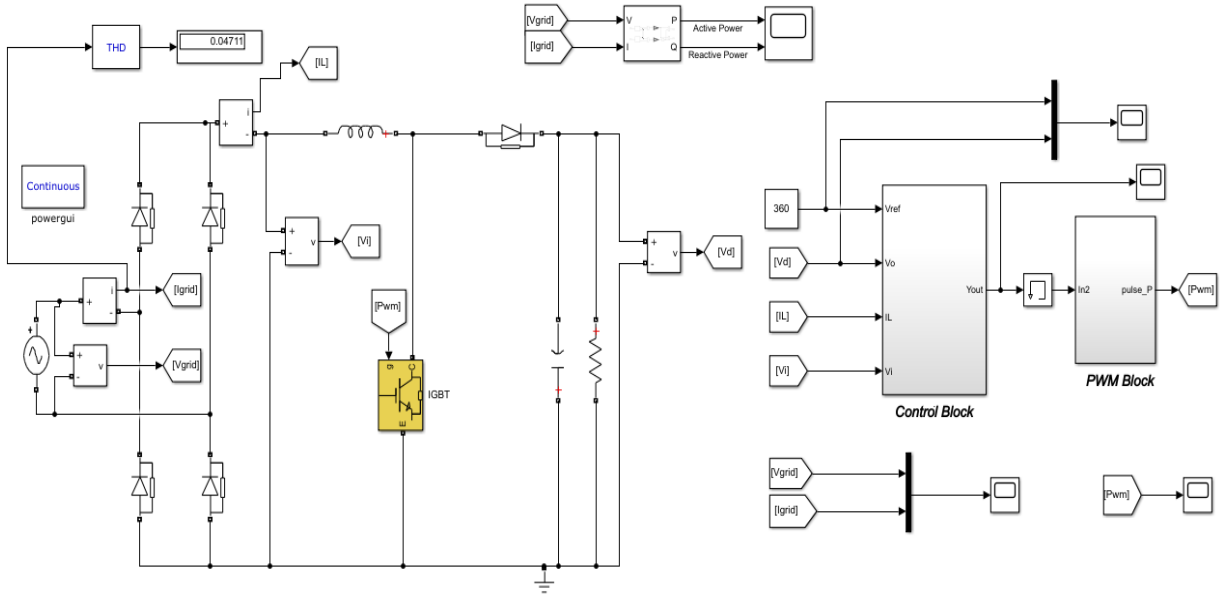


Fig.3.6 *Simulation diagram using boost converter*

The output voltage waveform is first shown in **Fig.3.7** to see whether the voltage follows the reference or not.

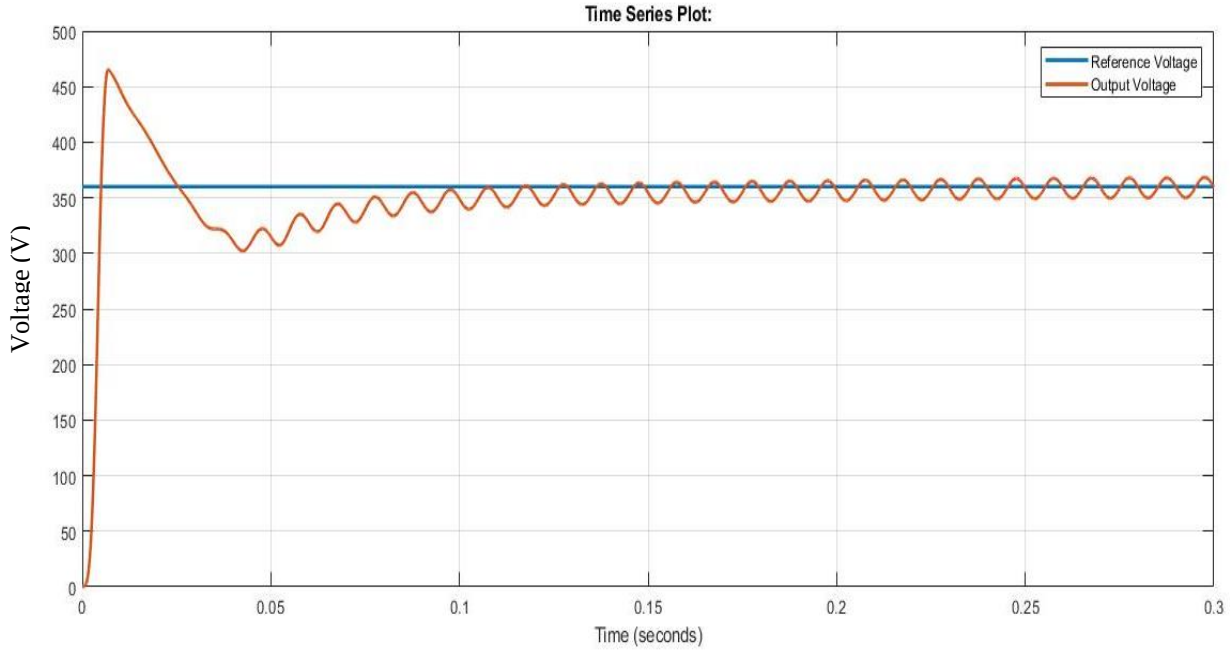


Fig.3.7 *Output voltage and reference voltage waveform*

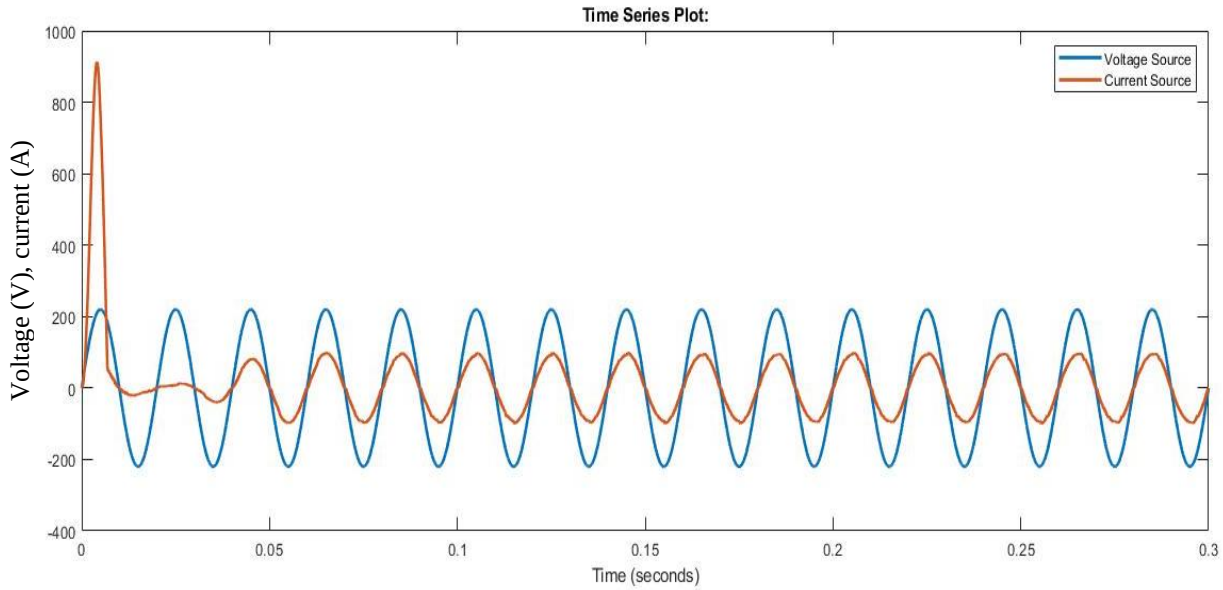


Fig.3.8 *Voltage source and current source waveform*

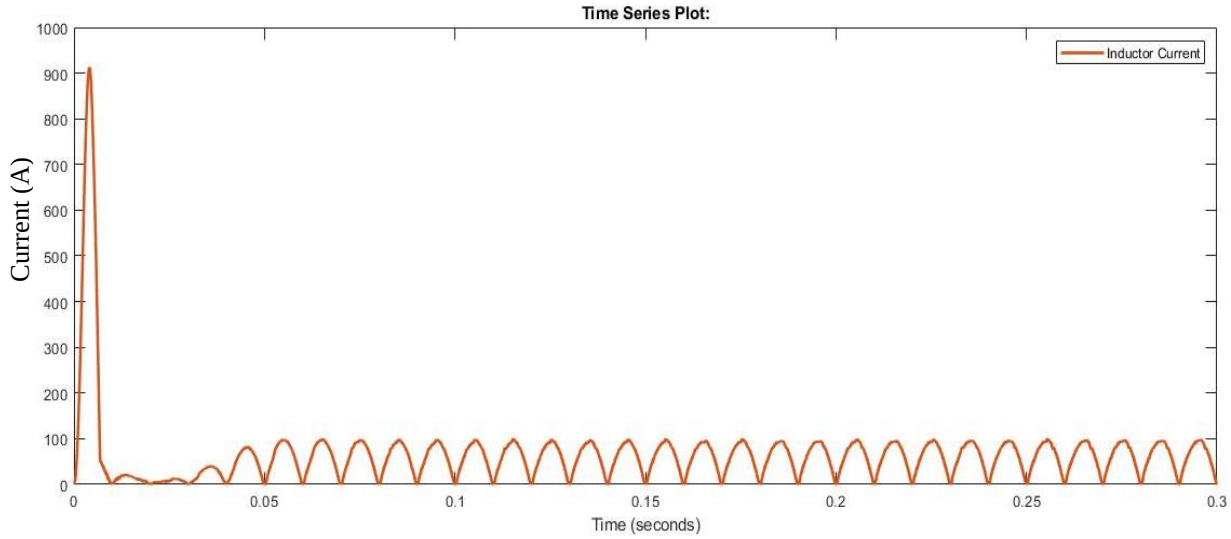


Fig.3.9 *Inductor current waveform*

As we can see from **Fig.3.8** input AC current is almost sinusoidal as the input AC voltage but there is fair amount of ripple is present in the input current.

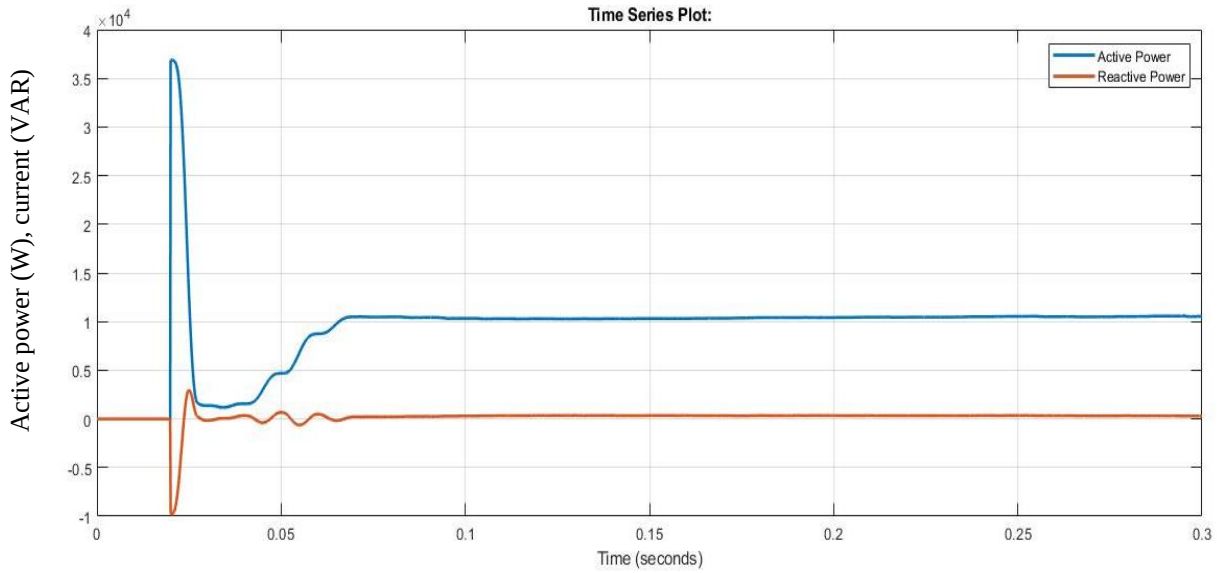


Fig.3.10 *Active and reactive power waveform*

From the above figure:

- Active power = **10203** W
- Reactive power =**560** VAR

So the power factor is **0.9985.**

The THD of input current is shown in the **Fig.3.11**

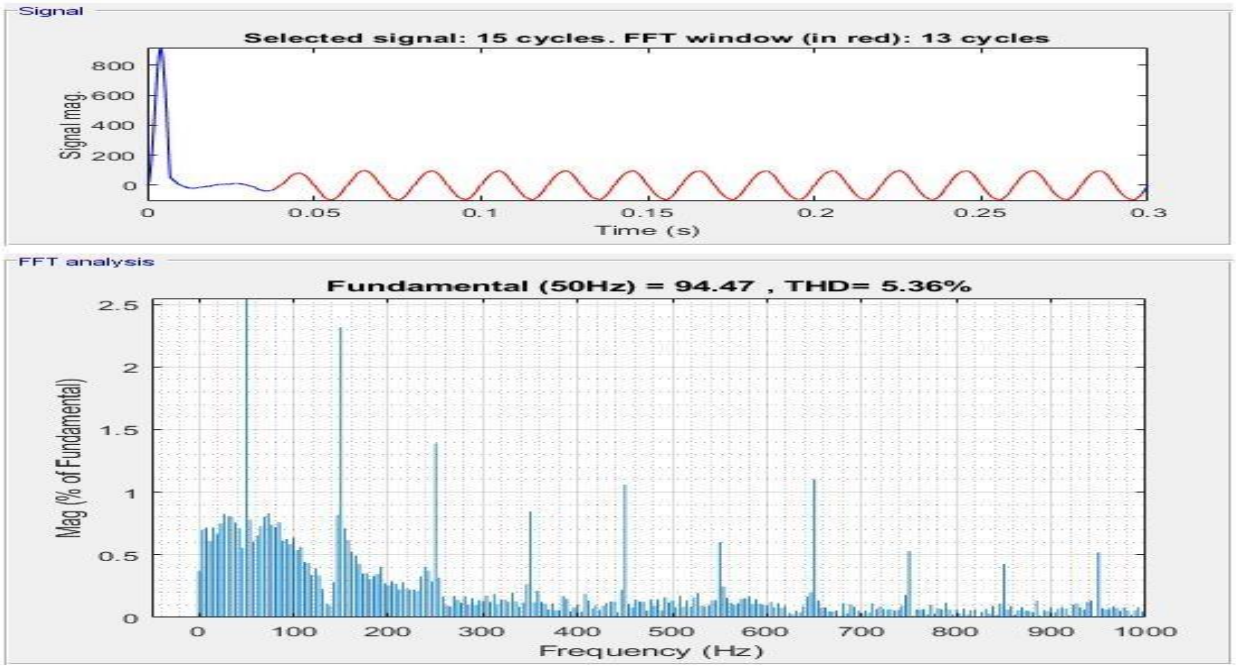


Fig.3.11 *THD of input current*

To ameliorate the THD and the power factor and minimize the ripple of the current source we use a two channel interleaved boost converter instead of one channel boost converter.

3.2.2 Interleaved Boost PFC Simulation Results:

The MATLAB Simulink model of interleaved boost PFC converter average current mode control by PI controller is shown in **Fig.3.12.**

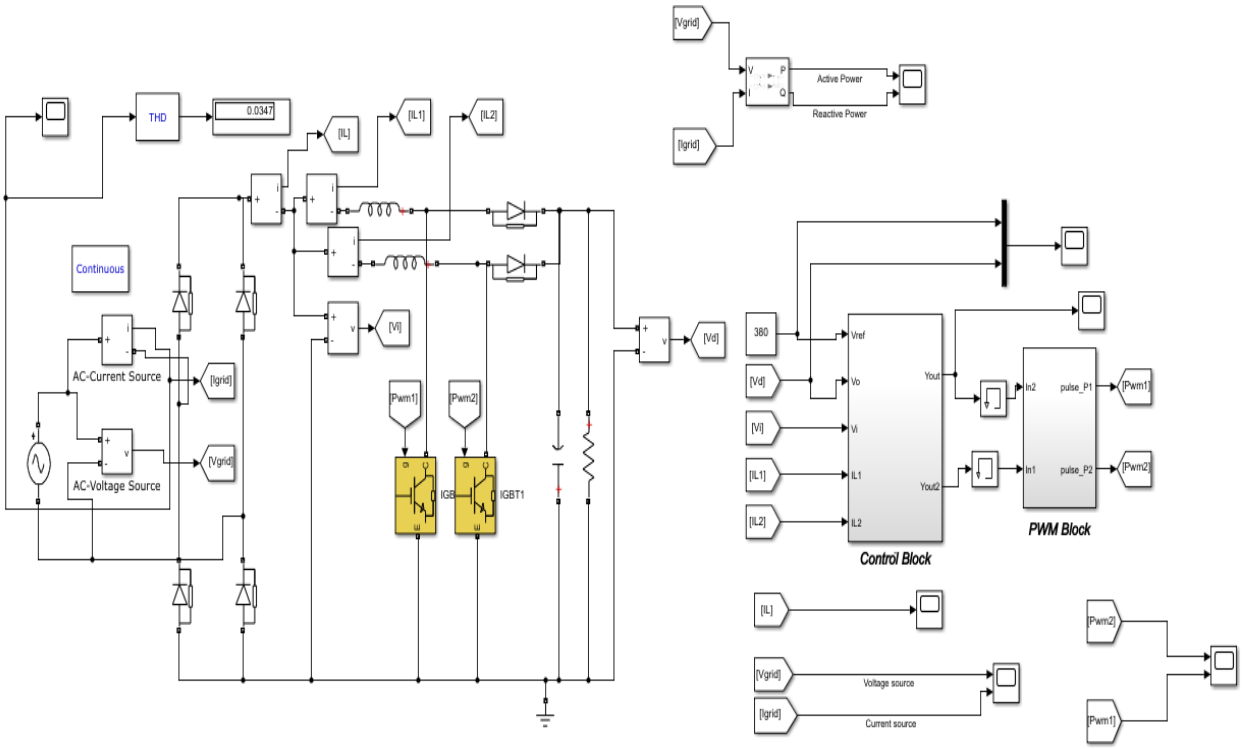


Fig.3.12 *Simulink model of interleaved boost converter*

The output voltage waveform is first shown in **Fig.3.13** to see whether the voltage follows the reference or not.

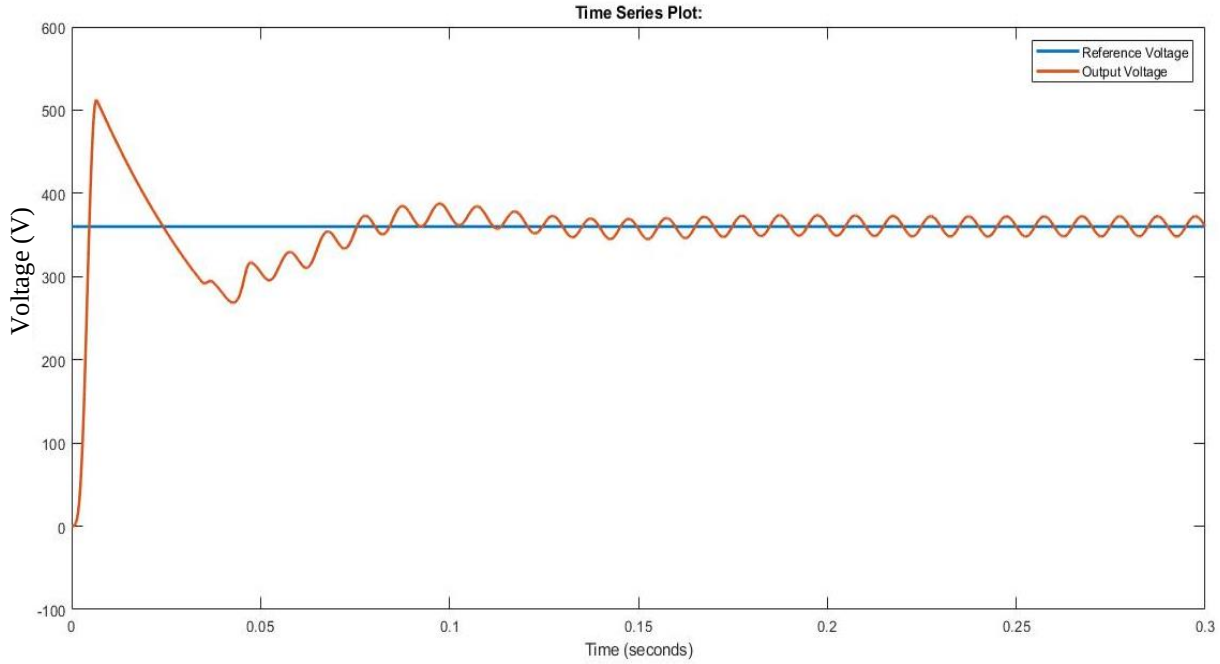


Fig.3.13 *Output voltage and reference voltage waveform*

As we can see from **Fig.3.14** input AC current is sinusoidal as the input AC voltage and there is no ripple is presented in the current source.

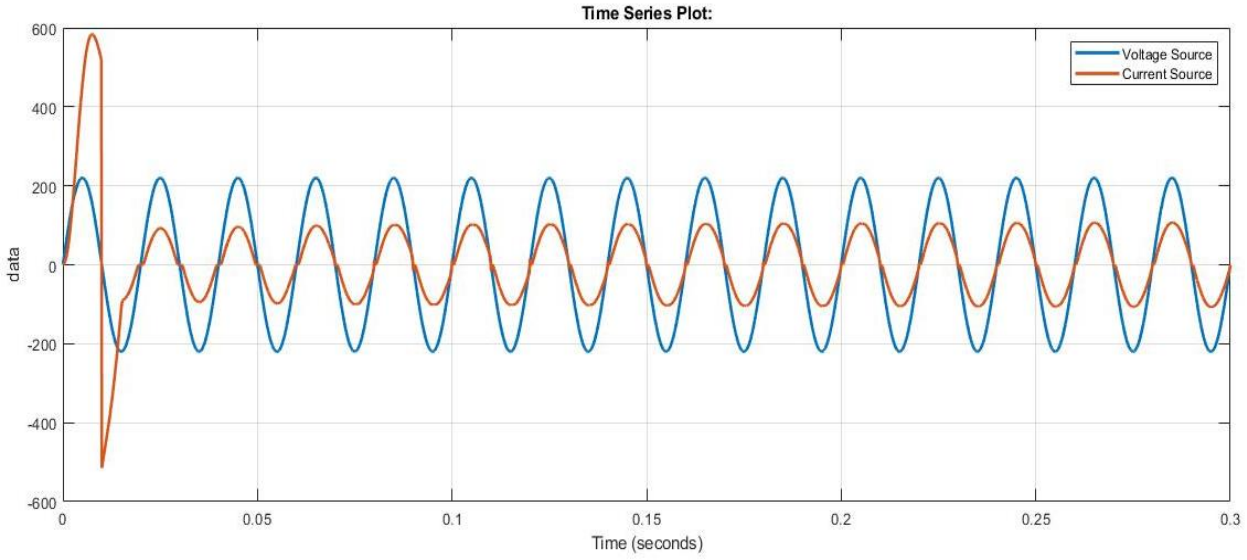


Fig.3.14 *Voltage source and current source waveform*

The total inductor current and the inductor currents I_{L1}, I_{L2} waveform as shown in the following figures.

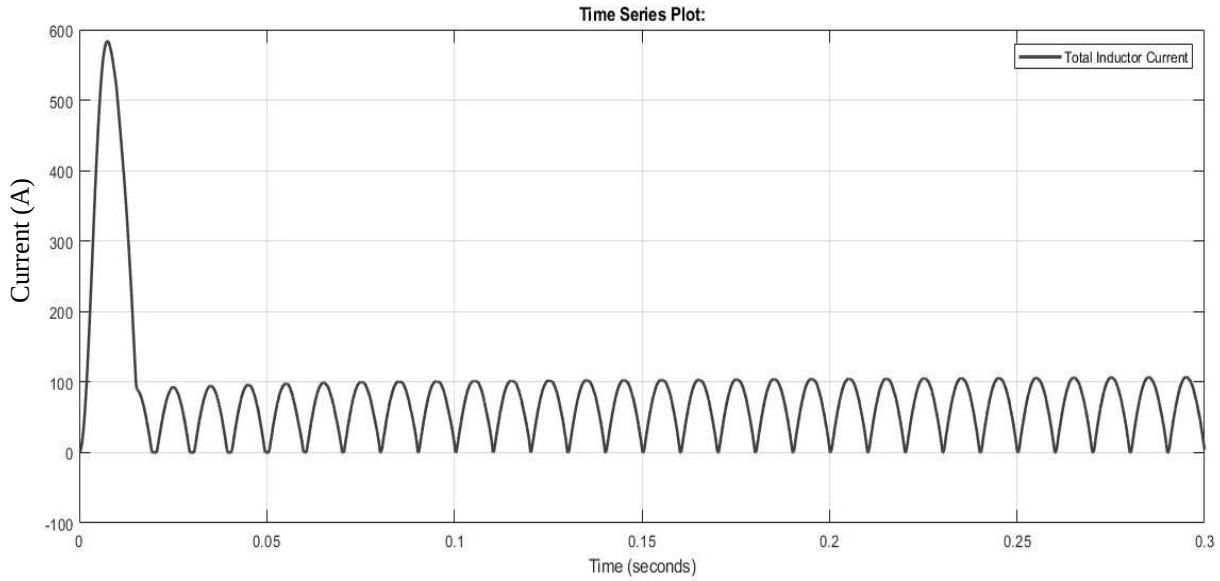


Fig.3.15 *Total inductor current waveform*

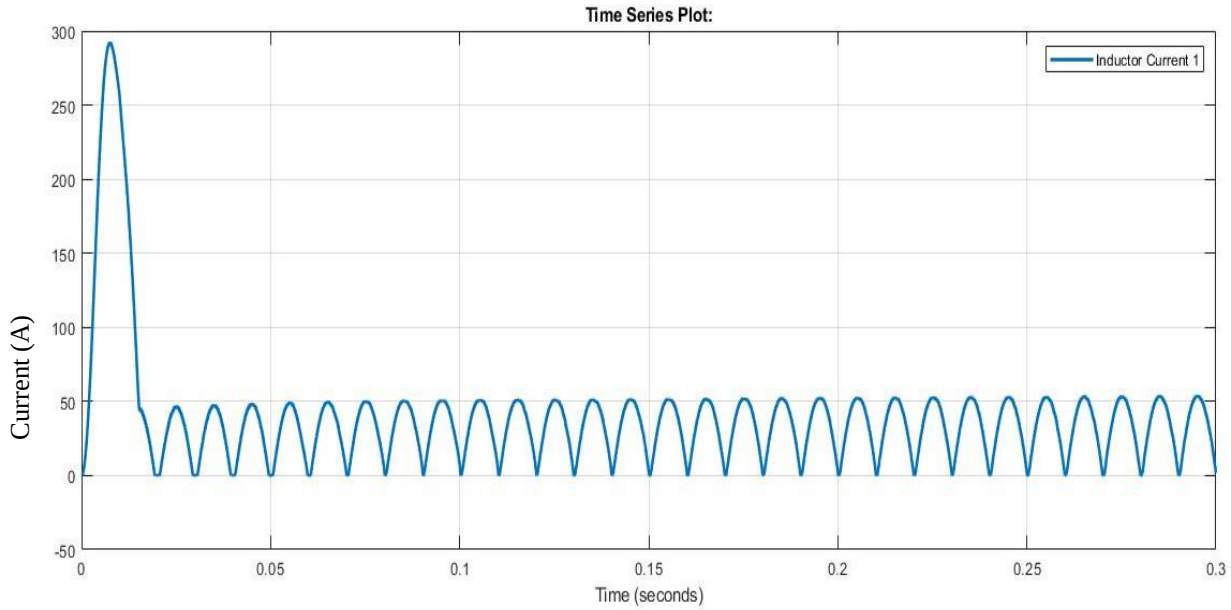


Fig.3.16 *Inductor current (I_{L1}) waveform*

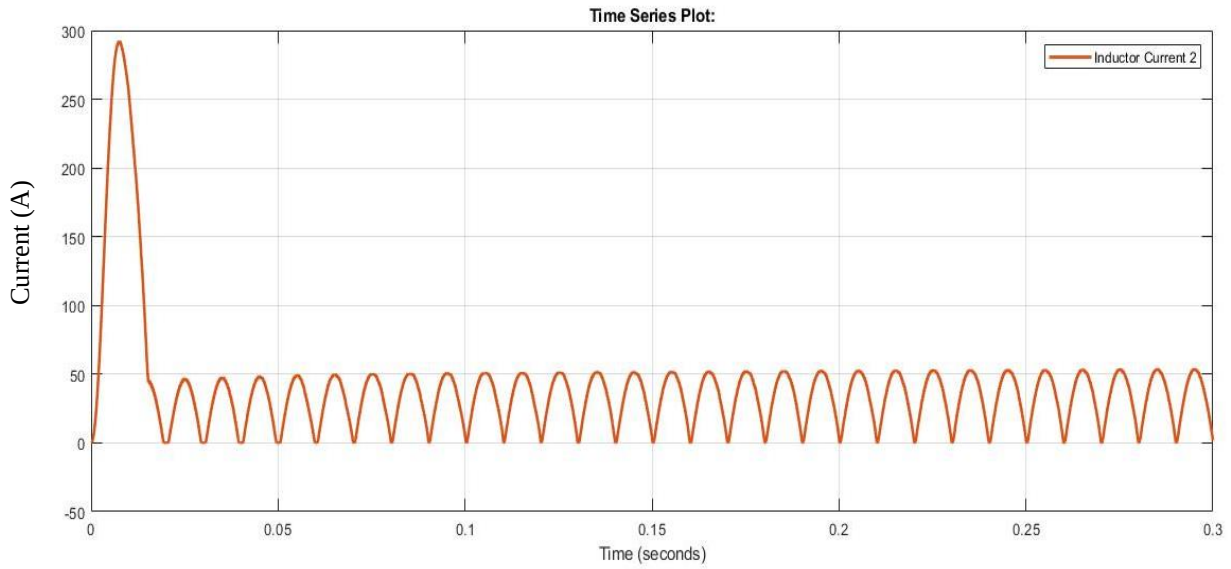


Fig.3.17 *Inductor current (I_{L2}) waveform*

In figures (**Fig.3.15, Fig.3.16** and **Fig.3.17**), the internal characteristics (inductor currents) of the converter are shown. As it is seen in figures (**Fig.3.16** and **Fig.3.17**), the inductor currents (I_{L1} and I_{L2}) are equally shared between two legs of the converter. As shown in **Fig.3.15** the total inductor current is the summation of two inductor currents. As the inductor current ripples are phase shifted by 180˚they cancel each other out. So the current source ripples are significantly minimized.

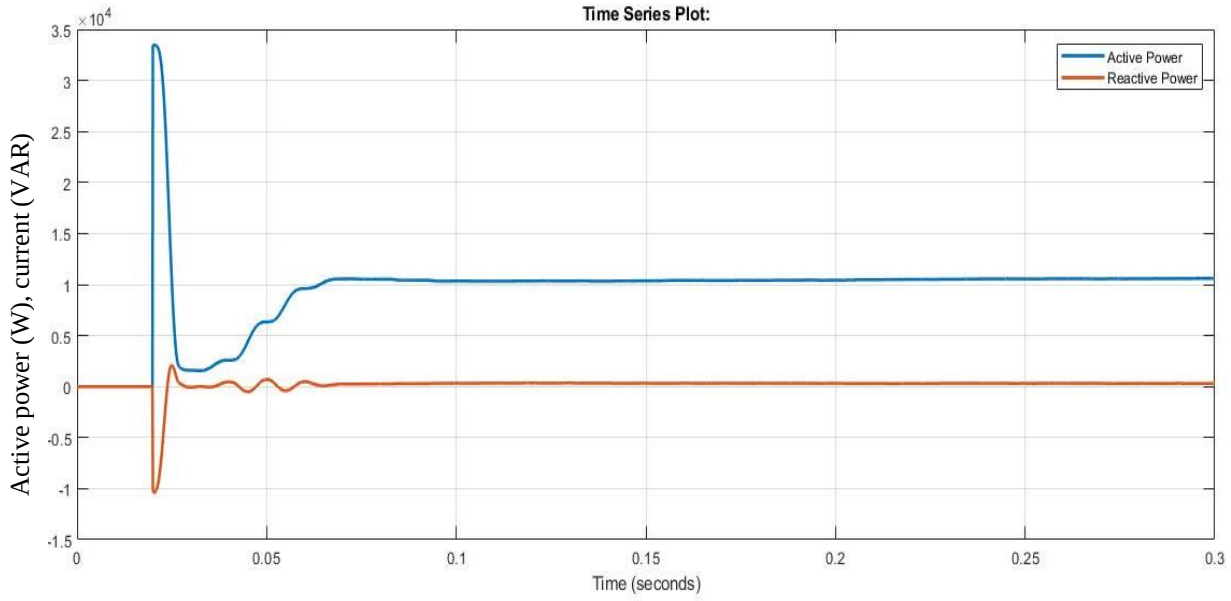


Fig.3.18 *Active and reactive power waveform*

From the above figure:

- Active power = **10350** W
- Reactive power =**127** VAR

So the power factor is **0.9999** which is almost unity.

Now the THD obtained of the input ac current is shown in **Fig.3.19**

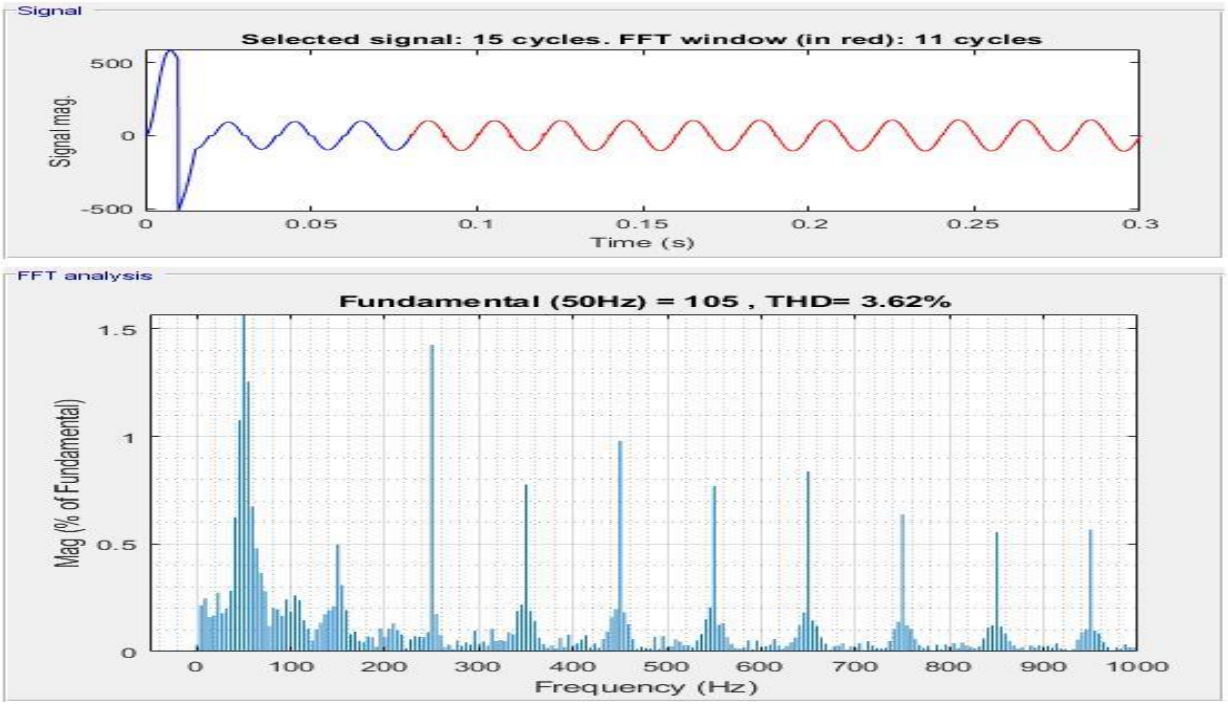


Fig.3.19 *THD of input current*

The THD of input current is 3.62%

So we can say that interleaved boost converter provides better power factor and THD.

A comparison between the different circuit topologies is shown in following table

Table.3.2 *The comparison of input power factor*

Circuit topology	Input power factor	THD_i (%)
Single phase diode rectifier	**0.86555**	**36.73**
Boost converter	**0.9985**	**5.36**
Interleaved Boost converter	**0.9999**	**3.62**

3.4 Conclusion

After viewing the results of the simulations in **Table.3.2**, it is clear that the interleaved boost converter is superior in terms of performance parameters.

For both single and two channel boost converter the output voltage is almost pure DC and has a good tracking to reference voltage.

The power factor correction using boost converter is a very powerful tool to decrease power losses, and both boost and interleaved PFC give the desired results.

General conclusion

General conclusion

Energy conversion is the main issue of the power electronics and widely applied in today's world. Also we cannot compromise with the power factor and THD. In this thesis power factor correction and THD minimization by interleaved boost converter in continuous conduction mode, with average current mode control using PI controller, has been theoretically analyzed. In the first chapter a general overview about power quality, power quality issues and power factor theories are introduced, the second chapter covers the system topologies and list some control strategies especially the average current mode control technique also a small signal model of the interleaved boost converter and its transfer functions are presented in this chapter. The last chapter (chapter three) discusses the simulation results using MATLAB Simulink, from this results it can be concluded that using interleaved boost converter power factor has been well improved and THD has been minimized significantly.

Future works

- For further improvement fuzzy logic controller or neural network can be used instead of PI controller.
- The association of the proposed APFC to feed a variable frequency drive system (Inverter +AC motor)
- The experimental implementation of the proposed APFC.

Appendices

Appendix A

A.1 Electric power quality issues

A recent survey of Power Quality experts indicates that 50% of Power Quality problems are related to grounding, ground bonds, neutral to ground voltages, ground loops, ground current or other ground associated issues[34].

The issue of electrical power quality is gaining a lot of importance and attention for several reasons, mainly the increasing dependence of society on the electrical energy, the sensitivity of new equipment to power variations and most importantly, the advent of new power electronic equipment that brought disturbances into the supply system.

The first sign of a power quality problem is a distortion in the voltage waveform of the power source from a sine wave, or in the amplitude from an established reference level, or a complete disturbance. The disturbance might be caused by harmonics in the current or by events in the main voltage supply system. These disturbances can go from a fraction of a cycle (milliseconds) to great durations (seconds to hours) in the voltage supplied by the source.

A.2 Symptoms of power quality problems

Here are some indicators for the presence of a power quality problem:

- Piece of equipment mis-operates.
- Circuit breakers trip without being overloaded;
- Automated systems stop for no apparent reason;
- Electronic systems fail or fail to operate on a frequent basis;
- Electronic systems work in one location but not in another location.

A.3 General classes of power quality problems

The IEEE Standards Coordinating Committee 22 (IEEE SCC22) has led the main effort in the United States to coordinate power quality standards [35] and the IEC has classified electromagnetic phenomena into the following groups and categories:

A.3.1 Transients

A transient is a sudden undesirable momentary change from one steady state operating condition to another. Transients are classified into two categories:

- **Impulsive**: It is defined by IEEE 1159 as a sudden, non–power frequency change in the steady-state condition of voltage, current, or both that is unidirectional in polarity (either primarily positive or negative) [35]. It is normally a single, very high impulse like lightning.
- **Oscillatory:** is a sudden, non–power frequency change in the steady-state condition of voltage, current, or both that is bidirectional in polarity (includes both positive and negative polarities).

  Fig.1.3 shows the different types of transients.

A.3.2 Long duration voltage variations

It is said that there is a long duration voltage variation when the RMS value of the voltage deviates for more than 1 minute. There are three types of long duration voltage variations:

- **Over voltage**: is usually the result of load switching off and incorrect tap settings on transformers.
- **Under voltage**: It is generally caused by load switching on or switching off a capacitor bank.
- **Sustained interruptions:** is when the supply voltage is null for longer than 1 minute.

A.3.3 Short duration voltage variations

It is said that there is a short duration voltage variation when the RMS value of the voltage deviates for less than 1 minute. It is categorized into the following three types:

- **Sags:** are usually the result of a fault in the system, equipment failure and control malfunctions.
- **Swells:** can be caused by switching off a large load or energizing a large capacitor bank.
- **Interruption:** occurs when the supply voltage decreases to 0.1 pu for less than 1 minute.

A.3.4 Voltage imbalance

It is described as a voltage variation in a power system where the voltage magnitudes or the phase shifts between them are not equal. It is calculated by dividing the maximum deviation from the average of the three-phase voltages or currents by the average of the three-phase voltages and currents and it is expressed in percent. It is mainly caused by single phase loads on a three phase circuit and blown fuses in one phase of a three-phase capacitor bank.

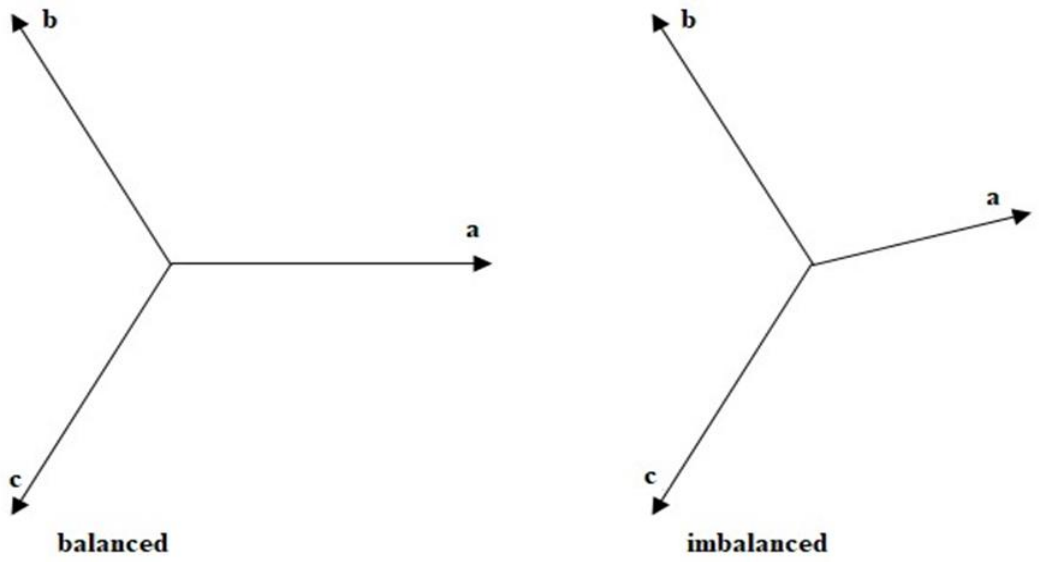


Fig.A.1 *Voltage imbalance*

A.3.5 Waveform distortion

It is known as a steady state deviation from an ideal sinewave of power frequency and there are five main types of it:

- DC offset
- Harmonics
- Interharmonics
- Notching
- Noise

A.3.6 Voltage fluctuation

It is described as random variations of the voltage envelope or a series of random voltage changes, of which the magnitude does not exceed the range 0.9 to 1.1 pu. Voltage fluctuations can be very harmful for loads as it could be the cause of motors and cables overheating and the malfunction of electronics.

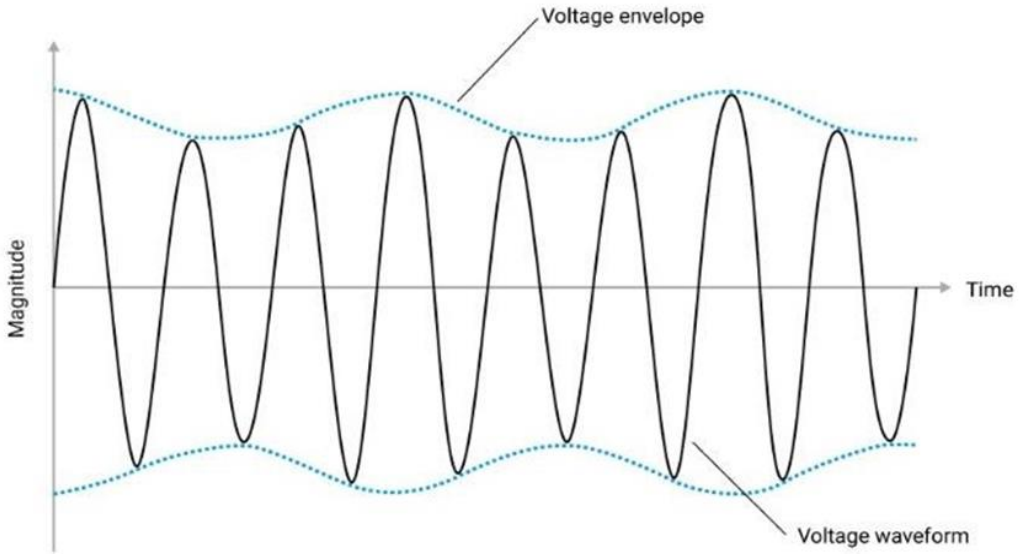


Fig.A.2 *Voltage fluctuation*

A.3.7 Power frequency variation

It is defined as the deviation of the power system's fundamental frequency from its nominal value (50 or 60 Hz). It is mainly the result of bulky power transmission system, large load disconnection. Frequency variations cause an increase or decrease of a motor's speed which can cause the motor to overheat.

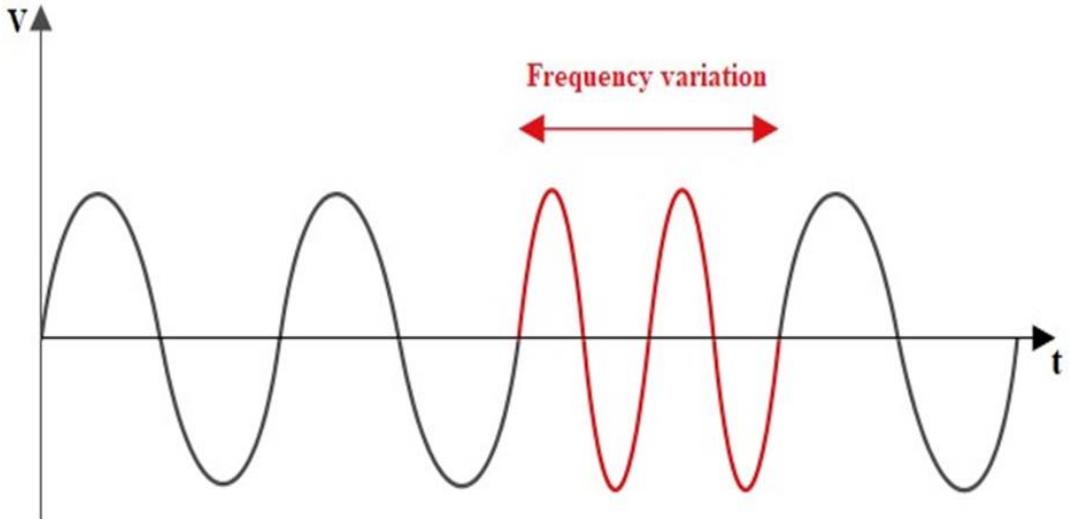


Fig.A.3 *Frequency variation*

Appendix B

B.1 PI controllers

Proportional-Integral-Derivative controller (PID controller) is a control loop feedback mechanism widely used in industrial control systems. A PID controller calculates an error value as the difference between a measured process variable and a desired setpoint. The controller attempts to minimize the error by adjusting the process through use of a manipulated variable. The PID controller algorithm involves three separate constant parameters, and is accordingly sometimes called three-term control: the proportional, the integral and derivative values, denoted P, I, and D. Simply put, these values can be interpreted in terms of time: P depends on the present error, I on the accumulation of past errors, and D is a prediction of future errors, based on current rate of change [26].

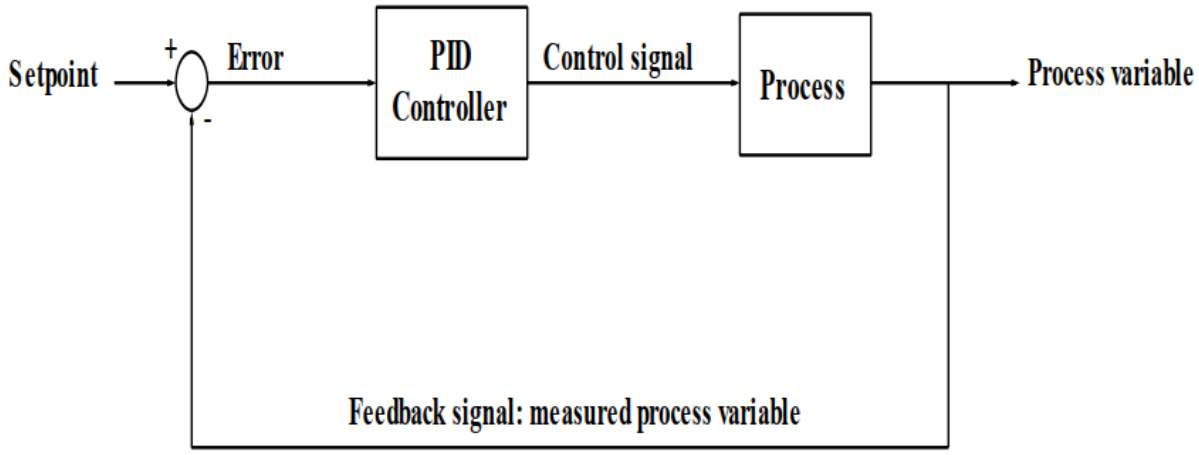


Fig.B.1 *Block diagram of process control using PID controller*

A PI is a special case of the PID controller in which the derivative term of the error is not used, the transfer function of a PI controller is

$$PI(s) = K_p + \frac{K_i}{s} = \frac{1+\tau s}{T_i s} \quad \text{(B.1a)}$$

Where:

$$K_p = \tau / T_i \quad \text{(B.1b)}$$

$$K_i = 1 / T_i \quad \text{(B.1c)}$$

B.2 Additional Simulation circuits

B.2.1 Control block for Interleaved Boost PFC

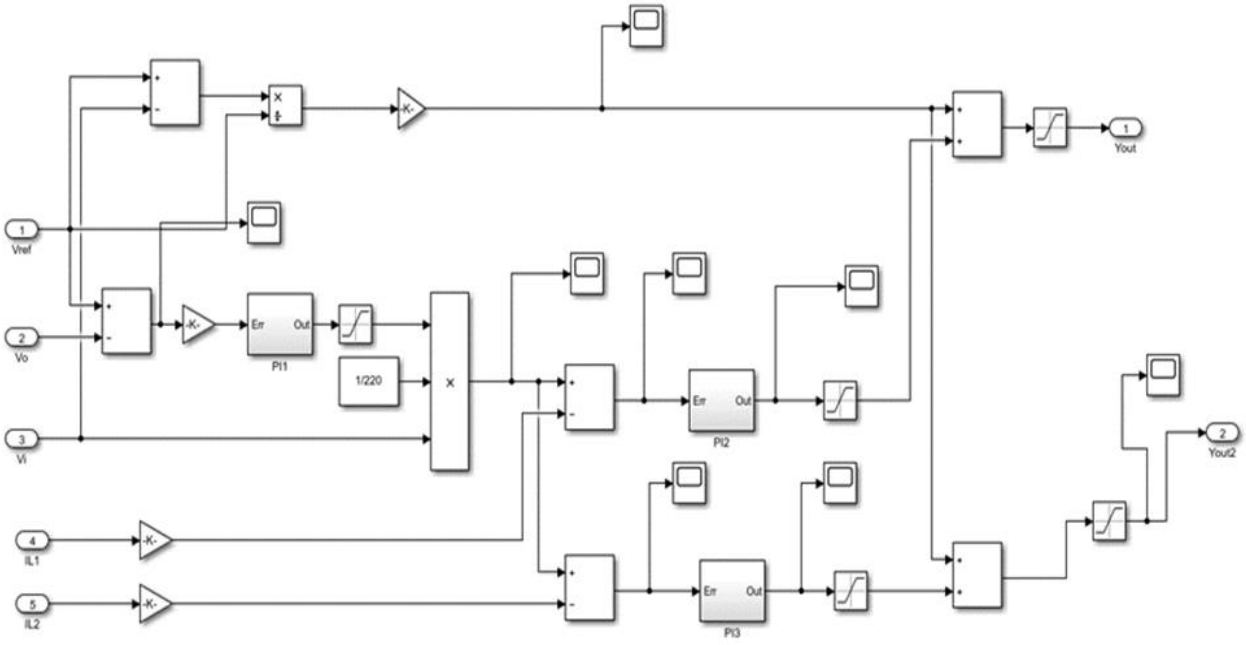


Fig.B.2 *Control block for Interleaved Boost PFC*

B.2.3 PWM block for Interleaved Boost PFC

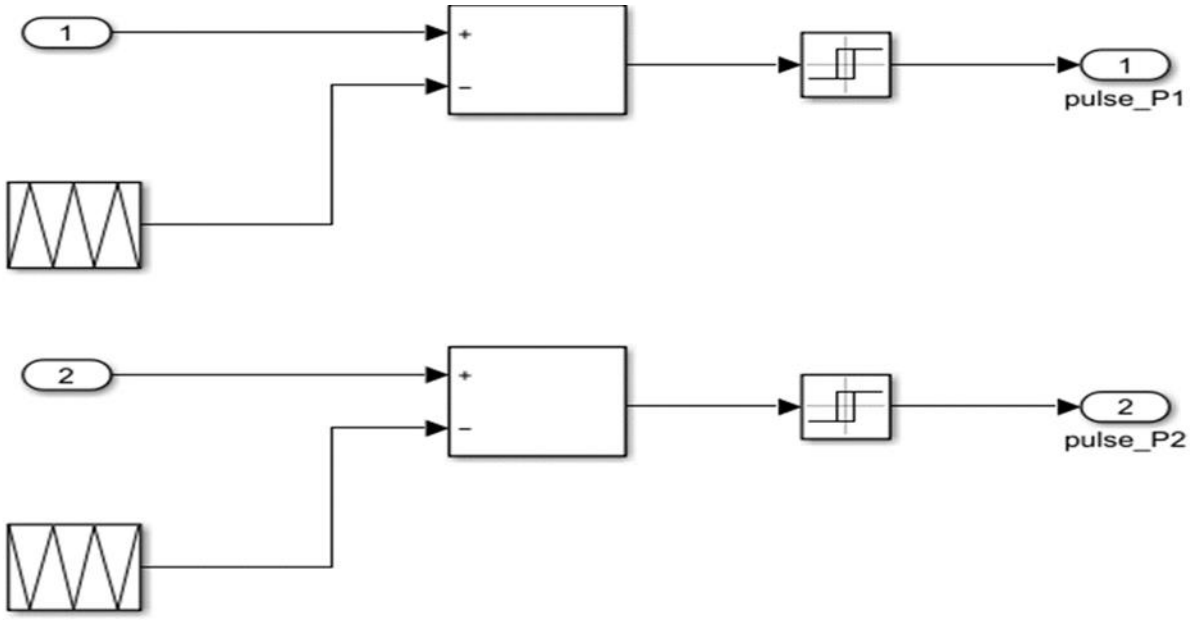


Fig.B.3 *PWM block for Interleaved Boost PFC*

References

References

[1] Muhammad H. Rashid, Power Electronics Handbook (Academic Press, 2001).

[2] "Brad Bryant, Member, IEEE, and Marian K.Kazimierczuk, Fellow, IEEE, Modeling the Closed-Current Loop of PWM Boost DC–DC Converters Operating in CCM with Peak Current-Mode Control, IEEE Transactions on circuit and systems—I: regular papers, vol. 52, no. 11, November 2005."

[3] "Wa Ma, Mingyu Wang, Shuxi Liu, Shan Li, and Peng Yu, Stabilizing the Average-Current-Mode-Controlled Boost PFC Converter via Washout-Filter-Aided Method IEEE Transactions on Circuits and Systems- II, Express Briefs, vol. 58, no. 9, September 2011."

[4] "Laszlo Huber, Member, IEEE, Brian T. Irving, and Milan M. Jovanovic´, Fellow, IEEE, Open-Loop Control Methods for Interleaved DCM/CCM Boundary Boost PFC Converters, IEEE Transactions on Power Electronics, vol. 23, no. 4, July 2008."

[5] RASHID, M. H., (2011). Power Electronics Handbook, Third Edition. Oxford : Elsevier Inc. ISBN: 978-0-12-382036-5.

[6] ON SEMICONDUCTOR (2011b). Power Factor Correction (PFC) Handbook, Choosing the Right Power Factor Controller Solution (HBD853/D Rev.4). SCILLC.

[7] "Brunel corporation. (2004). Capacitor, De-tuned Capacitor & Filter Bank Products. The ABB solution to harmonics."

[8] "Ramon Pinvol. (2015). HARMONICS: CAUSES, EFFECTES AND MINIMIZATION. Salicru white papers."

[9] H. Khan and A. K. Panda, "ELECTRICAL ENGINEERING," p. 69.

[10] "H.Z.Azazi, E. E. EL-Kholy, S.A.Mahmoud and S.S.Shokralla,'ReviewofPassiveand Active Circuits for Power Factor Correction in Single Phase, Low Power AC-DC Converters,'InProc.the 14th International-Middle-East-Power-Systems-Conference'10, 2010, pp. 217-224."

[11] "M. K. W.Wu and C. K. Tse, 'A review of EMI problems in switch mode power supply design,'J. Electric. Electron. Eng. Australia, vol. 16, no. 3/4, pp. 193-204, 1996."

[12] "B.K. Bose, Power Electronics and AC Drives, Prentice-Hall, New Jersey, 1986."

[13] "J.D. Irwin (Ed.), The Industrial Electronics Handbook, CRC/IEEE Press, Boca Raton, USA, 1996."

[14] "F. F. Mazda, Power Electronics Handbook. Amsterdam: Elsevier, 1997."

[15] "R. Dash, 'Power Factor correction using parallel boost converter', M. Tech. thesis, National Institute of Technology, Rourkela, 2007."

[16] "M. H. Rashid, Power Electronics: Circuits, Devices, and Applications.Upper Saddle River, New Jersey: Prentice Hall, 2013."

[17] "Fair Child Semiconductor, Appl.Note 42047 Power Factor Correction (PFC) Basics,pp. 1-10."

[18] "Y. Rozanov, S. Ryvkin, E. Chaplygin, and P. Voronin, Power Electronics Basics: Operating Principles, Design, Formulas, and Applications. Boca Raton, FL: CRC Press, 2015."

[19] "Unitrode, Application Note U-140, pp. 356-369."

[20] "S. B.Santra,'Design and Implementation of UPFC based Boost Converter for EfficiencyPage | 52 Optimization of Brushless DC Motor Drive System', M. Tech. thesis,Jadavpur University, Kolkata, 2012."

[21] D. W. Hart, Power electronics. New York: McGraw-Hill, 2011.

[22] B. Wu, Ed., Power conversion and control of wind energy systems. Piscataway, NJ : Hoboken, N.J: IEEE Press ; Wiley, 2011.

[23] Electric Economics: Regulation and Deregulation Geoffrey Rothwell and Tomas Gomez.

[24] "H. Benqassmi, J.-C. Crebier and J.-P. Ferrieux, 'Comparison Between CurrentDriven Resonant Converters Used for Single-Stage Isolated Power-Factorcorrection,' IEEE Transactions on Industrial Electronics, vol. 47, no. 3, pp. 518- 524, 06 August 2002."

[25] "S. Chattopadhyay, V. Ramanarayanan and V. Jayashankar, 'A Predictive Switching Modulator for Current Mode Control of High Power Factor Boost64 Rectifier,' IEEE Transactions on Power Electronics, vol. 18, pp. 114-123, Jan 2003."

[26] M. H. Rashid, Ed., Power electronics handbook: devices, circuits, and applications handbook, Fourth Edition. Oxford: Butterworth-Heinemann, an imprint of Elsevier, 2018.

[27] Ms. Kurma Sai Mallika,"Topological Issues in Single Phase Power Factor Correction", Thesis, Degree of Master of technology In Power control and drives, Department of electrical engineering National institute of technology Rourkela769008, 2007.

[28] Matada Mahesh, "Performance improvement of ac-dc power factor correction converters for distributed power system", Thesis, Degree of Doctor of Philosophy Under the supervision of Prof. Anup Kumar Panda, NIT, Rourkela, Oct 2011.

[29] Y. Zaohong, and P. C. Sen, "Recent developments in high power factor switch-mode converters‖, in Proc. IEEE-Elect. & Computer Engg., Conf., vol. 2, 1998, pp. 477480.

[30] K. Liu, and Y. Lin, "Current waveform distortion in power factor correction circuits employing discontinuous-mode boost converters,‖ in Proc. Power Electron. Spec. Conf. (PESC'89), 1989, pp. 533-540.

[31] "Fernandez, A.; Tonicello, F.; Aroca, J.; Mourra, O.; , 'Battery discharge regulator for space applications based on the boost converter,'in proc. IEEE APEC 2010, pp.1792-1799, 21-25 Feb. 2010."

[33] "Barrado, A.; Lazaro, A.; Vazquez, R.; Salas, V.; Olias, E., 'The fast response double buck DC-DC converter (FRDB): operation and output filter influence,' IEEE Trans. Power Electron., vol.20, no.6, pp.1261,1270, Nov. 2005."

[34] "Khalid, Saifullah & Dwivedi, Bharti. (2011). Power quality issues, problems, standards & their effects in industry with corrective means. International Journal of Advances in Engineering & Technology."

[35] "Ranjan Kumar Jena. ELECTRICAL POWER QUALITY. Department of Electrical Engineering. CET. BBSR."