Abstract

The present work reports the simulation and realization of a Digital Phase-Locked Loop (DPLL). The circuit consists of three major blocks: a Phase Frequency Detector (PFD), an RC Low-Pass Filter (LPF), and a Relaxation Voltage Controlled Oscillator (VCO). The analysis, design, and examination of each block were carried out, resulting in a successful assembly of the entire DPLL circuit. The designed PLL was simulated, measured, and then compared with the experimental observations using LM565 IC. The findings demonstrate the PLL capability to achieve frequency synchronization with minimal phase error at the desired frequency of 1 KHz, along with a wide lock-in range.

Acknowledgment

I would like to express my gratitude to my primary supervisor ***Prof. Mouloud CHALLAL*** *for his guidance and advice throughout this long journey.*
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I am grateful to my family and my best friends for their encouragement that motivated me to overcome the challenges.

Dedication

"This work is dedicated to my beloved family and best friends, who believed in me and encouraged me on this long and difficult journey. Words cannot express how grateful I am to each and every one of you!"

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List of Abbreviations

ADPLL All Digital Phase Locked Loop

APLL Analog Phase Locked Loop

CMOS Complementary Metal Oxide Semiconductor

CP Charge Pump

DFF D Flip Flop

DN Down

DPLL Digital Phase Locked Loop

FD Frequency Detector

FM Frequency Modulation

GNSS Global Navigation Satellite System

GPS Global Positioning System

IF Intermediate Frequency

LF Loop Filter

LO Local Oscillator

LPF Low-Pass Filter

NCO Numerically Controlled Oscillator

PCB Printed Circuit Board

PD Phase Detector

PFD Phase Frequency Detector

PLL Phase Locked Loop

PPS Pulse Per Second

RF Radio Frequency

SMD Surface Mount Device

TDC Time to Digital Converter

THT Through-Hole Technology

TTL Transistor-Transistor Logic

USB Universal Serial Bus

VCO Voltage Controlled Oscillator

XOR Exclusive OR

General introduction

Synchronization is a vital process in any communication system, it refers to the action of aligning the frequency and timing of a communication system's components. Synchronization ensures reliable communication between a transmitter and a receiver and allows them to communicate in harmony by transmitting and receiving signals accurately without suffering from transmission problems such as data loss, signal distortion, higher bit error rates... etc.

Achieving synchronization in communication systems involves the use of a precise reference clock and different circuits such as phase-locked loops (PLLs).

The reference clock aligns and coordinates the timing and frequency of the different components of the system. A common approach to obtain a precise clock is the use of GPS signals emitted by GPS satellites. The GPS satellites emit highly accurate 1PPS signals that are considered an available and reliable reference for synchronization purposes.

A Phase-Locked Loop plays an important role in the process of synchronization. It is is a feedback control system that generates an output signal whose frequency is aligned with that of a reference signal, ensuring that both signals either maintain a constant phase difference or have no phase difference. This is achieved by continuously comparing the phase and frequency of the input signals and adjusting its local oscillator until the synchronization is fulfilled. PLLs are of different types and are employed in a variety of applications.

In this project, we aim to design a Digital Phase Locked Loop (DPLL) that synchronizes with a clock reference of 1 KHz frequency. The project's work will be distributed across three comprehensive chapters, each addressing specific aspects to achieve the project's objective.

The following is a concise overview of each chapter's content and focus.

- **Chapter 1:**

  In the first chapter, we will explore the theoretical foundation and the generalities related to Phase Locked Loops, including their operating principles, types and classes, major building blocks, performance characteristics, and their wide-ranging applications. This chapter will provide a comprehensive understanding of Phase Locked Loops, laying the groundwork for the next chapters.

- **Chapter 2:**

  In this chapter, we will present the design and implementation of a Digital or Mixed-signal Phase Locked Loop (DPLL) using the simulation software Multisim. The design and implementation process of the DPLL will involve designing and simulating the three main blocks: PFD, LPF, and VCO. The performance and evaluation of the system will be examined by constructing and testing the whole system in simulation.

- **Chapter 3:**

  The last chapter will include the practical implementation of the PLL circuit and report the experimental results of testing the PLL ability to acquire the lock with the $1KHz$ reference signal and the 1PPS GPS signal captured by a GPS receiver. A comparison between the designed PLL and an IC PLL will also take place in this chapter.

Chapter 1

Introduction to Phase Locked Loops

1.1 Introduction

A Phase Locked Loop, or a PLL, is a closed-loop feedback control circuit that generates an output signal whose phase is related to its input signal (also called reference signal). In other words, a PLL synchronizes the frequency of an output signal with a reference signal and ensures they have either a constant phase difference or no phase difference [1].

In modern technology, PLLs are often implemented as integrated circuits (ICs), where various components of the PLL are integrated into a single chip. This allows for easy implementation of the PLL in a wide range of electronic systems, with minimal external components required and hence a small compact package. PLLs are widely used in wireless or radio frequency (RF) applications, including WIFI routers, broadcast radios, televisions, and mobile phones.

In this chapter, we will cover the most important principles of Phase Locked Loops, including their operating principle, types and classes, building blocks, performance, applications and more.

1.2 Operating Principles of PLLs

Phase Locked Loops are mainly used for synchronization, when two signals have a phase difference, the PLL causes the output signal to keep tracking the reference signal until the phase error between the two is zero or remains constant. The term "Locked" in PLL refers to the fact that the output signal is held in phase with the input signal, thus the locking process is the goal of using a PLL system [1].

Understanding the operating principle of a PLL requires including the basic building blocks that construct it. The PLL consists of three main basic blocks:

- A phase detector (PD).
- A loop filter (LF).
- A voltage-controlled oscillator (VCO).

Figure 1.1 depicts a block diagram of a unity feedback PLL, where the input of the system is the reference signal's phase ϕ_{ref} and the output is the VCO signal's phase ϕ_{out}.

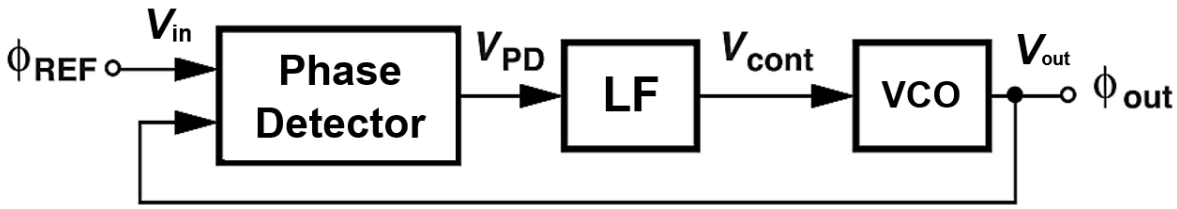

Figure 1.1: A Phase Locked Loop block diagram [2]

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The Phase Detector (PD) is used to compare the output signal and the reference signal and then generates a voltage signal called V_{PD}, the average of this signal is proportional to the phase error (or phase difference) ϕ_e as shown in Figure 1.2.

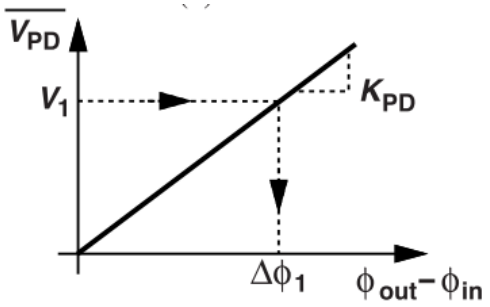


Figure 1.2: Phase detector characteristics [2].

In a simple mathematical equation, we can write:

$$\overline{V_{PD}}(t) = K_{PD}\phi_e \tag{1.1}$$

where K_{PD} is the gain of the Phase Detector. Its unit is $(Volt/rad)$. Note that the proportionality K_{PD} is satisfied within a limited range.

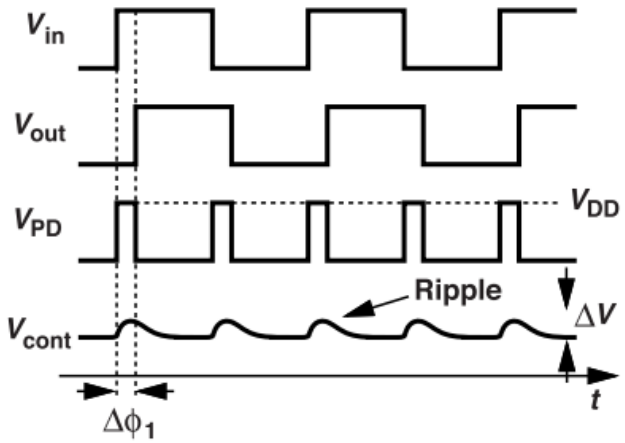


Figure 1.3: Input and output waveforms of a phase detector [2].

Figure 1.3 shows the output voltage V_{PD} of the PD and the control voltage V_{cont} generated by the LF when two digital input signals V_{in} and V_{out} are applied to the PLL. Note that these inputs are not in phase.

The output signal of the PD is an AC signal, which means that it is composed of a DC value and some harmonics that must be canceled by the Loop Filter (LF). The LF is responsible for extracting the control voltage V_{cont} which is the average value of the phase error signal $V_{PD}(t)$. In other words, the LF smooths and flattens the signal $V_{PD}(t)$ and makes it look like a DC value [1].

The Voltage Controlled Oscillator (VCO) is an electronic oscillator that generates an output signal whose frequency can be adjusted by varying the input voltage applied to it. In this case, the input signal that is controlling the VCO is V_{cont}. The angular frequency of a VCO is given by the following formula:

$$\omega_{out}(t) = K_{VCO}V_{cont} + \omega_0 \tag{1.2}$$

ω_0 is the free running frequency of the VCO in (rad) and K_{VCO} is the gain of the VCO, given in $(rad.Hz/Volt)$ [1].

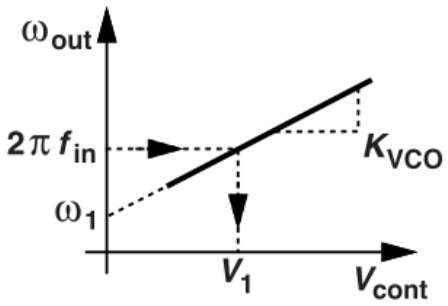


Figure 1.4: VCO characteristics [2].

The VCO characteristics are depicted in Figure 1.4, where there is a linear relationship between ω_{out} and V_{cont}.

If the reference signal leads or lags the feedback signal, then an error signal is generated by the PD, which is then filtered by the LF, this will cause the VCO to either increase its frequency (when the input signal is leading) or decrease its frequency (when the input is lagging). Thus, the feedback loop in the PLL ensures that the phase difference ϕ_e between the input and output signals remains constant or converges to zero, then the output signal will remain in phase with the input signal.

1.3 PLL Types

Phase Locked Loops are mainly classified into 3 categories: Analog PLLs, Digital PLLs, and All Digital PLLs. Each type is identified by the internal components that build up the PLL system [1].

- **Analog Phase Locked Loop (APLL)**

  It's also known as a Linear PLL (LPLL), this type of PLL contains only analog devices. The Phase Detector (PD) is known as an analog multiplier (four quadrant multiplier). The Loop filter contains passive or active components like resistors and capacitors. Moreover, an analog VCO is integrated with the system to generate the desired frequencies.

- **Digital Phase Locked Loop (DPLL)**

This type of PLL contains both analog and digital components. A Digital PLL has a digital Phase Detector including XOR phase detector, JK flip-flop phase detector, Phase Frequency Detector (PFD). The loop filter is normally based on passive elements, and the VCO is analog in nature. Digital phase-locked loops are typically smaller than analog PLLs, due to their digital phase detector and loop filter.

- **All Digital Phase Locked Loop (ADPLL)**

  This PLL does not contain any passive element, it is only built from digital components. The phase detector is digital and known as Time to Digital Converter (TDC), the loop filter is also digital. Concerning the VCO, it is replaced by an NCO which is a Numerically Controlled Oscillator.

We can also mention other types of PLL such as Software PLL and IC PLL.

In the software PLL, a hardware platform like a Digital Signal Processor (DSP) is needed to perform the required calculations. The signal processing algorithm takes a reference signal and a feedback signal from a local oscillator, calculates the phase difference between the two signals, and adjusts the frequency of the local oscillator to minimize the phase difference.

In the IC PLL, all components are integrated into a single chip. Some references are ADF4106 from Analog Devices and CD4046B, LM565 from Texas Instrument.

1.4 Building Blocks of PLL

As mentioned in the previous sections, a PLL is a feedback system that compares the phase of the input reference frequency to the phase of the output frequency and adjusts the output frequency based on this information. The PLL block diagram shown in Figure 1.1, represents the interconnection of the following circuit's building blocks: Phase Detector (PD), Loop Filter (LF), Voltage Controlled Oscillator (VCO), and a frequency Divider $(\div N)$ for some applications. Understanding how these components work and interact will help us understand how a PLL can be utilized in a variety of applications. In the following sections, each block will be discussed in detail.

1.5 Phase Detector

A Phase Detector is an electronic circuit that compares the phases of two signals and produces an output signal that represents the phase difference between them. Phase detectors are used in many different applications, such as frequency synthesis and communications systems. There are several types of phase detectors, including analog and digital types. Analog phase detectors are usually built with operational amplifiers, diodes, or other analog components, whereas digital phase detectors are built with logic gates or other digital components.

1.5.1 Analog Phase Detectors

An analog multiplier is an electronic circuit that multiplies two analog signals together to produce an output signal that is proportional to their product.

1.5.1.1 Double balanced mixer phase detector

One common type of analog phase detector is the balanced mixer, which is also known as the "Gilbert cell" phase detector. Figure 1.5 shows the circuit diagram of a balanced mixer.

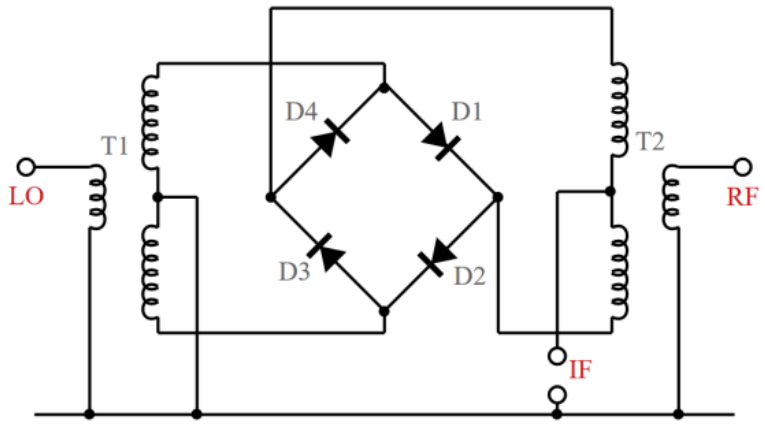


Figure 1.5: Schematics of a balanced mixer [3].

A balanced mixer is specifically designed to perform frequency conversion or mixing operations in radio frequency (RF) applications, it is used in Analog PLLs (APLL). This circuit has two input signals of different frequencies, the first input is applied at the RF node, this signal represents the reference signal. While the second input is applied at the LO (Local oscillator) node, note that this signal is the VCO output. The output signal is then produced at the IF nodes (Intermediate frequency), it is the sum and difference of the input frequencies [4].

Let's suppose that the RF and the LO inputs are sinusoidal, and are expressed as the following,

$$V_{RF}(t) = A_{RF} sin(\omega_{RF} t + \theta_{RF}) \tag{1.3}$$

$$V_{LO}(t) = A_{LO} sin(\omega_{LO} t + \theta_{LO}) \tag{1.4}$$

Then, the output signal $V_{IF}(t)$ is the multiplication of $V_{LO}(t)$ and $V_{RF}(t)$. Thus, the following equations are found.

$$V_{IF}(t) = V_{LO}(t) \times V_{LO}(t)$$

$$V_{IF}(t) = A_{LO} sin(\omega_{LO} t + \theta_{LO}) \times A_{RF} sin(\omega_{RF} t + \theta_{RF})$$

Some trigonometry manipulation leads to equation 1.5.

$$V_{IF}(t) = \frac{A_{LO} A_{RF}}{2} [cos((\omega_{LO} + \omega_{RF})t + \theta_{LO} + \theta_{RF}) + cos((\omega_{LO} - \omega_{RF})t + \theta_{LO} - \theta_{RF})] \tag{1.5}$$

Note that the signal $V_{IF}(t)$ contains two terms. The first term is $cos((\omega_{LO} + \omega_{RF})t + \theta_{LO} + \theta_{RF})$, which is contains high-frequency harmonics since it is the sum of ω_{LO} and ω_{RF}.

This term will be filtered using the Loop Filter that comes after the PD block. The remaining term is the desired one, since $cos((\omega_{LO} - \omega_{RF})t + \theta_{LO} - \theta_{RF})$ contains the difference of the signals' phases.

If the radian frequencies of $V_{RF}(t)$ and $V_{LO}(t)$ are equal, then the output signal after filtering becomes,

$$V_{IF}(t) = \frac{A_{LO}A_{RF}}{2} cos(\theta_{LO} - \theta_{RF}) \tag{1.6}$$

Equation 1.6 clearly shows that the output signal is proportional to the phase difference between the input signals, thus the Gilbert cell detects the phase difference by generating an output signal that contains information about the phase error.

Equation 1.6 is plotted in Figure 1.6, it is clear when ϕ_1 (which is $\theta_{LO} - \theta_{RF}$) is equal to *zero*, the PD loses its ability to measure the phase difference. The PD output reaches a maximum at $\phi_1 = 90°, 270°...$ etc. [2]

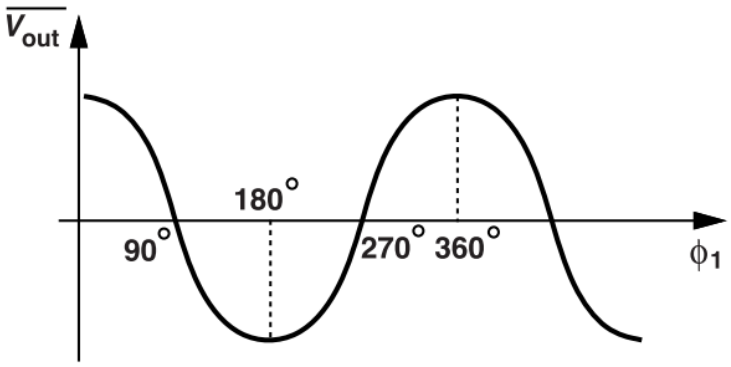


Figure 1.6: Average output characteristics vs the phase error of a mixer. [2]

1.5.2 Digital Phase Detectors

A digital Phase Detector is a circuit that compares the phases of two digital signals and generates an output signal that represents their phase difference. The output signal is a pulse or a digital signal with two possible states, high and low, and with a certain pulse width. The width of the output pulse is proportional to the phase difference between the two input signals.

Digital PDs are more accurate, have a wider dynamic range, and are more immune to noise and interference. They are also easier to integrate into digital circuits. Digital PDs can be implemented using some logic circuits, including Exclusive OR (XOR) gates, JK flip flops, and phase frequency detectors PFD. We will mainly focus on the XOR phase detector and the PFD. [1]

1.5.2.1 XOR Phase Detector

XOR is a digital logic gate that has two inputs, the output of an XOR is either a logical “1” or "HIGH" if the two input values are different, or a logical “0” or "LOW" if the two input are similar. The symbol and truth table for the XOR gate are shown respectively in Figure 1.7 and Table 1.1. [4]

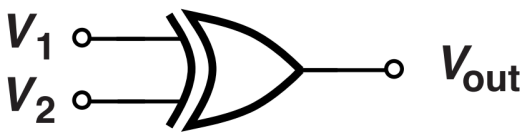


Figure 1.7: XOR gate symbol. [2]

V_1	V_2	V_{out}
0	0	0
0	1	1
1	0	1
1	1	0

Table 1.1: Truth table of an XOR gate

In Figure 1.7, the input V_1 is the reference signal, while V_2 is the feedback signal (output of the VCO), the output signal V_{out} is then fed to the LF.

Since the XOR gate outputs a logical "HIGH" if either of its inputs is 1, but not at the same time, it can be used as a phase detector to detect the phase difference between them.

Let's suppose that the inputs V_1 and V_2 are applied to the XOR gate as shown in Figure 1.8, it is clearly shown the output signal V_{out} is "HIGH" only when V_1 leads V_2, and therefore, the XOR PD is generating a series of pulses at *twice* the input frequency whose width is proportional to the phase error ϕ_1. The computation of the average of V_{out} results in a linear relationship with ϕ_1, this relationship is mentioned in the previous sections, it is the gain K_{PD}. [2]

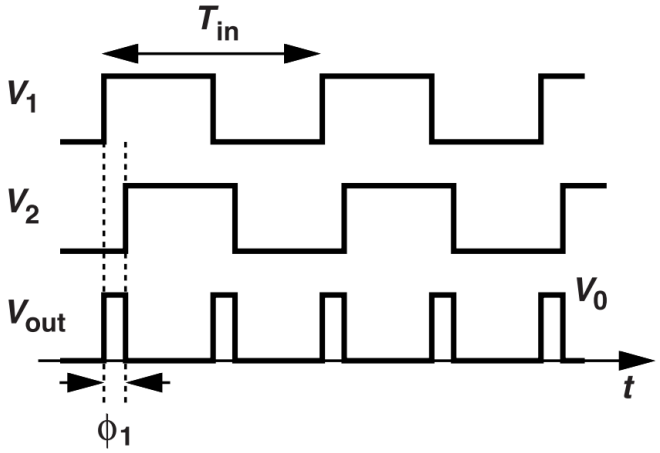


Figure 1.8: XOR gate operating as a PD. [2]

The following equations define the relationship between the average of the PD output and the phase error.

$$\overline{V_{PD}} = \overline{V_{out}} = \frac{Area\,of\,the\,2\,pulses}{Period\,of\,V_{in}}$$

$$\overline{V_{PD}} = 2V_0 \frac{T\phi_1}{2\pi}\frac{1}{T}$$

$$\overline{V_{PD}} = \frac{V_0}{\pi}\phi_1 = K_{PD}\phi_1 \tag{1.7}$$

Thus, if V_0 is the voltage level of the output signal, the gain of the XOR phase detector is,

$$K_{PD} = \frac{V_0}{\pi}(Volt/rad) \tag{1.8}$$

If we plot the characteristics of $\overline{V_{PD}}$ versus ϕ_1, we get the waveform shown in Figure 1.9

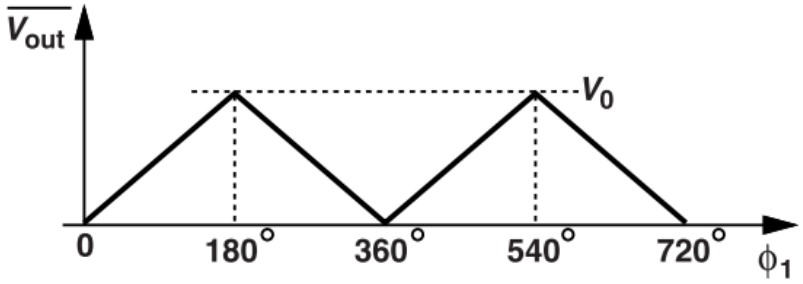


Figure 1.9: Input-output characteristic of XOR PD. [2]

Note that for $\phi_1 = 0$, the PD characteristic begins at zero which means that the two inputs are in phase. Then, the curve is linearly increasing as the phase error increases. Another important note is that the average $\overline{V_{PD}}$ reaches its maximum V_0 when the phase difference is exactly 180° (See Figure 1.10). After this point, the curve falls linearly, returning to zero at $\phi_1 = 360°$ and the behavior repeats and becomes periodic. [2]

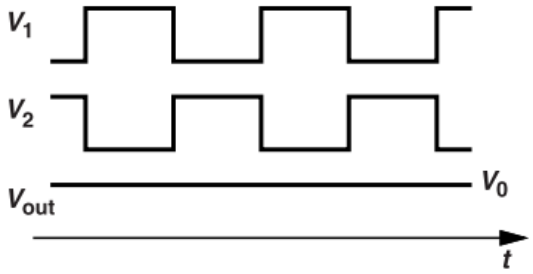


Figure 1.10: Input and output waveforms for a phase difference of $\phi_1 = 180°$. [2]

One drawback of the XOR PD is the limited phase range. This PD can only detect phase differences between 0° and 180° degrees as depicted in Figure 1.9. Beyond this range, the output becomes ambiguous because of the symmetry and cannot be used to determine the actual phase difference, which means that it will not be possible to know which signal is leading or lagging.

1.5.2.2 Phase Frequency Detector (PFD)

A Phase Frequency Detector (PFD) is a digital circuit that compares the phase and frequency of the reference signal, which is fixed in frequency, and the feedback signal and produces an output signal that indicates the difference between the two. The ability to accurately measure and correct the phase and frequency of signals is an essential property of the PFD in PLL design.

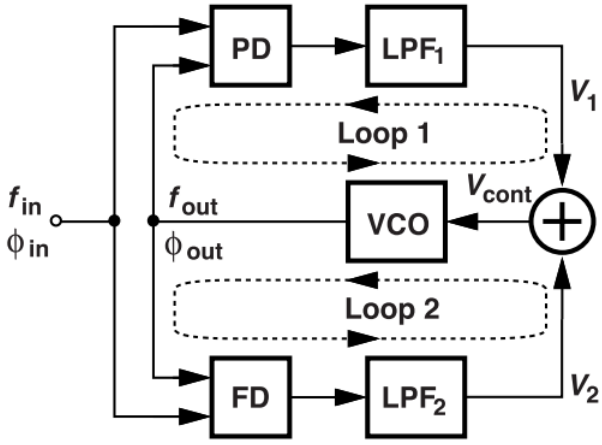


Figure 1.11: PLL block diagram with frequency acquisition aid. [2]

Basically, a PFD operates as a frequency detector FD and a phase detector PD at the same time. As illustrated in Figure 1.11, a PLL is realized with two loops that are interrelated and both share the same VCO.

In Loop 2, The FD measures the difference in frequency when f_{ref} and f_{out} are not equal, and then it adjusts the VCO with negative feedback. This will force f_{out} to converge toward f_{ref} until $|f_{out} - f_{ref}| \approx 0$. As $|f_{out} - f_{ref}|$ converges to zero, then the PD in Loop 1 begins to generate a meaningful dc value that guarantees phase-locking. [2]

As shown in Figure 1.12, a PFD can be represented as a system whose inputs are the $reference\,signal\,(A)$ and the $feedback\,signal\,(B)$ and generates two outputs Q_A and Q_B, their state is either "LOW" or "HIGH" indicating which input signal that is leading or lagging.

Figure 1.12: Phase Frequency Detector. [2]

The PFD operation is based on two principles,

1. if Q_A and Q_B are LOW and a rising edge occurs on A, then Q_A goes HIGH while Q_B remains LOW.
2. If Q_A is HIGH and a rising edge occurs on B, then Q_A is LOW.

This concept is well illustrated in Figure 1.13.

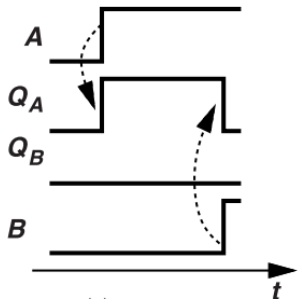


Figure 1.13: Q_A and Q_B states. [2]

To understand the concept of Q_A and Q_B states and their relationship with the phase error, two cases are considered.

If $\omega_A = \omega_B$, but $\phi_A \neq \phi_B$, as shown in Figure 1.14, since A leads B, the rising edge of A occurs first, then Q_A goes HIGH while Q_B remains LOW, once the rising edge of B occurs, Q_A goes LOW. This generates a pulse whose width is equal to the phase difference. Note that the same scenario will happen if A lags B resulting in a pulse on Q_B.

Now, if $\omega_A \neq \omega_B$, a series of pulses will be generated on Q_A if $\omega_A > \omega_B$ thus Q_A exhibits a greater average than Q_B. The opposite happens if $\omega_A < \omega_B$. [2]

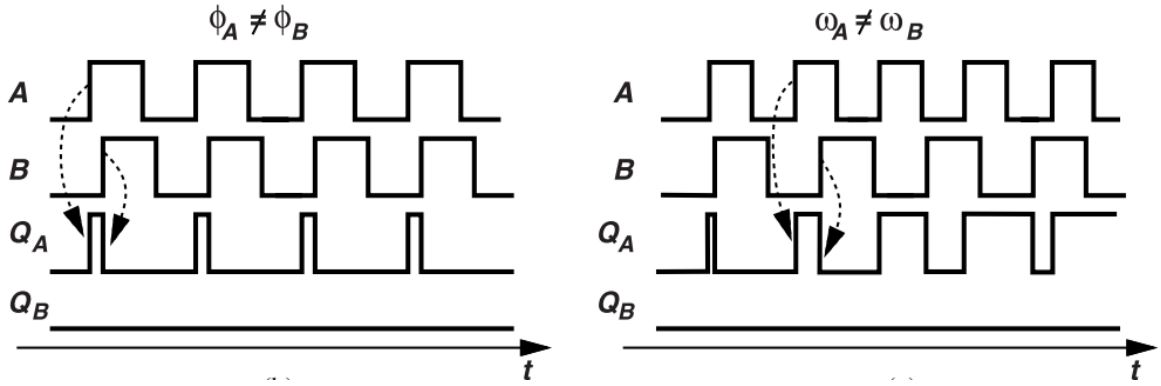


Figure 1.14: Case of phase difference and frequency difference. [2]

A basic PFD consists of two resettable D flip-flops and an AND gate. The D input of both DFFs is set at a logical ONE (V_{DD}), the clock inputs are connected to signals A and B, where A and B are the reference and the feedback signals. The outputs of the two DFFs are Q_A and Q_B, they are also called UP and DN. These signals are connected to the inputs of the AND gate, the output of the latter is attached with $RESET$ of the DFFs.

If A is leading then UP is HIGH and DN is LOW. However, If B is leading, then UP is LOW and DN is HIGH. If the two signals are in phase, then UP and DN will be HIGH, then the AND gate generates a ONE, forcing the DFFs to reset them.

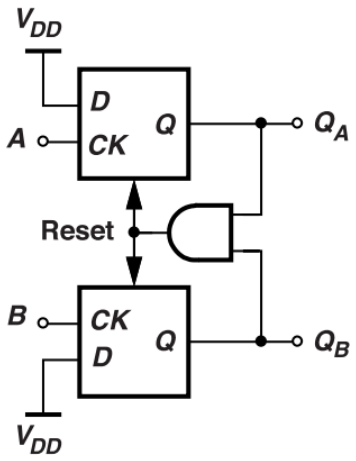


Figure 1.15: PFD implementation. [2]

Most PFDs are not directly connected to the loop filter, another block is included between the two, it is called a Charge Pump (CP). More details will be provided about the design of the PFD and the CP in chapter 2.

1.6 Loop Filter

In PLL design, a loop filter is a crucial block in the circuit, it is placed between the PD and VCO. The primary function of the LF is to filter out the noise and the unwanted ac harmonics present at its input (harmonics from the output of the PD), to provide a smooth dc output that is proportional to the phase error.

The dc output is then fed to the VCO to regulate the feedback output frequency. Since the LF passes the low frequencies and blocks the higher frequencies, it is then considered a Low Pass Filter LPF. Several types of loop filters are used in PLL circuits, such as passive RC filters, active filters, and digital filters. The choice of filter type depends on the application and the PLL type. [1]

1.6.1 Passive Filters

In many PLL designs, first-order loop filters are used, a common type of passive LPFs is the Lead-Lag filter. The schematic of the passive lead-lag filter is shown in Figure 2.27,

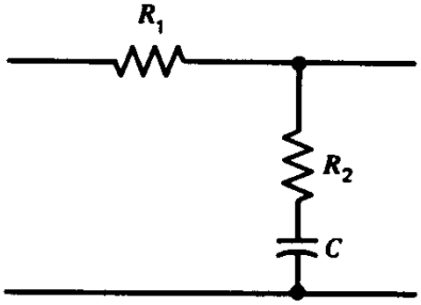


Figure 1.16: Schematic of a lead-lag filter. [5]

The transfer function $F(s)$ of a lead-lag filter has a zero and a pole, it is given by the following

equations.

$$F(s) = \frac{1 + sR_2C}{1 + s(R_1 + R_2)C}$$

By replacing R_1C and R_2C by the time constants τ_1 and τ_2 respectively, the transfer function $F(s)$ becomes

$$F(s) = \frac{1 + s\tau_2}{1 + s(\tau_1 + \tau_2)} \tag{1.9}$$

The frequency response function of a lead-lag filter has a pole at $\omega = \frac{1}{(R_1+R_2)C}$ and a zero at $\omega = \frac{1}{R_2C}$. The pole produces a phase lag, while the zero provides a phase lead.

The gain of the transfer function is calculated and given by,

$$|F(s)| = \sqrt{\frac{1 + \omega^2(R_2C)^2}{1 + \omega^2(R_1 + R_2)^2C^2}} \tag{1.10}$$

Therefore, at lower frequencies, the gain $|F(s)|$ is 1. But at higher frequencies, the filter acts as a resistive divider with gain $|F(s)|$ equal to $\frac{R_2}{R_1+R_2}$. Figure 1.17 depicts the bode diagram of an ideal lead-lag filter.

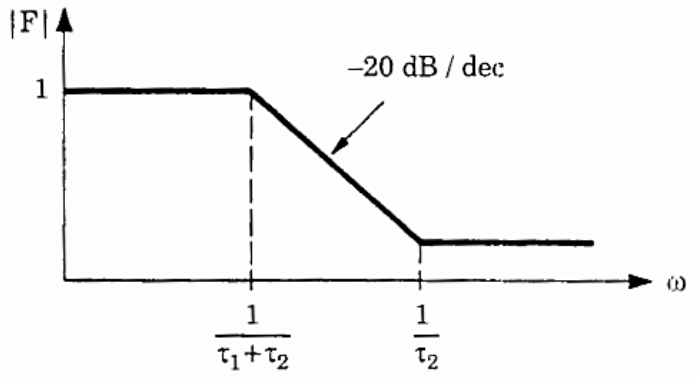


Figure 1.17: Bode plot of a lead-lag filter. [1]

1.6.2 Active Filters

Active filters are another common type that helps to ensure the stability and accuracy of the system by removing unwanted noise and signals from the input and output signals. The schematic of the active lead-lag filter is shown in Figure 1.18.

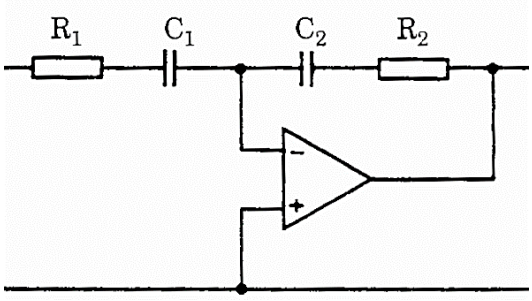


Figure 1.18: Schematic of an active lead-lag filter. [1]

The transfer function $F(s)$ of the active lead-lag filter is similar to the passive's one, it is given by the following equations.

$$F(s) = K_a \frac{1 + sR_2C_2}{1 + sR_1C_1}$$

As it was done in the passive filer, R_1C_1 and R_2C_2 are replaced by the time constants τ_1 and τ_2 respectively, the transfer function $F(s)$ is shown in equation 1.11. The term K_a represents is the gain, and it is equal to C_1/C_2.

$$F(s) = K_a \frac{1 + s\tau_2}{1 + s\tau_1)} \tag{1.11}$$

The amplitude response of the active lead-lag filter is depicted in Figure 1.19

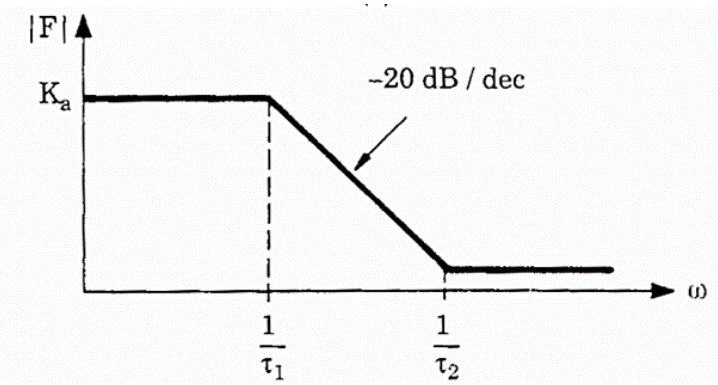


Figure 1.19: Bode plot of an active lead-lag filter. [1]

1.7 Voltage Controlled Oscillator

Before jumping straight into VCOs, it is important to understand some generalities about oscillators. In the next subsection, some essential information related to oscillators is discussed.

1.7.1 Generalities About Oscillators

An oscillator is an electronic circuit that is able to generate periodic signals, such as a sine wave, square wave, or triangle wave. In practice, an oscillator is a system that consists of an amplifier and negative feedback.

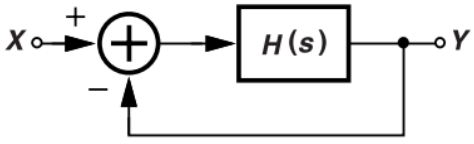


Figure 1.20: Simple feedback system. [2]

Figure 1.20 depicts the block diagram of a simple feedback system whose closed-loop transfer function is given by,

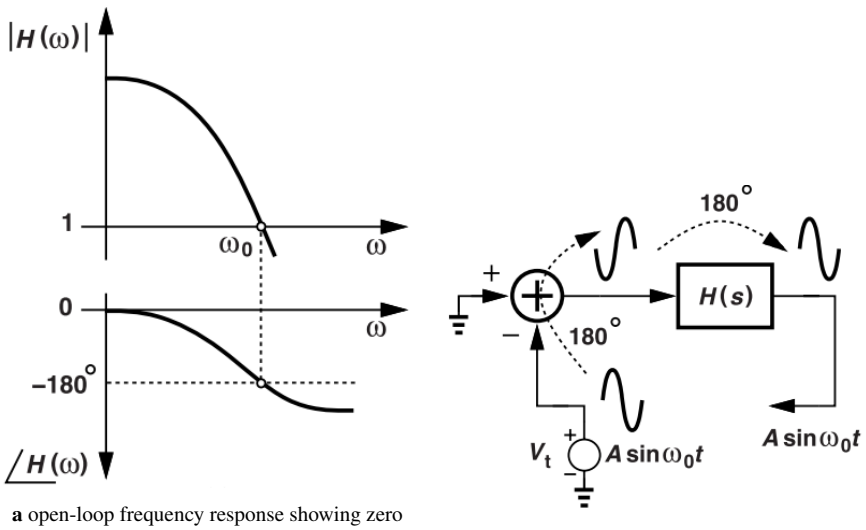
$$\frac{Y(s)}{X(s)} = \frac{H(s)}{1 + H(s)} \tag{1.12}$$

In order to create oscillations, the negative-feedback system should be unstable, this property is the necessary condition for an oscillation. It is clear that if the denominator is zero, this implies $H(s) = -1$. Therefore, If $H(s) = -1$ at a certain frequency ω_0, that is $H(j\omega_0) = -1$, then the open-loop frequency response exhibits a unity magnitude and a 180° phase shift at ω_0. These conditions are called *"Barkhausen's" criteria* for oscillation and are summarized in equation 1.13 and 1.14 and Figure 1.21a. [2]

$$|H(j\omega_0| = 1 \tag{1.13}$$

$$\angle H(j\omega_0) = 180^\circ \tag{1.14}$$

In Figure 1.21b, an example of a sinusoid is shown, where it's really important to note that the feedback signal is in phase with the test voltage, V_t. Thus, the loop contains a 180° phase shift due to the negative feedback and another 180° phase shift due to the open loop transfer function $H(s)$ resulting in the same sinusoid.



a open-loop frequency response showing zero phase margin

b propagation of a sinusoid at ω_0 around the loop

Figure 1.21: Barkhausen's criteria for oscillations. [2]

Different types of oscillators exist, the classification is based on the shape of the output waveform, the nature of the frequency of the output waveform...etc

If the shape is of concern, they can be divided into two groups: harmonic oscillators (also known as linear oscillators) and relaxation oscillators.

A harmonic oscillator is a circuit that generates a sinusoidal waveform at a fixed frequency. Reactive components, such as inductors or capacitors, and resistors, are typically used in the circuit. Examples of harmonic oscillators in electrical systems include LC oscillators, crystal oscillators, and RC oscillators. While a relaxation oscillator is a circuit that generates a non-sinusoidal waveform including triangular, square, and sawtooth waveforms. The circuit typically consists of a feedback loop that includes a non-linear element for switching, such as a diode or transistor, and a reactive component for storing and releasing energy, such as a capacitor.

Moreover, if the classification depends on the nature of the frequency of the output waveform, then two types are mentioned: fixed frequency oscillators and variable or tunable frequency oscillators. The tunable frequency oscillators allow the frequency of the output signal to be adjusted over a

certain range by just tuning the applied voltage. One example of these oscillators is the voltage-controlled oscillator (VCO).

1.7.2 VCO Parameters and Models

As explained in the previous subsection, the frequency of an oscillator can be adjusted by either varying electronically a parameter within the oscillator, such as a resistance, a capacitance, or an inductance. This technique is used for fixed-frequency oscillators. If the control is a voltage quantity, we call the circuit a voltage-controlled oscillator (VCO).

The VCO is characterized by its tuning range and its gain, where the frequency is linearly proportional to the voltage applied to its control input. This relationship is described by equation 1.15, [2]

$$\omega_{out} = K_{VCO} V_{cont} + \omega_0 \tag{1.15}$$

where K_{VCO} is the "gain" of the VCO and is expressed in $rad/s/V$ or Hz/V and ω_0 is the free running frequency of the VCO. Figure 1.22 depicts the VCO tuning range characteristics, where ω_{out} varies linearly with V_{cont} in the range $[V_1; V_2]$ with a slope K_{VCO}.

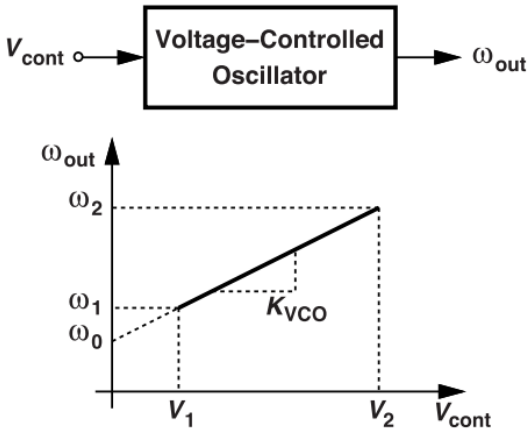


Figure 1.22: VCO tuning characteristic. [2]

Some important parameters of VCOs are the tuning range where the VCO must be adjustable over the range that the PLL is expected to operate over. The tuning gain is also of concern, it is the tuning shift for a given change in voltage. The gain of a VCO affects some of the overall loop design considerations and calculations. Phase noise is another essential performance parameter, it refers to the phase fluctuations or jitter in the output signal, the factors that effect the phase noise are device noise, power supply noise, and circuit non-idealities. [3]

According to *Behzad Razavi* [2, p. 45], VCOs can be represented by one of three models:

1. A static system characterized by $\omega_{out} = K_{VCO} V_{cont} + \omega_0$ if the output frequency is of interest.
2. A system generating $V_{out} = V_0 cos[\omega_0 t + K_{VCO} \int V_{cont}(t) dt]$ if the output waveform is of interest.
3. If the phase error ϕ_e is of interest, It is an ideal integrator characterized by

$$\frac{\phi_e}{V_{cont}} = \frac{K_{VCO}}{s} \tag{1.16}$$

In PLL design, the last model is interesting, because it relates between the V_{cont} that is generated by the LF and the phase error ϕ_e produced at the output of the VCO. The VCO can be modeled

as an integrator because the output frequency is proportional to the integral of the control voltage V_{cont} over time. Note that this model provides a simple and intuitive way to analyze and design VCO circuits.

1.8 PLL Transfer Function

In order to evaluate the stability of the PLL loop, the filtering properties, and the behavior of the loop in the time domain, the transfer function must be determined. The Transfer function $H(s)$ which is defined as ϕ_{out}/ϕ_{in} is derived after modeling each block of the PLL loop.

- The mathematical model of the phase detector is simply a gain block K_{PD}
- The loop filter is represented with its own transfer function $F(s)$, it has been derived in equation 1.9 for a lead-lag filter.
- The VCO is considered an integrator with a gain K_{VCO}, thus its transfer function is K_{VCO}/s

The figure shown below represents the linear model of a PLL, where each block is represented in the s domain.

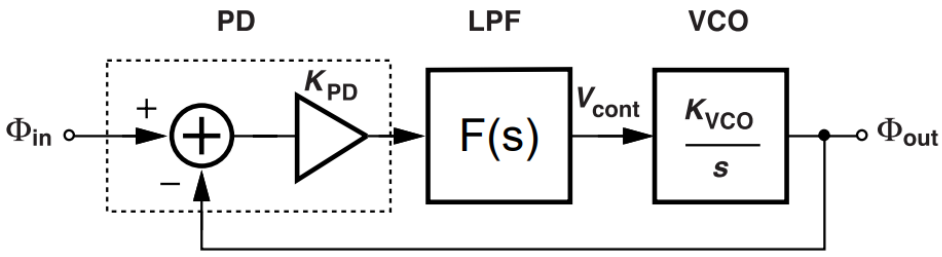


Figure 1.23: Linear model of simple PLL. [2]

The depicted block diagram in Figure 1.23 allows to find the open loop transfer function, $H'(s)$, it is given by the following formula,

$$H'(s) = \frac{K_{PD}K_{VCO}F(s)}{s} \tag{1.17}$$

It follows that the closed-loop transfer function is given by

$$H(s) = \frac{\phi_{out}}{\phi_{in}} = \frac{H'(s)}{1+H'(s)} = \frac{\frac{K_{PD}K_{VCO}F(s)}{s}}{1+\frac{K_{PD}K_{VCO}F(s)}{s}}$$

multiplying the numerator and the denominator by s results in equation 1.18

$$H(s) = \frac{K_{PD}K_{VCO}F(s)}{s+K_{PD}K_{VCO}F(s)} \tag{1.18}$$

Therefore, for a passive lead-lag filter, the closed-loop transfer function is

$$H(s) = \frac{K_{PD}K_{VCO}\frac{1+s\tau_2}{1+s(\tau_1+\tau_2)}}{s+K_{PD}K_{VCO}\frac{1+s\tau_2}{1+s(\tau_1+\tau_2)}} \tag{1.19}$$

In control theory, it is a common to write the denominator of $H(s)$ in the normalized form, where

$$Denominator = s^2 + 2\zeta\omega_n s + \omega_n^2$$

ω_n is called the natural frequency and ζ is the damping factor. So from the transfer function of the lead-lag filter given in equation 1.19, one can show that ω_n, ζ and $H(s)$ are as follows,

$$\omega_n = \sqrt{\frac{K_{PD}K_{VCO}}{\tau_1+\tau_2}},\ \zeta = \frac{\omega_n}{2}\left(\tau_2 + \frac{1}{K_{PD}K_{VCO}}\right) \tag{1.20}$$

$$H(s) = \frac{s\omega_n\left(2\zeta - \frac{\omega_n}{K_{PD}K_{VCO}}\right)}{s^2+2\zeta\omega_n s+\omega_n^2} \tag{1.21}$$

Another important parameter in the above equations is the *loop gain*, which is the product of the PFD gain and the VCO gain, that is $K_{PD}K_{VCO}$. The loop gain classifies the PLL system into a low-gain loop or a high-gain loop. If the condition,

$$K_{PD}K_{VCO} >> \omega_n$$

Then, the PLL is said to be a high-loop gain. Most PLLs are high-loop gain and this results to approximate equation 1.21 and get equation 1.22.

$$H(s) \approx \frac{2\zeta\omega_n s+\omega_n^2}{s^2+2\zeta\omega_n s+\omega_n^2} \tag{1.22}$$

1.9 PLL Order and Type

According to *GARDNER*, the PLL type is defined by the number of perfect integrators present in the loop. Since the VCO is modeled as an integrator, the PLL is always considered a Type I system. The type number increases if the LF includes an integrator.

The order of the PLL, on the other hand, is defined by the highest power of the transfer function's denominator, and thus by the number of poles.

If these definitions are applied to the previous PLL model, and from equation 1.22, we conclude that the system is a *type I second-order high-gain PLL* because the highest power in the denominator is 2 and there exists only one integrator (VCO). Second-order PLLs are usually simple to implement and have good performance.

Figure 1.24 depicted below represents the bode plot of the transfer function $H(s)$ in dB versus the ratio (ω/ω_n) for different ζ values. This bode plot is valid for every second-order high-gain PLL.

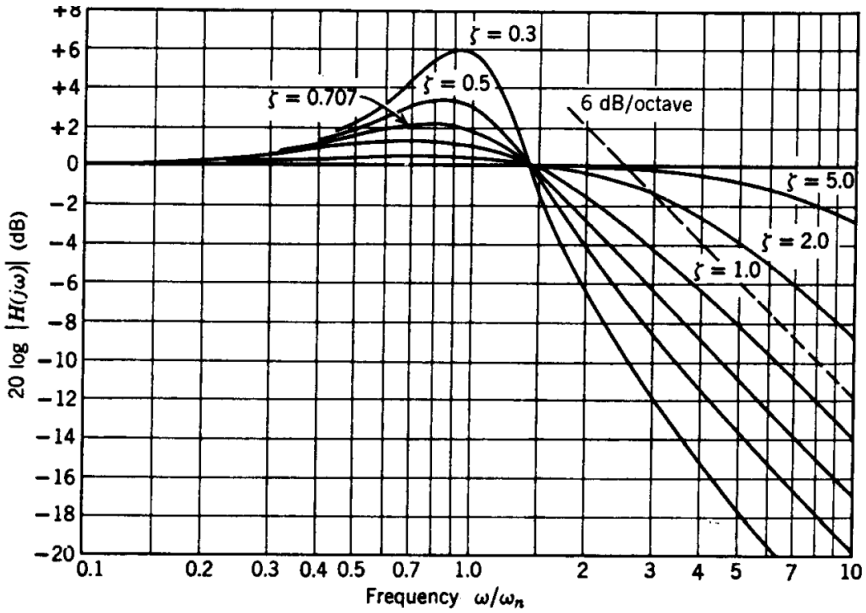


Figure 1.24: Frequency response of a high-gain second order PLL. [5]

The response of the PLL in the figure is similar to that of a low-pass filter. Note that the damping factor ζ has an important influence of the response.

The following points summarize the effect of ζ on the performance of the PLL. [1,3]

- If $\zeta << 1$

  The transient response becomes oscillatory; the smaller the damping factor, the larger the overshoot.

- $\zeta = 1$

  The system is critically damped, the system responds quickly to changes in the input signal without overshoot.

- $\zeta = \frac{\sqrt{2}}{2} = 0.707$

  The system performance is similar to that of a second-order Butterworth low-pass filter. The response time is slower and the settling time is longer than in a critically damped system. However, the phase response is stable and does not exhibit overshoot.

- $\zeta >> 1$

  The transfer function $H(s)$ flattens out, the response time is very slow and the settling time is very long. This means that the PLL may not be able to respond quickly to changes in the input signal.

The bandwidth of a second-order PLL is frequently defined as the radian frequency ω_{3dB} at which the phase response of the PLL loop filter reaches $-3dB$. It is commonly known as the *"3 dB bandwidth."*

The bandwidth is computed by solving equation 1.23 for ω.

$$|H(j\omega|^2 = 0.5 \tag{1.23}$$

The solution of equation 1.23 is given by ω_{3dB} as follows,

$$\omega_{3dB} = \omega_n \left[1 + 2\zeta^2 + \sqrt{(1+2\zeta^2)^2 + 1}\right]^{1/2} \tag{1.24}$$

The $3dB$ bandwidth indicates the frequency at which the PLL gain begins to decrease. At frequencies above the $3dB$ bandwidth, the gain of the PLL decreases as frequency increases, this results in filtering out the high-frequency noise and disturbances in the input signal. [1]

1.10 PLL Applications

PLLs have a wide range of applications in electronics and communication. A PLL's output can be used to generate a stable clock signal, recover data from a noisy signal, synthesize a new frequency, control the speed of a motor...etc. In this section, we discuss some of these applications.

- **Frequency synthesis**

  PLLs allow designers to generate an output signal with a frequency that is a multiple of the reference signal frequency. Figure 1.25 shows the block diagram of a synthesizer. Note that the feedback is not unity anymore, it contains a feedback divider that will generate $N \times f_{ref}$ if it is in parallel with the open loop.

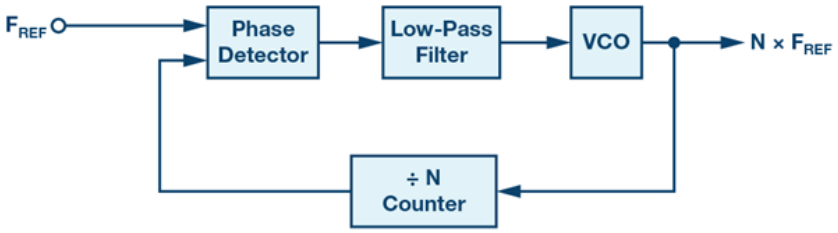


Figure 1.25: Block diagram of a PLL synthesizer. [6]

  This application is really useful in radio communication, where different frequencies are required for different channels. It is also used to generate local oscillator (LO) signals for the up and down conversion of RF signals. Figure 1.26 shows how a $900\,MHz$ output frequency is generated starting from a $13\,MHz$ reference frequency.

  First, a series input counter R reduces the reference f_{ref} by a factor of 65, the frequency present at the input of the PFD is given by $f_{PFD} = f_{ref}/R = 13\,MHz/65 = 200\,KHz$. Then, this frequency is now synthesized with the help of another counter N that multiplies f_{PFD} by N, therefore, $f_{out} = N \times f_{PFD} = 200\,KHz \times 4500 = 900\,MHz$.

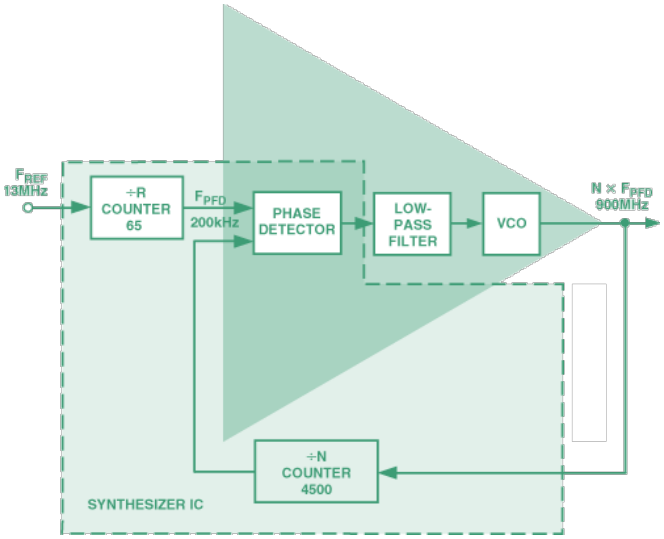


Figure 1.26: PLL as a synthesizer. [7]

- **FM demodulation**

  The function of a PLL FM demodulator is based on comparing the phase of the input FM signal with a stable reference signal, generated by a crystal oscillator. The phase detector's output is filtered by the LF and fed back to the VCO, which adjusts its frequency to keep a constant phase relationship with the input signal. This feedback loop causes the oscillator to track the variations in the frequency of the FM signal, and the frequency difference between the oscillator and the input signal is the demodulated output. [8]

  PLL FM demodulators have many advantages over other FM demodulation techniques. They are less susceptible to noise and distortion and produce a more stable output signal. Most importantly, they can be easily implemented using integrated circuits, making FM demodulation a low-cost solution. [8]

  LM565 and CD4046 are some common PLL ICs that may be used as FM demodulators or frequency synthesizers.

  Figure 1.27 shows an example of the connections of the CD4046B as an FM demodulator. For this example, an FM signal consisting of a $10\,kHz$ carrier frequency was modulated by a $400\,Hz$ audio signal. Note that the VCO center frequency is equal to the FM carrier frequency, thus an XOR PD is used (XOR PD is also referred to as Type I PD).

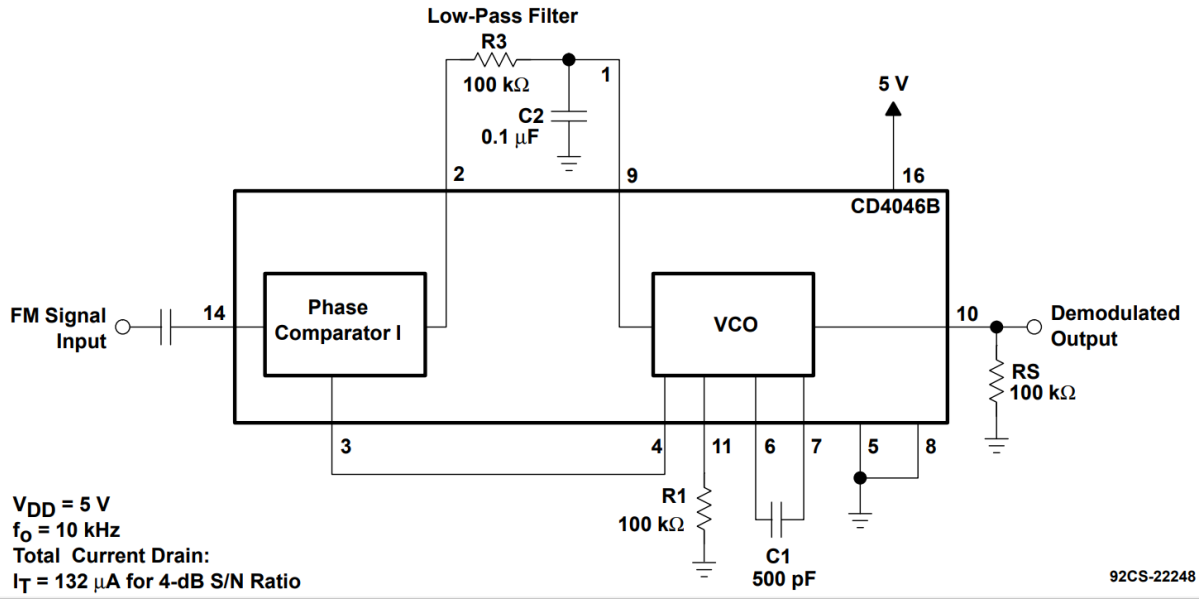


Figure 1.27: FM demodulator using CD4046. [9]

- **Frequency and phase tracking**

  PLLs can be used to track and maintain the frequency and phase of a signal in real-time, which is important in applications such as radar, sonar, and GPS systems. For instance, in a GPS system, a PLL can be used to track the frequency and phase of the GPS signal and adjust the timing of the receiver to match the GPS signal. This allows the GPS receiver to accurately determine the location and timing information.

1.11 Conclusion

In this introductory chapter, many essential concepts related to Phase Locked Loops design were explained. We have discussed the operating principles of PLLs, and the different types of PLLs (ADPLL, DPLL, APLL). We have also explored the characteristics of the phase detector (analog and digital), loop filters and their transfer functions, and oscillator types including voltage-controlled oscillators.

Moreover, the transfer function and dynamics of second-order PLLs and their corresponding formulas were shown. Finally, we have examined some of the many applications of PLLs, such as clock generation, frequency synthesis, and demodulation. we also conclude that it is extremely important to understand these principles before starting the design and the implementation of any phase-locked loop. In the next chapter, the design and simulation of a digital PLL (DPLL) will be covered.

Chapter 2

Design and Simulation of a Digital PLL

2.1 Introduction

As discussed in the previous chapter, Phase Locked Loops are widely used in communication systems for their ability to synchronize signals and track frequency offsets. PLLs are also of different types such as Analog PLL (APLL), Digital or Mixed-signal PLL (DPLL), All Digital PLL (ADPLL)... etc

In this chapter, we present the design and implementation of a Digital or Mixed-signal Phase Locked Loop (DPLL) for GPS synchronization. Our objective is to design a DPLL that synchronizes with a 1 KHz reference signal and achieve high precision and stability. The design and implementation of the DPLL involve designing and simulating each block diagram in open loop, which means designing the PFD, the VCO, and the LF separately and discussing their performance. Then, the closed loop DPLL system is constructed to study its behavior and to determine its ability to synchronize with the 1 KHz reference signal. The simulation and design procedures are carried out using **Multisim** software, which is a powerful tool for simulating, analyzing and providing reasonably accurate predictions of the PLL circuit behavior. Some details regarding this software are provided in the Appendix.

2.2 Design of Phase Frequency Detector (PFD)

The first building block in the DPLL is the PD. Multiple PDs exist as it was mentioned in Chapter 1 such as XOR PD, JK PD, and PFD... Since we are dealing with digital signals, The optimal type that should be selected in the design is the PFD or a Type IV PD [1].
The PFD detects the phase and the frequency difference with high accuracy compared to the other PDs. Moreover, it has a wide lock-in range, which means it can detect phase differences over a large range of frequencies. On top of that, it provides information about the phase relationship between the input signals, indicating which signal is leading or lagging.

PFDs are frequently employed in digital phase-locked loops, they are circuits that produce a stable output signal. The phase and frequency of the output signal and the reference signal are compared by the PFD, and a control signal is generated to adjust the output signal to track the reference signal.

In Multisim environment, we start by setting the parameters of the reference signal, whose frequency is 1 KHz and its duty cycle is 50%. This is done by selecting a PULSE_VOLTAGE generator from

the SIGNAL_VOLTAGE_SOURCES section. We have also created another PULSE_VOLTAGE generator for the second input and it refers to the feedback signal. The feedback signal parameters are similar to that of the reference, which means that the frequency is also 1 KHz and its duty cycle is 50%.

Figure 2.1 depicts the circuit of a PFD, where 2 D flip-flops (**4013BP**) and one AND gate (**4081BP**) are used. These ICs were selected because they belong to the CMOS family, which is a widely used digital logic technology for its low power consumption and high noise immunity.

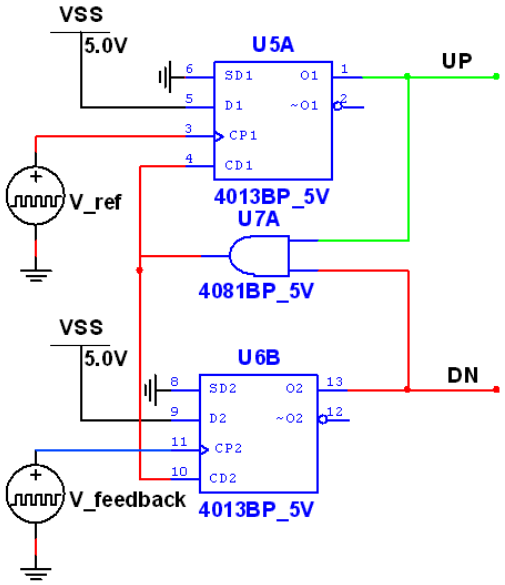


Figure 2.1: Schematic of phase frequency detector in Multisim.

The **4013BP** is a digital integrated circuit (IC) that contains four D flip-flops. Each flip-flop has a single data input (D), a clock input (CLK), a clear input (CLR), and complementary outputs (Q and $\overline{Q}$). The chip operates with a power supply voltage of 5V and is typically used for data storage and for timing control.

4081BP is a commonly used IC that provides simple and reliable logical AND operations in digital logic circuits, it contains four two-input AND gates and operates with a power supply voltage of 5V.

Note that the reference signal is connected to the (CLK) pin of the 1st D flip-flop, and the feedback signal is connected to the (CLK) pin of the 2nd D flip-flop. This PFD outputs two signals, UP and DN which are fed to the inputs of the AND gate, then its output is connected to (CLR) pin of each FF.

The basic operation of a PFD involves comparing the rising and falling edges of the input signals to detect phase differences. Thus, three cases are discussed.

- **If** V_{ref} **leads** $V_{feedback}$

  The rising edge of V_{ref} occurs first, then UP goes HIGH while DN remains LOW, once the rising edge of DN occurs, UP goes LOW. This generates a pulse whose width is equal to the phase difference as shown in Figure 2.2.

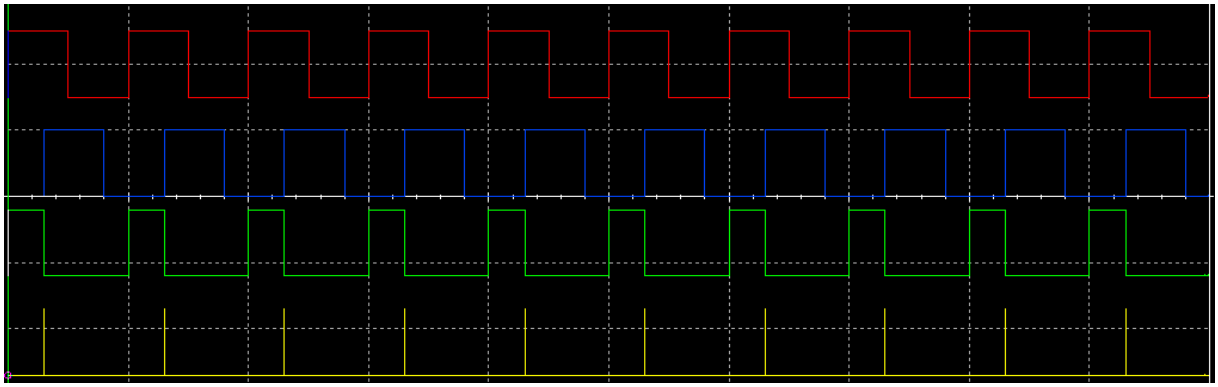


Figure 2.2: Case I: V_{ref} (in red) leads V_{fb} (in blue), UP in green and DN in yellow .

- **If V_{ref} lags $V_{feedback}$**

  The inverse happens, DN goes HIGH while UP remains LOW, once the rising edge of UP occurs, DN goes LOW. This also generates a pulse whose width is equal to the phase difference as shown in Figure 2.3.

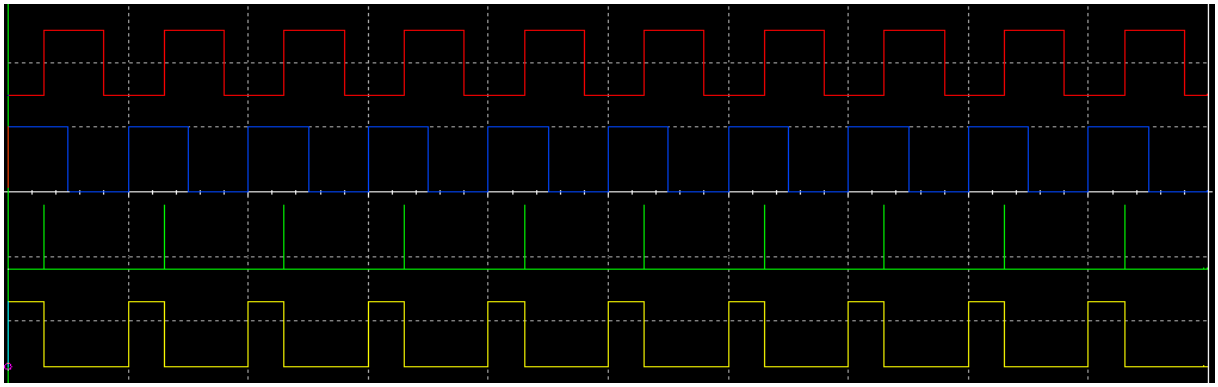


Figure 2.3: Case II: V_{ref} (in red) lags V_{fb} (in blue), UP in green and DN in yellow .

- **If V_{ref} and $V_{feedback}$ are in phase**

  When both V_{ref} and V_{fb} are in phase, UP and DN are high, the AND gate will then reset the 2 D flip flops and make them low as depicted in Figure 2.4. note that UP and DN are not perfectly zero, some glitches appear at each rising edge, this is due to the delay of the D FF.

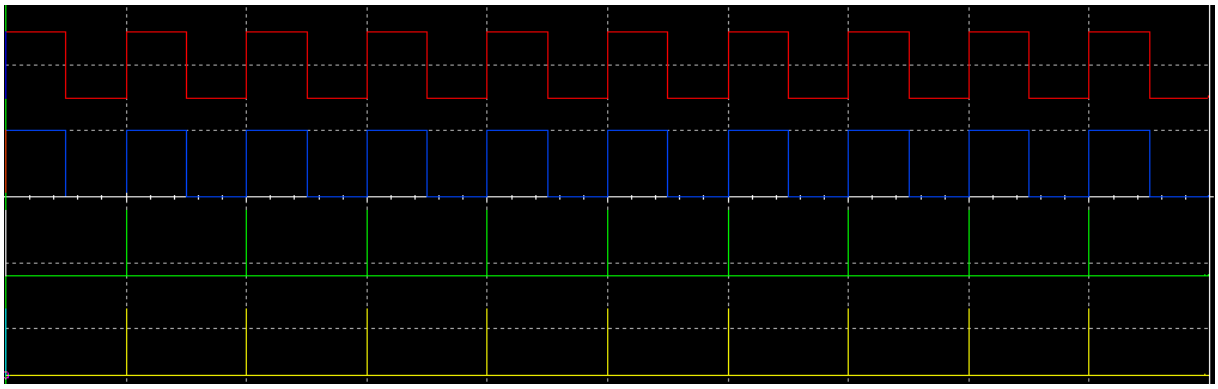


Figure 2.4: Case III: V_{ref} (in red) and V_{fb} (in blue) are in phase, UP in green and DN in yellow .

Note that these results are obtained when the frequencies of the two inputs are equal, but there is a phase difference between them, this phase error is detected by the PFD.

If the frequency of the feedback signal is set to another frequency, say $800\,Hz$, the output signals UP and DN are depicted in Figure 2.5.

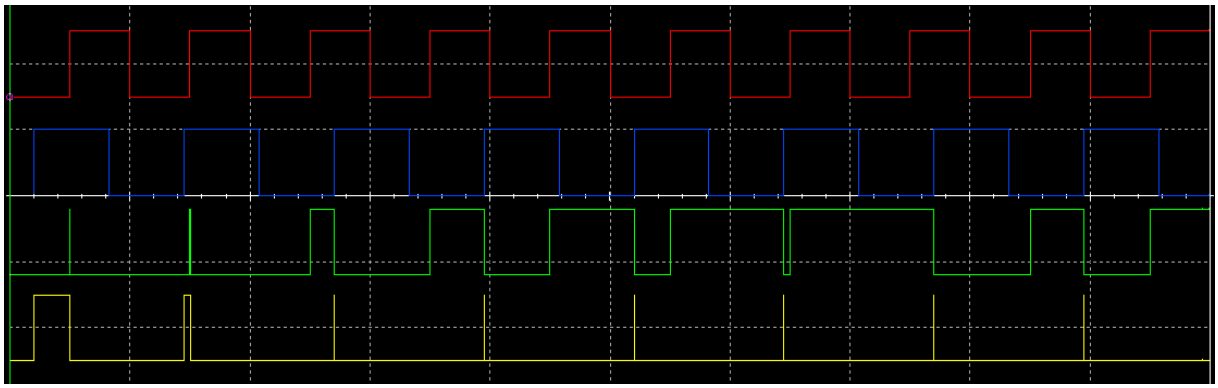


Figure 2.5: Outputs UP (in green) and DN (in yellow) when V_{ref} (in red) and V_{fb} (in blue) are not equal in frequencies.

Since the frequency of the reference signal is higher than that of the feedback, the PFD detects this difference by generating pulses in the UP signal, while DN stays low. On the other hand, if the frequency of the reference signal is lower, the pulses will be generated in the DN signal, and UP remains low. We conclude that the PFD is a circuit that detects both the phase and frequency difference between two input signals by knowing which signal is leading or lagging.

PFD is usually referred to as a tristate PFD, which means that the PFD has three outputs: UP, DN, and $RESET$. When V_{ref} is leading, then UP is high and the PFD is on "state $+1$". On the other hand, if V_{fb} is leading, then DN is high and the PFD is switched to "state -1". However, when both V_{ref} and V_{fb} are in phase, UP and DN are high, the AND gate output goes high to reset them, thus RST is activated, we say that the PFD is on "state 0". These results are summarized in Table 2.1 and in Figure 2.6

V_{ref}	V_{fb}	UP	DN	$State$
Leading	Lagging	1	0	+1
Lagging	Leading	0	1	-1
In phase	In phase	0	0	0

Table 2.1: Tristate PFD

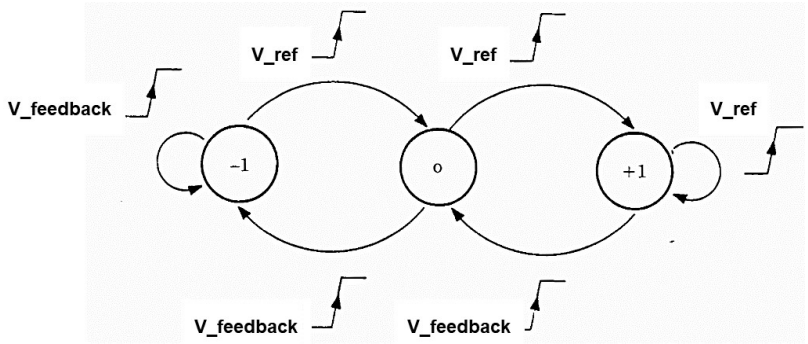


Figure 2.6: State diagram of the PFD. [1]

PFDs are classified into two types according to the output, a PFD can either have:

- Voltage output that represents the phase difference between the two input signals.
- Current output that is proportional to the phase difference between the input signals, such PFD is said to have a *charge pump* output.

In this design, the first approach is implemented. A PFD with voltage output is simpler to design and implement than a PFD with current output, as it does not require an additional charge pump circuit. They have wide operating frequency range and they can be easily integrated with other PLL components, such as loop filters and VCOs.

To create such type of PFD, it is required to design some switches that control the output voltage V_{ctrl}. Figure 2.7 depicts the schematic that represents the final circuit of the PFD. The concept of this circuit is easy, if the PD is on *state* $+1$, the UP is high and DN is low, this leads to closing the upper switch and opening the lower one, thus V_{ctrl} is connected to V_{cc}. On the other hand, if the PD is on *state* -1, the DN is high and UP is low, this results in closing the lower switch and opening the upper one, therefore, V_{ctrl} is connected to GND. Finally, if *state* 0 is activated, both UP and DN are low, the switches are opened and V_{ctrl} will be in a "floating" state, this state is also known as high-impedance output state.

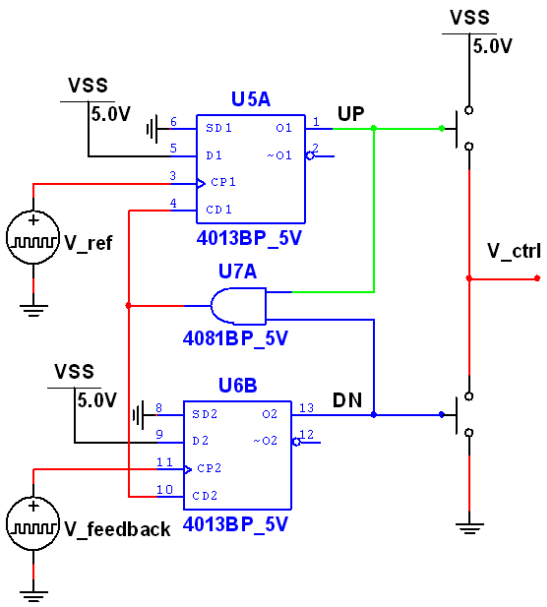


Figure 2.7: Schematic of phase frequency detector with an output voltage.

The design of the switches requires using MOSFETs since they have many advantages. MOSFETs have a **high input impedance**, so they draw very little current from the driving circuitry. They also have **low ON resistance**, which results in low power dissipation and low voltage drop across them. Most importantly, MOSFETs have **fast switching speeds**, making them suitable for use in PLL applications. Finally, MOSFETs are easily **controlled using a voltage signal** such as UP and DN. [10]

The upper switch in Figure 2.7 is replaced with an Enhancement-mode PMOS transistor, while the lower one is replaced by an Enhancement-mode NMOS transistor.

The NMOS transistor is ON if it's in the saturation or linear region. This condition is fulfilled if the voltage between the GATE and the SOURCE V_{GS} is much greater than V_{TH} the threshold voltage of the transistor ($V_{GS} > V_{TH}$). The NMOS is then treated as a low resistance R_{DS} or a closed switch [10].

Unlike NMOS, The PMOS transistor is in the saturation region if the voltage between the GATE and the SOURCE V_{GS} is much higher than V_{TH} the threshold voltage of the transistor ($V_{GS} > V_{TH}$). But since V_{TH} is negative, the Gate potential should be more negative with respect to the Source [10].

Figure 2.8 shows the conventional symbols of PMOS and NMOS transistors. It's important to mention that in an NMOS transistor, the conventional current flows from the Drain D to the Source S when the transistor is turned on. However, in a PMOS transistor when turned on, the conventional current flows from the Source S to the Drain D.

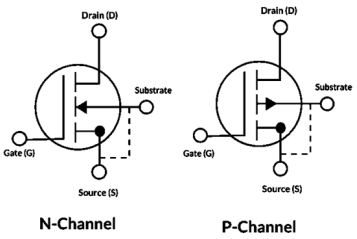


Figure 2.8: Symbols of enhancement mode MOSFET. [10]

The final schematic of the PFD with an output voltage is depicted in Figure 2.9, where the NMOS transistor **2N7000** and the PMOS transistor **BST110** were used with a power supply V_{DD} of $5\,Volts$.

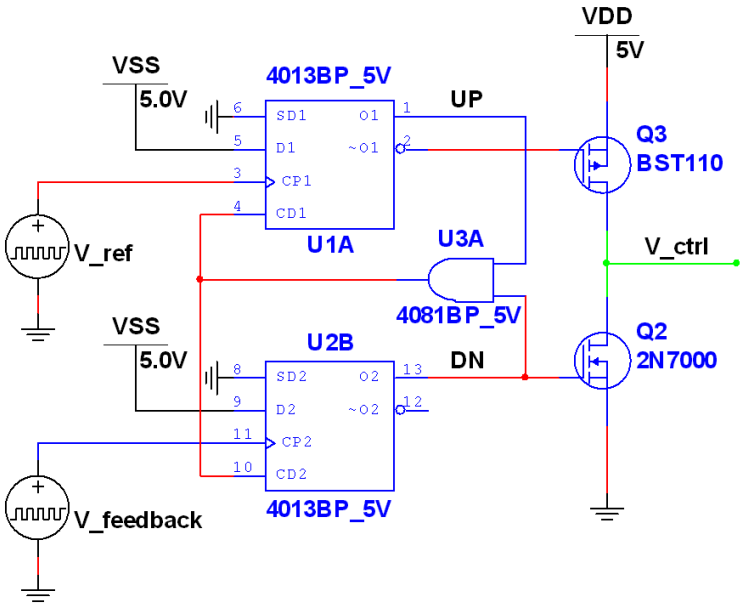


Figure 2.9: Final schematic of a PFD with output voltage.

The **2N7000** is an N-channel MOSFET transistor that is widely used in electronic circuits. It is a small signal transistor with a maximum voltage of 60 *volts* and a maximum current of 200 *mA*. The 2N7000 is used in our application as a switch to control the flow of current in the PFD. The typical threshold voltage of the 2N7000 MOSFET is around 2.1 *volts*, its resistance when being ON is 5Ω, and it is considered to be a fast transistor [11].

The **BST110** is also a small signal transistor with a maximum voltage of 50 *volts* and a maximum current of 250 *mA*. It is commonly used in electronic circuits as a switch or amplifier. The typical threshold voltage of the BST110 is around -1.5 *volts*, which means that a negative voltage must be applied to the gate to turn the transistor ON. Its maximum resistance when being ON is 10Ω The switching time of the BST110 is also similar to the 2N7000, typically in the range of a few nanoseconds [12].

For the PMOS transistor, the Source S_1 is connected to V_{DD}, and its Gate G_1 is connected to $\overline{UP}$, the complement of the signal UP. Concerning the NMOS, its Source S_2 is grounded while its Gate G_1 is connected to DN.

The connections among the signals UP and DN and the Gates G_1 and G_2 (which are the Gate pins of the PMOS and NMOS transistors respectively) are summarized in table 2.2.

V_{ref}	V_{fb}	UP	DN	V_{G_1}	V_{G_2}	V_{ctrl}
Leading	Lagging	1	0	0	0	+5 V
Lagging	Leading	0	1	+5 V	+5 V	0 V
In phase	In phase	0	0	+5 V	0	$HighZ$

Table 2.2: States of UP, DN and V_{ctrl} with respect to the voltage $V_{G_1S_1}$ and $V_{G_2S_2}$.

According to logic circuit design, the potentials V_{G_1} and V_{G_2} depend on the variables UP and DN. Note that the potentials V_{S_1} and V_{S_2} are fixed to $+5$ *volts* and 0 *volt* respectively.

From Table 2.2, it is clear that V_{G_1} is the complement of UP, whereas V_{G_2} is equal to DN. Therefore,

$$V_{G_2} = \overline{UP} \qquad V_{G_2} = DN$$

This explains why the Gate G_1 is connected to the complementary output of the first D FF and the Gate G_2 is directly connected to the output of the second D FF.

The PFD was tested in a simulation where it was first supposed that V_{ref} is leading, and then V_{ref} is lagging. Figures 2.10 and 2.11 show the variation of V_{ctrl} and the detection process of the PFD after simulation with Multisim.

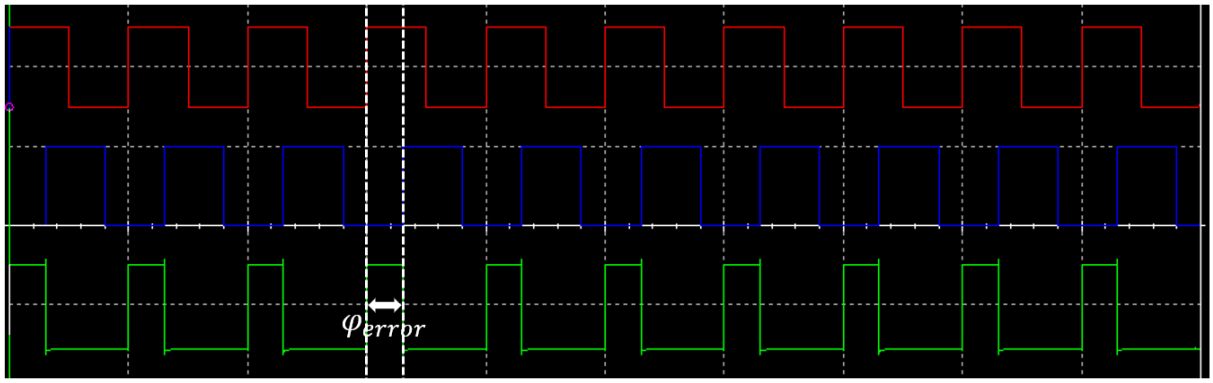


Figure 2.10: Case I: PFD output when V_{ref} is leading ($\omega_{ref} = \omega_{feedback}$ and $\phi_{error} \neq 0$).

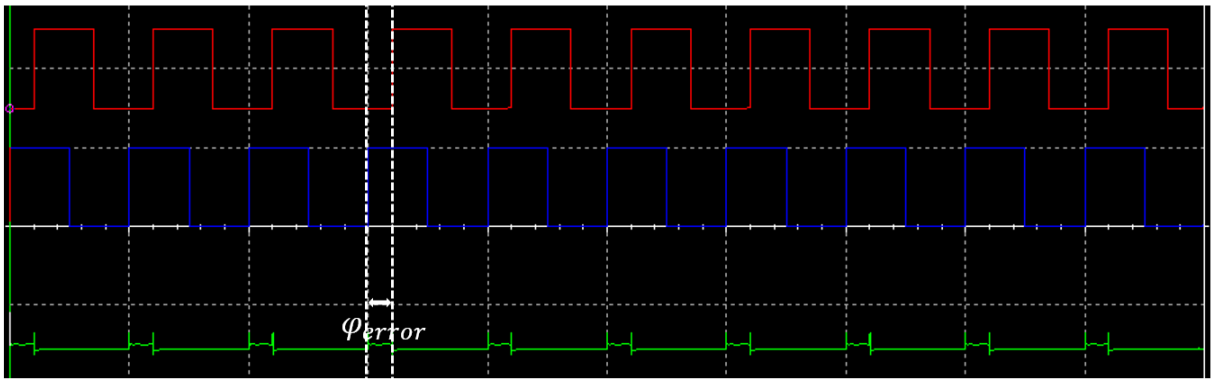


Figure 2.11: Case II: PFD output when V_{ref} is lagging ($\omega_{ref} = \omega_{feedback}$ and $\phi_{error} \neq 0$).

As it is shown in Figure 2.10, whenever V_{ref} proceeds, the PFD generates pulses of $5\,volts$ amplitude and width of ϕ_{error} to increase the frequency of the VCO until the feedback signal track the reference. However, case II, depicted in Figure 2.11, deals with the inverse scenario, the PFD generates pulses of $0\,volt$ amplitude and width of ϕ_{error} to decrease the frequency of the VCO until the feedback signal is locked with the reference. Hence, if the inputs' frequencies change, the PFD keeps detecting the differences and generates pulses to either decrease or increase the VCO output frequency to match the reference one.

2.3 Design of Voltage Controlled Oscillator (VCO)

The VCO is the building block that is responsible for generating the output signal that must be synchronized with the reference signal. The VCO is controlled by the *Control voltage* V_{ctrl} which

represents the dc output voltage generated by the LF. As discussed in Chapter 1, numerous types of VCO exist. But, since we aim to design a DPLL, a VCO that generates digital output voltages is needed. Thus, the type of VCO that was selected is the relaxation VCO. Relaxation VCOs can generate square, triangular, and sawtooth waveforms.

The proposed design of the relaxation VCO is built up of different components: storing components (capacitors) and a feedback loop, including switching components (transistors).
The VCO circuit consists of two main stages: an **Integrator** and an **Inverting Schmitt trigger**. The integrator is a circuit that is based on op-amps, its function is to integrate the dc input voltage V_{ctrl} over time, resulting in an output voltage that ramps up or down at a constant rate [13].
The Schmitt trigger is a comparator circuit that produces a square wave output when the input voltage reaches a certain threshold.

Figure 2.12 shows the schematic of a relaxation VCO based on an integrator and an inverting Schmitt trigger where V_{ctrl} and V_{out} are its input and output voltages respectively. Note that V_{ctrl} is a dc voltage while V_{out} is a square wave.

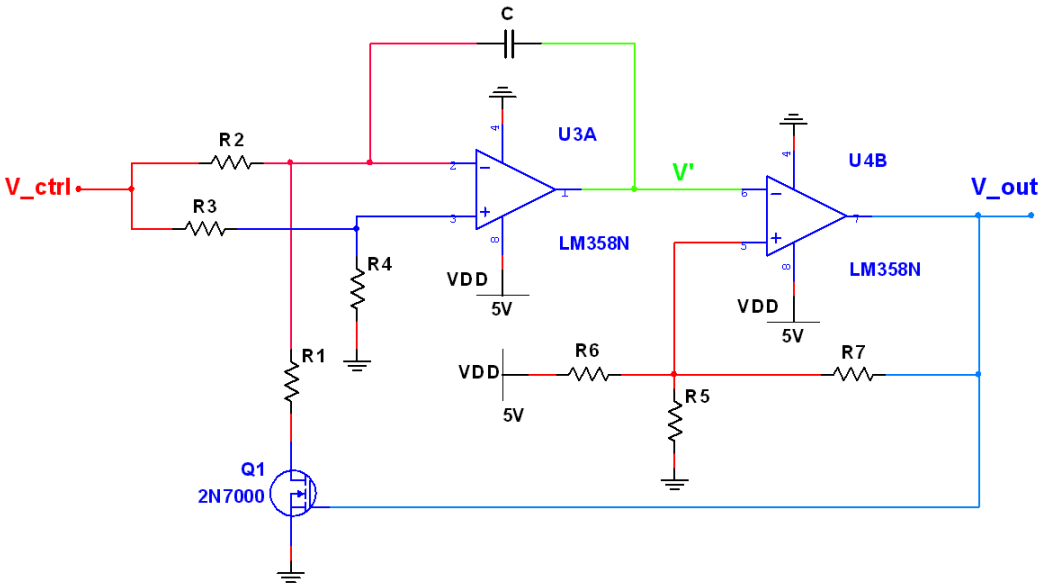


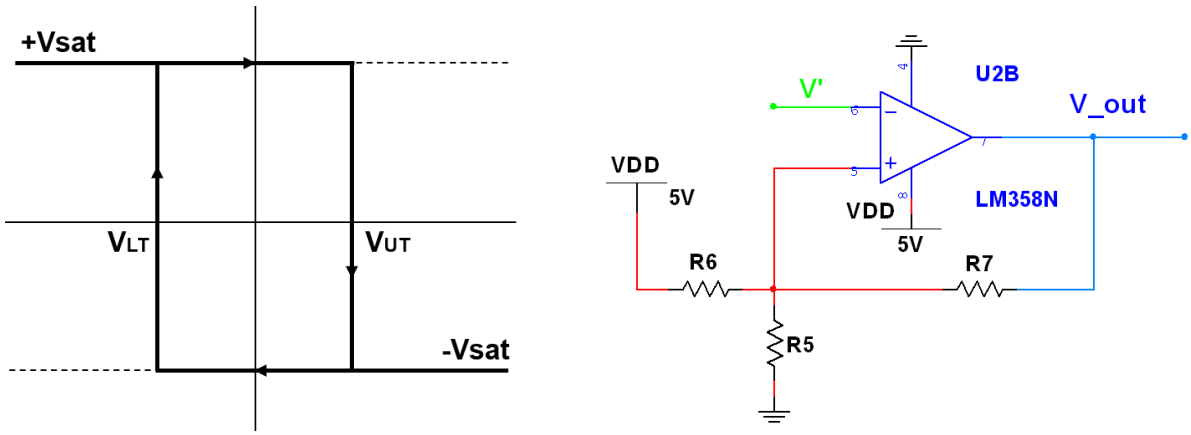
Figure 2.12: Schematic of a relaxation VCO.

The integrator stage consists of the resistors (R_1, R_2, R_3, R_4), the capacitor C and the op-amp $LM358$. The inverting Schmitt trigger stage includes the resistors (R_5, R_6, R_7) and the op-amp $LM358$. Note that the output of the integrator V' (in green) is fed to the inverting input of the Schmitt trigger, the output of the latter is then attached to the Gate of the NMOS transistor to form a feedback path.

2.3.1 Schmitt trigger stage

An inverting Schmitt trigger is a comparator circuit that generates an output with two stable states V_{sat}^{+} and V_{sat}^{-} (*sat* stands for *saturation*). The term *'inverting'* refers to the fact that input signal V' is applied at the inverting input of the operational amplifier. While the non-inverting input is set to a threshold voltage (V_{TH}). The Schmidt trigger differs from simple comparators by having two threshold voltages instead of one, they are defined as Upper Threshold Voltage (V_{UT}) and Lower Threshold Voltage (V_{LT}), thus the Schmidt trigger provides hysteresis. The presence of

hysteresis in a Schmitt trigger ensures that the output remains stable and immune to noise or small fluctuations in the input signal. [14]



a Transfer characteristics of an inverting Schmitt trigger.

b Inverting Schmitt trigger based on the LM358 op-amp.

Figure 2.13: The Schmitt trigger stage in the VCO schematic

Figure 2.13a depicts the transfer characteristics of the inverting Schmitt trigger. If the input voltage V_{out} is higher than V_{UT} or $(V' > V_{UT})$, the output V_{out} is LOW (V_{sat}^-), but if V' is lower than V_{LT} or $(V' < V_{LT})$, the output V_{out} turns HIGH (V_{sat}^+). Otherwise, V_{out} remains unchanged. Let's derive the threshold voltages V_{UT} and V_{LT} of the circuit shown in Figure 2.13b, which represents the second stage of the schematic shown in Figure 2.12.

- **Upper Threshold Voltage** V_{UT}

Applying KCL at the non-inverting $(+)$ input of the op-amp, we obtain the following,

$$\frac{V_{UT} - V_{DD}}{R_6} + \frac{V_{UT}}{R_5} + \frac{V_{UT} - V_{sat}}{R_7} = 0$$

If $R_5 = R_6 = R_7$, and $V_{sat} = V_{sat}^+$ the expression of the Upper Threshold voltage V_{UT} is,

$$V_{UT} = \frac{V_{DD} + V_{sat}^+}{3} \tag{2.1}$$

The resistors R_5, R_6, and R_7 are selected to be $1\,K\Omega$. The saturation voltage V_{sat}^+ is typically less than the supply voltage V_{DD}. It can vary depending on the specific op-amp being used. For $LM358$ op-amp, V_{sat}^+ was measured in the simulation and found to be $V_{sat}^+ = 3.76\,V$. Therefore,

$$V_{UT} = \frac{5 + 3.76}{3} = 2.92\,V$$

- **Lower Threshold Voltage** V_{LT}

By applying the same steps and considering $V_{sat} = V_{sat}^-$, V_{LT} is expressed as follows,

$$V_{LT} = \frac{V_{DD} + V_{sat}^-}{3} \tag{2.2}$$

The simulation indicated that the saturation voltage of the op-amp V_{sat}^- is $0.32\,V$. Hence,

$$V_{LT} = \frac{5 + 0.32}{3} = 1.77\,V$$

As a conclusion, for $R_5 = R_6 = R_7 = 1\,K\Omega$ and $V_{DD} = 5V$, if the input $V' > 2.92\,V$, the output voltage V_{out} saturates to $0.32\,V$. On the other hand, if $V' < 1.77\,V$, the output V_{out} flips to $3.76\,V$.

2.3.2 Integrator stage

At this stage, the resistors R_3 and R_4 are considered to be equal $(R_3 = R_4)$, they form a divider circuit whose output is fed to the non-inverting $(+)$ input of the first op-amp. Thus, the voltage V^+ at the non-inverting input is given by,

$$V^+ = \frac{R_4}{R_3 + R_4} V_{ctrl} = \frac{V_{ctrl}}{2}$$

The voltage levels at inverting and non-inverting inputs are equal to each other, that is $V^+ = V^-$ and therefore,

$$V^- = V^+ = \frac{V_{ctrl}}{2}$$

The resistor R_2 is twice the value of R_1. In this case, the current I flowing through R_2 is expressed in the following manner,

$$I = \frac{V_{ctrl} - V^-}{R_2} = \frac{V_{ctrl} - V_{ctrl}/2}{2R_1} = \frac{V_{ctrl}}{4R_1}$$

These parameters are essential to derive the expression of the frequency f of the output waveform with respect to the dc input voltage V_{ctrl}.

In the feedback path, the NMOS transistor Q_1 plays the role of a switch, it is controlled by the Gate to Source voltage V_{GS}. There are two possible situations to consider: Q_1 is open or Q_1 is closed.

Case I: *The transistor Q_1 acts as an open switch* ($V_{out} = V_{sat}^-$)

This case is satisfied only when V_{GS} is less than the threshold value of Q_1. This implies that V_{out} is LOW or $V_{out} = 0.32\,V$. When Q_1 is OFF, the schematic of the integrator stage becomes as it is depicted in Figure 2.14. No current flows through R_1 and the current I flows through both R_2 and C resulting in charging the capacitor. The integrator's output voltage V' is the integral of the dc voltage V^-, in other words, it is a ramp with a negative slope [13].

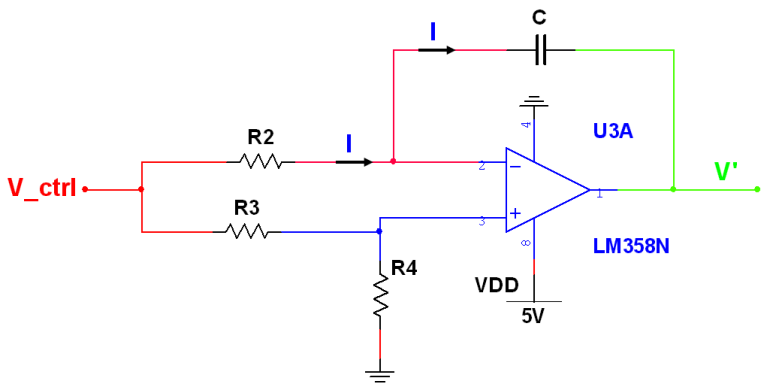


Figure 2.14: Schematic of the integrator when Q_1 is open.

Case II: *The transistor Q_1 acts as a closed switch* ($V_{out} = V_{sat}^{+}$)

As discussed in Case I, the voltage V' is a decreasing ramp, it keeps decreasing until it crosses V_{LT}; the Schmitt trigger changes its output level from V_{sat}^{-} to V_{sat}^{+}. This will result in closing the NMOS transistor and obtaining the circuit shown in Figure 2.16 [13].

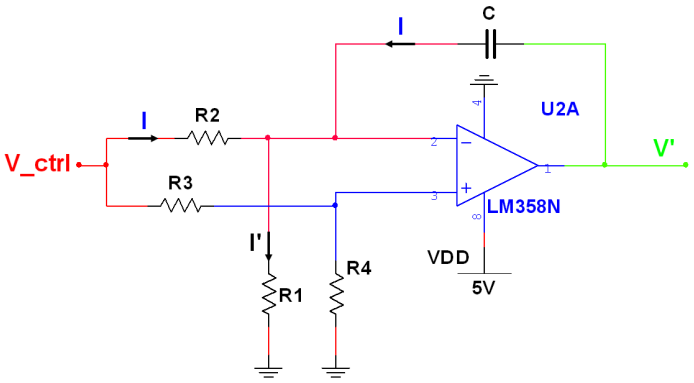


Figure 2.15: Schematic of the integrator when Q_1 is closed.

Unlike the first case, a current I' will flow through R_1. We can derive its expression using Ohm's law,

$$I' = \frac{V^{-}}{R_1} = \frac{V_{ctrl}/2}{R_1} = \frac{V_{ctrl}}{2R_1}$$

which can be rewritten as

$$I' = 2 \times \frac{V_{ctrl}}{4R_1} = 2I$$

Since I' is twice the value I, this implies that, according to KCL, the same current I will flow through C but in the opposite direction. This results in an increasing output ramp. V' will keep increasing until it crosses V_{UT} which forces the Schmitt trigger to switch its state from V_{sat}^{+} to V_{sat}^{-} and opens the switch Q_1. This process will continuously repeat at a constant rate. Hence, a square wave will be generated at the output of the Schmitt trigger [13].

The period of the square waveform depends on the charging and discharging time of the capacitor C. If q refers to the charge stored at C on charging phase or the discharging phase, then

$$q = C\,\Delta V = I\,\Delta t$$

where, $I = V_{ctrl}/(4R_1)$, $\Delta V = V_{UT} - V_{LT}$ and Δt is the time of either charging or discharging the capacitor.

Since we aim to design a relaxation VCO that generates a square wave with 50% duty cycle, the time of charging must equal the time of discharging. This implies that Δt is half of the period T.

$$\Delta t = \frac{T}{2} \implies q = C\,(V_{UT} - V_{LT}) = \frac{V_{ctrl}}{4R_1}\,\frac{T}{2}$$

It is concluded that the period of a 50% duty cycle square wave, generated by the relaxation VCO given in Figure 2.12, is given by

$$T = \frac{8R_1C(V_{UT} - V_{LT})}{V_{ctrl}} \tag{2.3}$$

Finally, the expression of the frequency f is deduced from equation 2.3,

$$f = \frac{1}{T} = \frac{V_{ctrl}}{8R_1C(V_{UT} - V_{LT})} \tag{2.4}$$

Since $V_{UT} - V_{LT} = 2.92 - 1.77 = 1.15\,V$, the frequency is approximated as the following,

$$f = \frac{1}{T} = \frac{V_{ctrl}}{8R_1C(2.92 - 1.77)} \approx \frac{0.11\,V_{ctrl}}{R_1C} \tag{2.5}$$

Note that equation 2.5 is valid only when: $R_2 = 2R_1$, $R_3 = R_4$, $R_5 = R_6 = R_7 = 1\,K\Omega$, and $V_{DD} = +5\,V$. The frequency is linearly related to the input voltage V_{ctrl}.

In the design of the DPLL, we suggest that the central frequency f_c (which was selected to be $1\,KHz$) is generated when the input voltage V_{ctrl} equals $V_{DD}/2$, that is $2.5\,V$. The operating frequency range of this VCO will depend on V_{ctrl} which ranges from $0\,V$ to $+5\,V$.
Let's compute the required R_1 and C, for a square wave of $f = 1\,KHz$ at $V_{ctrl} = 2.5\,V$. From equation 2.5, we obtain

$$R_1C = \frac{0.11V_{ctrl}}{f} = \frac{0.11 \times 2.5}{1000} = 2.75 \times 10^{-4}\,s$$

To unify the values of the resistors in the design, R_1 is fixed to $1\,K\Omega$. Thus, the appropriate capacitance C is,

$$C = \frac{2.75 \times 10^{-4}}{1000} = 2.75 \times 10^{-7} = 275\,nF$$

The remaining resistors are then selected as $R_3 = R_4 = 1\,K\Omega$ and $R_2 = 2\,K\Omega$. The complete schematic of the relaxation VCO with the appropriate resistors and capacitor is shown in Figure 2.16.

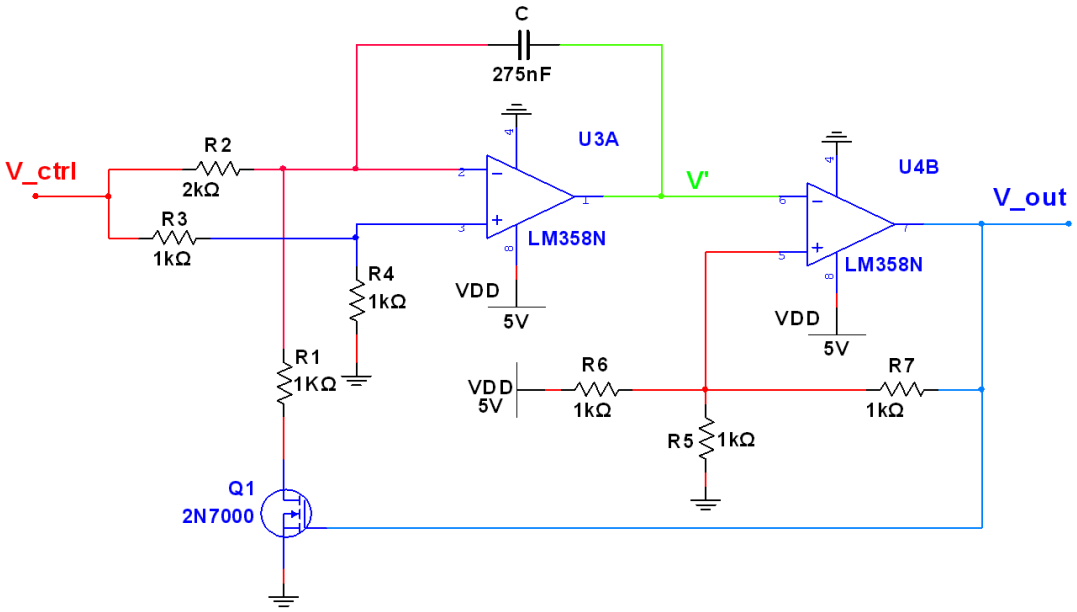


Figure 2.16: Schematic of a relaxation VCO with a 1 KHz central frequency.

To measure the output frequency of the VCO, a dc voltage V_{ctrl}, ranging from $0\,V$ to $+5\,V$, was applied at the input. The results obtained are presented in the table below. Table 2.3 contains the results of the measured output frequency after simulation and the calculated ones using the equation 2.5.

$V_{ctrl}\,(V)$	$Calculated\ f_{out}\,(Hz)$	$Measured\ f_{out}\,(Hz)$
0	0	0
0.5	200	204
1.0	400	406
1.5	600	606
2.0	800	803
2.5	1.0 K	1.0 K
3	1.2 K	1.19 K
3.5	1.4 K	1.39 K
4	1.6 K	1.58 K
4.5	1.8 K	1.77 K
5	2.0 K	1.96 K

Table 2.3: VCO output frequency versus the applied control voltage.

Note that the measured output frequency results are close to those obtained using electrical analysis equations. Figure 2.17 depicts two waveforms of frequencies 1 KHz (in red) and 2 KHz (in green) generated at the output when V_{ctrl} is $2.5\,V$ and $5\,V$ respectively.

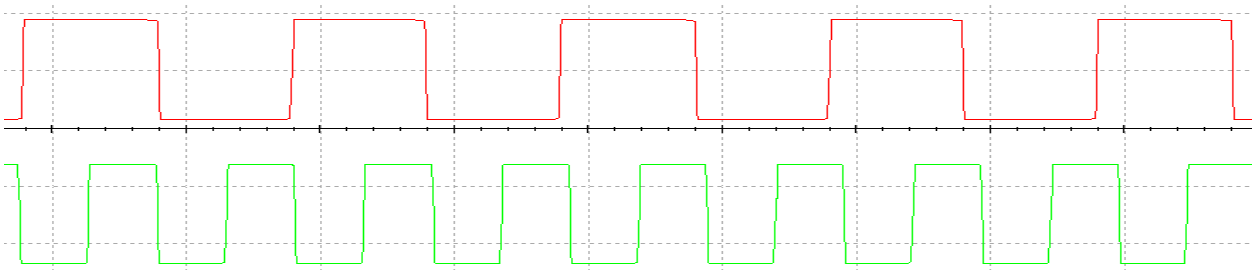


Figure 2.17: Output signals for different control input voltage.

As it was discussed earlier, the output signal will oscillate and switch its states from LOW ($V_{sat}^{-} = 0.32\,V$) and HIGH ($V_{sat}^{+} = 3.76\,V$). It is essential to mention that the VCO does not generate square wave signals only, but also triangular waveforms. The latter is referred to as V' in Figure 2.16, it is produced at the output of the integrator stage. Figure 2.18 shows triangular and square output waveforms generated when $V_{ctrl} = 2.5\,V$. The triangular wave swings between $V_{LT} = 1.77\,V$ and $V_{UT} = 2.92\,V$.

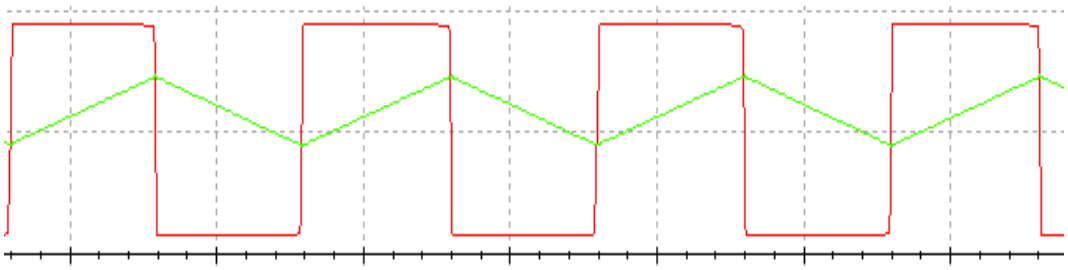


Figure 2.18: 1 KHz triangular and square waves generated at $2.5\,V$.

The measured frequencies in Table 2.3 are plotted versus their corresponding control voltage and shown in Figure 2.19. Note that the frequency varies linearly when V_{ctrl} is changing.

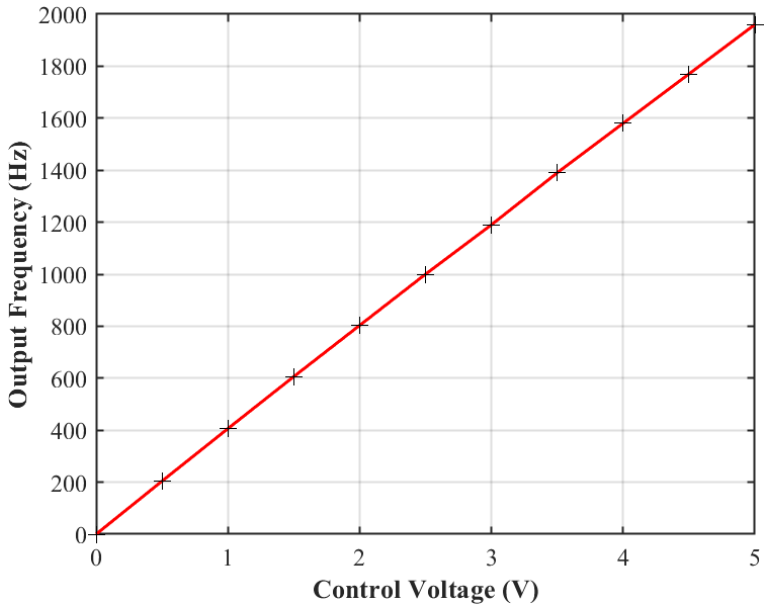


Figure 2.19: Plot of f_{out} versus V_{ctrl}.

As it was mentioned in Chapter 1, the output angular frequency ω_{out} satisfies the equation below,

$$\omega_{out}(t) = K_{VCO}V_{cont} + \omega_0 \tag{2.6}$$

In our case, the gain K_{VCO} is deduced from equation 2.5. Since

$$f = \frac{V_{ctrl}}{8R_1C(2.92-1.77)} \approx \frac{0.11\,V_{ctrl}}{R_1C}$$

Therefore,

$$K_{VCO} = \frac{2\pi}{8R_1C(2.92-1.77)} \approx \frac{2\pi \times 0.11}{2.75\times10^{-4}} = 2513.3\,rad/V$$

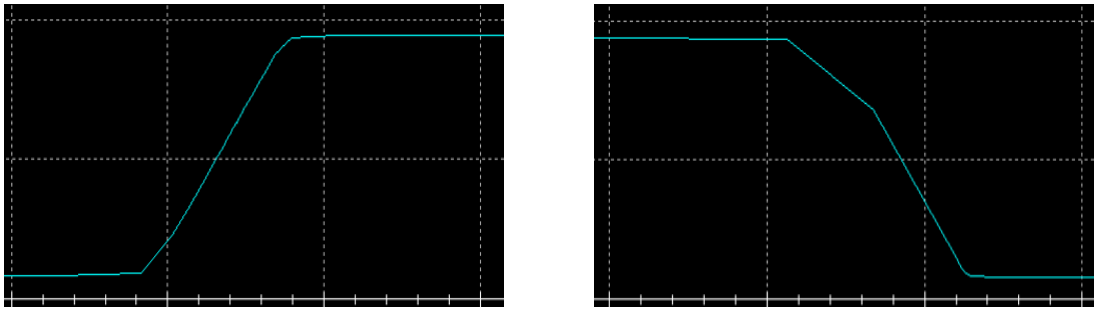
We conclude that the gain of this relaxation VCO is $K_{VCO} = 2513.3\,rad/V$. It is important to remind that this gain is deduced from the approximation equation of the electrical analysis of the circuit. K_{VCO} can be computed by finding the slope of the graph plotted in Figure 2.19. In this case, the points $(0.5;204)$ and $(5;1960)$ are selected.

$$K_{VCO} = 2\pi\frac{1960-204}{5-0.5} = 2451.8\,rad/V$$

One can notice two important remarks. From Figures 2.18 and 2.17, the output voltages do not look like perfect square waves. The second remark is that the free running frequency ω_0 of this VCO is *zero*, which is not practical since most VCOs oscillate at their free running frequency when their input voltage is zero.

The first problem is mainly caused by the non-idealities of the op-amps. Op-amps have many properties such as input and output impedance, gain, bandwidth, slew rate...etc. Since the Schmitt trigger stage is just an op-amp that switches its states between V_{sat}^{+} and V_{sat}^{-}, the slew rate becomes an essential parameter to have a well-shaped output wave. The slew rate of an op-amp refers to the highest possible rate of voltage change at its output. It is typically measured in V/s or $V/\mu s$. Operational amplifiers may have different slew rates for positive and negative voltage transitions. If the slew rate is too low, it can cause the output signal to become distorted when the input signal changes too quickly resulting in inaccuracies and errors [15].

For the *LM*358 op-amp, the slew rate is $0.3V/\mu s$. So the transition at the output from LOW to HIGH ($0.32\,V$ to $3.76\,V$) and vice-versa will take about $11.5\,\mu s$. This may cause problems when the PLL tracks the input since its output does not have sharp rising and falling edges [16].



a Rising edge of the output. **b** Falling edge of the output.

Figure 2.20: The rising and falling edges of an output waveform.

To solve this issue, adding a Buffer at the output stage of the VCO was suggested. The **7407N** buffer is a part of the 7400 series of TTL logic chips with open-collector outputs. As shown in Figure 2.21, a positive power supply voltage ($+5\,V$) and a $1\,K\Omega$ pull-up resistor (R_8) are connected to the output of the VCO. By adding the buffer, the rise and fall times of the output square wave can be improved since the buffer is specifically designed to have fast switching characteristics and ensure a minimal delay.

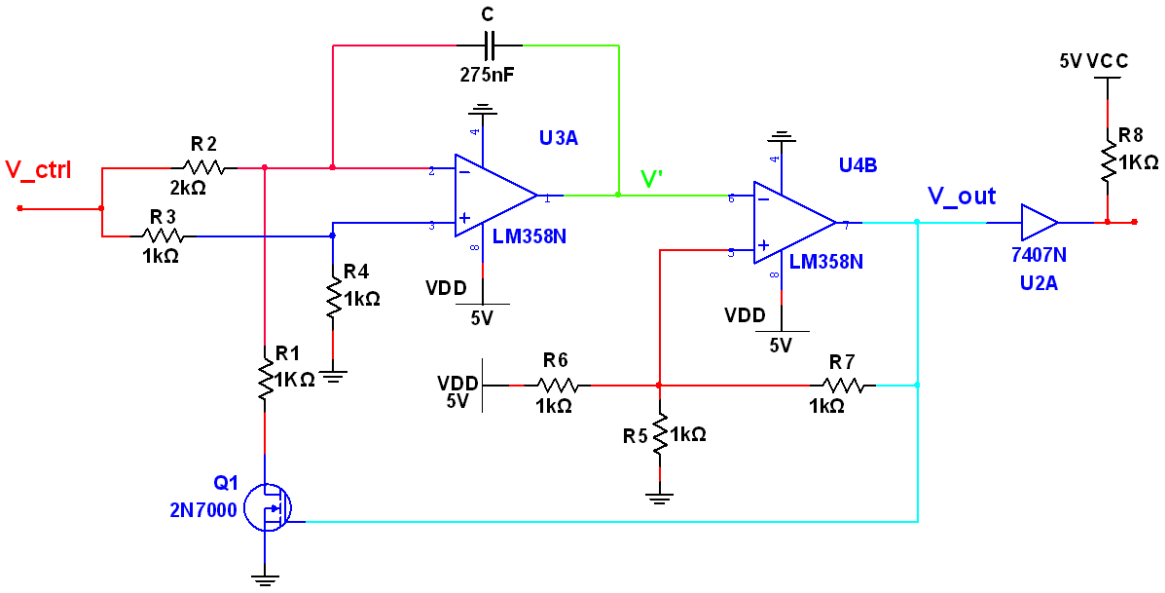


Figure 2.21: Relaxation VCO with an additional buffer.

The circuit was simulated by applying a $2.5\,V$ at the input, the VCO generated a $1\,KHz$ square wave as shown in Figure 2.22. The transition caused by the low slew rate of the op-amps is now replaced by a sharp rising falling edge, the delay caused by the buffer was measured in simulation, it is less than $20\,ns$.

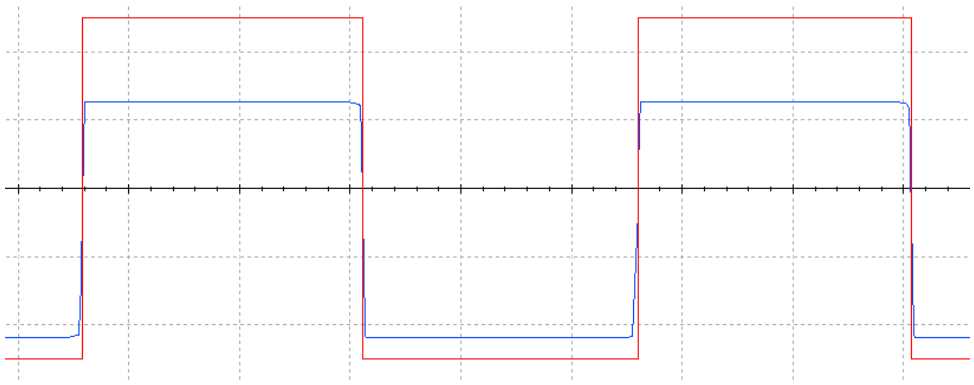
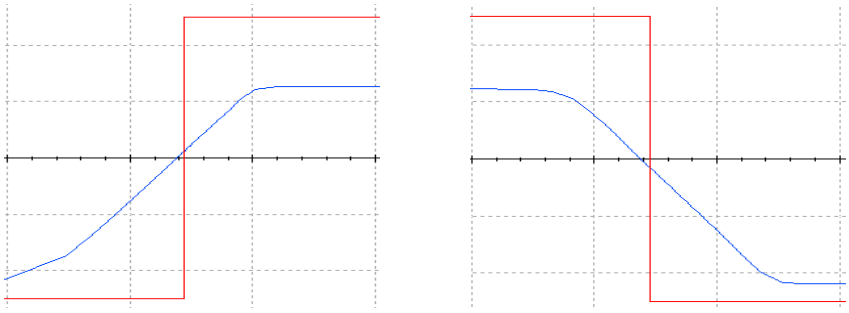


Figure 2.22: $1\,KHz$ output waveform with (in red) and without (in blue) a buffer.

The output signal looks sharper, it is now either LOW ($0\,V$) or HIGH ($+5\,V$) instead of V_{sat}^{+} or V_{sat}^{-}. The effect of the Buffer is well seen if we zoom in on the output signal.



a Rising edge of the output (in red) when adding buffer.

b Falling edge of the output (in red) when adding buffer.

Figure 2.23: Effect of adding a buffer on an output signal's rising and falling edges.

Moving to the second problem, which is the free running frequency of the VCO. It is not common for a VCO to generate a frequency at $0\,V$. To enhance this VCO, it was recommended to design an adder circuit. The adder circuit is also based on om-amps. We tried to map two values of the control voltage V_{ctrl} to new ones. $0\,V$ is mapped to $0.5\,V$ to ensure an oscillation at the output while $2.5\,V$ is transformed to $2.5\,V$ to obtain the same central frequency.

If the voltage V'_{ctrl} is the output of the adder circuit, that is the result of mapping V_{ctrl}, then simple mathematical equations lead to the following,

$$V'_{ctrl} = a\,V_{ctrl} + b$$

where

$$a = \frac{2.5-0.5}{2.5-0} = 0.8 \quad and \quad b = 0.5$$

Therefore,

$$V'_{ctrl} = 0.8\,V_{ctrl} + 0.5 \tag{2.7}$$

Based on equation 2.7, we can simply design the adder circuit using a non-inverting adder op-amp. Figure 2.24 shows the schematic of a non-inverting adder, where an $LM358$ op-amp was used with a set of resistors R_a, R_b, R_c and R_f. The op-amp is fed with $+6\,V$.
This circuit adds the input voltages V_{ctrl} and V_1 and scales the result to obtain V'_{ctrl}.

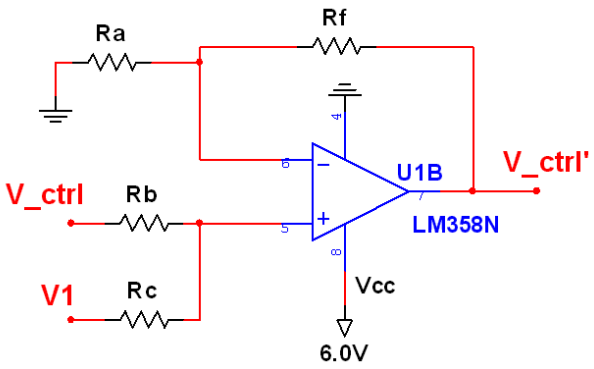


Figure 2.24: Schematic of a non-inverting adder.

Note that the relationship between V'_{ctrl} and V_{ctrl} is as follows,

$$V'_{ctrl} = \left(1 + \frac{R_f}{R_a}\right)\left(\frac{R_c}{R_b + R_c}V_{ctrl} + \frac{R_b}{R_b + R_c}V_1\right) \tag{2.8}$$

Equating equation 2.7 and 2.8, and by setting V_1 to $1\,V$, the values of the resistors are chosen such that,

$$\left(1 + \frac{R_f}{R_a}\right)\left(\frac{R_c}{R_b + R_c}\right) = 0.8 \qquad \left(1 + \frac{R_f}{R_a}\right)\left(\frac{R_b}{R_b + R_c}\right) = 0.5$$

After some mathematical analysis, it is concluded that,

$$R_c = 1.6R_b \quad and \quad R_f = 0.3R_a$$

So, if $R_b = R_a = 1\,K\Omega$ and $V_1 = 1\,V$, then $R_f = 300\Omega$ and $R_c = 1.6\,K\Omega$. As a result, the voltage range of V_{ctrl}, which is $[0\,V; 5\,V]$, is mapped to the range of V'_{ctrl} where $V'_{ctrl} \in [0.5\,V; 4.5\,V]$.

The final improved schematic of the VCO is then depicted in Figure 2.25 where the input voltage V_{ctrl} is mapped to V'_{ctrl} using the non-inverting adder. The latter is fed to the input of the integrator stage. Finally, the output voltage V_{out} is obtained at the buffer's output.

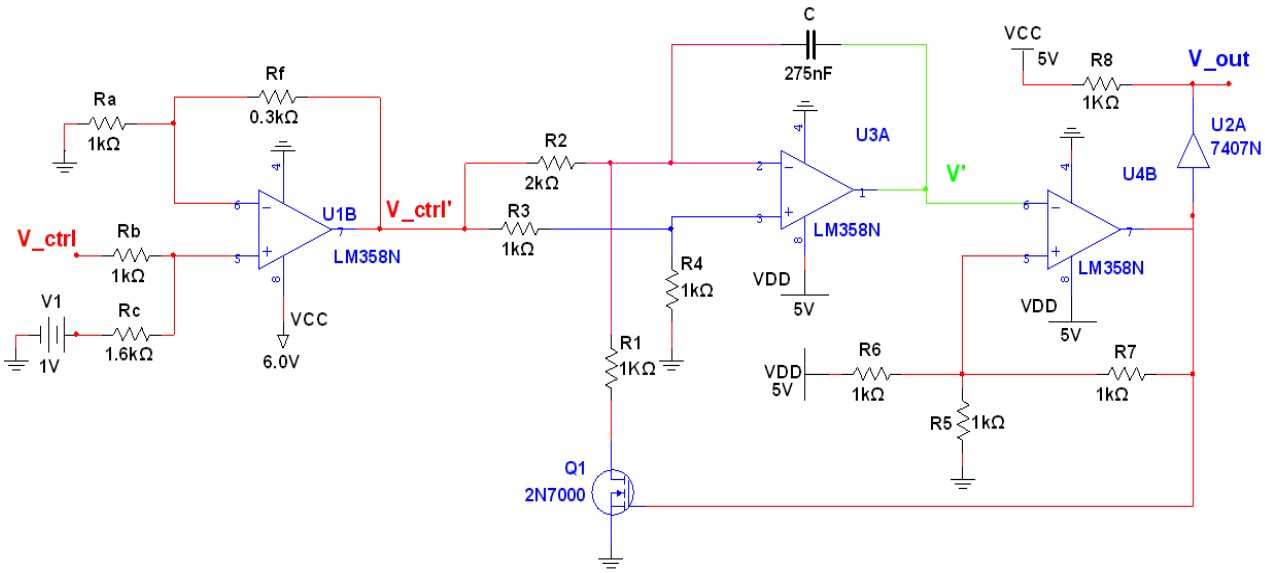


Figure 2.25: Final schematic of the relaxation VCO.

After conducting simulations, the measurements of the output frequency f_{out} and the voltage V'_{ctrl} are tabulated in Table 2.4.

$V_{ctrl}\,(V)$	$V'_{ctrl}\,(V)$	$f_{out}\,(Hz)$
0	0.5	204
0.5	0.9	365
1.0	1.3	525
1.5	1.7	685
2.0	2.1	844
2.5	2.5	1.0 K
3	2.9	1.16 K
3.5	3.3	1.31 K
4	3.7	1.46 K
4.5	4.1	1.62 K
5	4.5	1.77 K

Table 2.4: Measured VCO output frequency versus the applied control voltage.

The data in Table 2.3 and 2.4 are plotted together versus the applied control voltage V_{ctrl}. The graph is shown in Figure 2.26. It is clear that both responses are linear. When no adder circuit is used $(red\ plot)$, the minimum frequency is *zero* $(f_{min} = 0)$, so the designed VCO has no offset frequency at $V_{ctrl} = 0\,V$.
On the other hand, if the non-inverting adder circuit is integrated $(blue\ plot)$, the minimum frequency f_{min} is $204\,Hz$, so the designed VCO is said to have an offset frequency at $V_{ctrl} = 0\,V$. Note that the frequency range has been reduced and ranges between $204\,Hz$ and $1.77\,KHz$.
For both cases, the central frequency $f_c = 1\,KHz$ is produced at $2.5\,V$, this is represented by the crossing of the two plots.

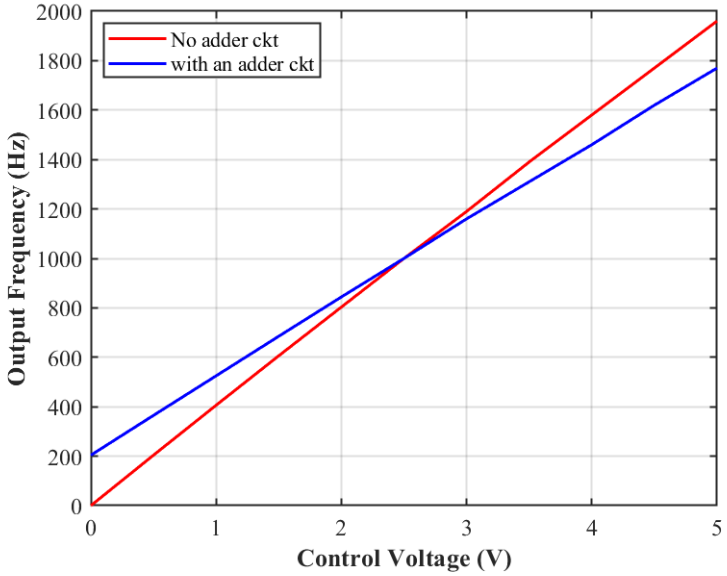


Figure 2.26: Plot of f_{out} versus V_{ctrl} when the non-inverting adder is used.

To compute the new gain K_{VCO}, the points $(0.5;204)$ and $(5;1770)$ are selected to find the slope of

the blue graph. The gain has been reduced a little, it is given by,

$$K_{VCO} = 2\pi \frac{1770-204}{5-0.5} = 2186.5\, rad/V$$

2.4 Design of the Low-Pass Filter (LPF)

The low-pass filter is the second block in the DPLL system. It is used to remove unwanted harmonics of the PFD output signal and generate the control voltage V_{ctrl} to adjust the frequency of the relaxation VCO. The proper functioning of the entire phase-locked loop relies heavily on the design of the LPF. While the actual circuitry of the loop filter is quite simple, its influence on the loop's performance is significant. Some performance parameters are the settling time, loop bandwidth, stability...etc [17]

As mentioned in Chapter 1, there are various filters including passive and active ones. In this design, we attempted to design the DPLL using a simple passive LPF. Recall that the transfer function of a simple LPF is given by,

$$F(s) = \frac{1}{s\tau+1} \quad where \quad \tau = R_9 C_1$$

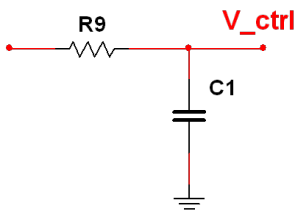


Figure 2.27: Schematic of a simple LPF.

Since this LPF becomes similar to a Lead-Lag filter when $R_2 = 0$, the natural frequency ω_n, the damping factor ζ, and the filter bandwidth ω_f are then deduced from equation 1.20.

$$\omega_n = \sqrt{\frac{K_{PD}K_{VCO}}{\tau}}, \quad \zeta = \sqrt{\frac{1}{4K_{PD}K_{VCO}\tau}}, \quad \omega_f = \frac{1}{\tau} \tag{2.9}$$

According to the application note *'CMOS Phase-Locked-Loop Applications Using the CD54 / 74HC / HCT4046A and CD54 / 74HC / HCT7046A'* by Texas Instruments [17], the LPF is designed by choosing a ω_f/ω_n ratio, then we solve for τ to determine the values of R_9 and C_1. it is important to mention that if the cut-off frequency of the LPF is set to a lower value, it will result in a slower response of the loop. On the other hand, if the loop requires a quick response to frequency changes, a higher cut-off frequency is necessary for the filter. If we assume that the ratio $\omega_f/\omega_n = a$, then

$$\left(\frac{\omega_f}{\omega_n}\right)^2 = a^2 \quad \Leftrightarrow \quad \frac{1}{\tau^2}\frac{\tau}{K_{PD}K_{VCO}} = a^2 \quad \Leftrightarrow \quad \frac{1}{\tau\, K_{PD}K_{VCO}} = a^2$$

therefore, the time constant is given by,

$$\tau = \frac{1}{a^2\, K_{PD}K_{VCO}} \tag{2.10}$$

The gain K_{PD} of the PFD and the gain K_{VCO} of the VCO are given by,

$$K_{PD} = \frac{V_{cc}}{4\pi} = \frac{5}{4\pi} \approx 0.4\,V/rad \qquad K_{VCO} = 2451.8\,rad/V$$

$$K_{PD}K_{VCO} = 980.72$$

Different values for a were set, and the time constant was computed using equation 2.10. Then with the help of simulation, C_1 was deduced by fixing the value of R_9. The results are summarized in Table 2.5.

ω_f/ω_n	$\tau\,(ms)$	$R_9\,(\Omega)$	$C_1\,(nF)$	ζ
4	0,064	1280	50.054	2.00
2.8	0.131	1280	102.15	1.40
2	0.256	1280	200.22	1.00
1.6	0.400	1280	312.84	0,80

Table 2.5: Calculation of the LPF parameters.

An important PLL parameter is the settling time; it is the time required for the PLL's output to reach a stable state after tracking the reference signal. According to the simulation results, the settling time T_s, for the different values of τ, takes values between $10\,ms$ and $20\,ms$. The values of R_9 and C_1 in table 2.5 achieved the frequency synchronization of the output signal to the $1\,KHz$ reference signal but with different phase errors. Based on the experiments, the optimal parameters of the LPF are $R_9 = 1.28\,K\Omega$ and $C_1 = 200\,nF$. These values ensured a stable output signal and a small phase error compared to the other values.

Figure 2.28 depicts three signals, the $1\,KHz$ reference signal (in red), the PLL's output signal (in green), and the LPF output signal (in blue). Note that the LPF response fluctuates around $2.5\,V$ which is the required dc value to generate a $1\,KHz$ square wave output as discussed in the VCO section. The phase error is getting decreased after each time period due to the quick filtering operation.

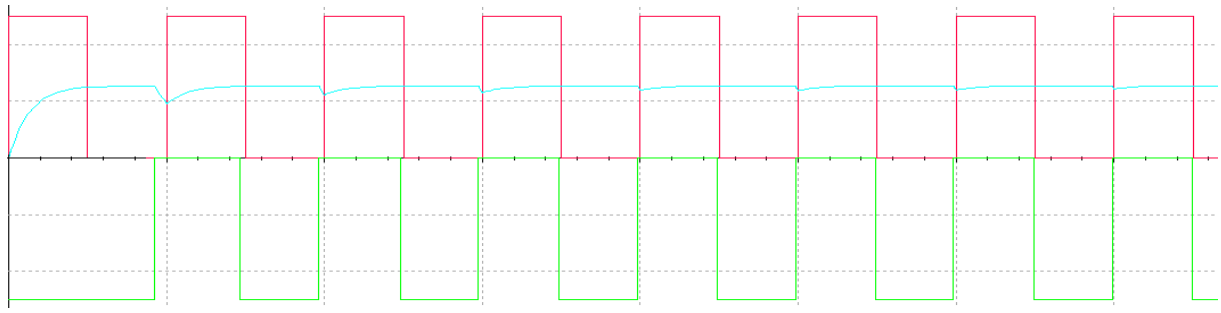


Figure 2.28: PLL response (in green) versus the reference signal (in red) and the LPF output (in cyan).

2.5 Entire DPLL Block

After conducting comprehensive testing on each individual block, the entire DPLL system was evaluated. This involved integrating the entire block, which includes the Phase Frequency Detector (PFD) connected to the Low Pass Filter (LPF) with specific resistor and capacitor values ($R =$

$1.28K\Omega$, $C = 200nF$), and further connected to the Voltage Controlled Oscillator. The circuit diagram of the implemented DPLL with the specified resistor and capacitor values can be seen in Figure 2.25.

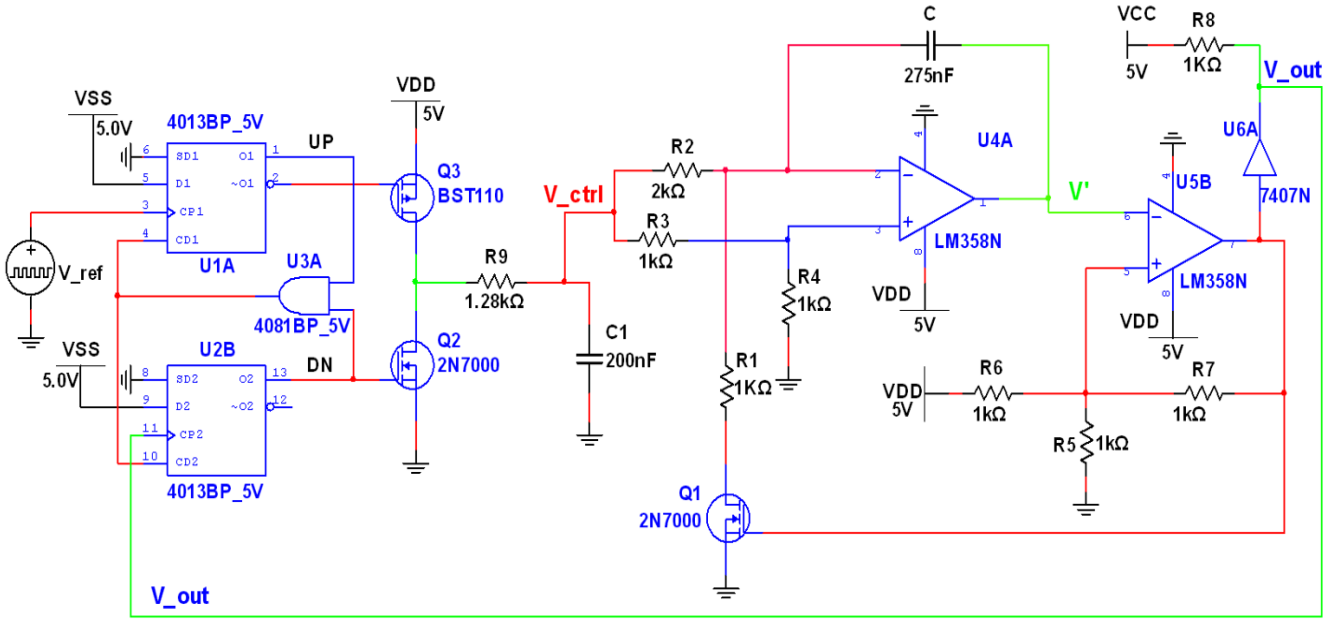


Figure 2.29: Final schematic of the DPLL.

2.6 DPLL Parameters

2.6.1 Lock-in Range

The lock-in range, also known as the capture range, refers to the range of input frequencies over which the PLL can acquire and maintain phase lock with the input signal. The lock-in range specifies the range of input frequencies within which the PLL can achieve phase lock. Outside this range, the PLL may fail to lock or exhibit unstable behavior. A wider lock-in range implies that the PLL can effectively track a broader range of input frequencies and maintain stable phase lock. Conversely, a narrower lock-in range limits the frequency range over which the PLL can achieve phase lock.

By varying the input frequencies, it was possible to determine the lock-in range of the DPLL. The DPLL achieved phase lock at frequencies above 200 Hz, but it failed to maintain phase lock when the frequency is more than 1200 Hz.

2.6.2 Settling Time

The settling time of a PLL refers to the duration it takes for the PLL's output signal to stabilize and accurately track the input reference signal after a change or disturbance. It represents the time required for the PLL to achieve and maintain phase lock with the input signal. According to the simulation results, the PLL takes 18 ms to lock at the reference frequency.

2.6.3 Power Consumption

In order to determine the total consumed power, the power of each individual block was measured, then the sum of the powers was calculated. Based on the simulation measurements using a watt-meter, it was found that the power consumption of the PFD is 9.60882 mW. The VCO consumes 4.753 mW of power, and the LPF has a power consumption of 9.390 mW. Therefore, the total power consumption is 23.75182 mW.

Note that the PFD and the VCO are fed with 5 V power supplies, the voltage at the VCO input depends on the output of the LPF, it ranges from 0 to 5 V. The op-amps of the VCO have a power supply range of 3 V to 32 V when a single supply is used.

2.7 Colusion

In this chapter, we focused on the design and implementation of the building blocks of the DPLL system where each block was designed and tested individually. First, the PFD was designed using appropriate logic gates and its performance was evaluated through simulations and testing. Next, the challenge of designing a reliable and linear VCO was examined, and the designed relaxation VCO was verified and simulated ensuring the linearity and the ability to generate the desired frequency range accurately. After that, the LPF was designed using the appropriate resistor and capacitor values, the latter provided the PLL with the ability to lock at the desired frequency of 1 KHz ensuring a synchronization with a small phase error. Finally, we successfully integrated all the building blocks together to obtain the complete DPLL circuit. The functionality and synchronization of the DPLL system were verified through comprehensive testing and measurements. In the next chapter, the practical implementation of the DPLL will be carried out.

Chapter 3

Experimental Evaluation: Results and Discussion

3.1 Introduction

This chapter reports the experimental results of the DPLL and presents the interpretation and analysis of the findings. Based on the completed design of the DPLL and the circuit simulation in Multisim, the focus now shifts toward practical implementation. We present the implementation and the evaluation of the DPLL system including the circuit construction and essential measurements conducted on the output of its main blocks. We focused on the frequency synchronization, the phase error, and the lock-in range. The PLL's performance will be compared with an IC PLL under similar conditions. The process of synchronizing the DPLL with the accurate 1PPS GPS signal, using a GPS module and GNSS software, will be performed.

3.2 VCO Measurements

We started by implementing the VCO circuit on a breadboard as Figure 3.1 shows.

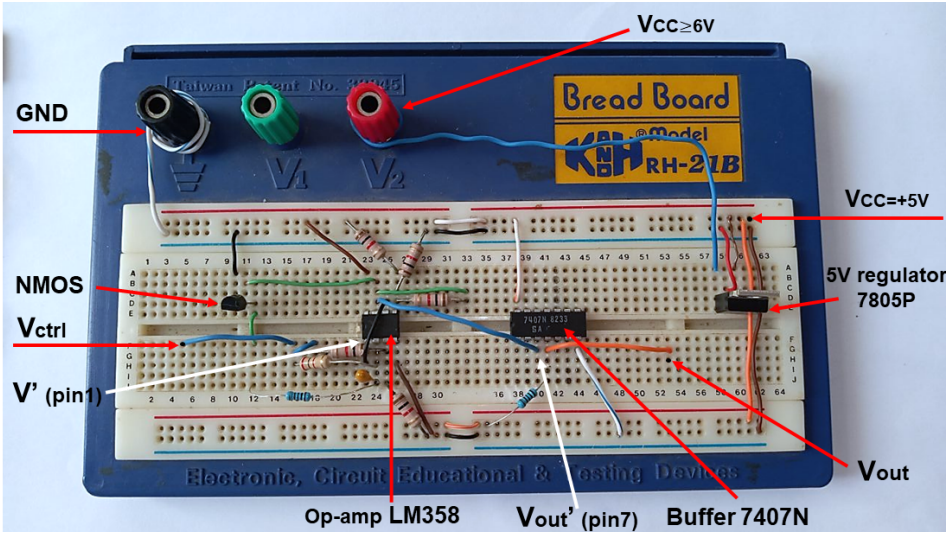


Figure 3.1: Implementation of the VCO circuit.

Note that V' represents the triangular output waveform generated by the VCO at the 1^{st} pin of the op-amp. Whereas V'_{out} represents a square waveform obtained at the op-amp 7^{th} pin. After feeding V'_{out} to the buffer, the resulting signal V_{out} becomes the VCO output signal.

The frequency of the output signal was measured when applying different control voltages. Note that the value of C (see Figure 2.29) was changed from $275\,nF$ to $330\,nF$. This is because the results of measured frequency using $275\,nF$ did not align with the design specifications. Our design required the 1 KHz being the central frequency. Therefore, the measured results were conducted using $330\,nF$. The results are presented in Table 3.1.

$V_{ctrl}\,(V)$	$f_{out}\,(Hz)$	$V_{ctrl}\,(V)$	$f_{out}\,(Hz)$
0	0	3	$1.08\,K$
0.5	240	3.5	$1.25\,K$
1.0	421.7	4	$1.40\,K$
1.5	591.5	4.5	$1.56\,K$
2.0	755.2	5	$1.72\,K$
2.5	924.5	5.5	$1.87\,K$
2.75	$1\,K$	5.9	$2.0\,K$

Table 3.1: Measurements of the VCO output frequency versus the applied control voltage.

Figure 3.2 depicts the graphical representation of the relationship between V_{ctrl} and f_{out}. The graph consists of two distinct plots, both results are obtained when $C = 330\,nF$. The first plot, represented in blue, shows the experimental measurements of the frequency versus the applied voltage. Whereas the second plot, colored in red, represents the simulated measurements of the output signal frequency.

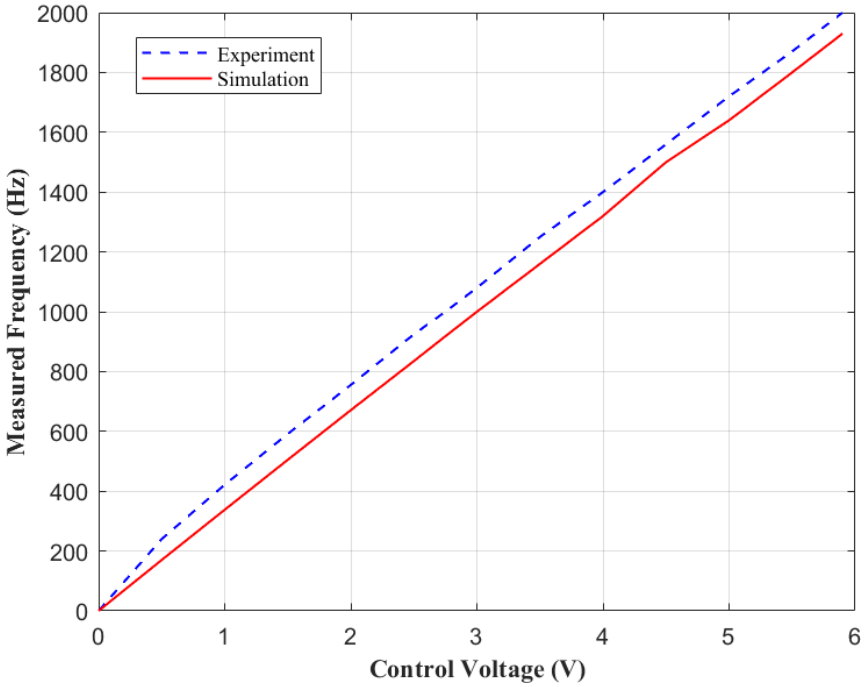


Figure 3.2: Plot of f_{out} versus V_{ctrl}.

Although there is a slight shift in the frequency values, the graphs indicate a linear response between V_{ctrl} and f_{out}, thus the VCO is linear.

The output waveforms generated by the VCO, using a **SIGLENT** oscilloscope, are shown in Figure 3.3.a. The two signals, triangular and square wave of $1\,KHz$ frequency, were obtained when a control voltage of $2.75\,V$ was applied at the input stage of the VCO. Note that these output signals are seen at the op-amp pins 1 and 7 respectively (refer to Figure 3.1).

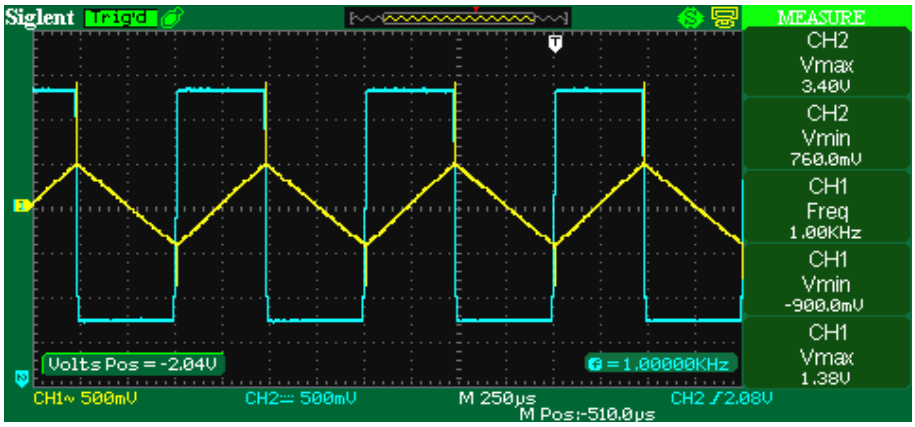


Figure 3.3.a: 1KHz square and triangular output waveforms when the buffer is not used.

The saturation voltages of the square wave V_{sat}^{+} and V_{sat}^{-} are $3.40\,V$ and $0.76\,V$ respectively.

After adding the $7407N$ buffer, the output signal is depicted in Figure 3.3.b (in blue). The output signal looks sharper at its rising edges and smoother at its maximum and minimum levels. The saturation voltages became $V_{sat}^{+} = 4.96\,V$ and $V_{sat}^{-} = 40\,mV$.

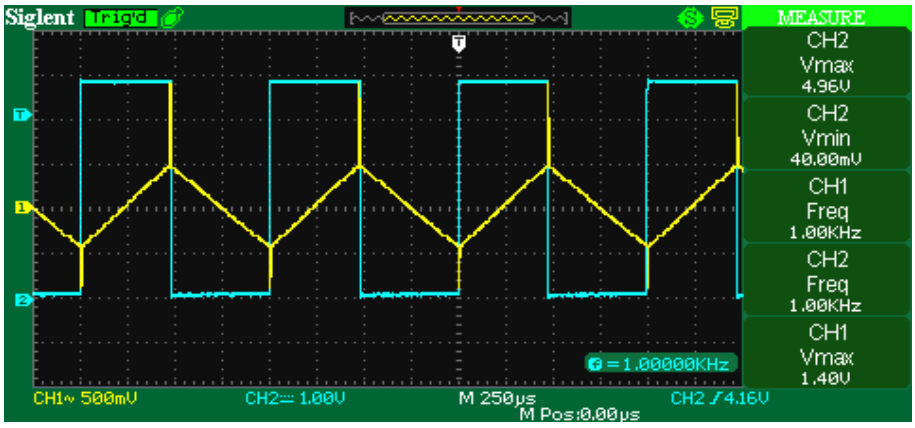


Figure 3.3.b: 1KHz square and triangular output waveform when the buffer is used.

As discussed in Chapter 2, the buffer was added to eliminate the op-amp's slew rate effect and provide the output signal with a sharp rising edge to obtain the right phase error ϕ_{error} when the PFD compares the output and the reference signals.

In Figure 3.4, the rising edges of the output signals are depicted in two scenarios: without utilizing a buffer (highlighted in yellow) and with the presence of a buffer (indicated in blue). It is clearly observed that the buffer took less than $5\,\mu s$ to change its states from LOW to HIGH. On the other hand, the op-amp switches from V_{sat}^{-} to V_{sat}^{+} in more than $25\,\mu s$.

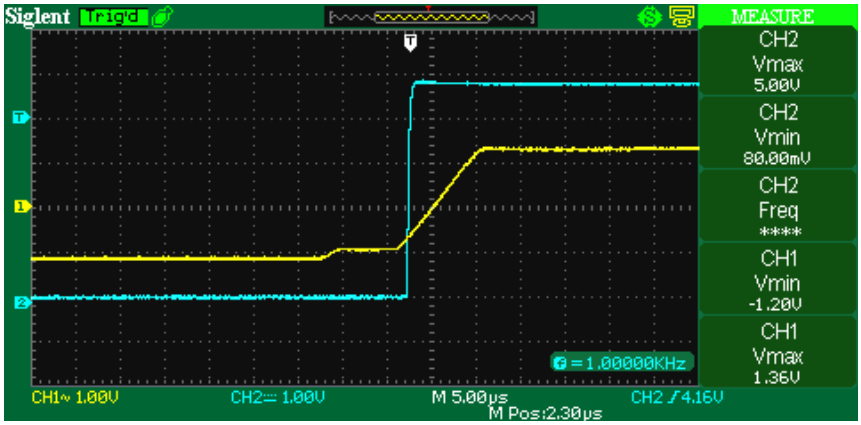


Figure 3.4: Effect of adding a buffer on the rising edge of the output.

3.3 Measurements of the Entire System

In order to test the PLL shown in Figure 2.29, the circuit was constructed with the simulation values, but unfortunately the PLL did not meet the requirements. Moreover, the absence of some electronic components at the institute led to the reconstruction of the circuit with some modifications. The capacitors C and C_1 were replaced by $330nF$ and $230nF$ respectively. Regarding the resistor R_9, 1.28 $K\Omega$ was the optimal value in simulation but not in practice, the PLL could not lock at 1 KHz using that resistance. Experiments showed that the RC filter resistor R_9 should be replaced by $680\,\Omega$. The PMOS and the NMOS transistors of the PFD were swapped by $BS250$ and $BS170$ respectively. The VCO was fed by $+5\,V$ (including the LM358 op-amp, and the 7407N buffer), while the PFD was powered by $+6.3\,V$ (including the 4013 D FF, the 4081 AND gate, and the BS250 PMOS transistor). The voltage $+6.3\,V$ was enough voltage to feed the three components at the same time, if 5 V is used instead, the output voltage at the LPF stage would be small, and thus the VCO will generate only lower frequencies. Another resistor of $1\,K\Omega$ was added between the Source of the BS250 PMOS and the $+6.3\,V$ power supply to limit the current flowing through the PMOS and to prevent it from damage since it handles a maximum current of 250 mA. The PFD and the DPLL circuits are shown in Figure 3.5 and 3.6.

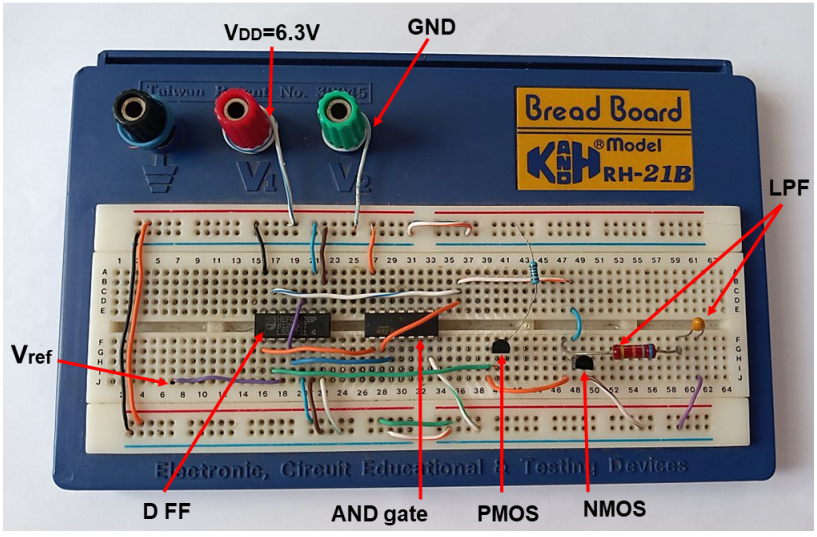


Figure 3.5: Implementation of the PFD and the LPF circuit.

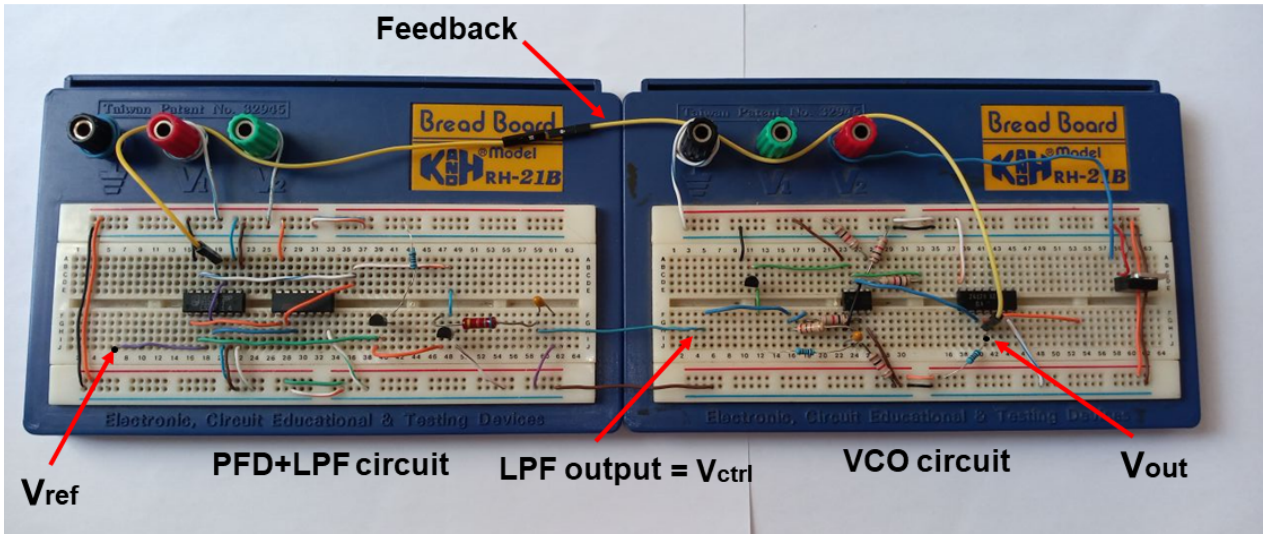


Figure 3.6: Implementation of the DPLL circuit.

After constructing the whole circuit, a 1 KHz square signal was generated by a function generator and fed to the input port of the PLL, this is the reference signal. The reference and the PLL output signal were displayed on the scope screen. The waveforms are depicted in Figure 3.7.

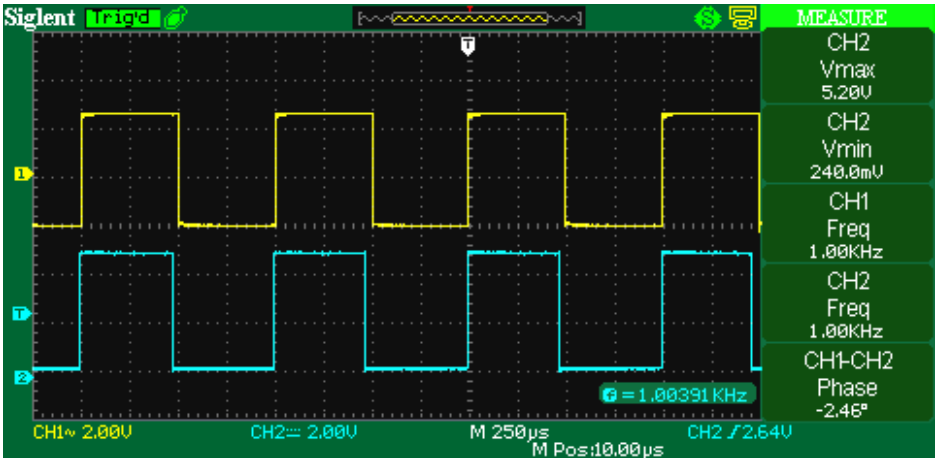


Figure 3.7: The output signal (in blue) and the 1 KHz reference (in yellow)

It is clear that the two signals are synchronized in frequency (1 KHz) with a small phase error of $\phi_{error} = -2.5^{\circ}$ as shown in the figure. Since ϕ_{error} is negative, this means that the output signal lags the reference signal with a short delay of 7 μs. This phase error remains constant as the PLL continuously compares the two signals. The PFD and the LPF output signals are depicted in Figure 3.8. Note that the LPF output signal is an exponentially increasing and decaying signal due to the use of an RC filter.

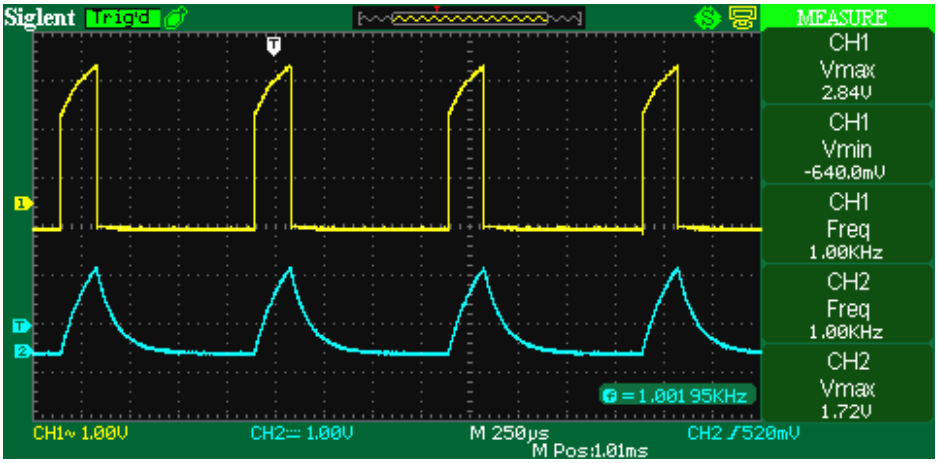


Figure 3.8: PFD output (in yellow) and LPF output (in blue) at $f_{ref} = 1\,KHz$

Since the output lags the reference signal, DN signal is HIGH, it appeared as a train of narrow pulses of width equal to the ϕ_{error} as it is illustrated in Figure 3.9. UP signal appeared as glitches and it remained zero.

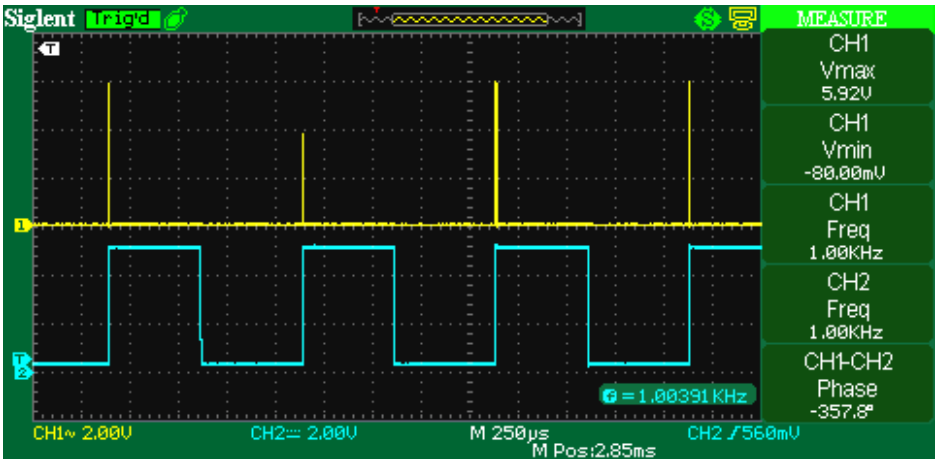


Figure 3.9: DN signal (in yellow) and output signal (in blue) at $f_{ref} = 1\,KHz$

We tested the PLL for different frequency input signals, the PLL generated an output signal that is frequency synchronized over a range that starts from $100\,Hz$ to $1.6\,KHz$, but with different phase errors. The error was small in the neighborhood of the central frequency $1\,KHz$. Table 3.2 summarizes the phase error ϕ_{error} (in degrees) obtained at each frequency, note that the PLL maintains the error and keeps tracking the input signal.

The measurements show that the phase error is small when the frequency is close to $1\,KHz$, but as we move further away from it, the error gets increased but remains constant at each frequency.

After testing the PLL locking for various input frequencies and recording the phase error for each frequency, the next step was to compare it with a commercial PLL IC, specifically the LM565.

$f\,(Hz)$	$\phi_{error}\,(^\circ)$	$f\,(Hz)$	$\phi_{error}\,(^\circ)$
1280	48.74	1020	9.12
1250	42.17	1010	3.2
1210	36.37	**1000**	**-2.46**
1180	29.3	990	-7.99
1150	26.24	976	-10.82
1130	22.38	934.5	-13.46
1110	20.3	877.8	-26
1090	18.34	870.7	-27.59
1080	15.79	863.5	-29.84
1070	14.11	856.1	-31.44
1060	14.41	842.6	-35.07
1050	12.9	828.9	-39.27
1040	11.57	809.3	-44.87
1030	11.03	796.9	-48.87

Table 3.2: Measurements of the phase error using the DPLL.

3.4 PLL performance comparison: Implemented PLL vs LM565 IC PLL

The LM565 is a commercial integrated circuit that serves as a general-purpose phase-locked loop. The LM565 is a 14-pin-out IC and it includes a PD, an amplifier, a fixed resistor for filtering, and a linear VCO. This IC is equipped with a stable and highly linear voltage-controlled oscillator and it's widely used in synchronization, FM demodulation, FSK demodulation...etc. The pins of the PLL are illustrated in Figure 3.10. The availability of this IC allowed us to conduct the comparison.

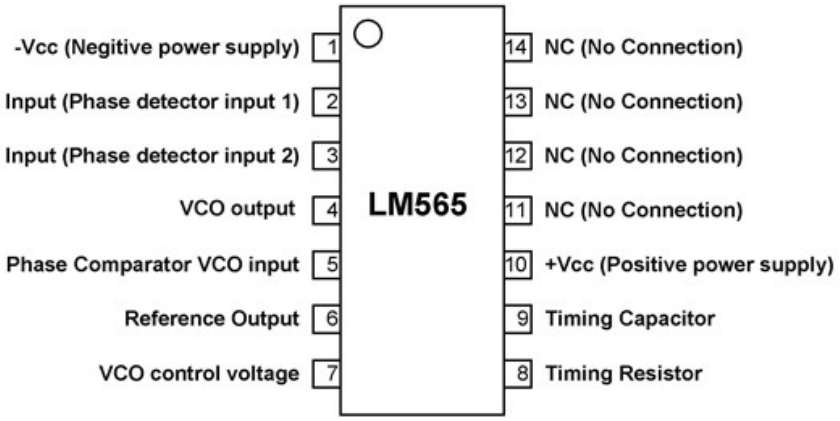


Figure 3.10: LM565 PLL pin-out.

To use this IC PLL, Pins 1, 2, 4, 5, 7, 8, 9, and 10 are used and connected as shown in Figure 3.11. The input (reference) voltage is applied at pin 2 which is then connected to the input of the PD. The PD is followed by an amplifier that is attached to an RC filter consisting of a fixed resistor ($R = 3.6\,K\Omega$) and a capacitor C_2. The output of the RC filter is fed to the VCO whose free running frequency is set by the external resistor and capacitor R_1 and C_1. Finally, the output signal is obtained at pin 4 and looped back to pin 5 (2nd input of the PD). Pins 10 and 1 represent the positive and negative supply voltages (V_{CC} and V_{EE}) respectively.

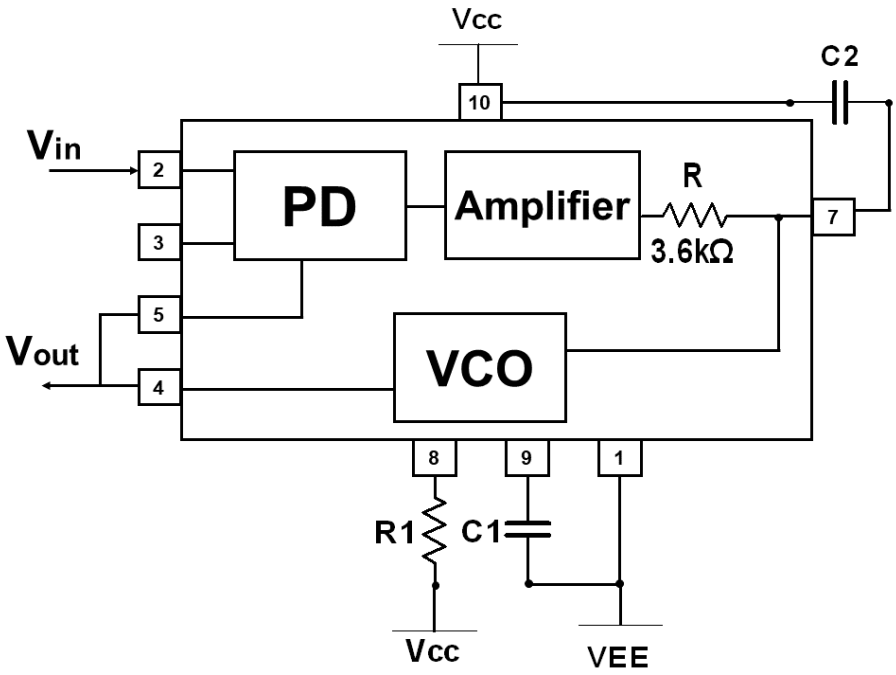


Figure 3.11: Block diagram of LM565 IC PLL.

The parameters of interest are the free running frequency f_0, the loop gain K_0K_D, the natural frequency f_n, and the damping factor ζ. They are approximated by the following equations,

$$f_0 = \frac{0.3}{R_1C_1} \qquad K_0K_D = \frac{33.6f_0}{V_{CC} - V_{EE}} \qquad f_n = \frac{1}{2\pi}\sqrt{\frac{K_0K_D}{R_1C_1}} \qquad \zeta = \frac{1}{2}\sqrt{\frac{1}{K_0K_DR_1C_1}}$$

The free running frequency f_0 was set to $1\,KHz$, and the difference $V_{CC} - V_{EE}$ was selected to be $12\,V$. Then, the gain and the time constant were obtained,

$$K_0K_D = 2800 \qquad R_1C_1 = 0.3\,ms$$

If $R_1 = 3\,K\Omega$, then $C_1 = 0.1\,\mu F$, and for a damping factor ζ of 0.5, the capacitor C_2 of the RC filter is equal to $0.1\,\mu F$. The PLL was constructed using these components and tested with a $1\,KHz$ input signal from a function generator. The results recorded in Table 3.3 show the phase error for each input frequency.

This PLL locks starting from $330\,Hz$ to $1040\,Hz$. Outside these boundaries, the PLL cannot acquire the lock. Measurements revealed that as we deviated from the $934.5\,Hz$ frequency and approached $300\,Hz$, the phase error increased; however, it remained constant at each input frequency. For the desired frequency $1\,KHz$ and its neighborhood, the IC worked perfectly, both input and output signals are phase and frequency synchronized. If the frequency exceeds $1.05\,KHz$, the synchronization is no longer achieved.

$f\,(Hz)$	$\phi_{error}\,(^\circ)$	$f\,(Hz)$	$\phi_{error}\,(^\circ)$
790.3	-49.62	934.5	0
808.8	-41.94	976	0
828.9	-31.61	990	0
842.6	-33.83	1000	0
855.5	-19.96	1010	0
842.6	-33.83	1000	0
855.5	-19.96	1010	0
877.1	-17.68	1020	0
893.5	-8.62	1030	0
900.9	-4.54	1040	0
909.4	-5.76	1050	no locking

Table 3.3: Measurements of the Phase error using LM565 PLL.

The results presented in Tables 3.2 and 3.3 demonstrate that in the neighborhood of the central frequency, the IC PLL performs exceptionally well, which aligns with expectations. In contrast, the proposed PLL achieves frequency synchronization within this range while maintaining a consistently small phase error. Moreover, the lock-in range of the designed PLL is wider than that of LM565 since it tracks the input signals of frequency up to $1.6\,KHz$. These results indicate that with further enhancements, the DPLL has the potential to replace the LM565 PLL in practical applications.

3.5 External Hardware-based 1PPS Signal Use

In order to evaluate more the DPLL performance, the reference signal generated by a voltage source is replaced by the 1PPS signal generated by a real GPS receiver, namely **NEO-M8N GPS** module as shown in Figure 3.12.

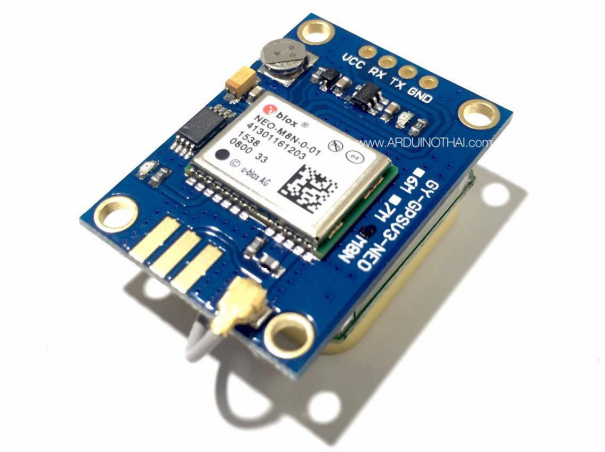


Figure 3.12: NEO-M8N GPS Module.

The NEO-M8N GPS module is a highly capable and widely used GPS receiver module that offers accurate positioning and timing capabilities. This module provides a range of features and interfaces for seamless integration into various applications. One notable feature is the ability to provide a stable and accurate 1PPS signal, making it ideal for synchronization purposes. This module is connected to an external GPS antenna that captures signals transmitted by satellites.

Figure 3.13: External GPS antenna.

The "1PPS" signal is a timing signal whose rising or falling edge occurs once every second, this signal serves as a reliable and precise reference point. It is commonly used in applications that require precise timekeeping and synchronization such as in Telecommunications, network synchronization, and navigation systems.

The 1PPS signal is generated by satellites, which are part of the Global Positioning System (GPS). GPS satellites are equipped with highly accurate timing systems such as atomic clocks. They transmit precise timing information to the GPS receivers on the ground, along with positioning data (latitude, longitude, and altitude) that are widely used in navigation and mapping. Therefore, receivers derive the 1PPS signal from the satellite's signal.

According to the datasheet of NEO-M8N, a total of 24 pins are available, each serving a unique purpose. Among them, three pins are particularly noteworthy. Pin 24 is designated as the GND, pin 23 serves as the input power supply Vcc while pin 3 is specifically assigned as the TIMEPULSE pin, from which the desired 1PPS signal is obtained.

To interact with the NEO-M8N GPS module and make use of all of its features, the software **U-center** from U-blox manufacturer was utilized. This software is designed for evaluating and analyzing Global Navigation Satellite System (GNSS) data. It is used to process and interpret the data received from GNSS receivers, such as NEO-M8N module. The interface of U-center software is shown in Figure 3.14.

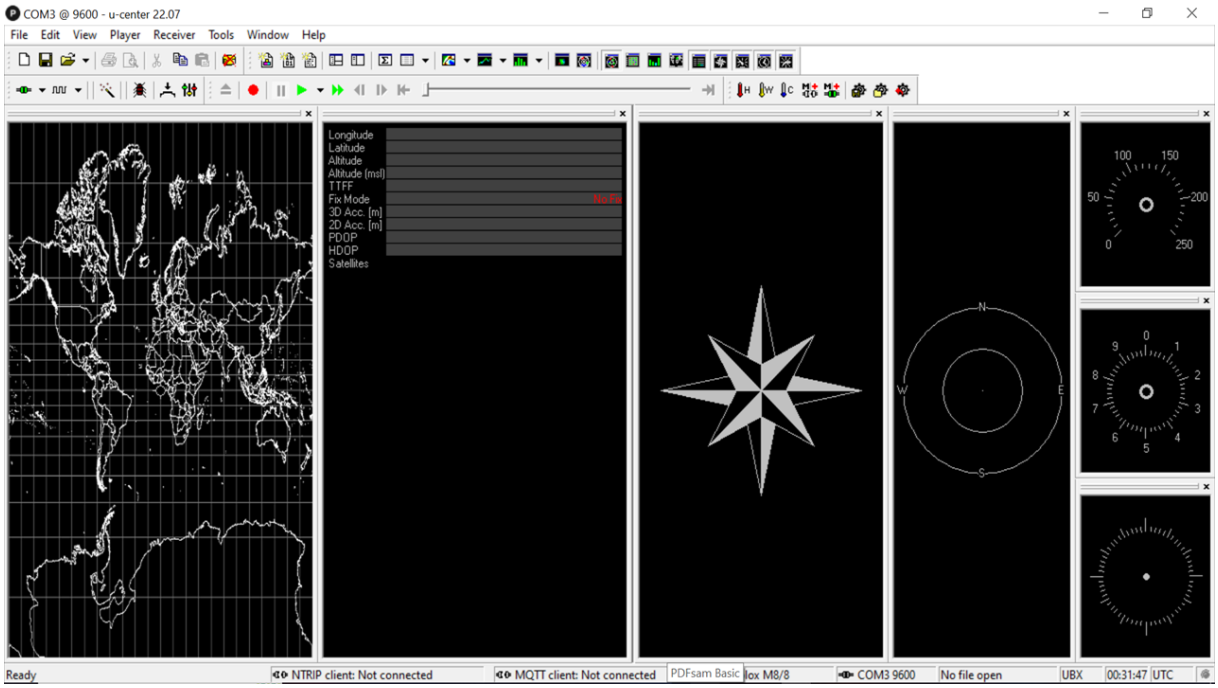


Figure 3.14: U-center interface.

To establish the connection between the GPS module and the software, the CH340 module shown in Figure 3.15 is employed. This module is responsible for converting the TTL-level signals from the GPS module into USB-compatible signals. It acts as an interface between the TTL-level signals from the GPS receiver and the USB port of the computer. The conversion is required since USB is typically used as a standard communication interface by computers and the majority of today's devices.

Figure 3.15: CH340 USB to TTL Converter Module.

Overall, the combination of the NEO-M8N GPS module, the external antenna, the CH340 USB to TTL Converter Module, and the U-center software allowed us to effectively utilize the accurate 1PPS signal generated by the GPS module.

It is important to mention that one of the advantages of using U-center is that we can configure the behavior of the 1PPS signal by adjusting the TIMEPULSE parameters such as Timepulse Rate (frequency) and the Timepulse Length (duty cycle). Since the designed DPLL synchronizes at $1\,KHz$, the 1PPS frequency was modified to $1\,KHz$ with a duty cycle of 50%, that is a Timepulse Length of $0.5\,ms$. This signal was then introduced to the input of the PLL, and the phase error was measured following the same procedure as before.

The 1PPS signal is shown in Figure 3.16, it's a train of pulses of $100\,ms$ width, $1\,Hz$ frequency, minimum voltage of $160\,mV$, and a maximum pulse voltage of $3.60\,V$.

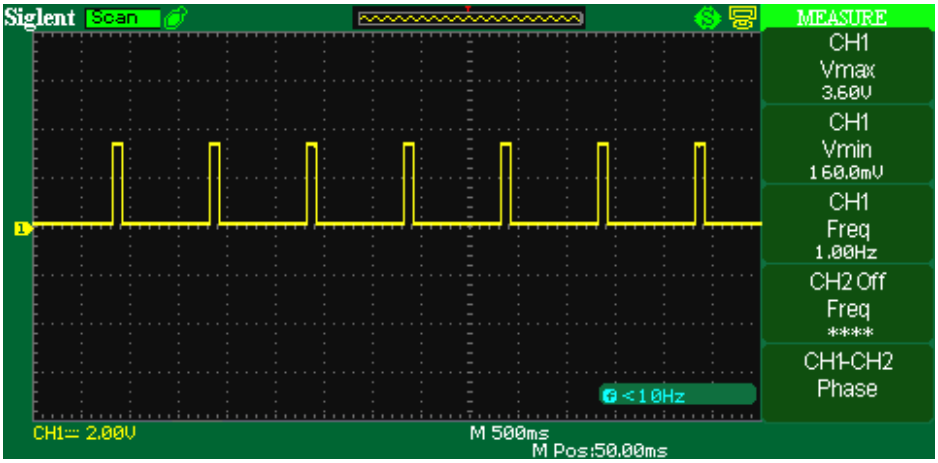


Figure 3.16: The 1PPS GPS signal received by NEO-M8N .

To adjust the parameters of the pulse in U-center, the following sections were selected: **"View"** ⇒ **"Configuration View"** ⇒ **"Timepulse"**. Then the frequency was set to 1000 Hz and the duty cycle to 50%. These parameters are depicted in the figure below.

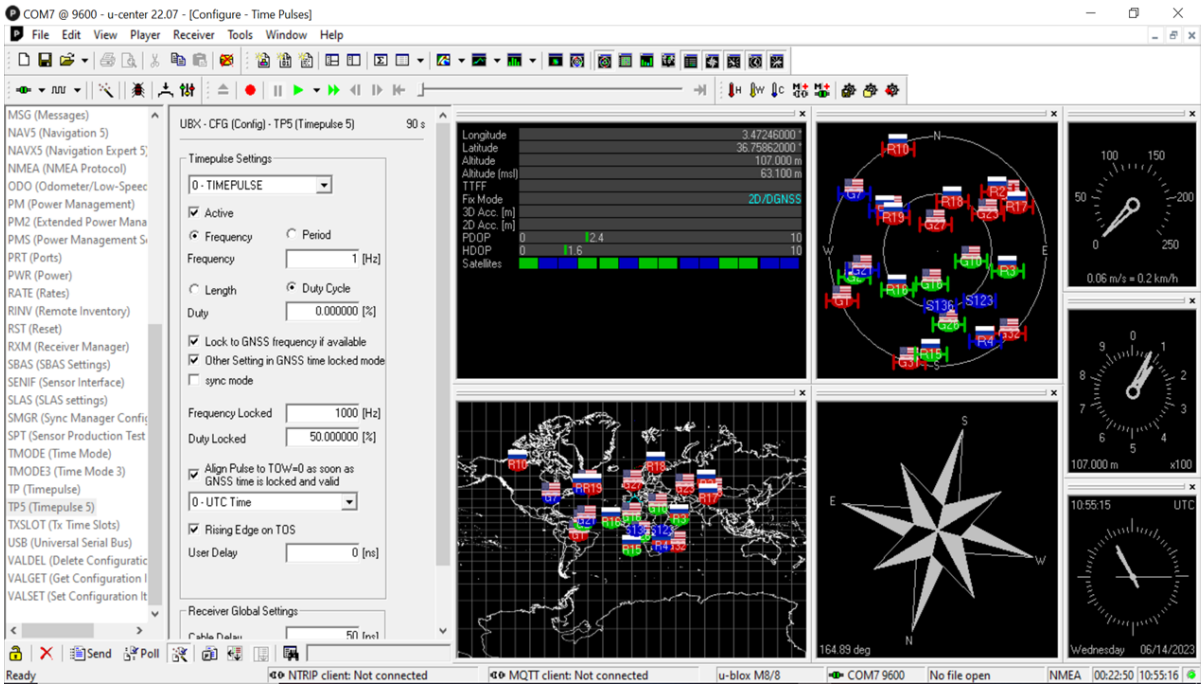


Figure 3.17: The configuration of the TIMEPULSE parameters.

As shown in the U-center interface, it is possible to access and monitor real-time data from the GPS receiver. The software provides a graphical interface that allows users to visualize satellite information, signal strength, and the number of satellites in view. it also allows to access detailed positioning information, including latitude, longitude, altitude, and velocity. More information and figures are included in the Appendix.

The 1 KHz reference signal was displayed using an oscilloscope as depicted below.

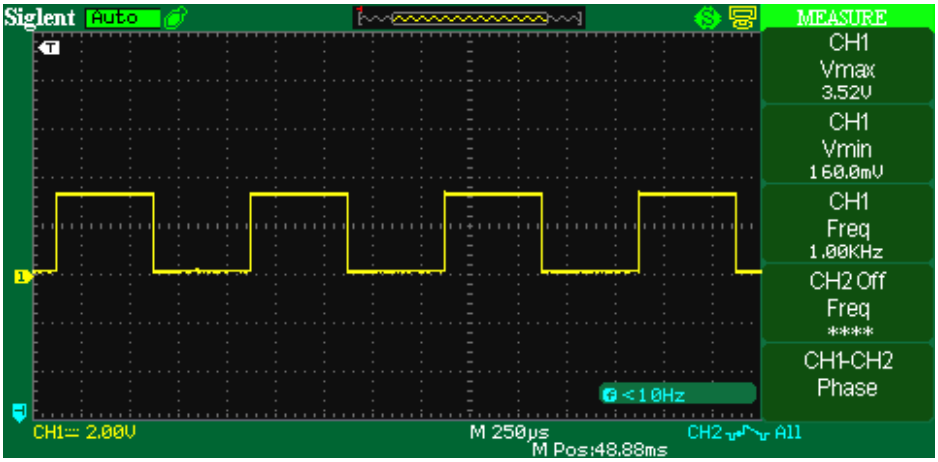


Figure 3.18: The 1PPS GPS signal configured as reference of $f = 1\,KHz$ and $D = 50\%$.

By inputting this signal to the DPLL, the latter generated a signal whose frequency is equal to 1 KHz with a small error $\phi_{error} = -2.88^{\circ}$ which means that the output leads the reference by 8 μs.

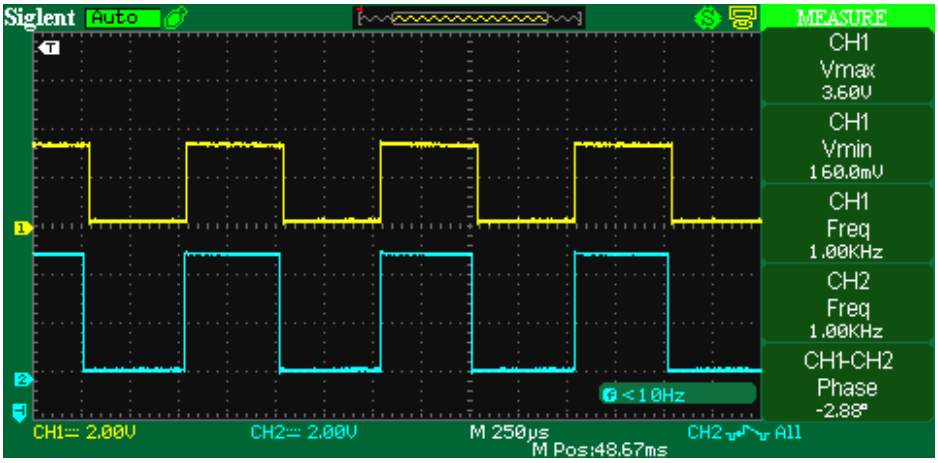


Figure 3.19: PLL Output signal (in blue) and the GPS reference signal (in yellow).

The DPLL was tested for different input frequency signals, and the phase error was recorded for each frequency as shown in Table 3.4. These results are close to those of Table 3.2.

$f\,(Hz)$	$\phi_{error}\,(^\circ)$	$f\,(Hz)$	$\phi_{error}\,(^\circ)$
700.2	-81.08	950.5	-10.06
730.1	-69.81	970.5	-11.46
750.3	-62,7	980.3	-10.79
790.1	-49.38	1000	-2.88
800.2	-45.86	1100	20.92
820.2	-39.69	1200	36.7
850.3	-31.35	1300	55.82
890.3	-21.28	1400	79.51
900.5	-19.19	1500	110.6
930	-12.59	1600	183.9

Table 3.4: Measurements of the Phase error using the 1PPS as a reference signal.

It is concluded that the phase error is small when examining frequencies close to 1 KHz, but it progressively grows (either positively or negatively) as we move further away from that frequency.

3.6 PCB Layout of the DPLL

A Printed Circuit Board, also referred to as PCB, is a substrate made of non-conductive material plastic or glass-fiber and resin with printed conductive copper traces. Electronic circuits can be implemented by soldering the leads or terminals of the components onto designated areas or pads on the PCB surface. Components are basically mounted using two methods, either via Surface Mount Device (SMD) or Through-Hole Technology (THT). The PCB of the DPLL, whose design was carried out using Kicad software, has a size of $10cm \times 10cm$, the traces on the PCB have a thickness of $0.25mm$ to ensure effective conductivity. A single-layer PCB configuration is utilized and the THT method is employed as a component mounting method. The PCB layout of the DPLL is shown in Figure 3.20.

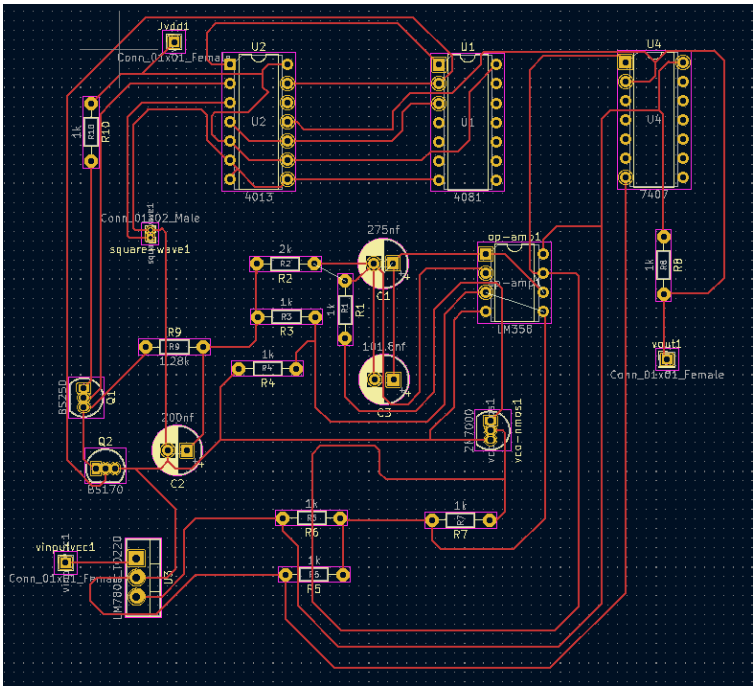


Figure 3.20: PCB layout of the PLL.

Kicad allows designers to have a 3D View after completing the Layout design. 3D models can accurately represent the physical appearance of the circuit. Figure 3.21 depicts the DPLL circuit in 3D.

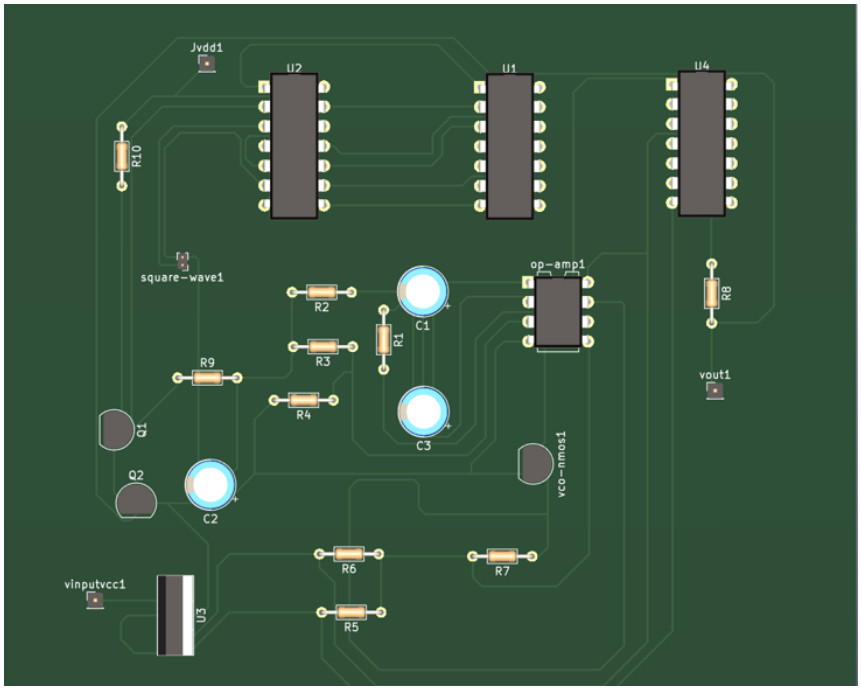


Figure 3.21: 3D view of the DPLL PCB.

At the current stage, the PCB design discussed in this section is in the fabrication phase and is not yet ready for usage.

3.7 Conclusion

In conclusion, this chapter presented the implementation and evaluation of the DPLL system. The DPLL blocks (PFD, LPF, and VCO) were successfully implemented and tested, leading to the complete implementation of the PLL. The performance of the PLL was first assessed using a reference signal generated by a function generator, then it was examined using an actual reference signal obtained from GPS satellites, specifically the 1PPS signal. Through these experiments, the DPLL demonstrated effective synchronization at the desired frequency of 1 KHz. Moreover, a comparative analysis was conducted between the performance of the implemented PLL and the IC PLL LM565, providing a foundation for comparison. Finally, the final layout and the arrangement of the employed electronic components, as well as their interconnections, were created using the PCB design software Kicad.

General Conclusion

In conclusion, this study focused on the design, implementation, and evaluation of a Digital Phase Locked Loop system that synchronizes with 1 KHz reference signal.

The beginning of the project required investigating the essential concepts of a PLL system and having a deep understanding of the function of the DPLL building blocks. The design process of the PLL involved the integration of various building blocks, including the Phase Frequency Detector (PFD), Loop Filter, and Voltage-Controlled Oscillator (VCO). Each building block was designed, tested, and evaluated with the help of Multisim. Then, the DPLL's ability to synchronize at 1 KHz was examined. The simulation results showed that the system achieved synchronization with a small constant phase error.

Moving to practice, The DPLL blocks were successfully implemented and tested, leading to the complete implementation of the entire system. The performance of the PLL, regarding the frequency synchronization and the lock-in range, was assessed using a reference signal generated by a function generator and using an actual reference signal obtained from GPS satellites, specifically the 1PPS signal. The results demonstrated the successful synchronization of the PLL at the desired frequency of 1 KHz, Validating its functional performance.

Moreover, a comparative analysis was conducted between the implemented PLL and the IC PLL LM565. The outcomes revealed the synchronization capabilities of the DPLL and that with further enhancements, the DPLL performance will improve.

We concluded our work by designing the PLL on PCB, where the PCB layout and the components' interconnections were created with the help of Kicad.

To achieve further improvements, adjustments can be made to the VCO to operate at different lower or higher frequencies. This can be achieved by modifying the resistance and capacitance values used in the electrical analysis equations. Additionally, utilizing higher-quality op-amps can enhance the performance of the VCO. These modifications offer the potential to expand the frequency range and enhance the overall functionality of the PLL. Furthermore, alternative loop filter types can be utilized to minimize fluctuations in the control voltage, thereby providing the VCO with a precise DC voltage input.

Appendix

Multisim Software

Multisim is a simulation software developed by National Instruments that is used for designing, analyzing, and prototyping electronic circuits. It allows users to create circuit diagrams and simulate the behavior of those circuits using virtual instruments and signal generators. Multisim allows designers to simulate circuits with various components such as resistors, capacitors, inductors, diodes, transistors, and more. It also includes a variety of virtual instruments, such as oscilloscopes, signal generators, and multimeters, that help in the analysis of the circuit's behavior.
Multisim has numerous applications in a variety of fields, including:

- **Electronic circuit design and analysis**

  Multisim can be used to design and evaluate complex electrical and electronic circuits for hundreds of applications that involve control systems, power electronics, signal processing, and communication systems.

- **Education and research**

  Multisim is a popular tool in universities and technical institutions for teaching and learning the analysis and design of electronic circuits. It is also employed in the field of electronics research.

- **PCB design**

  Multisim provides a complete solution for designing and prototyping printed circuit boards (PCBs), including schematic capture, component placement, routing, and layout.

Figure 1: Multisim logo.

U-center Software

The NEO M8N is a common GPS module that can receive signals from many satellite constellations (including GPS, GLONASS, Galileo, and BeiDou) to provide precise position, velocity, and time. U-center has a graphical interface that displays satellite information, signal strength, and the number of satellites in view.

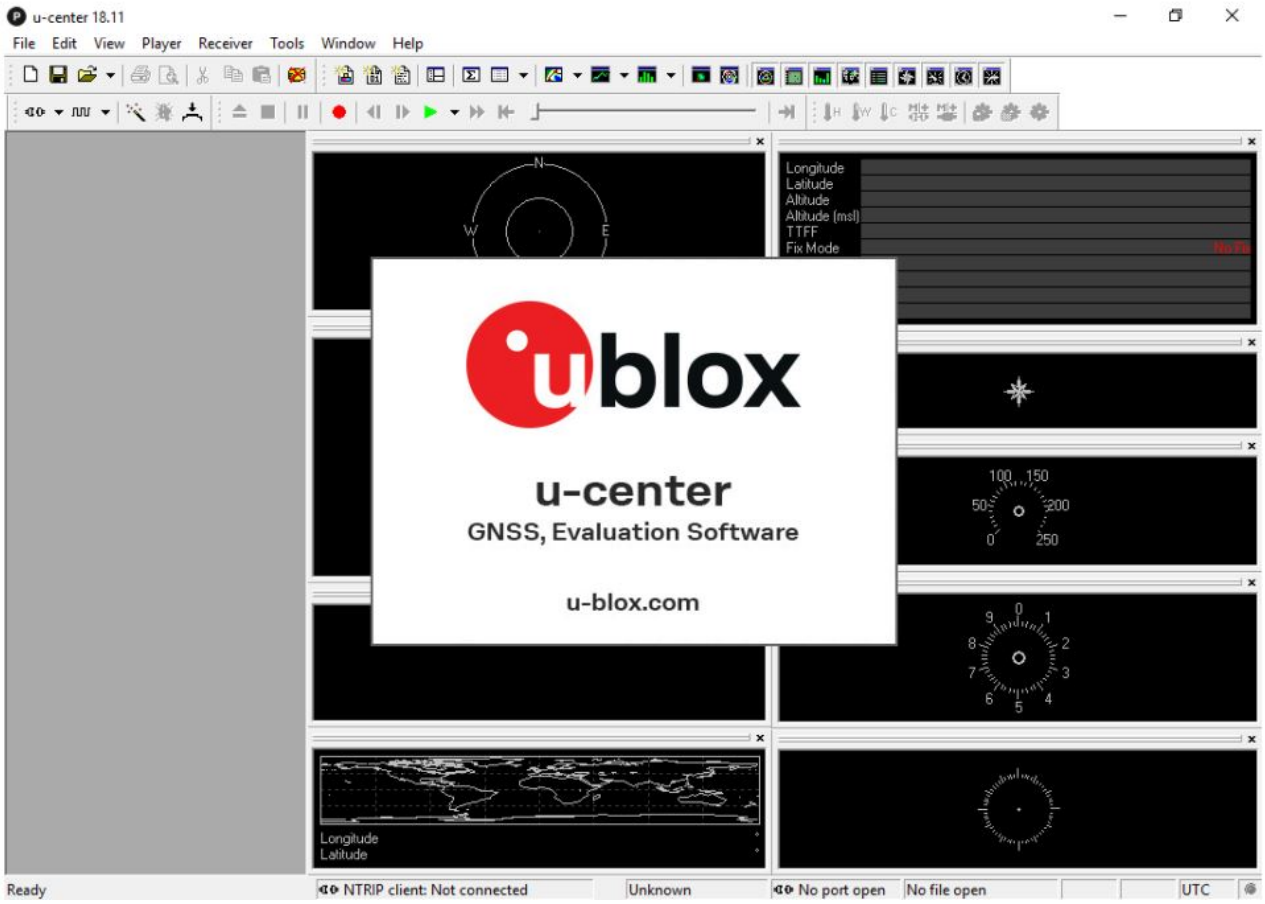


Figure 2: U-center interface.

It is also possible to obtain precise positional data such as latitude, longitude, altitude, and velocity.

The following figures were collected from U-center when connecting the computer with the GPS receiver, they represent some information regarding the experiment place and time.

Figure 3: The Satellites recognized by the GPS Receiver.

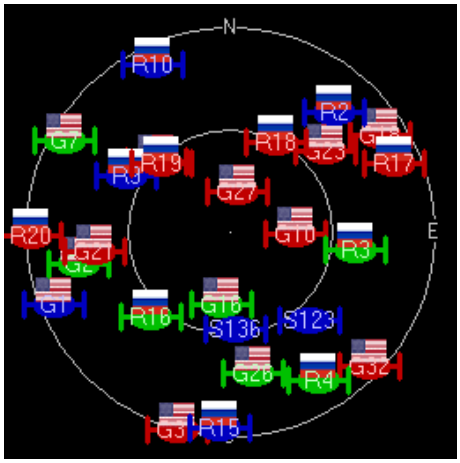


Figure 4: Satellites Position in the sky.

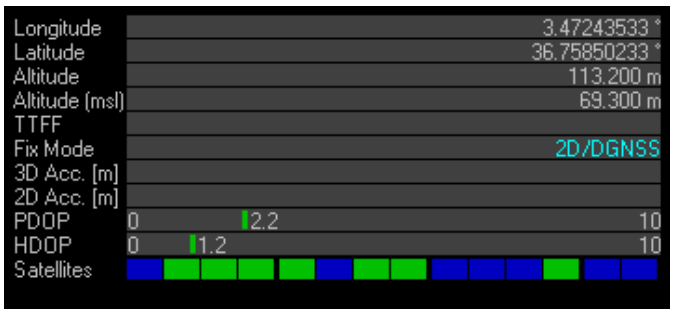


Figure 5: Positional coordinates of the experiment Lab.

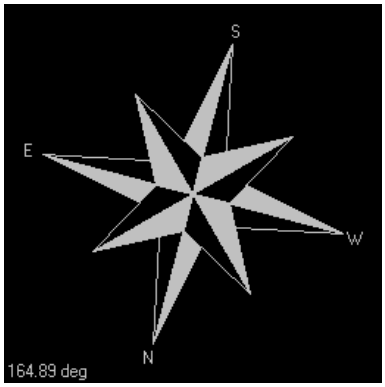


Figure 6: Compass information.

Figure 7: The precise experiment timing information provided by the GPS module.

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