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Présentée par :

Boualem DJEZZAR

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TITRE

ETUDE DES EFFETS NBTI ET PBTI SUR LA FIABILITE DES DISPOSITIFS MOS

Devant le jury composé de :

Mr	BENFDILA	Arezki	Professeur	UMMTO	Président
Mr	KECHOUANE	Mohamed	Professeur	USTHB	Examinateur
Mr	BENTARZI	Hamid	Professeur	UMBB	Examinateur
Mr	KRIBES	Youcef	MCA	UMBB	Directeur de thèse

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الملخص

الدمج المتسارع للمركبات الإلكترونية أدى إلى تخفيض كبير لسمك عازل القطب (Gate) للمقحل (ترانزستور) من عقدة تكنولوجية إلى أخرى. هذا أدى إلى إرتفاع الحقل الكهربائي للقطب و كذا ارتفاع حرارة الدارات المدمجة أثناء عملها. نتيجة لهذا ظهرت عدة مشاكل على كفاءة (Reliability) الدارات المدمجة، خصوصا مشكل الإختلال من الحرارة والاستقطاب السالب/الموجب (Negative/Positive Bias temperature Instabililty) (N/PBTI).بالطبع BTI يؤثر على عمل الدارة المدمجة و كذلك على مدة صلاحيتها باستحداث أفخاخ (Traps) على مستوى السطح الفاصل بين السلكون و ثاني أوكسيد السلكون (Si/SiO_2) و داخل ثاني أوكسيد السلكون (SiO_2). إن فهم ميكانيزمات تكوُّنْ هذه الأفخاخ مهم جدًا لتصميم نمودج للتدهور "NBTI" و التنبؤ به و بمدة صلاحية الدارات المدمجة. لهذا السبب يأتي هذا البحث المخصص لتشخيصْ الكهربائي للتدهور "NBTI" باستعمال طرق و تصاميم جديدة من أجل فهم و تحليل جيد للأفخاخ المتسببة في التدهور، منه تطوير نموذج فعّال للتنبؤ بمدة صلاحية المكونات الكهربائية و الدارات المدمجة.

بهذا الصدد، نطرح طريقة جديدة، المسماة On The Fly Oxide Trap (OTFOT) أو "أفخاخ ثاني أوكسيد السلكون على الطائر"، لقياس التدهور NBTI. هذه الطريقة ترتكز أساسًا على تقنية ضخ الشُحنات بإستعمال تواترات منخفضة وعالية. بهذه الوسيلة يمكن إستخراج و فصل كثافة الأفخاخ الموجودة على سطح الفاصل (ΔN_{it}) والموجودة داخل ثاني أوكسيد السلكون قرب السطح الفاصل (ΔN_{bt}) و كذا مساهمتهما في إنحراف تواتر العتبة (ΔV_{th}) بدون اللجوء إلى إستعمال طرق أخرى مكملة و إضافية.

إضافة إلى ما سبق، فإننا تمكنّاً من استكشاف و تتبع كيفية نشوء و تطور وتوزع كثافة (ΔN_{it}) بدلالة طول قناة المقحل (ترانزستور),حيث أنّ (ΔN_{it})، المُحدثةُ من طرف "Stress NBTI"، موزعة بطريقة غير منتظمة داخل قناة المقحل. نتائج التجارب بيّنت أنّ التدهور ينتشر و يبدأ انتشاره من أطراف قناة المقحل، أي من جهة "Source /Drain" نحو مركزها، هذا الانتشار يتسارع بفعل الحرارة و الحقل الكهربائي، حيث هذا الأخير يسبب تسارع أكبر من الذي تسببه الحرارة، كما أن المقاحل ذات قنوات قصيرة تتدهورسريعا من المقاحل ذات قنوات طويلة.

أخيرا قمنا بتمشيط الأفخاخ الموجودة في ثاني أوكسيد السلكون القريب من السطح الفاصل (ΔN_{bt}) بدلالة العمق (z) في المقحل (MOSFET). فحسب نتائج التجارب، فإن القوة (n) لدالة القوة (t^n)، التي تحاكي التطور الزمني ل (ΔN_{bt})، وكذا طاقة النشاط الظاهري ($E_{a,eff}$) تنخفضان بفعل الحرارة و الحقل الكهربائي. من جهة أخرى، العزم القطبي الظاهر و طاقة النشاط (مستقلة عن الحقل الكهربائي) يُظهران ارتباطا خطيًا مع العمق (z)، هذا الأخير يمكنه تفسير تغيّر n و $E_{a,eff}$ بفعل V_{Gstr} و T. بالفعل إن إنخفاضهما يمكن أن يعود الى مساهمة تراكمية لعدة أفخاخ ذات طاقات نشيطة و عزوم أقطاب مختلفة، حيث قمنا بإقتراح إنّ هذه الأفخاخ تنتمي إلى عائلة العيوب O_{3-X}-Si_X-Si-H (أو مركز P_b مركب هيدروجيني).

المفاتيح: NBTI، أفخاخ السطح الفاصل، أفخاخ "Border traps"، ضخ الشُحنات، OTFOT، انتشار التدهور، توزع أفقي للأفخاخ، توزع عمودي للأفخاخ، الأوكسيد القريب من السطح الفاصل.

RESUME

La miniaturisation des composants électroniques a entraîné une réduction accélérée de l'épaisseur du diélectrique de la grille des transistors d'un nœud technologique à un autre. Ceci a induit une augmentation du champ électrique de la grille ainsi qu'une augmentation de la température de fonctionnement des circuits intégrés (CI's). En conséquence, plusieurs problèmes de fiabilité des CI's sont apparus, en particulier Negative/Positive Bias Temperature Instability (N/PBTI). En effet, le BTI influence le fonctionnement des CI's ainsi que leurs durées de vie en créant des pièges à l'interface (Si/SiO_2) et dans l'oxyde de grille. De ce fait, la compréhension des mécanismes de formation des pièges, créés à l'interface substrat/isolant et dans la région d'oxyde près de l'interface, est importante et utile pour la modélisation de la dégradation NBTI et la prédiction de la durée de vie des composants. Ainsi donc, l'objectif de cette thèse est la caractérisation électrique de la dégradation NBTI en utilisant de nouvelles méthodes et de nouveaux concepts afin de mieux appréhender et analyser les pièges impliqués dans la dégradation NBTI, et par voie de conséquence développer des modèles fiables pour prédire la durée de vie des dispositifs.

A cet effet, nous proposons une nouvelle méthode, nommée On The Fly Oxide Trap (OTFOT), pour extraire la dégradation NBTI. En utilisant le pompage de charge à haute et basse fréquences. La méthode OTFOT permet d'extraire et de séparer les densités des pièges d'interface (ΔN_{it}) et d'oxyde prés de l'interface « border trap » (ΔN_{bt}) et aussi leurs contributions à la dérive de la tension de seuil (ΔV_{th}) sans recourir à d'autres méthodes complémentaires.

De plus, nous avons exploré la génération et l'évolution de la distribution de ΔN_{it} en fonction de la longueur du canal. Nous avons trouvé que la densité ΔN_{it}, induite par le stress NBTI, n'est pas uniforme le long du canal. Les résultats expérimentaux révèlent une propagation de la dégradation. Cette dernière commence à partir des bords source/drain et puis pénètre au centre du canal. Elle est accélérée par la température et le champ électrique jusqu'à la saturation. Cependant, l'accélération par le champ électrique et plus important que celle de la température. Aussi, les transistors à canaux courts se dégradent plus rapidement que ceux à canaux longs.

Finalement, Nous avons aussi scanné le profile de ΔN_{bt} en fonction de la profondeur (Z) dans l'oxyde de grille prés de l'interface des transistors PMOS. Selon nos données expérimentales, l'exposant (n) de la loi en puissance (t^n) qui gère l'évolution temporelle de ΔN_{bt}, ainsi que l'énergie apparente d'activation ($E_{a,eff}$) diminuent avec la température (T) et la tension (V_{Gstr}) de stress. En outre, le moment dipolaire effectif (a_{eff}) et l'énergie d'activation (E_a) (indépendante du champ électrique) ont montré une dépendance linéaire avec Z. Ceci peut expliquer la variation de n et $E_{a,eff}$ avec T et V_{Gstr}. En effet, leur diminution peut être causée par la contribution cumulative des pièges ayant différentes énergies d'activation et différents moments dipolaires. Nous avons suggéré que ces pièges sont probablement liés à la famille de défauts $O_{3-x}Si_xSi$-H (ou le centre complexe P_b hydrogéné) localisé dans la région sub-oxyde prés de l'interface.

Mots clés: NBTI, Pièges d'interface, "Border-trap", Pompage de charge, OTFOT, Propagation de la dégradation, Distribution latérale, Profile vertical, Oxyde prés de l'interface.

ABSTRACT

The continuous device shrinking has accelerated the reduction of the gate dielectric from technology node to another. This fact has induced a gate electric field increase and enhanced the IC's working temperature. As a consequence, many reliability issues have been taken place, especially Negative/Positive Bias Temperature Instability (N/PBTI). Indeed, the BTI impacts IC's working as well as their life times by creating traps at the interface (Si/SiO_2) and in the gate oxide. Therefore, understanding the mechanisms of trap formation at the dielectric/substrate interface and interfacial region is useful for NBTI modelling and life time prediction. The aim of this thesis is the electrical characterization of the NBTI degradation by using new methods and concepts in order to better analyze the traps involved in NBTI and subsequent development of reliable models.

We propose a new method, named on the fly oxide trap (OTFOT), to extract NBTI degradation in MOS transistors. Using alternatively high and low frequencies, OTFOT method separates and extracts the interface trap (ΔN_{it}) and border trap (ΔN_{bt}) densities independently and also their contributions to the threshold voltage shift (ΔV_{th}), without needing additional methods.

In addition, we have investigated the generation and evolution of ΔN_{it} distribution with respect to the transistor gate length. We have found that NBTI-induced ΔN_{it} is not uniform along the channel length. The experimental results reveal an evident propagation of the NBTI degradation. This propagation starts from source/drain channel edges and penetrates into the channel center. It is accelerated by temperature and electric field until saturation. However, field-accelerated propagation seems more important than temperature-accelerated one. Moreover, transistors with shorter channel length degrade more rapidly than those with longer channel length.

Finally, we have also screened ΔN_{bt} depth in the interfacial oxide region of PMOS transistors. According to experimental data, the exponent (n) of the power-law time dependence of ΔN_{bt} as well as its apparent activation energy ($E_{a,eff}$) decrease with stress temperature (T) and voltage (V_{Gstr}). Furthermore, the effective dipole moment (a_{eff}) and field-independent activation energy (E_a) have revealed a linear relation with depth distance (Z), hence could consistently explain the variation of n and $E_{a,eff}$ with T and V_{Gstr}. In fact, the former parameters decrease because of the cumulative contribution from traps having different thermal activation energies. We hypothesize that such traps could most likely be related to $O_{3-x}Si_xSi$-H family defects (or P_b center hydrogen complex) located in the interfacial sub-oxide region.

Index-Terms: NBTI, Interface-trap, Border-trap, Charge-pumping, OTFOT, Lateral distribution, Vertical profiling, interfacial oxide layer.

ACRONYMS

BTI … Bias Temperature Instability
BTS … Bias temperature stress
B–H … Boron-hydrogen bond
C-P … Charge-pumping
CDTA … Centre de Développement des Technologies Avancées
CDS … Caractérisation des dispositifs à semi-conducteurs
CMOS … Complementary metal oxide semiconductor
C-V … Capacitance-voltage characteristics
DCIV … DC current-voltage characteristics
DMN … Microelectronics and Nanotechnology Division
DOS … Density of state distribution
DRR … Dispersive-reaction-rate
DSO … Digital scope
DUT … Device under test
EOT … Equivalent oxide thickness
EPR … Electron paramagnetic resonance
ESR … Electron spin resonance
FNR … National Funding of Research
GC … Geometric component
GPIB … General Purpose Interface Bus
GEEI … Genie Electric et Electronic Institute
h^+ … Hole carriers
H … Neutral atomic hydrogen
H_2 … Hydrogen molecule
H^+ … Hydrogen ion
HCI … Hot carrier injection
HBr … Hydrogen bromide
HDL … Harry-Diamond-Laboratories
HPSMU … High power source monitor units
IC's … Integrated circuits
I_{CP}–V_L … Gaussian-like CP-current characteristics
I_{DS}-V_{GS} … Transfer characteristics
I_{DS}-V_{DS} … Direct characteristics
ISiT … Institut SiliziumTechnologie
LabVIEW … Laboratory Virtual Instrument Engineering Workbench
LPCVD … Low pressure chemical vapour deposition
LOCOS … Local oxidation of silicon
LDD … Lightly doped drain
MFCP … Multi-frequency charge pumping
MOS … Metal oxide semiconductor
MOSFET … Metal oxide semiconductor field effect transistor
MPE … Multiphonon emission
MPFAT … Multiphonon-field-assisted tunneling
MSM … Measure/stress/measure
NBTI … Negative Bias Temperature Instability
OTF … On the fly
OTFIT … On the fly interface-trap
OTF-V_{th} … On the fly threshold voltage
OTFOT … On the fly oxide trap

PBTI	...	Positive Bias Temperature Instability
PARES	...	Process and reliability evaluation structures
PEV	...	Process evaluation vehicle
PID	...	Proportional integral derivative
P–H	...	Phosphorous -hydrogen bonds
$POCL_3$	...	Phosphorous oxychloride
P_b-H	...	Saturated interface dangling bond
PGU	...	Pulse generator unit
$O_{3-x}Si_xSi\text{-}H$	...	P_b center hydrogen complex
R-D	...	Reaction-diffusion
RDD	...	Reaction-dispersive-diffusion
RIE	...	Reactive ion etching
RTNO	...	Rapid thermal-nitrided oxides
SDR	...	Spin dependent recombination
Si	...	Silicon
Si/SiO_2	...	Silicon/silicon dioxide interface
SiO_x,	...	Interfacial oxide region (transition region, SiO_x, $x < 2$)
SiO_2	...	Silicon dioxide
Si–H	...	Silicon-Hydrogen Bond
SILC	...	Stress-induced leakage current
SMU	...	Source monitor units
SiON	...	Nitrided oxide
HfSiON	...	Halfnium Nitrided oxide
HK	...	High k
TDDB	...	Time-Dependent Dielectric Breakdown
TDDS	...	Time-dependent defect spectroscopy
TEOS	...	Tetra-ethyl-ortho-silicate
TFT	...	Thin film transistor
$(Si_3 \equiv Si^{\bullet})$	...	P_b and P_{b0} center defects
$(Si_2O \equiv Si^{\bullet})$	...	P_{b1} center defect
$(O_3 \equiv Si^{\bullet})$	...	*E’* center defect
UMBB	...	Université M’hamed Bougara Boumerdes
VMU	...	Voltage monitor units
VSU	...	Voltage source units
WKB	...	Wenzel-Kramers-Brillouin
ZTC	...	Zero temperature coefficient

LIST OF SYMBOLS

Symbol	Unit	Description
A_G	cm^2	Gate area
a_{eff}	q. Å	Effective dipole moment
a_0	q. Å	Effective dipole moment at Z_0
C_{OX}	F/cm^2	Oxide capacitance
C_{Dep}	F/cm^2	Capacitance of the depletion layer
C_{fb}	F/cm^2	Flatband capacitance
D_{it}	$cm^{-2}eV^{-1}$	Density of interface state
$E_{a,eff}$	eV	Apparent activation energy
E_a	eV	Activation energy
E_i	eV	Midgap energy
$E_{em,e}$	eV	electron emission energy level
$E_{em,h}$	eV	hole emission energy level
E_{inv}	eV	Lower energy bound sensed by CP
E_{acc}	eV	Upper energy bound sensed by CP
ΔE^*	eV	Band energy scanned in the oxide
$E_{a,f}$	eV	Activation energy of forward reaction
$E_{a,r}$	eV	Activation energy of reverse reaction
E_D	eV	Combined activation energy for D_{H2}, k_H, and k_{H2}
E_0	eV	Activation energy at Z_0
E_{g0}	eV	Energy bandgap at $T = 0 K$
E_{am}	eV	Median activation energy
E_{ox}	V/cm	Oxide electric field
E_{ref}	V/cm	reference electric field
E_c	V/cm	Electric field due to the inversion layer carriers
E_L	V/cm	Lateral electric field
f	Hz	Frequency
f_H	Hz	High frequency
f_L	Hz	Low frequency
f_i	-	Occupation function of the state i
g_m	A/V	Transconductance
$g_{m,max}$	A/V	Maximum transconductance
h	J.s	Planck's constant
$\hbar$	J.s	Reduced Planck's constant($h/2\pi$)
I_{off}	A	Off current
I_{Dlin}	A	Linear drain current
I_{Dsat}	A	Saturation drain current
I_{CP}	A	Charge pumping current
$I_{CP,H}$	A	Maximum CP-current at f_H
$I_{CP,L}$	A	Maximum CP-current at f_L
ΔI_{CP}	A	NBTI-induced *CP*-current degradation
ΔI_{Geo}	A	NBTI-induced Geometric component current
K	eV /K	Boltmann's constant
K_{ij}	s^{-1}	Transition rates from state f_i to state f_j.
k_H	cm^2/s	Generation rate of H_2
k_{H_2}	s^{-1}	Dissociation rate of H_2
L_{eff}	cm	Effective gate length
L_G	cm	Gate length
ΔL	cm	LDD overlap
$m_{n(p)}$	kg	Effective mass of electron(hole) in the dielectric
N_0	cm^{-2}	Initial saturated Si-H bonds
N_{it}	cm^{-2}	Interface trap density

N_{CP}	cm^{-2}	Trap density measured by charge pumping
$N_H^{(0)}$	cm^{-3}	Hydrogen density at the interface
N_H	cm^{-3}	Diffusing hydrogen atom density
N_{H^+}	cm^{-3}	Hydrogen ion
N_{H_2}	cm^{-3}	Hydrogen molecule density
n	-	Power-law time exponent
n_i	cm^{-3}	Intrinsic carrier concentration in silicon
n_S	cm^{-3}	Concentration of detrapping states at substrate
n_G	cm^{-3}	Concentration of detrapping states at poly-Si
N_D	cm^{-3}	Substrate doping
ΔN_{it}	cm^{-2}	NBTI-induced interface trap density
ΔN_{ot}	cm^{-2}	NBTI-induced oxide trap density
ΔN_{bt}	cm^{-2}	NBTI-induced border trap density
ΔN_{ht}	cm^{-2}	NBTI-induced hole trap density
n_T	$cm^{-3}eV^{-1}$	Volume density of the oxide-trap
N_t	cm^{-2}	Total density of localized states
q	C	Electron charge
Q_{ss}	C	Surface state charge
Q_{it}	C	Interface-trapped charge
Q_{ot}	C	Oxide-trapped charge
Q_{bt}	C	Border charge
Q_{CP}	C	Charge recombined per cycle
$Q_{CP,H}$	C	Charge recombined per cycle at f_H
$Q_{CP,L}$	C	Charge recombined per cycle at f_L
Q_f	C	Fixed charge
Q_m	C	Mobile oxide charge
Q_{inv}	C	Mobile charge of the inversion layer
Q_T	C	Total charge in the Si/SiO_2 system
S	decade/V	Subthreshold slope
SS	V/decade	Subthreshold swing
t	s	Time
t_{str}	s	Stress time
$t_{em,e}$	s	Electron emission time
$t_{em,h}$	s	Hole emission time
t_r	s	Rise time
t_f	s	Fall time
t_{acc}	s	Electron capture time during accumulation of pMOSFET
t_{inv}	s	Hole capture time during inversion of pMOSFET
T_H	s	High level voltage duration
T_L	s	Low level voltage duration
T	°C	temperature
T_0	°C	Reference temperature
T_S	-	Tunneling probability of holes from Si/SiO_2 to trap
T_G	-	Tunneling probability from trap to poly
T_{ox}	Å	Gate oxide thickness
V_{th0}	V	Unstressed threshold voltage
V_{th}	V	Threshold voltage
V_{fb}	V	Flatband voltage
V_L	V	Pulse low level voltage
V_H	V	Pulse high level voltage
ΔV_{th}	V	NBTI-induced threshold voltage shift
ΔV_G	V	Pulse amplitude
V_D	V	Drain voltage
V_S	V	Source voltage
V_G	V	Gate voltage
V_R	V	Reverse voltage
V_{Gstr}	V	Stress voltage
V_{GS}	V	Gate/source voltage

V_{DS}	V	Drain/source voltage
ΔV_{it}	V	Voltage shift induced by interface-trap
ΔV_{bt}	V	Voltage shift induced by border-trap
ΔV_{ot}	V	Voltage shift induced by oxide-trap
W_G	cm	Gate width
Z	Å	Depth distance in the oxide
Z_0	Å	Interface roughness thickness (Z_0 ~ 3.2 Å)
Z_{max}	Å	Maximum depth in the gate oxide
Z_{min}	Å	Minimum distance
$Z_{n(p)}^{CP}$	Å	Maximum CP tunneling depth of electron(hole)
α	V/°C	Threshold voltage temperature coefficient
β	-	Dispersion parameter
δ	Å	Length of Si-H bond (1.5 Å)
δ'	-	Dirac function
ε_{si}	$F.cm^{-1}$	Permittivity of the silicon
ε_0	$F.cm^{-1}$	Permittivity of the air
ε_{sc}		Dielectric constant of the silicon
ε_{ox}		Dielectric constant of the oxide
ϕ_F	eV	Fermi-level energy
ϕ_{ms}	eV	Metal-semiconductor work function
$\phi_{n(p)}$	eV	Energy barrier height for (electron)hole tunneling
χ	eV	Semiconductor electron affinity
χ_i	eV	Insulator electron affinity
$\lambda_{n(p)}$	Å	Attenuation coefficient for electron (hole)
γ	cm/V	field accelerator factor
μ_0	$cm^2V^{-1}s^{-1}$	Low vertical electric field mobility
μ_{eff}	$cm^2V^{-1}s^{-1}$	Carrier effective mobility
μ_{H+}	$cm^2V^{-1}s^{-1}$	Hydrogen ion mobility
ν	Hz	Attempt frequency
v_{sat}	cm/s	Saturation velocity
v_{thp}	cm/s	Thermal velocity of hole
v_{thn}	cm/s	Thermal velocity of electron
ρ_{ht}	cm^{-3}	Density of trapped holes
σ_n	cm^2	Capture cross section of electron
σ_p	cm^2	Capture cross section of hole
σ	eV	Spread of trap energy distribution
τ	s	Electron transit time from source to drain

PREAMBLE

The metal-oxide-semiconductor field oxide transistor (MOSFET) was invented in 1960 and integrated circuits (ICs) using these new transistors which were commercially available few years later. Since that time, IC manufacturing faced major yield and reliability concerns. At the beginning, quality targets were believed to be reached and products to be free of defects or systematic failures, after final packaging. The constantly growing complexity of IC products and the increasing cost incurred by loss of operation caused by failures have made reliability, maintainability, availability, and safety, critical points. Consequently, today expectations is that IC products are not only free from defects and systematic failures at time t = 0 (when they are used at the first time), but also perform the required function without failure for a stated time interval. However, the question of whether a given item will operate without failures during a stated period of time cannot be answered by a simple yes or no, on the basis of a compliance test. Experience has shown that only a probability for this occurrence can be given. Therefore, reliability is the probability that the item will perform its required function under given conditions for a defined time interval.

As reliability issues become nowadays more critical parameter in IC fabrication, modeling is increasingly requested to provide design tools not only to achieve better device performance, but also more robust reliability margins. Modeling is required for the theoretical investigation of the failure mechanisms and their root causes, but also it is needed to explore their relationships with front- and back-end-of-the-line technology on one hand and with design needs and test effectiveness on the other hand. Since failures are mostly related to the presence of defects and traps in active and passive layers, modeling is expected not only to investigate the intrinsic defects associated with new materials and their interfaces, but also extrinsic defect creation mechanisms during wafers processing, such as plasma damage and ion implantation induced damage in gate stacks. **Figure 1** illustrates the failure rate over time for a given set of devices. The failure follows distribution referred as bath tub curve.

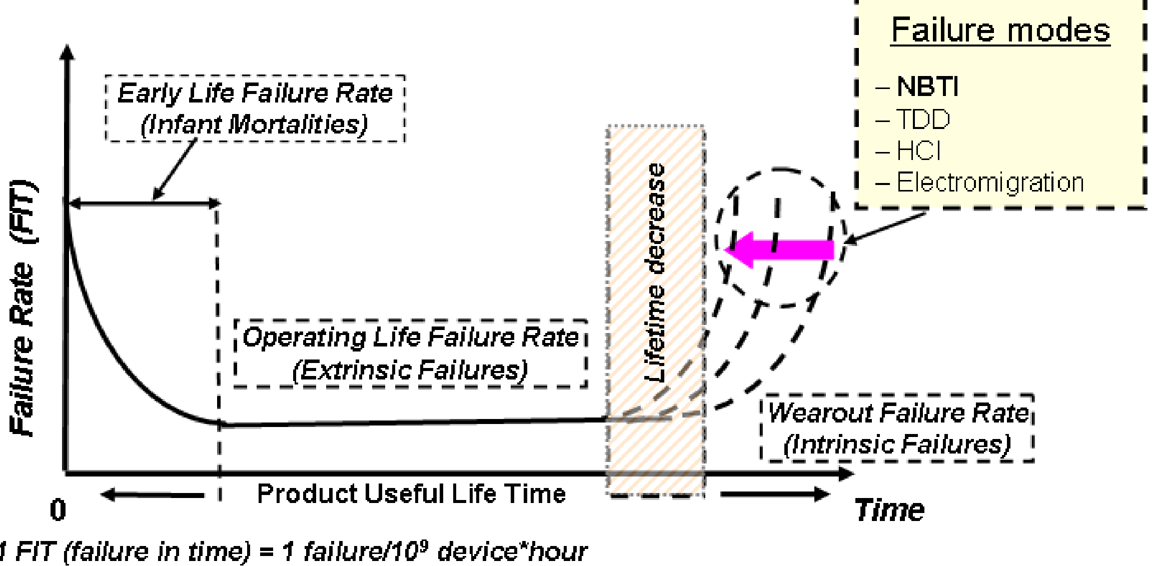

Figure 1: Reliability Bath Tub Curve

Early failures (infant mortalities) occur primarily to process defects, such as the introduction of extrinsic impurities, improper deposition bonding materials, or the deposition of excess material causing an errant conduction pathway. Once these devices have failed, the failure rate level becomes constant for the useful lifetime of the device. Wearout mechanisms begin to increase at the end and play a significant role. However, failure modes, such as hot carrier injection (HCI), time dependent dielectric breakdown (TDDB), electromigration, and negative bias temperature instability (NBTI), shift the right edge of the bath tub to the left causing reduction of the useful life time (or end of life).

However, among all failure modes, the root causes of NBTI are still under a controversial debate. While most researchers agree that the creation of oxide and interface charges is at the origin of NBTI, models are often different. It has been revealed that the degradation is particularly difficult to predict under dynamic (stress and recovery) bias conditions. Lacking a suitable model for the description of the degradation under arbitrary bias conditions, the degradation of a transistor in a realistic circuit setting is hard to predict. Model development is particularly slowed down by the difficulties of fitting the experimental data. As such, model evaluation is closely tied to the development and detailed understanding of fundamental physical mechanisms of trap creation and annealing during wafer processing as well as under operating conditions. This predictive model for BTI (p-MOSFET and n-MOSFET) can assist design for reliability through electrical simulation and behavioral level modeling of degradation to check impact on analog/digital circuits.

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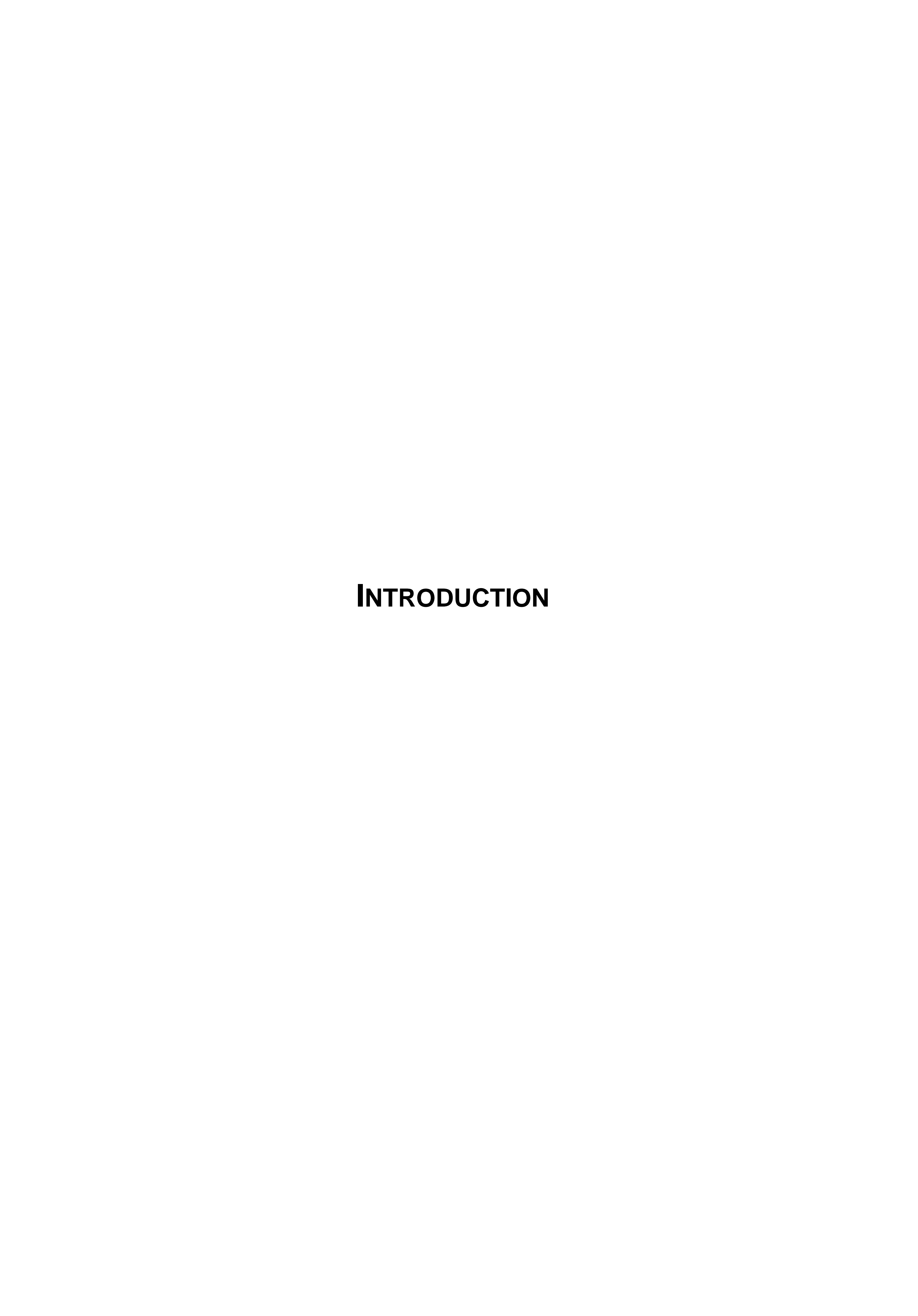

INTRODUCTION

INTRODUCTION

Since its invention, metal oxide semiconductor field effect transistor (MOSFET) has revolutionized semiconductor industry. It has allowed the development of the integrated circuits by placing a large number of transistors on a single chip. As predicted by Moore's law **[1]**, the integration complexity has doubled every 18 months, affecting many aspects of our life. The continuous downsizing of the device has greatly advanced the semiconductor industry by increasing the performance, decreasing the power consumption, and reducing the manufacturing cost per transistor of IC components. This makes products smaller, faster, and cheaper. At present, there are more than a billion of transistors in microprocessor. This integration has been drained by reducing the transistor critical elements such as the channel gate length and the gate dielectric thickness. However, when the gate oxide thickness had reached the 1 nm range and the gate length the 100 nm in the early 2000s, the conventional MOSFET scaling trend began to run out. The deviation from conventional scaling was firstly caused by the exponentially increase of the gate leakage current. Conventional scaling also required a continuous reduction of the chip supply voltage (V_{DD}) as the gate oxide thickness was scaled to maintain a constant oxide electric field, and consequently it also required a corresponding device threshold voltage (V_{th}) reduction. Due to the non-scaling subthreshold slope of the MOSFET, a reduced device V_{th} unavoidably induced subthreshold leakage current increase, which started to become itself another large portion of total chip power. For these reasons, conventional geometrical scaling had to come to run out. However, performance enhancements did not stop in the early 2000s but keep still going due to introduction of three main innovations in the recent CMOS technology nodes: channel strain engineering for mobility enhancement (90 and 65 nm nodes), high-k/metal gate technology for reduced gate leakage current (45 and 32 nodes), tri-gate device architecture for improved electrostatic control (22 nm node). Actually, the aggressive scaling of MOS transistor toward 22 nm technology node has arisen a statistical (device to device, die to die, wafer to wafer, *etc.*) fluctuation of transistor parameters. These fluctuations, in nano-dimensions, could have been easily ignored in micron-size transistors of 1990s, but cannot be avoided in nano-scale transistors studied in current MOS technology.

Additionally, defects in the Si-SiO_2 system were always a source of instabilities of MOS devices and their long term reliability. They are either pre-existing in the Si-SiO_2 system due to poor fabrication process or induced by stress. Historically, the pre-existing defects as such the mobile ions (Q_m), fixed oxide charge (Q_f), and oxide traps (Q_{ot}) were the major obstacles in the development of stable MOSFETs in the 60s. However, after the identification of its origin, it has been eliminated by the combination of cleanroom environment, deionized water and gettering processes. The fixed oxide charge in the bulk oxide, residing close to the interface with silicon substrate, can be minimized by appropriate oxidation recipes, and has been well controlled. In addition, defects are formed not only within the bulk of the amorphous oxide structures, but also at the Si/SiO_2 interface (Q_{it}) e.g., dangling bonds. This is mainly due to the lattice mismatch between two dissimilar materials combined together. However, interfacial defects cannot be removed or reduced, like bulk defects, through any sort of purification. At the Si/SiO_2 interface of a MOS transistor, interfacial defects (dangling Si-bonds) are passivated by using hydrogen (Si-H), which only provides a time-zero solution. However, under high

electric field and elevated temperature, interface and oxide properties may degrade by different modes:

- Gate dielectric film may breakdown under high field, and completely loses the insulating property. Dielectric breakdown is a long-standing subject in the study of IC's. The defect related transistor instabilities discussed above; formation of oxide defects and their subsequent alignment can increase the gate leakage current to such an extent that the dielectric film will no longer be effective in insulating the gate of a MOS structure, hence inducing dielectric breakdown of transistors. It is easy to see that as the oxide thickness scales down the oxide sustains less voltage. In practice, MOSFET operates at voltages much lower than the dielectric breakdown voltage, but there is still a finite probability of breakdown. Time dependent dielectric breakdown (TDDB) is a key transistor reliability issue in modern MOS transistor, which often limits its operating lifetime **[2-4]**.
- Another failure mode is the hot carrier injection (HCI), which induces non-uniform generation of defects near the drain of MOS transistors **[5]**. HCI was the most critical reliability issue in the 80s and early 90s, and was extensively studied since then. It occurs when high voltage is present on both gate and drain terminal, a lot of carriers are flowing in the channel, and there is high longitudinal electric field near the drain region. Carriers are accelerated in this high-field region, and the carrier temperature increases. If the carriers gain sufficient energy, they can cross the energy barrier of the silicon/oxide interface and get injected into the insulator. Typically the maximum hot carrier generation occurs when gate voltage is around half of the drain voltage. This bias condition only occurs when the transistor is switching from off state to on state or *vice versa*. The attempt to minimize HCI led to the development of lightly doped drain (LDD) structure, the nitrided silicon oxide gate dielectric, and is one of the motivations for the scaling of supply voltage. As the supply voltage has scaled to around 1 V, which is less than the bandgap of silicon, hot carriers are much less a reliability concern to current technologies, though it is still regularly examined.
- The saturated interface dangling bonds (Si-H) break, which allows to dangling bond to reappear again during the operation of a transistor, inducing time-dependent instabilities in the transistor parameters, which is one of the major reliability concerns in current MOSFET technology. Such interface defect related instability is dominant in p-MOSFET and associated with negative bias temperature instability (NBTI) phenomenon.

Moreover, the introduction of new materials within MOS structure such as high-k gate dielectric and oxide nitride to reduce gate leakage current **[6]** and metal gate to avoid poly-depletion effects **[7]** have generated additional issues related to defects in the oxide material during NBTI stress. Consequently, hole trapping into oxide defects has become an additional NBTI mechanism and electron trapping into oxide defects of n-MOSFET associated with positive bias temperature instability (PBTI) **[8]**. According to the International Technology Roadmap for Semiconductor prediction **[9]**, the physical gate length of CMOS devices can be expected to scale down to 7 nm before it approaches the physical limitation, the reliability concerns become one of the major barrier preventing the technology to scale down further. One of the consequences of non-ideal scaling in the below-100 nm technology nodes is that the electric field in the gate dielectric becomes significantly large, which accelerates the intrinsic failure mechanisms like TDDB, HCI, and so on. As the device dimensions shrink, the number of transistors per area increases, therefore in turn, the on-chip power density increases. The increasing leakage

current makes the power dissipation situation even worse. In fact, the high temperature in the circuits due to the high power density accelerates intrinsic failure mechanisms such as NBTI and PBTI. In a word, the decreasing reliability trend in advanced technology nodes is worsened due to the high gate dielectric electric field and power density in devices and circuits.

BTI is a wearout mechanism resulting in the generation of traps at the Si/SiO_2 interface and in the oxide under high gate voltage (V_G) at elevated temperature. The worst degradation is observed occurring in p-MOS transistor under negative gate bias stress. In these stress conditions, the degradation is called NBTI. Typically, the NBTI stress conditions lie below a temperature of 200°C and below an electric field of ~ 5-8 MV/cm in inversion regime ($V_G < 0$ for p-MOSFET). Higher electric fields cause additional degradation due to stress induced leakage current (SILC) and should be avoided to capture pure (or intrinsic) NBTI damage. The most important manifestations of the NBTI degradation consist of an increase of the threshold voltage (V_{th}) and off current (I_{off}), and a decrease of linear drain current (I_{Dlin}) and saturation drain current (I_{Dsat}), transconductance (g_m), subthreshold slope (S), and channel carrier mobility (μ_{eff})

Historically, the effect of NBTI on the surface states (Q_{ss}) was observed for the first time in the sixties by Miura et *al.* **[10]** and investigated in more details by Deal et *al.* **[11]**. However, a physical interpretation of the phenomenon started arising in 1977, when Jeppson and Svenssons proposed for the first time the Reaction-Diffusion (R-D) model to explain the NBTI-induced surface-trap growth **[12]**. The R-D model assumes that the gate bias initiates a field-dependent reaction at the Si/SiO_2 interface that generates interface traps by breaking the passivated Silicon-Hydrogen (Si–H) bonds. It can reproduce the power-law dependence of the surface trap generation without making pre-assumption on surface bonds. Even if the R-D model of Jeppson and Svenssons **[12]** explained the time power-law dependence of NBTI degradation, the exact mechanisms behind such behavior were still unclear and the causes of bond dissociation unspecified. Alam et *al.* **[13-18]** were the first to link temperature and electric field to R-D framework. Indeed, as the NBTI degradation is enhanced by high negative electric field at the interface, holes of the inverted layer of the p-MOSFET participate to Si-H bonds dissociation **[14-17,19,20].** The released hydrogen species diffuse away from the interface and dimerize to form H_2 molecule **[19,21]**, subsequently explaining the observed 1/6 power-law time exponent in the experimental data **[14-18]**. In addition, this model gives a consistent interpretation of interface trap creation dependence on nitrogen **[17,18]**.

However, if only holes are playing an essential role in NBTI degradation for p-MOSFET in inversion regime and since n-MOSFET biased in accumulation regime also have holes at the surface, they should show similar degradation of threshold voltage. However, they do not **[22,23]**. To explain this behavior, Tsetseris *et al.* **[24,25]** have proposed the interaction between the positive hydrogen ion (H^+) at the interface and the Si-H bonds. Based on first-principal calculation **[24]**, they conclude that it is more difficult for boron-hydrogen bonds to be broken in p-substrates. Thus, the different behavior of p- versus n-MOSFETs in this model is due to the ease or difficulty of breaking P–H and B-H bonds in the Si substrate. Threshold voltage shifts in this case are due to interface traps, oxide charge, and a change in the substrate doping density after P–H or B-H depassivation. Another explanation involves the interface and oxide charge states **[26]**. Interface traps, being acceptors in the upper half of the band gap and donors in the lower half affect threshold voltage shifts in n- and p-MOSFETs differently.

At inversion, the n-MOSFET has negative and the p-MOSFET has positive interface trap charge. Since the oxide charge is positive in both cases, then p-MOSFET is more severely affected **[26]**.

Later, it has been shown that reaction-diffusion theory presents inconsistency regarding the relaxation phase of NBTI **[27-29]**. That fact has led to the development of several extended and modified R-D models **[30-40]**. Assuming two different diffusion coefficients; fast diffusion in the oxide and slow diffusion in the polysilicon, Alam et *al.* **[31]** proposed a model named “two-region R-D model”. The authors were motivated by the actual gate oxides which are a few nanometers thick making the interpretation based on the diffusion of hydrogen into the oxide questionable. Hence, they suggested that the diffusion process not only occurs in the oxide, but inside the polysilicon as well. This model was expected to explain the much larger observed recovery range, but actually this range is slightly increased. Other groups **[30,32]** proposed two-interface R-D model, in which a released atomic hydrogen diffuse in the oxide until reaching the polySi/oxide, where a second chemical reaction takes place at the interface creating H_2 molecule. Since the diffusivity in the oxide is considered to be very high compared to the diffusivity in the polysilicon, the hydrogen stacked in the oxide is able to cause a fast initial recovery. However, for long stress times, this higher oxide diffusivity locks the hydrogen in the polysilicon. This means that the short recovery effect vanishes. In addition, immediate dimerization in the oxide was suggested in **[21,34]**, where both H and H_2 diffuse in the oxide, hence affecting the initial stress phase, but the relaxation is still the same compared to the standard R-D model. Some authors **[35-37**] proposed dispersive distribution of Si-H bond energy at the interface. At the beginning, the weaker Si-H bonds break, followed later by the breakage of the strong one at longer stress time or higher voltage. The charge pumping (*C-P*) technique, which is an appropriate tool for interface trap measurements, revealed a small recovery of interface trap after NBTI stress. This amount is not able to explain the overall recovery of the NBTI-induced threshold voltage shift. That is why the interface traps are considered as permanent component once created **[35,37-40].** Dispersive hydrogen transport, so-called reaction-dispersive-diffusion (RDD) model, was also suggested to explain the long recovery tails observed in experiments **[41, 42]**. In this model, the hydrogen concentration is divided into a contribution of free hydrogen in a conduction state and hydrogen setting at trap with a deeper energy level, which needs to be thermally activated prior to be able to diffuse. Therefore, only hydrogen located at the interface is allowed to re-passivate the dangling bond which delays the reverse rate since most of the hydrogen is trapped.

Dispersion of the defect creation is also assumed in R-D theory based models to improve the quality of the prediction **[21, 42-44].** However, these models do not take into account the frequently observed correlation between the created interface states and the oxide charges **[45,46]**. Consequently, they often fail to reproduce the temperature and voltage dependence of the overall degradation behavior, especially the relaxation phase. In fact, investigations of the universal recovery have revealed that there exists a permanent component in addition to a recoverable component, each one of them is caused by its own physical mechanism **[28,41].** The appearance of oxide traps and interface traps was explained by independent processes adding up into the two components, i.e. the recoverable and the more or less permanent part of the BTI degradation. As a result, hole trapping into defects was suggested as the recoverable component and assumed to be due to elastic tunneling of holes into preexisting traps **[35].** By contrast, a hydrogen reaction like the Si-H bond breakage in the

R-D model was ascribed to the permanent component. However, Grasser *et al.* **[46]** recognized that the recorded threshold voltage curves follow the same pattern at different stress temperatures and voltages. Therefore, these curves can be scaled so that they overlap for the stress and the relaxation phase. As a consequence, both mechanisms were assumed to be coupled and therefore do not take place independently. In fact, they proposed a so-called two-stage model **[29]**, which is based on four-well-energy model, as an alternative to R-D and its variants. In the first stage, the model assumes an inelastic tunneling of holes into deep traps, inducing E' defect creation which can be repeatedly charged and discharged by electrons tunneling in or out of its dangling bond. The associated switching behavior is in agreement with the experimental observations of relaxation component. In the second stage, the switching trap interacts with Si-H bonds, detaching the hydrogen and leaving an interface trap. Thus, the switching trap acts as a catalyst to interface state generation **[29]**. More recently, the two stage model has been severely criticized regarding the duration of stress time **[47,48]**. Indeed, the two stage model has extensively been studied for short stress time (<1s) **[29,49]** and recovery followed short stress time. However, when the model was extended to longer stress time, its predictions showed discrepancies with experimental observations **[47]**. It was concluded that there are no combination of input parameters that reproduces the observed DC, AC, and duty cycle stress dependent NBTI degradation **[47]**. As an alternative, Mahapatra *et al.* **[48]** suggested a framework based on H/H_2 conversion R-D model, in which uncorrelated contribution from interface trap generation and recovery, together with hole trapping and detrapping in preexisting and generated bulk oxide traps, are involved in NBTI phenomena.

In spite of the above-cited models proposed in several publications, no model can nowadays successfully explain all features of the BTI phenomenon. However, it is widely accepted that there are two components responsible for NBTI; permanent and recoverable components **[51,52]**. Regarding the origin of these components, the scientific opinion is divided whether hole trapping is insignificant and only the interface traps degrade and recover **[14,48]**, or the switching trap drives the interface state generation **[29]**, or interface trap generation leads to the formation of a positive oxide trapped charge **[12]**. While some authors **[29]** claim that both components are coupled, others don't find any apparent relationship between them (uncorrelated) **[48,50]**. One component is fast and generally attributed to recoverable NBTI, while the second is permanent **[22,40]**. The fast component is ascribed to hole trapping/detrapping into/from hole oxide traps **[53,54]**. Since, the recoverable component is fast, only fast measurement could capture it. That is why, Ming-Fu Li *et al.* **[54,55]** proposed fast electrical measurement methods to overcome the measurement delay and reduce the relaxation effect of the classical methods **[56,57]**. They showed that the power-law time exponent (n) dependence of NBTI degradation is highly affected by the measurement methods **[53,54]**. However, this has not resolved the controversial debate regarding the NBTI components as well as the exponent, n. Indeed Gasser *et al.* **[58]** have later shown that the so-called permanent actually is not so permanent and is recoverable at large timescale. This quasi-permanent component is itself constituted of two sub-components, one attributed to the interface traps and the other to slower switching oxide traps **[58]**. More recently, based on spin dependent recombination (SDR), Aichinger *et al.* **[59,60]** have identified the microstructure defects of the quasi-permanent component. Besides the conventional P_{b0} center for

interface traps, they have also evidenced P_b center-hydrogen complexes for slower switching oxide traps.

In summary, although many of its different aspects have been recently revealed and discussed. NBTI degradation is still the most controversial topic in reliability community. In fact, several experiments were performed on different technologies using a large variety of sophisticated measurement to properly capture the degradation and to identify its origin. Also, different models have arisen from large amount of data to explain the NBTI features such as the power law exponent, relaxation, the AC behavior, and process effects. All this effort was and is still oriented toward developing know-how as well as know-why to make better predictions for long term reliability and longer useful lifetime of devices under use conditions. In spite of the enormous effort, there is, unfortunately, no consensus regarding the correct physical interpretation of NBTI and theoretical understanding of the degradation phenomena necessary for lifetime projection.

The aim of this thesis is principally the characterization of the permanent or quasi permanent component of NBTI using a new experimental approach based on novel experimental setups. In addition, we propose an original approach of modeling based on the propagation concept of the NBTI degradation. The propagation is related to the lateral progression of the degradation along the transistor channel and the vertical progression into the interfacial oxide region.

This work is not only motivated by the absence of the model that can capture all NBTI features, but also mainly by the ongoing project of the **Clean-Room Facility** at **CDTA**. Indeed, the latter needs hard/soft reliability platform at the backend as well as the qualified manpower with necessary know-how to undertake the evaluation of product reliability i.e. estimation of the lifetime of the devices and circuits issued by this clean-room. The manuscript first starts with the evolution of MOSFET and its instability issues. It also gives the definition the NBTI degradation as well as its historical background. Besides the introductory **Chapter**, the thesis covers five additional **Chapters**. We start by summarizing the most important physical models and the potential defect precursors describing the NBTI degradation. A critical analysis is given on R-D and two stage models giving a clear insight on their controversial results. NBTI gate oxide thickness dependence is also reviewed in the first **Chapter**. In the second **Chapter**, we relate commonly used measure/stress/measure (MSM) protocols in NBTI experiments. It concerns the classical and on the fly (OTF) methods. All are based on current-voltage (*I-V*) and charge pumping (*C-P*) techniques. These techniques are described; especially the capabilities of *C-P* to extract trap distributions as a function of the gate oxide depth and the gate length. Then after, we describe the experimental setups and instrumentations for NBTI stress as well as devices and their process in the third **Chapter**. We also give the electrical test results of characterized MOS devices before NBTI at ambient and elevated temperatures. The theoretical concept of on the fly oxide (OTFOT) method as well as its MSM protocol are presented in the fourth **Chapter**. In addition, NBTI-induced interface and oxide traps extracted by OTFOT are also discussed. Furthermore, we analyze the gate length effect on NBTI and the role of the LDD regions. Finally, in the last **Chapter**, we highlight the lateral and the vertical profiling of NBTI degradation along the gate length and gate oxide, respectively. Moreover, thorough descriptions of their respective MSM protocols are given.

Chapter I

NBTI MODELS AND RELATED-DEFECT IN MOSFET DEVICES

I.1- Introduction

I.2- Metal Oxide Semiconductor (MOS) System

I.3- Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

I.4- Microstructures of Defects in Si-SiO_2 System

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CHAPTER I

NBTI MODELS AND RELATED-DEFECT IN MOSFET DEVICES

I.1- Introduction

Since the first report on NBTI **[10]**, different research groups have attempted to take it into consideration in different models. The most used model for NBTI is the reaction-diffusion (R-D) model. It was first suggested by Jeppson and Svensson in 1977 **[12]**. The model explains the NBTI degradation in two steps. The first step, an electrochemical reaction, assisted by electric field and temperature, occurs at the interface passivated silicon dangling bonds Si-H. The reaction generates interface traps and hydrogen. The second step of R-D model describes the transport of the hydrogen species away from interface into the oxide. Recently, a lack of correct description of relaxation phenomenon, pushes researches to modify and extend R-D models **[17,44,61].** However, the recovery phase is still not captured by the extended R-D models **[62]**. Grasser et *al.* **[29]** have proposed a completely different approach based on hole trapping in the oxide trap followed by interface trap creation. More recently **[48]**, the capabilities of two-stage model in describing the most NBTI degradation features have been fundamentally revised showing only its consistency at short stress period (up to 1s) and fails to interpret data for long stress time. All above cited models are based on traps located at the interface and in the oxide. It is therefore important to start this **Chapter** by giving a description of the physical microstructure of different types of traps before getting insight the main NBTI models.

In this **Chapter**, we first describe MOS System as well as MOSFET devices in sections **§ I.2** and **§ I.3**. Different defects at the interface Si/SiO_2 and in the oxide, which are most involved in NBTI degradation, are also explained in sections **§ I.4**. The R-D model and its variants are reviewed in section **§ I.5** and **§ I.6,** respectively. In section **§ I.7**, the two-stage model is described. Section **§ I.8** clarifies the oxide thickness dependence of NBTI. Discussion and conclusions are respectively given in sections **§ I.9** and **§ I.10.**

I.2- Metal Oxide Semiconductor (MOS) System

In this section, we are concerned primarily with the MOS system. This system has been extensively studied because it is directly related to most silicon planar devices and the actual integrated circuit **[63,64]**. The MOS structure is shown in **Fig. I.1**, where the metal gate and the silicon substrate form the metal plates and the oxide with thickness *(d)* forms the dielectric between the two plates. The MOS capacitor is the structure that creates the conductive channel in a MOSFET. It is used extensively in research as a process control that addresses the need for characterization of ultra-thin oxides and alternative gate dielectrics.

I.2.1- Ideal case

The energy-band diagram of an ideal MOS structure without bias is shown in **Fig. I.2**, for both n-MOS and p-MOS capacitors. In the ideal case, several assumptions have been made such as i) there are no charges present in the dielectric film; ii) the dielectric is a perfect insulator where no current can pass through under different biasing conditions; iii) the semiconductor thickness must be large enough

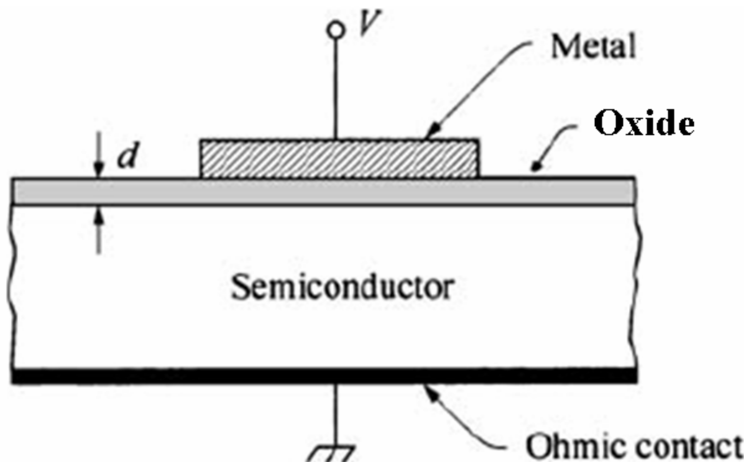


Figure I.1: Metal-oxide-semiconductor (MOS) capacitor **[63]**.

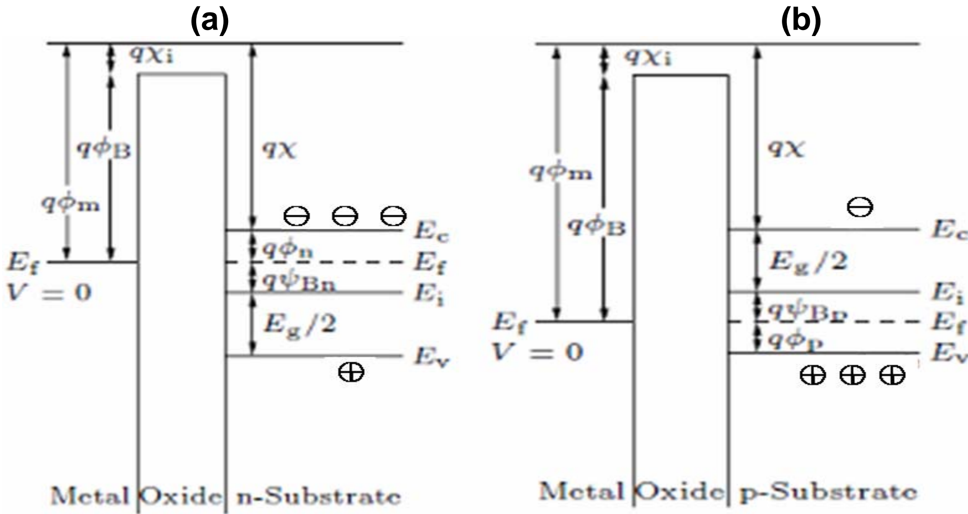


Figure I.2: Energy band diagram of ideal MOS capacitors at V = 0. (a) n-substrate MOS capacitor. (b) p-substrate MOS capacitor **[63]**.

to contain a field free region in the bulk of the substrate despite the applied gate potential; iv) the semiconductor is a uniformly doped substrate; and v) the backside semiconductor-metal contact must be ohmic. Furthermore, we assume that the metal is chosen such the difference between the metal work function ϕ_m and the semiconductor work function is zero, or $\phi_{ms} = 0$. From **Fig. I.2** with above conditions, one can write **[63]**:

$$\phi_{ms} = \phi_m - \left(\chi + \frac{E_g}{2q} - \psi_{Bn} \right) = \phi_m - (\chi + \phi_n) = 0 \qquad \text{for n-type} \qquad (I.1)$$

$$\phi_{ms} = \phi_m - \left(\chi + \frac{E_g}{2q} + \psi_{Bn} \right) = \phi_m - \left(\chi + \frac{E_g}{q} - \phi_p \right) = 0 \qquad \text{for p-type} \qquad (I.2)$$

where χ and χ_i are the electron affinities for the semiconductor and insulator, respectively. ψ_{Bn} ,ψ_{Bp} , ϕ_n , ϕ_p are the Fermi potentials with respect to the midgap and band edges. In other words, the band is flat (flatband condition) when there is no applied voltage. When an ideal MOS

capacitor is biased with positive or negative voltages, basically three cases may exist at the semiconductor surface as illustrated by **Fig. I.3**. These cases are called accumulation (a), depletion (b), and inversion (c).

In the following the n-substrate capacitor will be explained:

(a) When a positive voltage is applied at the contact the conduction band E_C bends down towards the Fermi level E_f that is set constant in the semiconductor where no current flows. This bending yields an accumulation of the majority carriers (electrons) near the interface [see **Fig. 3 (a)**].

(b) Under a small negative voltage the majority carriers are repelled from the interface, involving that the bands are bend up. The intrinsic energy E_i gets closer to E_f [see **Fig. 3 (b)**].

(c) When further increasing the negative voltage this bending continues and once E_i crosses E_f the minority carriers (holes) exceed the majority carriers at the interface. Hence, this case is called inversion, as the interface is inverted [see **Fig. 3 (c)**].

For the p-type structure with holes as majority carriers and electrons as minority carriers only the polarity of the voltage has to be changed.

I.2.2- Non-deal case

In the case of non ideal MOS structure, where charges in the oxide and at the interface affect its electrical properties. Traditionally four basic types of charge are distinguished in dielectrics **[65]**:

- The mobile ionic (charge Q_m, density N_m): they are ionic impurities present in the film. These impurities include Na+, Li+, K+, and possibly H+ which can readily move under bias. However, the processing technologies of today have greatly limited the existence of these ionic impurities due to a process called "gettering" **[66]**. The introduction of HCl in the ambient oxidation would "getter" mobile charge and greatly reducing metal contamination (lifetime killers) and mobile ions.

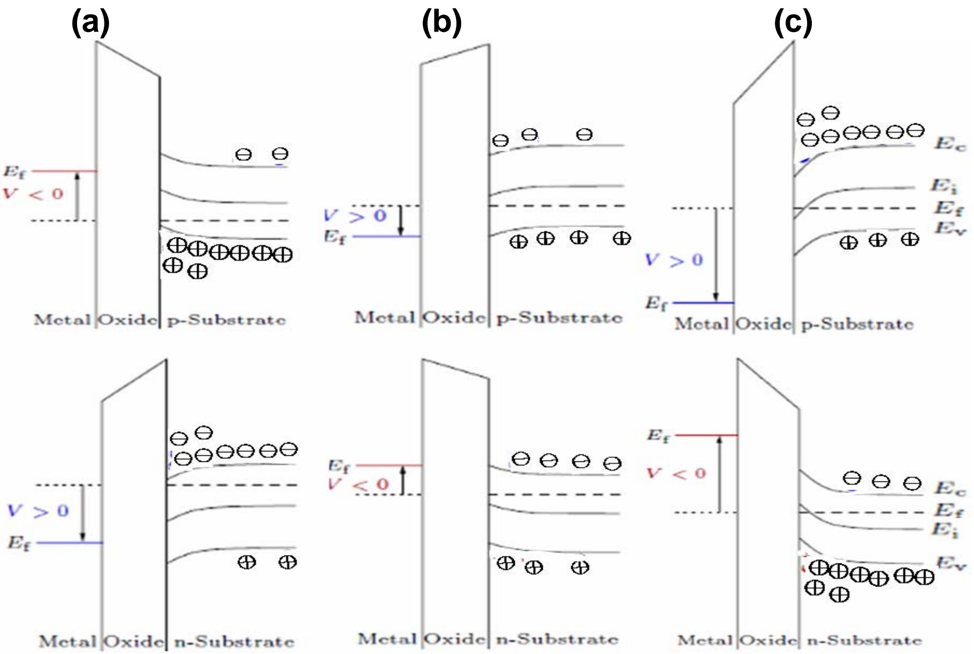


Figure I.3: Energy band diagram of ideal MOS capacitors under different bias. (a) accumulation, (b) depletion, and (c) inversion. Top and bottom figures are for p- and n-substrate capacitors, respectively **[63]**.

- The trapped charge (charge Q_{ot}, density N_{ot}): whose sign depends on the nature of the trapped carriers (mostly holes in the case of silicon dioxide and mostly electrons in the case of silicon nitride) distributed in the bulk of the insulator).
- The interface-trapped charge (charge Q_{jt}, density N_{it})., which is made up of carriers trapped on those interface defects which, depending on bias, can exchange carriers with the semiconductor. They can be negative or positive. Although usually positive, these polarities are determined by the structural and oxidation-induced defects. Also, interface charge is determined by defects caused over time such as radiation, hot electron injection, NBTI. The important issue here is that the interface trapped charge electrically communicates with the silicon substrate. These traps can be charged or discharged based on the surface potential.
- The fixed charge (charge Q_f, density N_f): which is the sum of all the other charges which do not changes in bias conditions. It is a positive charge that comes from structural defects in the dielectric. For SiO_2 films, these charges are located less than 2 nm from the SiO_2-Si interface. The amount of fixed charge found in films is due to the oxidation process. For instance, the process temperature, "oxidation" ambient, post–processing, and substrate orientation are oxidation process issues. Determining this particular type of charge is difficult to establish in the presence of moderate densities of interface trapped charge. The amount of oxide fixed charge is more readily distinguished after the interface trapped charge is removed with a low-temperature (~450 ºC) hydrogen or forming gas annealing **[66]**.

The impact of these charges is given by the equation for the flatband voltage (V_{fb}) **[66]**:

$$V_{fb} = \phi_{ms} - \frac{Q_f}{C_{OX}} - \frac{Q_m}{C_{OX}} - \frac{Q_{ot}}{C_{OX}} - \frac{Q_{it}(\phi_s)}{C_{OX}} \tag{I.3}$$

The flatband voltage is the amount of bias necessary to create a "flatband" condition (see **Fig. I.2**) in the gate, insulator, and silicon substrate. Both fixed charge and interface charge are assumed at the SiO_2-Si interface, while mobile and oxide trapped charge can be located into the insulator. The effect of these charges depends on their placement within the oxide. If these charges are located close to the SiO_2-S interface, the effect on the flatband is greatest due to the fact that the charge is "imaged" on the semiconductor. If the mobile and/or oxide trapped charge are located at the gate electrode/dielectric interface, the effect on the flatband voltage is negligible due to the "imaging" all the charge on the gate.

I.3- Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

I.3.1 Principles of operation

There are two types of MOS transistors: the n-channel MOSFET (n-MOSFET), in which current flow is due to electron transport and the p-channel MOSFET (p-MOSFET) in which holes are responsible for current flow. Today the most commonly used technology is CMOS (Complementary MOS) in which both n-MOSFET and p-MOSFET are fabricated. In this chapter, we will limit our analysis to n-MOSFET devices. The current-voltage expressions describing a p-channel device can readily be derived from the n-channel equations provided the appropriate changes of sign are made. The n-MOSFET is fabricated in a P-type semiconductor substrate, usually silicon. Two n-type

diffusions are made in the substrate and the current flow will take place between these two diffusions. The diffusion with the lowest applied potential is called the "source" and the diffusion with the highest applied potential is called the "drain". The MOSFET is a four terminal device, as shown in **Fig. I.4**. The gate and the substrate terminals define a capacitor where the gate is isolated from silicon by a dielectric, such as SiO_2. The region under the gate oxide and between source and drain is named the channel. Primary, it will be assumed that substrate, drain and source are at the same potential. Depending on whether V_{GS} (gate-substrate voltage), the voltage between gate and the other terminals, is equal to, less than, or greater than the flatband voltage V_{fb}, the channel can be in the flatband condition, in accumulation, in depletion or inversion, respectively. The flatband voltage is the external voltage used between the gate and the substrate terminals to keep the channel neutral by canceling the effects of the contact potentials and the charges that exists within the oxide as well as at the Si/SiO_2 interface.

In the case of NMOS device of **Fig. 1.4**, if a voltage, applied between gate and substrate, is less than the flatband voltage, a positive charge is induced at the Si/SiO_2 interface. As the substrate is p-type, accumulation of excess holes occurs at the interface. If V_{GS} increases above V_{fb} the positive charge on the gate will induce a negative charge in the channel. If V_{GS} is not much higher than V_{fb}, the positive potential at the surface with respect to the substrate will simply drive holes away from the surface, leaving it depleted from mobile carriers. This condition is called depletion. The charge in the channel consists of ionized acceptor atoms. If V_{GS} increases further, more acceptor atoms are uncovered and the potential in the channel becomes sufficiently positive to attract a significant number of free electrons to the surface. Eventually, with a sufficiently high V_{GS}, the density of electrons will exceed that of holes at the surface, creating the so called inversion layer.

The inversion layer is contacted electrically at the two ends by the source and the drain. By applying a voltage between these ends (V_{DS}), a current can flow in the layer. Since the number of carriers available for conduction depends on the gate voltage, the latter can be used to create or eliminate the inversion layer as well as to modulate its conduction. We summarize the transistor regimes as follows:

- $\psi_S < 0$: Accumulation regime [**Fig. I.3 (a)**].

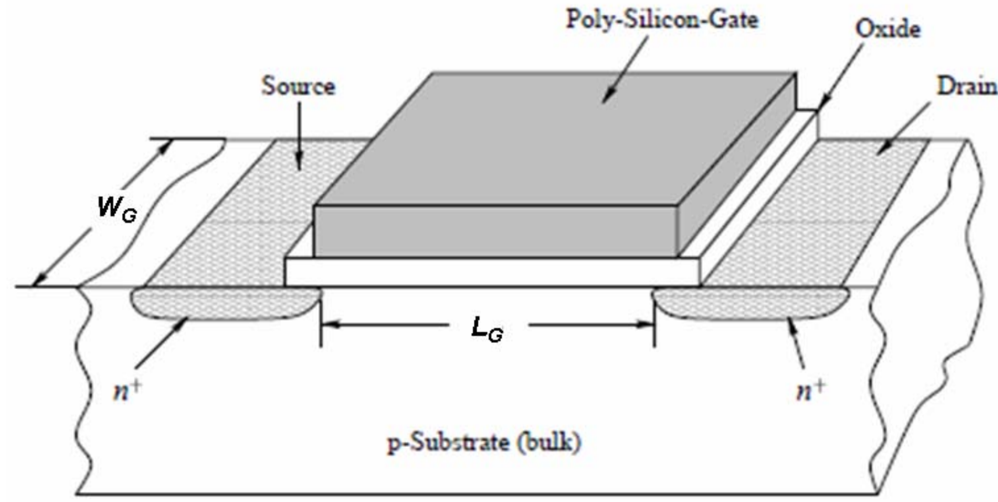


Figure I.4: Simplified structure of n-MOS transistors **[63]**.

- $0 < \psi_S < \phi_F$: Depletion regime [**Fig. I.3 (b)**].
- $\psi_S = \phi_F$: Flatband regime [**Fig. I.2 (b)**].
- $\phi_F < \psi_S < 2\phi_F$: Weak inversion regime [**Fig. I.3 (b)**].
- $\phi_S > 2\phi_F$: Strong inversion regime [**Fig. I.3 (c)**].

where ψ_S is the surface potential and ϕ_F is the Fermi potential with respect to the midgap in the bulk ($\phi_F = \psi_{BP}$)

I.3.2 Charge of the inversion layer

As the inversion layer plays an important role in the electric conduction of the transistor, it will be delaminated deeply. Q_{inv} is the charge of the inversion layer that participates in the conduction current is equal to the difference between the total charge in the silicon Q_{SC} and the maximum depleted charge caused by the depletion region:

$$Q_{inv} = Q_{SC} - Q_{Depm} \tag{I.4}$$

Q_{SC} is given by **[66]**:

$$Q_{SC} = -C_{OX}\left(V_{GS} - V_{fb} - 2\phi_F\right) \tag{I.5}$$

and Q_{Depm} writes as **[66]**:

$$Q_{Depm} = -\sqrt{2q\varepsilon_{si}N_A(2\phi_F)} \tag{I.6}$$

where N_A (cm^{-3}) is the substrate doping, ε_{si} is the dielectric constant of the silicon.

By substituting **Eqs. I.5** and **I.6** in **Eq. I.4,** Q_{inv} becomes:

$$Q_{inv} = -C_{OX}\left(V_{GS} - V_{fb} - 2\phi_F\right) + \sqrt{2q\varepsilon_{si}N_A(2\phi_F)} \tag{I.7}$$

I.3.3 Drain current

The potential at any point along the channel varies from V_S (x=0) to V_D (x=L). As a consequence, the energy band curvature, from the substrate to the surface near the source, is equal to $2q\phi_F + qV_S$. Similarly, the energy band curvature near the drain is equal to $2q\phi_F + qV_D$. Since the potential *V(x)* along the channel varies from V_S to V_D, the depth of the depletion layer also varies. Thus **Eq. 1.7** writes as:

$$Q_{inv} = -C_{OX}\left(V_{GS} - V_{fb} - 2\phi_F - V(x)\right) + \sqrt{2q\varepsilon_{si}N_A\left[2\phi_F + V(x)\right]} \tag{I.8}$$

The current in the channel is given by **[66]**:

$$I_{DS} = \frac{W_G}{L_G}\mu_{eff}\int_{V_S}^{V_D} Q_{inv}(x)dV(x) \tag{I.9}$$

solving **Eq. I.9** for V_S = 0 yields:

$$I_{DS} = \mu_{eff} C_{OX} \frac{W_G}{L_G} \left\{ \left(V_{GS} - V_{fb} - 2\phi_F - \frac{V_{DS}}{2} \right) V_{DS} - \frac{2}{3}\gamma \left[\left(2\phi_F + V_{DS}\right)^{3/2} - \left(2\phi_F\right)^{3/2} \right] \right\} \quad \text{(I.10)}$$

where V_D is changed to V_{DS} and γ is defined as: $\gamma = \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{OX}}$.

For very small V_{DS}, the level of inversion can be considered the same along the channel (the maximum depth of the depletion region is the same along the channel). The current I_{DS} in the linear region can be approximated by using power series around V_{DS} and taking the initial terms **[63]**, hence **Eq. I.10** reduces to:

$$\begin{aligned} I_{DS} &= \mu_{eff} C_{OX} \frac{W_G}{L_G} \left[\left(V_{GS} - V_{fb} - 2\phi_F - \frac{V_{DS}}{2} \right) V_{DS} - \frac{2}{3}\gamma \left(3\sqrt{\frac{\phi_F}{2}} V_{DS} \right) \right] \\ &= \mu_{eff} C_{OX} \frac{W_G}{L_G} \left(V_{GS} - V_{th} - \frac{V_{DS}}{2} \right) V_{DS} \end{aligned} \quad \text{(I.11)}$$

where V_{th} (V) is the threshold voltage and is given by:

$$V_{th} = V_{fb} + 2\phi_F + \frac{\sqrt{2q\varepsilon_{si}N_A(2\phi_F)}}{C_{OX}} = V_{fb} + 2\phi_F + \gamma\sqrt{2\phi_F} \quad \text{(I.12)}$$

For $V_{DS} < V_{GS}-V_{th}$, I_{DS} of **Eq. I.11** can be written as:

$$I_{DS} = \mu_{eff} C_{OX} \frac{W_G}{L_G} \left(V_{GS} - V_{th}\right) V_{DS} \quad \text{for linear region} \quad \text{(I.13)}$$

For $V_{DS} = V_{GS}-V_{th}$, I_{DS} of **Eq. I.11** can be written as:

$$I_{DS} = \mu_{eff} C_{OX} \frac{W_G}{2L_G} \left(V_{GS} - V_{th}\right)^2 \quad \text{for saturation region} \quad \text{(I.14)}$$

I.4- Microstructures of Defects in Si-SiO$_2$ System

The quality of the interface is essential to the success of the CMOS technology. The electrical characteristics of MOS devices are highly dependent on the properties of the thermally grown Si/SiO$_2$ interface. The oxide (SiO$_2$) is, due to its properties, the most predominant material in integrated circuit technology. It has been studied intensively over several years. Compared to other insulators, SiO$_2$, grown on a Si substrate with optimized fabrication processes for very low defect density, is of an excellent quality. The large barrier height (about 3.2 eV) of the Si/SiO$_2$ interface associated with the large bandgap (about 8.9 eV) leads to much reduced leakage current for sufficiently thick films and results in highly resistive insulators. Its melting temperature makes it very compatible with CMOS process steps performed after the formation of SiO$_2$-based gate dielectrics. However, when looking closer to the Si/SiO$_2$ interface, one finds that it is characterized by a disordered interfacial region (see **Fig. I.5**) **[67].** The latter is induced due to mismatch between atomic structures of crystalline Si and amorphous SiO$_2$. In fact, the atomic distance in the silicon crystalline is about 2.35 Å, while it stands at 3.05 Å in amorphous silicate. That means oxidation of one Si atom enhances the volume by a factor of

about 2.2. Therefore, the interfacial region presents more constrained and dangling bonds than the oxide bulk. This point will be presented in more details in section **§ I.4.4**.

According to the Deal nomenclature **[65]**, there are four general types of charges associated with the Si-SiO_2 system, as illustrated in **Fig. I.6 (a) [68]**. The fixed charge density (Q_f), due to structural defects in the oxide. The oxide-trapped charge density (Q_{ot}); due to holes and electrons trapped in the bulk of the oxide. The mobile oxide charge density (Q_m); primarily caused by ionic impurities. The interface-trapped charge density (Q_{it}); located at the Si/SiO_2 interface. Unlike fixed oxide charge, oxide trapped charge, and mobile oxide charge, interface trapped charge communicates electrically with the underlying silicon. In 1992, Fleetwood **[69]** completed this picture of charges by introducing a new charge type termed border charge (Q_{bt}). As illustrated in **Fig. I.6 (b)**, the border-trap is an oxide-trap located near the Si/SiO_2 interface and communicates with the underlying silicon via the interface-trap.

I.4.1- Defects at the Si/SiO_2 interface

Silicon in its crystalline state is tetrahedrally bonded with each Si atom bonded to four Si atoms in the wafer bulk. When oxidation occurs, the bonding configuration at the surface is as shown in **Fig. I.7**

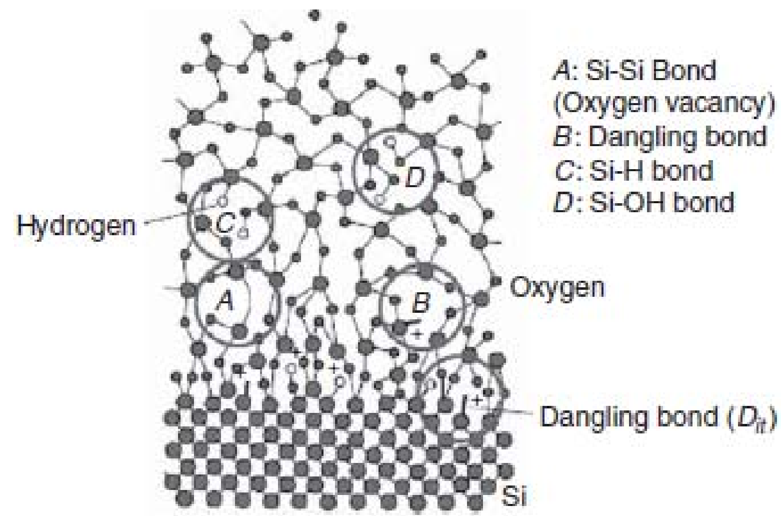


Figure I.5: Schematic presentation of types of bonds created at the Si/SiO_2 interface **[67].**

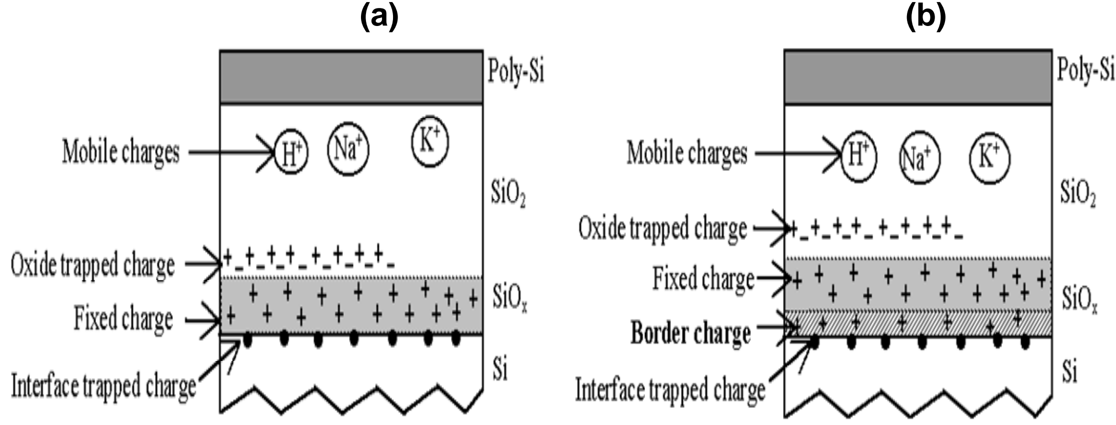


Figure I. 6: Schematic illustration of different charges in MOS devices **[68]**. **(a)** Different charges in Si-SiO_2 system according to Deal **[65]**. **(b)** Different charges in Si-SiO_2 system according to Fleetwood **[69]**.

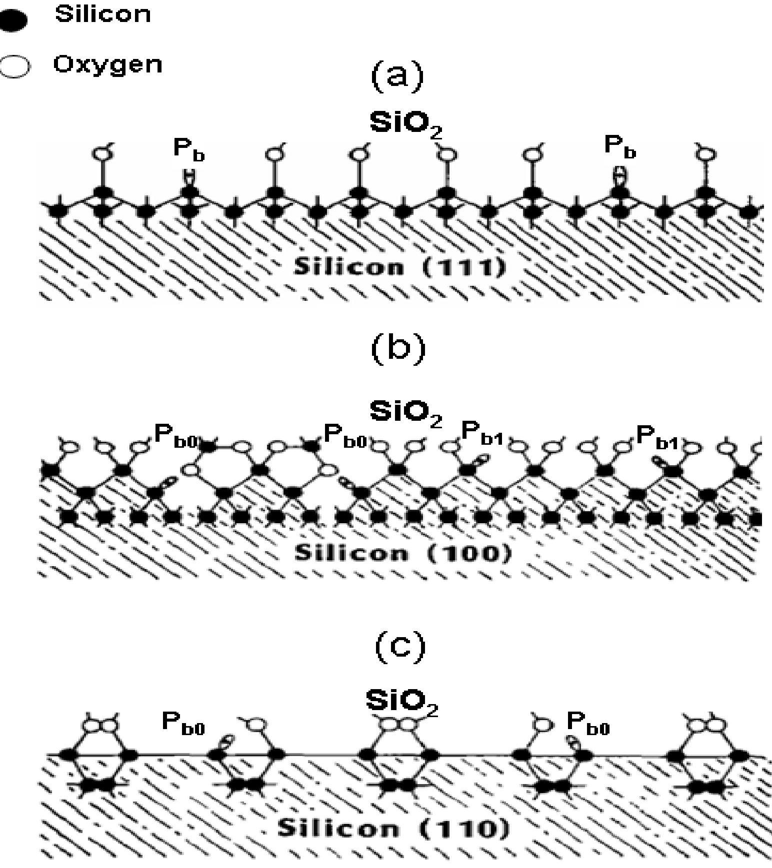


Figure I.7: Structural model of P_b, P_{b0}, and P_{b1} interface defects on oxidized (111), (100), and (110) silicon wafers **[70]**.

(a), (b), and (c) with most Si atoms bonded to oxygen **[70]**. Some Si atom bonds remain free. These dangling bonds are called interface traps, fast surface states, interface-trapped charges, and interface states. Their physical structures were intensively studied using electron spin resonance (ESR) technique, **[70-72]**. **Figure I.7 (b)** illustrates two defects along Si (100) orientation, named P_{b0} and P_{b1} **[67,70]**. They have been shown related to strain relaxation at the Si/SiO_2 interface and have different dangling bond axis of symmetry and their electronic density of states are different, while they are chemically identical. The orientation (111), illustrated in **Fig. I.7 (a)**, is characterized by dangling bond P_b. The defect is formed by an unpaired valence electron of a silicon atom back-bonded to three other silicon atoms $(Si_3 \equiv Si^{\bullet})$. P_b and P_{b0} centers also show similar magnetic resonance properties. Thus, P_b and P_{b0} centers are (electrically) equivalent dangling bonds **[70]**. In addition, The P_{b0} (110) center is nearly the same as P_b (111) and P_{b0} (100), thus, assigned to $(Si_3 \equiv Si^{\bullet})$ centers, while P_{b1} is identified as two silicon atoms and an oxygen atom $(Si_2O \equiv Si^{\bullet})$ **[70]**. It was also shown that P_{b0} defects found at interfaces of (100) wafer orientation are very similar to the P_b centers found at (111) interfaces **[45,73-75]**. Reversely, P_{b1} centers are found to comprise of completely different levels in energy. Lenahan et *al.* **[73]** gives an estimation of the energy distribution of P_{b0} and P_{b1} centers, as shown in **Fig. I.8**. The number of P_{b1} centers is assumed to be lower than that of P_{b0} centers. Still, around the peak levels of the P_{b1} centers, a small change in the Fermi-level can have a significant impact on the charge state because of these P_{b1} centers and their narrow distribution. All three types

of silicon dangling bonds investigated up to now (P_b, P_{b0}, *and* P_{b1}) are reported to be of amphoteric nature. Their energy distribution comprises two distinct peaks in the silicon bandgap, (see **Fig. I.8)**. The two peaks have different properties regarding their possible charge states and their energetic positions depend on the type of the trap center.

More importantly, the P_{b0} and P_{b1} play a key role in interface traps creation during NBTI degradation. Indeed, an experimental evidence showing interface trap generation as a part of the NBTI damage was given by spin-dependent recombination (SDR) spectra **[45,75]**. **Figure I.9** illustrates the corresponding pre- and post-NBTI SDR traces, obtained after a uniform NBTI stress (140 °C, V_G = - 5.7 V), with the magnetic field vector perpendicular to the (100) surface. The interface defect density in the unstressed device is below the used SDR detection limit. After NBTI, Campbell et *al*. **[74]** have observed two strong signals at g = 2.0057 ± 0.0003 and at g = 2.0031 ± 0.0003 (**Fig. I.9**). They have attributed the g = 2.0057 signal to P_{b0} centers and the g = 2.0031 signal to P_{b1} centers.

I.4.2- Amphoteric nature of interface traps

The interface traps have an amphoteric nature, thus behaving like acceptors, donors or neutrals, depending on their position in the Si energy bandgap. They are respectively located in the upper, lower, and middle of the energy bandgap. That means, the interface trap can, depending on the position of the Fermi level at the Si/SiO_2 interface, be positively charged, negatively charged, and neutral in the lower part, upper part, and in the midgap, respectively **[26,63,76]**. **Figure I.10** illustrates

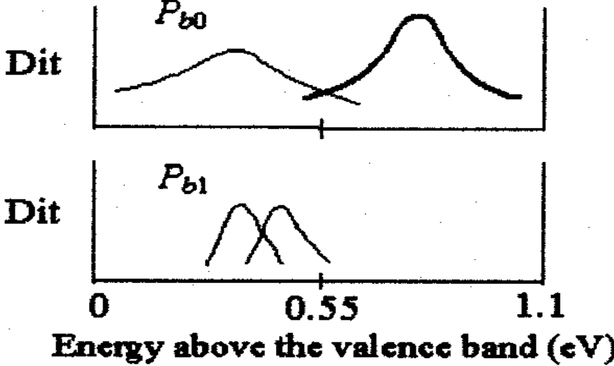


Figure I.8: An illustration of the P_{b0} and P_{b1} densities of states. The important points to note in this illustration are that the P_{b1} density of states distribution is significantly narrower than that of the P_{b0} density of states and that this distribution is almost certainly skewed toward the lower part of the Si bandgap **[73]**.

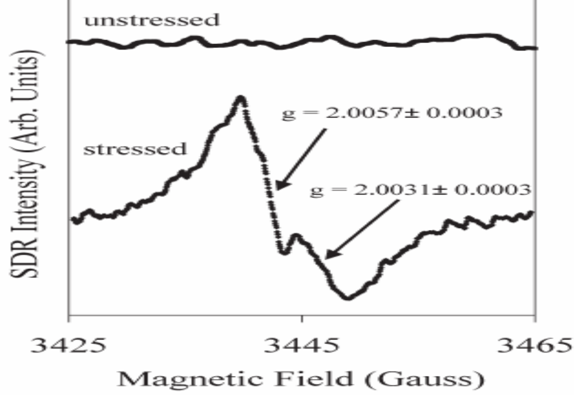


Figure I.9: SDR traces of p-MOSFET with the magnetic field vector perpendicular to the (100) surface both before and after the application of NBTI (140 °C for 250000 sec with V_G = - 5.7 V on the gate contact) **[75]**.

the energy band diagram of p-MOSFET [**Fig. I.10 (a)**] and n-MOSFET [**Fig. I.10 (b)**]. The Fermi-level at the interface of a p-MOSFET, biased into inversion ($2\phi_f$), is below the midgap energy (E_i). As **Fig. I.10 (a)** shows, in this regime the acceptor like trap levels are empty, and the donor like trap levels are partially filled, assuming the trap energy levels to be symmetrically aligned around midgap. The net interface trap charge resulting from this configuration is positive. At flatband, p-MOSFET has negative interface trap charge. For the n-MOSFET the situation is completely different, see **Fig. I.10 (b)**. Here, the Fermi-level at the interface is located above the midgap energy. The donor like trap levels in the lower half of the bandgap are therefore completely filled and the acceptor like trap levels are partially filled. The result is a negative interface trap charge, while at flatband, n-MOSFET has positive interface trap charge.

I.4.3- Defects in SiO_2 oxide

Several microscopic point defects have been identified in thermally grown oxide and summarized in **[77]**. The most important point defects are *E'* center defects. The crystallographic structural information on *E'* center defect can be obtained using a powerful measurement technique, namely electron paramagnetic resonance (EPR) or ESR **[78].** The *E'* centers are identified most likely at the origin of oxide hole trapping center **[71, 79-82]**, which are characterized by an unpaired electron highly localized on a silicon atom bonded to three oxygen atoms. The chemical notation for the *E'* center is given by $(O_3 \equiv Si^{\bullet})$ **[83]**. **Figure I.11 (a)** shows a single dangling bond of neutral *E'* center. One of the more common types of *E'* centers identified in thermally grown oxides are the E'_γ center, which is often the paramagnetic silicon site, coupled to a positively charged diamagnetic silicon, as shown in **Fig. I.11 (b).** As for P_{b0} and P_{b1}, Ryan et *al*. **[84]** have demonstrated that *E'* centers (positively charged vacancy sites) are present during NBTI. **Figure I.12** illustrates an ESR trace of *E'*, taken on sample

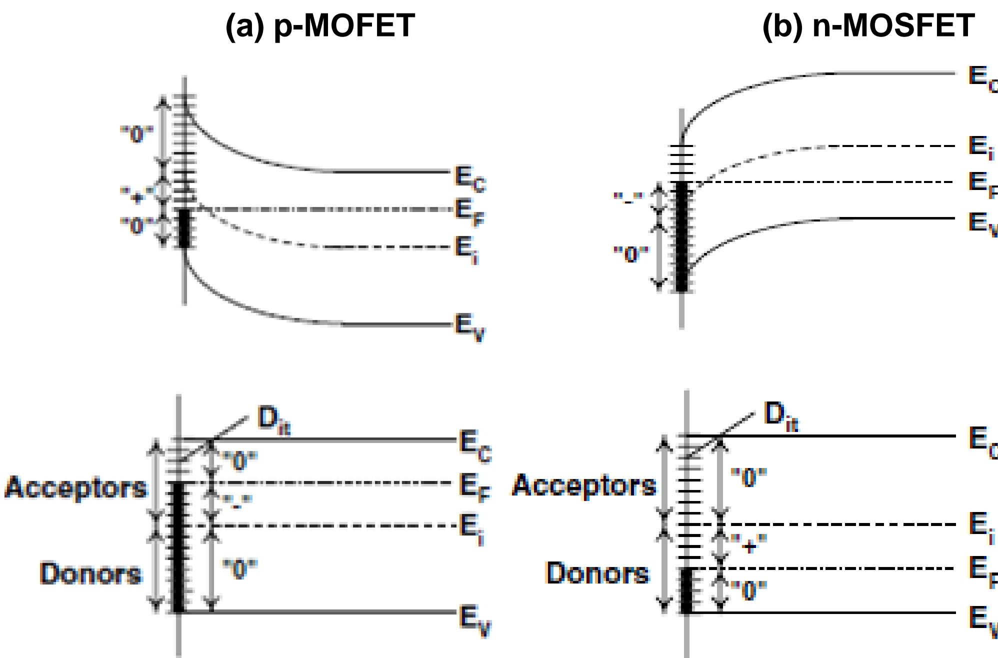


Figure I.10: Energy band diagrams of a p-channel MOSFET (a) and an n-channel MOSFET (b) at the Si/SiO_2 interface showing the occupancy of interface traps. At inversion, n-channel has negative interface trap charge and p-channel positive interface trap charge. At flatband, the situation is completely opposite.

during NBTI stress, and showing double humped structure at $g_{//}$ = 2.0016 and $g_{\perp}$ =2.0006 **[84]**. They have found a close match between the *E'* ESR signals during stress and the commercially available *E'* standard signals (bottom curve in **Fig. I.12**)

I.4.4- Interfacial sub-oxide region

For thermal oxides, the defect precursors exist prior to stress. It occurs naturally in large density close to the Si/SiO_2 interface due to the lattice mismatch between the crystalline silicon substrate and the amorphous oxide (which may indicate an incomplete oxidation process). This region is called the interfacial region and is characterized by a sub-oxide transition phase SiO_X. Much effort has been made to understand SiO_x sub-oxide detects at Si/SiO_2 interface since it has a significant effect on MOS device characteristics and reliability **[85-87]**. The shift in chemical transition from Si to SiO_2 was investigated in details in thick oxides through photoelectron spectroscopy studies by Grunthaner et *al.* **[86]**. They showed that there are five possible formal oxidation states for silicon as illustrated in **Fig. I.13**. Si and SiO_2 are denoted as Si^{+1} and Si^{+4}, respectively. This notation emanates from the chemical picture in which the silicon atom loses one electron to oxygen for each formed bridging bond. No charge transfer occurs in the formation of the Si-Si bond. However, the non stoichiometric interfacial region contains intermediate oxidation state Si^{+1}, Si^{+2}, and Si^{+3} lying over several nm near Si/SiO_2

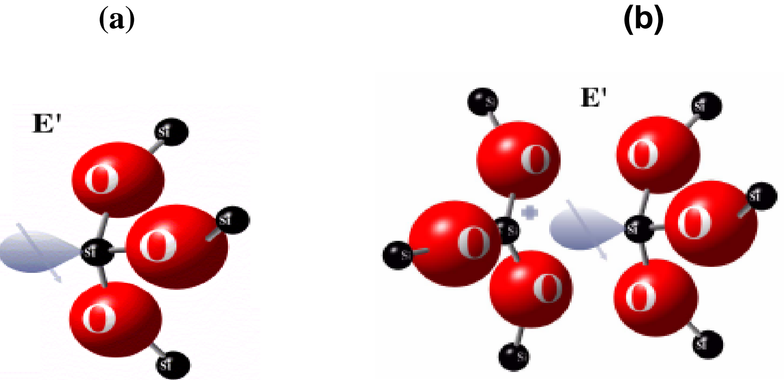


Figure I.11: Schematic illustration of two *E'* centers commonly found in pure SiO_2. (a) A neutral oxygen vacancy. (b) A positive charged oxygen vacancy **[84]**.

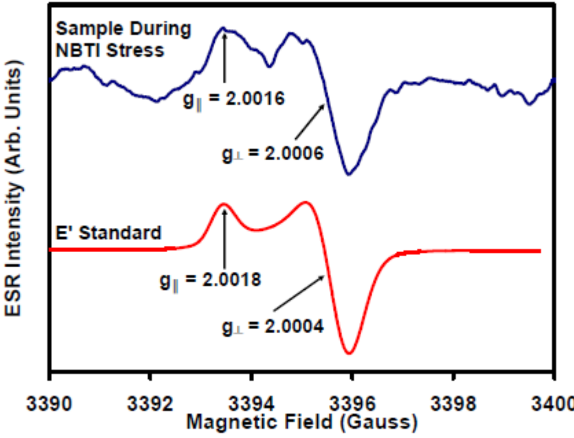


Figure I.12: Electron spin resonance (ESR) spectrum of *E'* centre during NBTI stress (top trace). Note a clear generation of *E'* during NBTI stress. A good correlation was found between top trace and a commercially *E'* standard (bottom trace) **[84]**.

interface Si^{+1}, Si^{+2} are within 5 to 10 Å, while Si^{+3} extends over 30 Å into the oxide. Later, high-resolution X-ray photoelectron spectroscopy (XPS) has showed evidence that the sub-oxide layer lyes within 6 Å from interface, giving further understanding of the oxidation state observed with depth along the interfacial transition region in thin oxides **[88,89]**. Based on the above experiments and observations, it is clear that the transition between Si and SiO_2 is not abrupt due to the presence of transition region whose composition and properties differ from those of the SiO_2 bulk. **Figure I.14** summarizes different regions of the local atomic view of the interfacial region. The strained region of about 1.5-3 nm in which the Si-Si distance is 30% smaller than that in the bulk SiO_2. In addition, there is a transition region, SiO_x of approximately 0.5 nm and containing ~75% of oxidized silicon monolayer. The interface roughness is determined by the net stress of the oxide across the interface boundary.

I.4.5- Border traps

Border traps, originally proposed in 1992 **[69]**, are suggested to describe traps located in the oxide close to the interface that communicate with the Si interface through capture and emission of electrons and/or holes on the measurement timescale. Their switching nature makes them look electrically like interface traps, but their location is in the oxide instead of the interface. Besides the location, border traps mainly communicate with Si substrate via tunneling mechanism, while for interface trap the

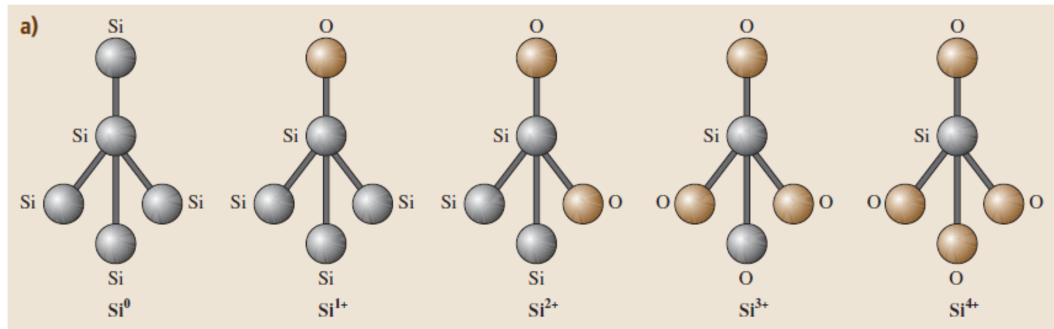


Figure I.13: Oxidation states and local chemical bonding variations associated with the Si/SiO_2 interface **[89]**.

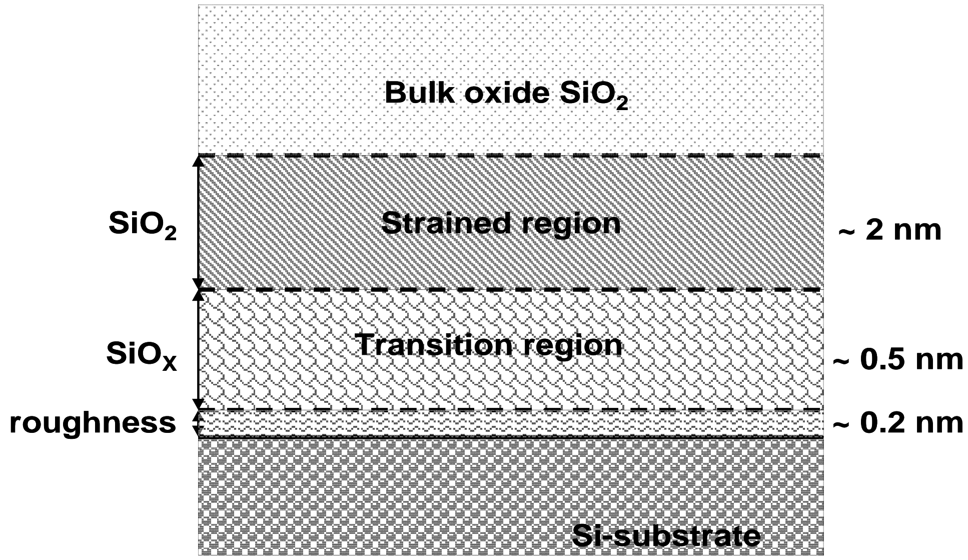


Figure I.14: Schematic view of simplified interfacial region of Si/SiO_2 structure.

communication is predominantly by capture/emission process. Unlike the interface traps, which are only distributed in energy, the border traps are distributed in space and energy **[90]**. According to Fleetwood et *al.* **[69, 90]**, all near interfacial traps, located at 3 nm from Si/SiO_2 interface in the oxide, are more likely border traps, while traps located more than 3 nm are oxide traps. However, the exact limit line between oxide and border traps will depend on process and measurement conditions.

Moreover, border traps have typically different microstructures than interface traps. Based on electrical, EPR, and SDR data, Fleetwood et *al*. **[91]** have proposed a structural picture for interface and border traps (see **Fig. I.15)**. The interface trap, represented by site (1) in **Fig. I.15**, is the well known P_b centre discussed above in section **§ I.4.1**. However, the border traps are divided into two groups; one group named slow border traps and the other fast border traps. The slow border trap illustrated in **Fig. I.15** is $E_{\gamma}^{'}$ defect and is consistent with the theoretical calculation model **[92]**. The fast border trap candidate is $(O_{3-X}Si_X Si^{\bullet})$ defect family **[91]**. For x = 0, the Si atom is surrounded by three O atoms ($E_S^{'}$, which is mainly one half of the $E_{\gamma}^{'}$ center). For *x* = 3, the Si atom above site (2) is surrounded by three Si atoms, which is a Si cluster in the oxide that looks very much like a P_b. Therefore, it is not surprising that such a defect might act like an interface trap, it only switches more slowly since it is in the near-interfacial oxide and not at the interface. Cases for *x* = 1 and x = 2 are similar to structures invoked by Poindexter et *al.* **[70]** to describe the P_{b1} center at the (100) Si/SiO_2 interface.

I.4.6- Hydrogen-related defect

Hydrogen is a very common impurity in oxide. It can be deliberately or unintentionally incorporated into the oxide. The latter is due to technological process steps, such as chemical etching, polishing,

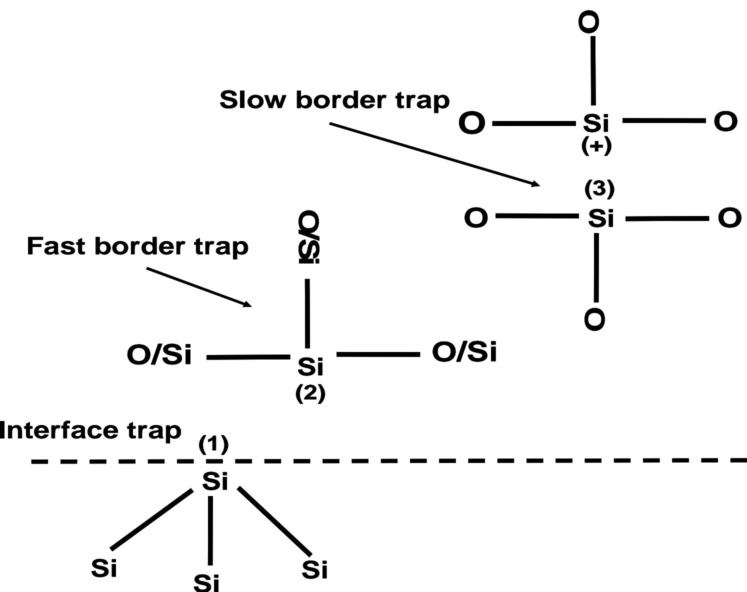


Figure I.15: Schematic of interface traps (P_b defects), and possible fast $(O_{3-X}Si_X Si^{\bullet})$ and slow ($E_{\gamma}^{'}$) border traps in SiO_2. The $E_{\gamma}^{'}$ without site (3) is a bulk oxide trap. Sites (1) and (2) are amphoteric, and are charged positively at large negative bias and negatively at large positive bias. Site (3) is neutral at large negative bias and negative at large positive bias **[91]**.

and plasma processing, which release considerable quantities of hydrogenated species. However, the former is used to passivate the interface traps by heating devices in forming gas (H_2/N_2) at about 450°C **[74]**. In fact, during process several hydrogen species such as H, H^+, H_2, OH, etc. can be released and diffuse in the oxide. The presence of hydrogen related species in SiO_2 can create new defects by distorting bonds or modifying the existing ones.

In general, the traps do not usually exist as such, but are generated by the reaction of a "precursor" with an outside element like hole, photon, electron, or hydrogen atom. The precursor can be an oxygen vacancy, a strained Si-O-Si bond, or a hydroxyl group. It has been reported that *E'* center could be transformed from a neutral (diamagnetic) oxygen vacancy to paramagnetic (but stray neutral) defect under the action of hydrogen **[80,83]**. The reaction reads as follows:

$$O_3 \equiv Si - Si \equiv O_3 + H \rightarrow O_3 \equiv Si^{\bullet} + H - Si \equiv O_3 \tag{I.15}$$

Two other paramagnetic defects associated with the presence of hydrogen complex *E'* have been identified and called the 74 G doublet and the 10.4 G doublet according to their EPR traces **[80,83]**. They result from the interaction of *E'* center with hydrogen molecule. The first defect (10.4 G doublet) most likely involves an unpaired electron on silicon back bonded to three oxygen atoms with one of the oxygen atoms bonded to hydrogen. Its microscopic structure is symbolized by **[80,83]**:

$$O_2 = Si^{\bullet} - O - H \tag{I.16}$$

The second defect (74 G doublet) involves a paired electron on silicon back bonded to two oxygen and one hydrogen. After hole trapping, the paramagnetic structure of this defect can be written as follows:

$$O_2 = \overset{\overset{\displaystyle H}{|}}{Si} - Si \equiv O_3 + h^+ \rightarrow O_2 = \overset{\overset{\displaystyle H}{|}}{Si^{\bullet}} + {}^{+}Si \equiv O_3 \tag{I.17}$$

Conley and Lenahan **[80,94]** showed that exposing an oxide, previously flooded with holes (to generate *E'* centers), to an H_2/N_2 mixture leads to a conversion of conventional *E'* centers to 74 G doublet centers and other hydrogen complexed *E'* centers and might generate interface traps. They found that the number of *E'* centers converted to hydrogen complex centers is approximately equal to the number of generated interface traps, with the time period involved in interface trap formation approximately equal to the time required to saturate the *E'*/hydrogen via a complex process.

Combining *E'* center and hydrogen, Grasser et *al*. **[29]** have been able to propose the two-stage model for NBTI degradation. Another source of atomic hydrogen is represented by saturated dangling bonds. As we have shown before, hydrogen can passivate the dangling Si bonds during process **[93]**. These passivated dangling bonds (Si-H) became a source of device instability under NBTI. The dangling Si bonds reappear as interface traps and generate hydrogenated species that move away from the interface and diffuse in the oxide. Once diffused in the oxide, the hydrogen species interact with oxide defects to product positively charged defects. Based on first-principal calculation, Tsetseris et *al.* **[25]** have proposed passivated dopant in silicon substrate such as phosphorous-hydrogen (P-H) and boron-hydrogen bonds (B-H) complexes. The P–H bonds dissociate and the hydrogen becomes positively charged (H^+) by capturing holes present in the inverted p-MOS substrate, then reacts with the *H* from the Si-H bond to form H_2 leaving behind a positively charged Si dangling bond. However, it

is more difficult for B-H to be broken in p-substrate, which can explain the reduction of NBTI effect in n-MOSFET.

The interaction of hydrogen with the defect precursor, under some given conditions of stress such as radiation, electric field, and temperature, modifies the transistor characteristics. Consequently, hydrogenated species and *O* vacancy-related defects play an important role in device reliability.

I.5- NBTI Reaction-Diffusion (R-D) Model

The reaction-Diffusion (R-D) model is largely accepted to describe the interface trap generation during NBTI degradation. The first R-D model was suggested by Jeppson *et al.* **[12]**. In this model, see **Fig. I.16**, interface trap creation is ascribed to the Si-H bond dissociation under gate field influence, which initiates a field-dependent electrochemical reaction at the Si/SiO_2 interface. Then, an electrically active interface trap, N_{it} and mobile hydrogen related species are formed. Although Jeppson *et al.* **[12]** proposed the first version of R-D model, they did not clarify the dissociation mechanism of Si-H bonds. Later Alam and Mahapatra **[34]** have improved the R-D model. This version of R-D model considers direct dissociation of Si-H bond due to the existence of high negative electric field at the interface **[14,16,34,95]**. Since the inversion layer holes, h^+ (during p-MOSFET inversion or n-MOSFET accumulation) enhances the bond dissociation, the reaction that weakens the Si-H bonds at the interface can be written as follows:

$$Si_3 \equiv Si - H + h^+ \underset{k_r}{\overset{k_f}{\rightleftarrows}} Si_3 \equiv Si^+ + H \tag{I.18}$$

Under NBTI conditions, the passivated interface dangling bonds are activated basically by electrochemical reaction. At first glance, the neutral atomic hydrogen is detached and interface trap increase is governed by the following differential equation:

$$\frac{dN_{it}}{dt} = k_f\left(N_0 - N_{it}\right) - k_r N_{it} N_H^{(0)} \tag{I.19}$$

where N_0 (cm^{-2}) is the initial saturated Si-H bonds, k_f (s^{-1}) is the bond dissociation rate factor, k_r (cm^3/s) is the bond annealing rate factor, $N_H^{(0)}$ (cm^{-3}) is the hydrogen density at the interface, and N_{it}

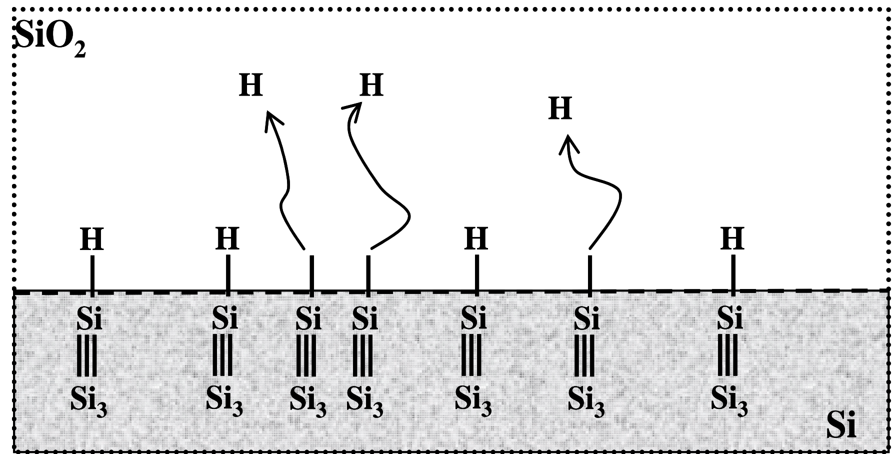


Figure I.16: Schematic illustration of the reaction-diffusion (R-D) model. The Si-H bonds at Si/SiO_2 interface are broken and the hydrogen diffuses into the SiO_2 leaving behind an electrically active interface trap.

(cm^{-2}) is the interface trap density.

The hydrogen diffuses away from the Si/SiO_2 interface obeying the diffusion equation:

$$\frac{dN_H}{dt} = D_H \frac{d^2 N_H}{dx^2} \quad \text{(I.20)}$$

where D_H (cm^2/s) is the diffusion coefficient of the neutral *H, and* N_H (cm^{-3}) is the density of diffusing hydrogen in the oxide bulk. From **Eqs (I.19) and (I.20)**, it is clear that the temperature and electric field dependence of NBTI is not explicit in the R-D model. As will be illustrated later, the temperature dependence is accounted through the activation energies of k_f and k_r, while the electric field is included in k_f term.

To satisfy the boundary condition near the interface between reaction and diffusion fluxes, the following equation is set:

$$\frac{dN_{it}}{dt} = \frac{\delta}{2}\frac{dN_H^{(0)}}{dt} - D_H \frac{dN_H^{(0)}}{dx} \quad \text{(I.21)}$$

where δ is considered as the interface thickness, which can be approximated to one or two length of Si-H bond (2 to 3 Å) **[31]**. The microscopic details of the trap generation and trap annealing processes that occurs within few angstroms of the Si/SiO_2 interface (i.e., δ) are assumed included in the constants k_f and k_r **[34]**. These parameters are measured and parameterized in terms of device variables like stress bias and stress temperature.

The general solution of R-D model in stress phase can be divided into four stages **[34,61]** (summarized by **Fig. I.17**).

I.5.1- Stage 1

At the beginning, the densities of both N_{it} and N_H are small (N_0>>N_{it}), and so the reaction is exclusively limited by dissociation of Si-H. Therefore, the increase in N_{it} is given, from **Eq. (I.19)**, as:

$$N_{it} = k_f N_0 \, t \quad \text{(I.22)}$$

I.5.2- Stage 2

During this stage, sufficient hydrogen builds up very near to the interface allowing equilibrium between forward and reverse hydrogen fluxes. This means that the generation rate of interface traps $\left(dN_{it}/dt\right)$ in **Eq. (I.19)** is equal 0. In addition, all free hydrogen remains at the interface (N_H = N_{it}), so:

$$N_{it} \approx \left(k_f N_0 / k_r\right)^{0.5} t^0 \quad \text{(I.23)}$$

I.5.3- Stage 3

When t>>0, the hydrogen diffuses away from the interface, thus the generation rate of interface traps becomes limited by hydrogen diffusion, which is controlled by **Eq. (I.20)**. The solution is approximated by a triangular profile **[14,34]** and expressed as:

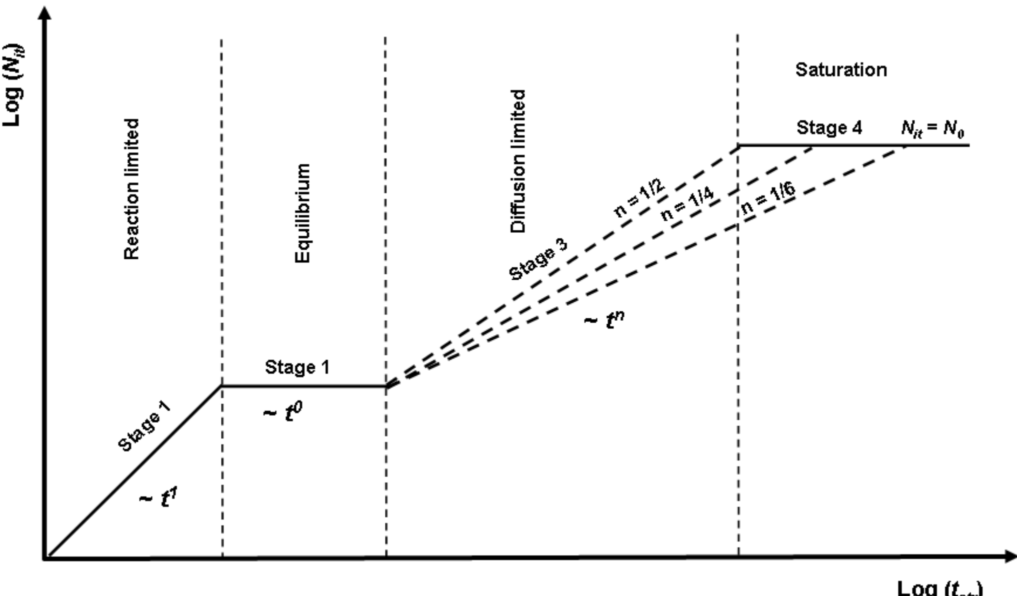


Figure I.17: The schematic time evolution of standard R-D model. Stage 1 reaction limited regime, stage 2 equilibrium regime, stage 3 diffusion limited regime, and stage 4 saturation regime. Stage 3 gives the poser law behavior for NBTI. The time exponent n = 1/6, 1/4, and 1/2 are observed for the three species H^0, H^+, H_2 in the diffusion regime. The degradation in the first two stages is very fast and not observable in experimental measurements.

$$N_{it} = \int_{x=0}^{x=f(D_H,t)} N_H(x,t)dx \approx \frac{1}{2} N_H \left(D_H t\right)^{0.5} \tag{I.24}$$

where x varies from 0 to $f(D_H, t) = \left(D_H t\right)^{0.5}$.

During the diffusion-dominated regime, $\left(dN_{it}/dt\right)$ term is negligible compared to the dissociation and annealing terms in **Eq. (I.19)**, thus:

$$k_f N_0 \approx k_r N_H N_{it} \tag{I.25}$$

Combining **Eqs. (I.24)** and **(I.25)**, we find:

$$N_{it} \approx \left(\frac{k_f N_0}{2k_r}\right)^{0.5} \left(D_H t\right)^{0.25} \tag{I.26}$$

Finally the last stage is reached when all Si-H bonds are broken$\left(N_{it} \sim N_0\right)$, then the interface trap generation slows down and tends to saturation.

All these NBTI degradation phases are described by the asymptotically analytic solutions of the coupled **Eqs. (I.19), (I.20), and (I.21)**. It is worth to note that the third phase is usually observed in experiments since it falls into the measurement time scope. These analytical approaches are helpful to understand the basic kinetics of reaction-diffusion at the interface and near the interfacial oxide. However, the above analysis is only given for the neutral hydrogen, such as H or H_2, which is one of the most commonly reported hydrogenate species at the Si/SiO_2 interface and SiO_2 oxide.

I.5.4- Case of H^+ diffusion

The passivated Si-H dangling bond may dissociate and result in a positively charged atomic hydrogen or proton (H^+), which is known to be more stable from atomic hydrogen **[96,97]** using first-principal calculation. The reaction giving H^+ has the following form:

$$Si_3 \equiv Si - H + h^+ \Leftrightarrow Si_3 \equiv Si^+ + H + h^+ \rightarrow H^+ \quad \text{(I.27}$$

As hydrogen is charged, we have to account for drift due to electric oxide field E_{ox}. Therefore, **Eqs. (I.20) and (I.21)** read as:

$$\frac{dN_{H^+}}{dt} = D_{H^+}\frac{d^2N_{H^+}}{dx^2} - E_{OX}\mu_{H^+}\frac{dN_{H^+}}{dx} \quad \text{(I.28)}$$

$$\frac{dN_{it}}{dt} = -D_{H^+}\frac{dN_{H^+}}{dx} + E_{OX}\mu_{H^+}N_{H^+} + \frac{\delta}{2}\frac{dN_{H^+}}{dt} \quad \text{(I.29)}$$

Practically, drift process of H^+ through the oxide dominates the H^+ diffusion. Assuming drift front as rectangle **[14]**, similarly to triangular approximation of diffusion, we rewrite **Eq. (I.24)**:

$$N_{it} = \int_{x=0}^{x=f(\mu_{H^+},t)} N_H(x,t)dx \approx N_{H^+}\mu_{H^+}E_{OX}t \quad \text{(I.30)}$$

where $f(\mu_{H^+},t) = \mu_{H^+}E_{OX}t$, $\mu_{H^+}E_{OX}$ is the drift velocity, and μ_{H^+} is the H^+ mobility. Using **Eqs. (I.25) and (I.30)**, we find:

$$N_{it} \approx \left(\frac{k_f N_0 \mu_{H^+} E_{OX}}{k_r}\right)^{0.5} (t)^{0.5} \quad \text{(I.30)}$$

I.5.5- Case of H_2 diffusion

Direct Si-H bond dissociation creates atomic hydrogen species *H*, which can also react again with another Si-H bond to generate molecular hydrogen H_2:

$$\begin{aligned} &Si_3 \equiv Si - H + h^+ \Leftrightarrow Si_3 \equiv Si^+ + H \\ &Si_3 \equiv Si - H + h^+ + H \Leftrightarrow Si_3 \equiv Si^+ + H_2 \end{aligned} \quad \text{(I.32)}$$

The conversion between *H* and H_2 is given by the mass action law:

$$[N_H][N_H] = [N_{H_2}] \quad \text{(I.33)}$$

Hence, $N_H = \sqrt{N_{H_2}}$. Together with **Eqs. (I.24)** and **(I.25)** (where **Eq. (I.24)** have to be rewritten for H_2 diffusion), we obtain N_{it} as:

$$N_{it} \approx \left(\frac{k_f N_0}{k_r}\right)^{2/3} \left(D_{H_2} t\right)^{1/6} \quad \text{(I.34)}$$

R-D model with H_2 diffusion predicts a power-law time exponent, n ~ 1/6, which is more consistent with recent measurements **[17,48]**. Therefore, we will use H_2 diffusion to discuss k_f, k_r, and D_{H2} parameters.

I.5.6- R-D model for NBTI relaxation phase

R-D model is also used to explain the relaxation phase through the annealing of the interface defects by the near interfacial hydrogen species generated during the stress phase. They are based

on hydrogen back diffusion to Si/SiO_2 interface with no generation **[13]**. According to the latter, when the transistor is off, the forward dissociation factor, k_f in **Eq. (I.19)** is equal to zero and the reverse process characterized by k_r allows annealing of existing traps. This phase is expressed assuming symmetric dynamic of stress and relaxation phases. At the end of the first phase (at time t_s), the number of generated traps, N_{it}^{s} and the density of hydrogen at the interface N_{H}^{s} are the same. During the relaxation phase, a fraction (N_{it}^{r}) of N_{it}^{s} is annealed at time $t+t_s$, while hydrogen density N_{H}^{s} decreases with the same amount. As $k_f = 0$, N_{it}^{s} can be written using **Eq. I.24**:

$$N_{it}^{s}\left(t_s\right) = \frac{1}{2} N_{H}^{s} \sqrt{D_H t_s} \tag{I.35}$$

The amount of annealed traps can be expressed as:

$$N_{it}^{r}\left(t + t_s\right) = \frac{1}{2} N_{H}^{r} \sqrt{\eta D_H t} \tag{I.36}$$

where η represents the diffusion dimension. For double-side diffusion $\eta = 0.5$. In the assumption of symmetric diffusion of hydrogen during relaxation phase, the evolution of N_{it} can be approximated as:

$$N_{it}\left(t + t_s\right) = \frac{1}{2} N_{H}^{r} \sqrt{D_H \left(t + t_s\right)} \tag{I.37}$$

As the initial hydrogen amount N_{H}^{s} is equal to the sum of the recombined hydrogen at the interface and the hydrogen in the bulk oxide, $N_{it}^{s}\left(t_s\right)$ reads:

$$N_{it}^{s}\left(t_s\right) = N_{it}\left(t_s + t\right) + N_{it}^{r}\left(t_s + t\right) \tag{I.38}$$

From **Eqs. (I.36) and (I.37)**, we obtain:

$$\frac{N_{it}^{r}\left(t_s + t\right)}{N_{it}\left(t_s + t\right)} = \sqrt{\frac{\eta t}{t + t_s}} \tag{I.39}$$

Substituting **Eq. (I.39)** in **Eq. (I.38)** yields:

$$N_{it}\left(t_s + t\right) = N_{it}^{s}\left(t_s\right)\left(1 + \sqrt{\eta \frac{t/t_s}{t/t_s + 1}}\right)^{-1} \tag{I.40}$$

I.5.7- Generalized R-D model

In the classical R-D model **[14]**, the atomic hydrogen *H* instantaneously react with another Si-H bond to give molecular hydrogen (H_2) before diffusing away from the interface. Such instantaneous reaction assumption would not be appropriate to interpret very short term NBTI data **[17]**. Hence, it would require explicit consideration of *H* within the R-D framework, as this should be the first by-product after *Si–H* bond dissociation into Si dangling bonds and atomic H, before getting transformed into H_2 **[98]**. Although neutral charge state may not be a stable form of atomic hydrogen, its transient

formation is indeed possible **[99]**. Therefore, diffusion of both *H* and H_2 as well as $H \leftrightarrow H_2$ conversion are given in the **appendix (A.1)** and explicitly incorporated in the generalized R-D framework by the following **[17,21]**:

$$\frac{dN_{it}}{dt} = k_f \left(N_0 - N_{it}\right) - k_r N_{it} N_H^{(0)} \tag{I.41}$$

$$\frac{dN_H}{dt} = D_H \frac{d^2 N_H}{dx^2} - k_H N_H^2 + k_{H_2} N_{H_2} \tag{I.42}$$

$$\frac{dN_{H_2}}{dt} = D_{H_2} \frac{d^2 N_{H_2}}{dx^2} + \frac{1}{2} k_H N_H^2 - \frac{1}{2} k_{H_2} N_{H_2} \tag{I.43}$$

Boundary conditions are defined as:

$$\frac{\delta}{2} \frac{dN_H^{(0)}}{dt} = D_H \frac{dN_H^{(0)}}{dx} + \frac{dN_{it}}{dt} - \delta k_H \left(N_H^{(0)}\right)^2 + \delta k_{H_2} N_{H_2}^{(0)} \tag{I.44}$$

$$\frac{\delta}{2} \frac{dN_{H_2}^{(0)}}{dt} = D_{H_2} \frac{dN_{H_2}^{(0)}}{dx} + \frac{\delta}{2} k_H \left(N_H^{(0)}\right)^2 - \frac{\delta}{2} k_{H_2} N_{H_2}^{(0)} \tag{I.45}$$

Eqs. (I.42) and (I.43) correspond to *H* and H_2 diffusion, respectively. **Eqs. (I.44) and (I.45)** represent the conservation of diffusing hydrogen specie fluxes, *H* and H_2 near the interface, respectively. $k_{H_2} N_{H_2}$ and $k_H N_H^2$ terms in **Eqs. (I.42)-(I.45)** describe the conversion of *H-H*$_2$ in the generalized R-D framework. k_H and k_{H_2} represent the generation and dissociation rates of H_2, D_H and D_{H_2} represent the diffusion coefficients for *H* and H_2, N_H and N_{H_2} represent the concentration of atomic and molecular hydrogen, and *δ* is the interfacial thickness (~ 2−3 Å) **[31]**.

I.5.8- Physical hole-assisted, field-enhanced, thermal Si-H dissociation

As shown in **appendix (A.2),** NBTI-induced N_{it} in the *H-H*$_2$ framework model at long stress time writes as:

$$N_{it} = \left(\frac{k_H}{k_{H_2}}\right)^{1/3} \left(\frac{k_f N_0}{k_r}\right)^{2/3} \left(6 D_{H_2} t\right)^{1/6} \tag{I.46}$$

Eq. (I.46) is the analytic solution of the generalized R-D model. Since the diffusing hydrogen species are neutrals (*H* and H_2), k_r, D_{H2}, k_H, and k_{H2} are field independent. Therefore the field dependence of N_{it} generation must be exclusively incorporated in k_f. **Figure I.18** summarizes the model proposed by Islam *et al.* **[17]**. It assumes that the electric field to be related to k_f via the inversion layer hole concentration ($p_s \propto E_c$), where E_c is the electric field due to the inversion layer carriers, excluding the depletion region from the total electric field E_{ox}, while it equal E_{ox} in accumulation. Hole carriers at Si/SiO$_2$ interface tunnel into Si-H bonds ~1.5 Å (Si-H bond length) with tunneling probability of $T_H \propto P_T \exp(\gamma_T E_{ox})$, where γ_T is field accelerator factor and $P_T \propto \exp(-\sqrt{m_h \phi_{bh}})$ is field independent pre-factor (m_h is the effective mass of holes in the

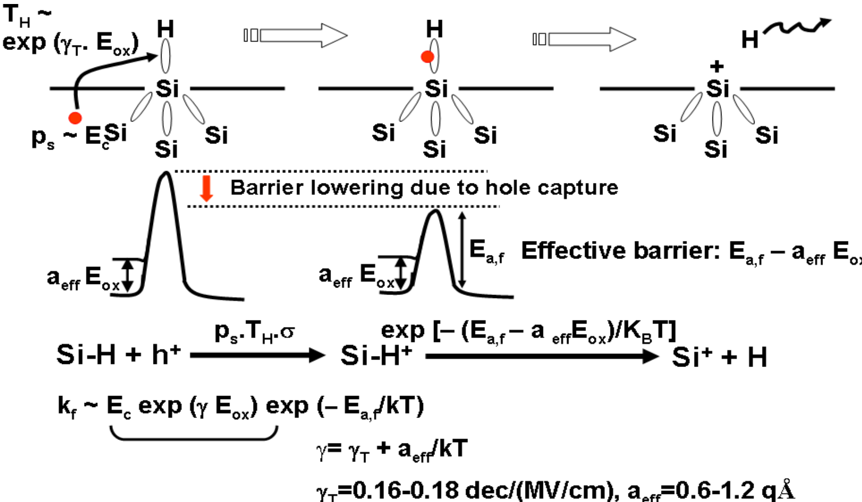


Figure I.18: The proposed model for k_f assumes that inversion layer holes (concentration p_s ~ Ec) near the Si/dielectric interface tunnel into and is captured by Si-H bonds ~1.5 Å (Si-H bond length) away from the interface, leading to a hole assisted field-enhanced thermal generation of interface defects **[17]**.

oxide and ϕ_{bh} is the barrier height for hole tunneling). The rate of field enhanced thermal dissociation of Si-H bond can be expressed as $B_T \propto \exp\left[-\left(E_{a,f} - a_{eff} E_{ox}\right)/KT\right]$, where $a_{eff} E_{ox}$ represents thermal barrier lowering due to positioning of Si-H dipole in the dielectric field, and a_{eff} is the effective dipole moment **[100]**. Therefore, the forward factor, $k_f \propto p_s T_H B_T$ can be written:

$$k_f \propto E_c \exp\left(-\sqrt{m_h \varphi_{hb}}\right) \exp\left[\gamma_T E_{ox} - \left(E_{a,f} - a_{eff} E_{ox}\right)/KT\right] \tag{I.47}$$

Moreover, considering both forward and reverse reaction as well as diffusion processes as Arrhenius activated (*i.e.*, follow $\propto \exp\left(E_a / KT\right)$, where E_a is the activation energy for the process under consideration. Using **Eqs. (I.46) and (I.47)**, the following expression for activation energy associated with N_{it} formation for long term temperature dependence holds **[17]**:

$$E_{a,it} = nE_D + \frac{2}{3}\left(E_{a,f} - E_{a,r} - a_{eff} E_{ox}\right) \tag{I.48}$$

where, $E_{a,f}$, $E_{a,r}$, and E_D are activation energies for k_f, k_r, and the combined activation energy for D_{H2}, k_H, and k_{H2}, respectively, respectively.

In the R-D framework, NBTI-induced threshold voltage shift is exclusively caused by the interface trap generation:

$$\Delta V_{th} = \Delta V_{it} = \frac{q \Delta N_{it}}{C_{ox}} \approx A_{it} T_{ox} (E_c)^{2/3} \exp\left(\frac{2\gamma E_{ox}}{3}\right) \exp\left(-\frac{nE_{D1}}{KT}\right) t^n \tag{I.49}$$

where

$$\gamma = \gamma_T + a_{eff} / KT \tag{I.50}$$

$$nE_{D1} = nE_D + \frac{2}{3}\left(E_{a,f} - E_{a,r}\right) \tag{I.51}$$

$$A_{it} \sim \left(N_0 P_T\right)^{2/3} \sim \left[N_0 \exp\left(-\sqrt{m_h \varphi_{hb}}\right)\right] \tag{I.52}$$

However, R-D model alone fails to explain the cycling behavior and the relaxation in on the fly (OTF) threshold voltage OTF-V_{th} and ultra fast V_{th} experiments observed by Ang *et al.* **[50]**. That is why, hole trapping/detrapping process has to be considered before a comparison with R-D model is carried out. This point will be discussed in section **§ I.6.3**.

According to the R-D theory, time dependence of V_{th} during BTI is modeled by using forward and backward rates k_f and k_r, respectively. During stress, forward and backward processes were assumed to take place simultaneously, implying a superposition of both processes. While during recovery only backward rate is assumed to occur.

I.6- Reaction-Diffusion (R-D) Variant Models

The classical R-D model has fairly succeeded to explain the power-law time evolution of NBTI-induced traps with a form of At^n **[34]** with exponent *n* independent of temperature. However R-D model fails to describe a large range variation of *n* with temperature and time as reported in the literature **[22,34,44,101-103]**. Furthermore, R-D model is not able to describe the relaxation phase, which motivates its extension. Two possible physical interpretations have been given to explain this behavior. One reason is the bulk oxide disordered material, which induces dispersive diffusion of hydrogen **[34,44,101,102]**. The second is the dispersive distribution of Si-H bonds at the interface **[22]**.

I.6.1- Reaction-dispersive-diffusion (RDD) model

The argument of this model is the fact that the bulk oxide is intrinsically amorphous and disordered. Consequently, the disorder will modify the properties of hydrogen transport in the oxide, which will influence the properties of the NBTI process. Thus, The hydrogen diffusion in such SiO_2 should be considered as dispersive **[44,61,101,102]**. In fact, Kaczer et *al.* **[101]** have observed that the exponent, *n* depends on temperature. Accordingly, they have proposed a model based on dispersive transport of hydrogen in the bulk of SiO_2 to explain temperature dependence of *n*. They have reported measurements on threshold voltage shift in multigate p-MOS transistor devices, showing non-arrhenius behavior of the NBTI process. In their model, the disorder arises from the energy distribution of allowed hydrogen states. The latter is schematically illustrated in **Fig. I.19**, where the random energy distribution of potential wells influences the hydrogen transport properties and subsequently modifies the NBTI process.

The RDD model **[44,61,101,102]** is based on the approximation of Arkhipov et *al.* **[104]** to describe the dispersive diffusion in an amorphous dielectric, given by:

$$N_H\left(x,t\right) - D_H \tau\left(t\right)\frac{d^2 N_H}{dx^2} = 0 \tag{I.53}$$

The generalized form of **Eq. (I.53)** is more detailed in **[61]**. The function $\tau\left(t\right)$ is determined as **[61,101]**:

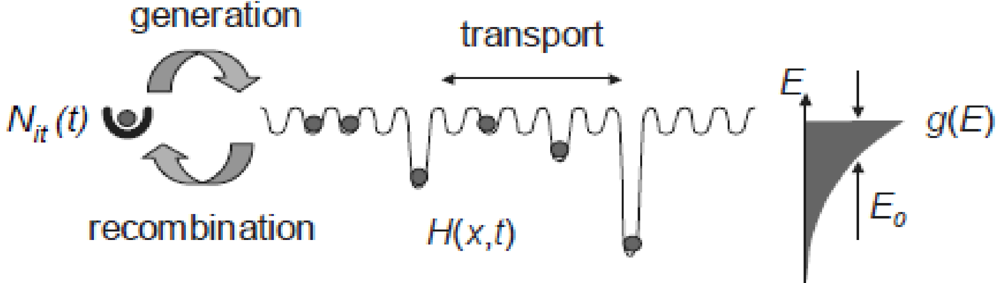


Figure I.19: Illustration of the hydrogen disorder-controlled kinetic. Energy distribution *g(E)* of deep localized hydrogen state is assumed at the Si/SiO$_2$. The hydrogen particles spend most of their time in the deep states, which thus control their transport properties **[44]**.

$$\tau(t) = \frac{N_C}{\nu}\left[\int_{KT\ln\nu t}^{\infty} g(E)dE\right]^{-1} \tag{I.54}$$

where N_C is the density of shallow hoping site for hydrogen. ν is the attempt frequency. $g(E)$ is the density of state (DOS) distribution. The exponential DOS density is commonly used **[44,61,104]**:

$$g(E) = \frac{N_t}{E_0}\exp\left(-\frac{E}{E_0}\right) \tag{I.55}$$

with N_t is the total density of localized states. E_0 is the energy width of the density of state.

Combining **Eqs. (I.54) and (I.55)**, and integrating yields:

$$\tau(t) = \frac{N_C}{\nu N_t}(\nu t)^{\frac{KT}{E_0}} \tag{I.56}$$

The exponent ratio KT/E_0 is the dispersion parameter set to β. Using the triangular profile approximation **[14,34]** and **Eq. (I.26)**, we can express N_{it} as:

$$N_{it} \approx \left(\frac{k_f N_0}{2k_r}\right)^{0.5}\left(D_H \tau(t)\right)^{0.25} \tag{I.57}$$

Finally,

$$N_{it} \approx \left(\frac{k_f N_0}{2k_r}\right)^{0.5}\left(\frac{D_H}{\nu}\right)^{0.25}\left(\frac{N_C}{N_t}\right)^{0.25}(\nu t)^{0.25\beta} \tag{I.58}$$

It is worth noting that for $\beta = 1$, we found the classical power-law time exponent found for atomic hydrogen non-dispersive diffusion [see **Eq. (I.26)]**. That means the dispersion transport regime is possible only for $E_0 > KT$ ($\beta < 1$). At $E_0 < KT$ ($\beta > 1$), the dispersive transport characteristics approaches their equilibrium value. So, the dispersive regime is still valid only if the deeper states are not totally filled.

I.6.2- Dispersive-reaction-rate (DRR) model

Another modeling approach for NBTI is based on reaction-limited process rate of interface trap creation **[22]**. This model was motivated by time and temperature dependencies of the exponent *n*

observed, eliminating the diffusion-limited regime as, at least, the sole source of time dependence of NBTI degradation. Further, due to disordered SiO_2 material, the Si-H bonds at the interface are subjected to a wide spread of bond lengths and angles, which are both related to large variations of bond strengths. That is why Huard *et al.* **[22]** have proposed a distribution of Si-H bonds energy at the Si/SiO_2 interface. Originally, the dispersion of the Si-H bond energy distribution was inspired from broadened distribution in the energy of interface traps measured by Haggag *et al.* **[37]** using charge pumping method.

Therefore, from **Eq. (I.19)** and neglecting the backward rate related to passivation, one can write:

$$\frac{dN_{it}\left(E_a,t\right)}{dt} = k_f\left(E_a\right)\left(N_0 - N_{it}\left(E_a,t\right)\right) \tag{I.59}$$

with $k_f\left(E_a\right)$ is the breaking bond rate factor and depends on the activation energy. It follows Arrhenius law **[22]**:

$$k_f\left(E_a\right) = k_{f_0}\exp\left(-\frac{E_a}{KT}\right) \tag{I.60}$$

where k_{f0} is an attempt frequency and is independent of energy.

From **Eq. (I.59)**, $N_{it}\left(E_a,t\right)$ writes:

$$N_{it}\left(E_a,t\right) = N_0\left[1-\exp\left(-k_f\left(E_a\right)t\right)\right] \tag{I.61}$$

In order to account for the above cited disorder, the related activation energy barrier is taken to be distributed rather than single-valued. So, Si–H bonds at the interface show a broadened Fermi derivative distribution $g\left(E_a,\sigma\right)$ **[22]**:

$$g\left(E_a,\sigma\right) = \frac{1}{\sigma}\frac{\exp\left(\frac{E_{am}-E_a}{\sigma}\right)}{\left[1+\exp\left(\frac{E_{am}-E_a}{\sigma}\right)\right]^2} \tag{I.62}$$

where E_{am} is the median activation energy and σ is the spread of the distribution. $N_{it}(t)$ reads:

$$N_{it}\left(t\right) = \int_0^\infty g\left(E_a,\sigma\right)N_{it}\left(E_a,t\right)dE_a \sim \frac{N_0}{1+\left(\frac{t}{\tau}\right)^{-\alpha}} \tag{I.63}$$

with $\alpha = KT/\sigma$ and $\tau = 1/k_f$.

In this approach, each bond breaks following the reaction equation, but with a specific time constant depending on its own activation energy. As a result, bonds with lower energy would be broken rapidly than bonds with higher activation energy.

I.6.3- Hole-trapping in R-D model

Although it explains many experimental results of NBTI in p-MOS transistor **[13,16,17]**, R-D model fails to describe ultra-fast NBTI measurements in p-MOSFET with nitride gate oxide. This discrepancy has raised a doubt about the correctness of the R-D theory **[27,29,62,109,110]**. Attempting to overcome this issue, the Purdue University research group **[48,106,107]** has proposed a theoretical framework based on the R-D theory for a central component and hole trapping/detrapping into/from

oxide defects theory for an auxiliary component. These components are uncorrelated, where the first is related to interface defect and the second to pre-existing and generated oxide traps. The group tries to show that the theory-experiment gap in interpreting NBTI can be bridged or reduced if one takes account hole trapping into oxide traps due to pre-existing traps (ΔN_{ht}) and generated traps (ΔN_{ot}). ΔN_{ht} is used to explain the fast and temperature independent part of NBTI and relaxation as well as the abrupt decrease of duty part above 50% of duty cycle. ΔN_{ot} is used to explain the disparity of start recovery time in different nitrided gate dielectrics **[17,48,106,107]**.

I.6.3.1- Hole-trapping into pre-existing oxide trap (ΔN_{ht})

The pre-existing defects exist in the as-is-fabricated gate oxide, but they are more important in almost all high-k dielectric, such as oxynitride and Hafnium (Hf). The trapping into this kind of trap leads to ΔV_{ht}, which is independent from the generation of interface and oxide traps. Regarding the modeling of hole trapping into the pre-existing oxide defects, three possible mechanisms are considered by Tewksbury *et al.* **[108]**, which are (see **Fig. I.20**): (a) elastic tunneling of carriers from the conduction band and valence band, (b) interfacial defect assisted trapping/ detrapping of carriers, and (c) phonon assisted trapping/detrapping of carriers.

Tewksbury's approach is the most suited one for MOSFETs since it accounts for the energy and depth dependence and uses a convenient one-dimensional formulation of tunneling. It is commonly used for explaining hole trapping (during NBTI stress) involving pre-existing oxide defects **[22,27,109,110]**. The approximation of Tewksbury considers the contribution from substrate carrier fluxes only in calculating trapping dynamics. This has worked well for the thick dielectric (25~75 nm) structures. However, transferring the same concept in case of ultra-scale MOS structures with thin dielectric (1.5~3 nm) becomes questionable **[15,17,111].** Islam *et al.* **[17]** have incorporated carrier fluxes from gate electrode of thin gate dielectric, within Tewksbury's trapping/detrapping model. Using such modified version of Tewksbury's model, they have modeled hole trapping (N_{ht}) in thin Hf-based dielectric. They used a simple elastic trapping/de-trapping model, in which holes from the inversion

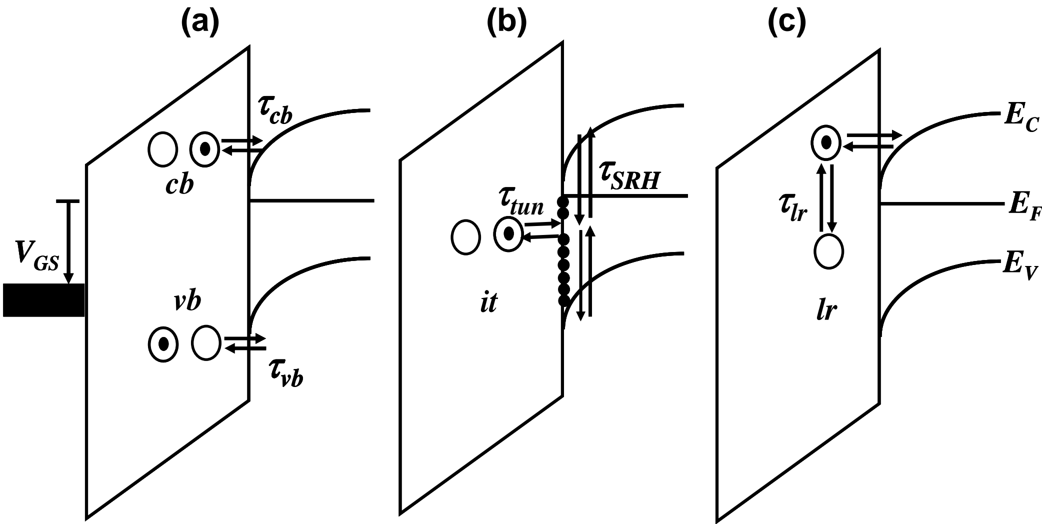


Figure I.20: Three mechanisms proposed by Tewksbury *et al.* **[108]** for trapping/detrapping charges into/from pre-existing oxide traps. (a) Elastic tunneling of charges from the conduction band (*cb*) and valance band (*vb*). (b) interfacial defect (*it*) assisted trapping/detrapping of charges. (c) phonon-assisted (relaxation lattice, *lr*) trapping/detrapping of changes.

layer are first trapped in the pre-existing defects within the oxide and then these trapped holes detrap towards the empty states in poly-Si and channel. Trap filling probability (f_T) writes:

$$\frac{df_T}{dt} = \sigma_p v_{thp} \left[p\ T_S \left(1 - f_T\right) - n_S T_S f_T - n_G T_G f_T \right] \quad \text{for thin gate oxide} \quad (I.64)$$

$$\frac{df_T}{dt} = \sigma_p v_{thp} \left[p\ T_S \left(1 - f_T\right) - n_S T_S f_T \right] \quad \text{for thick gate oxide} \quad (I.65)$$

where p is the inversion layer hole density, v_{thp} is the thermal velocity, n_s and n_G are the concentration of detrapping states at substrate and poly-Si, respectively, and T_s and T_G are the tunneling probability (obtained using the Wentzel–Kramers–Brillouin, WKB approximation) of holes from Si/dielectric interface to trap and trap to poly-Si, respectively. The solution of **Eqs. (I.64) and (I.65)** are:

$$f_T = \frac{T_S \left[1 - \exp(-\sigma_p v_{thp} \left(pT_S + n_S T_S + n_G T_G\right) t\right]}{(1 + n_S / p) T_S + n_G T_G / p} \quad \text{for thin gate oxide} \quad (I.66)$$

$$f_T = \frac{1 - \exp(-\sigma_p v_{thp} \left(pT_S + n_S T_S\right) t}{1 + n_S / p} \quad \text{for thick gate oxide} \quad (I.67)$$

The density of trapped holes located at the position x and at energy E_i writes:

$$\rho_{ht}\left(x, E_i, t\right) = N_0^{ht} \delta'(E - E_i) f_T(x, E_i, t) \quad (I.68)$$

where N_0^{ht} is the density of pre-existing hole traps, and E_i is the energy level at which elastic trapping is possible. δ' is Dirac function (δ' = 1 when $E = E_i$ and 0 when $E \neq E_i$). ΔV_{ht} is given by:

$$\Delta V_{ht} = \frac{q \Delta N_{ht}}{C_{OX}} = \frac{q}{C_{OX}} \int_0^{Tox} \int_E \left(1 - \frac{x}{T_{ox}}\right) \rho_{ht}\left(x, E, t\right) dE dx \quad (I.69)$$

x *is* measured into the oxide from the substrate/oxide interface. ΔV_{ht} can be expressed as **[17,112]**:

$$\Delta V_{ht} = A_{ht}(1 - \exp - (t / \tau)^{\beta'}) \quad (I.70)$$

where $\tau = 1 / \left[\sigma_p v_{thp} \left(pT_s + n_s T_s\right)\right]$ for thick oxide. A_{ht}, τ, and β' are fitting parameters that depends on the dielectric quality and thickness. In general, τ, and β' are larger for larger dielectric thickness, see details for SiON gate oxide in **[17,112]**). The hole trapping in pre-existing defects should saturate rapidly, where the saturation depends on the dielectric quality and thickness. The main model parameters are also given in **appendix (A.3)**.

I.6.3.2- Hole-trapping into generated oxide trap (ΔN_{ot})

The hole trapping/detrapping into a newly generated traps (ΔN_{ot}) also plays a role in NBTI degradation, specially at high stress voltage, where NBTI is similar to Time-Dependent Dielectric Breakdown TDDB. In stress condition, ΔN_{ot} dynamic follows the same **Eqs. (I.64) and (I.65)** as for ΔN_{ht}. However, as opposite to ΔN_{ht}, trapping/detrapping into generated traps is a slow process and expected to show no-saturation. Indeed, it has been shown that NBTI time exponent remains independent stress voltage and temperature under certain conditions of stress **[15],** but higher stress

voltage indicates a signature of oxide defect creation, inducing exponent n to increase at longer stress time **[113,114]**. ΔN_{ot} is responsible for stress-induced leakage current (SILC) and TDDB or gate oxide breakdown. Several techniques have been used for direct estimation of trap generation during NBTI at Si/SiO_2 and SiO_2/poly-Si interfaces using low-voltage stress-induced leakage current (SILC) **[30,115]**, at and near the Si/SiO_2 interface by *DCIV* **[112,115,116]** and charge pumping (*C-P*) **[15,113,117]**, and within SiO_2 bulk by SILC **[113]**; these techniques measure current due to trap-assisted tunnelling (for SILC and LV SILC) and trap-assisted recombination of electrons and holes (for *DCIV* and *C-P*) before and after stress, and generated traps are estimated from the increase in current after stress.

However, the elastic tunneling does not account for the anticipated temperature and bias dependence needed to explain the recent experimental findings **[117]**. Therefore, a new approach has to be found, i.e. probably inelastic (thermally activated tunneling) mechanism **[46,118]**.

I.7- NBTI Two-Stage Model

Motivated by a broad scalability of both NBTI stress and relaxation phases at various voltages and temperatures for several technologies (thick SiO_2, ultra-thin SiO_2, ultra-thin SiON, and high-k), Grasser et *al.* **[29]** proposed the two-stage model to capture this behavior. Unlike the R-D model (which considers hole trapping in pre-existing and generated SiO_2 bulk traps somewhat as a parasitic component that has to be removed from NBTI before comparison with R-D theory is made **[48,107,119]**), the two-stage model considers the hole trapping as the heart of the NBTI degradation **[29,49,62]**.

The two-stage model is based on two step creation processes of NBTI-induced defects **[29]**. In stage one, holes are trapped into near-interfacial oxygen vacancy via the multiphonon-field-assisted tunneling (MPFAT) **[120]** process and multiphonon emission (MPE) process, which are thermally activated process **[121]**. This process induces $E_{\gamma}^{'}$ center creation. In the second stage, P_b centers, which are poorly recoverable defects, are created. The latter process occurs because of the migration of the hydrogen from saturated interface dangling bond P_b-H to the newly created $E_{\gamma}^{'}$, where it saturates an unpassivated dangling bond of one half of $E_{\gamma}^{'}$ center ($E_{s}^{'}$), subsequently locking the second half at the positive charge. Often, one-one correlation is reported **[29]** between interface and oxide traps.

This model uses the Harry-Diamond-Laboratories (HDL) model for switching $E^{'}$ center **[122,123]**. Grasser et *al.* **[29,49,62]** have modified the HDL model by introducing E'-P_bH complex to couple between *E'* center and P_b center. **Figure I.21** illustrates the two-stage model, where E'-P_bH complex is assumed to be in one of four states with states one, two, and three same as *E'* center **[123]** and are used to model the recoverable component of NBTI. Upon stress application, the Si-Si bond of the neutral precursor *E'* (state one in **Fig. I.21**) can capture a hole causing the breakage of Si-Si bond and resulting in structural relaxation. While one of the Si atoms takes the positive charge, the other Si atom carriers a dangling bond (see state two in **Fig. I.21**).

The positively charged $E_{\gamma}^{'}$ center in state two is capable, via its dangling bond, of trapping/detrapping charge carriers from the silicon substrate. This is represented as transition from

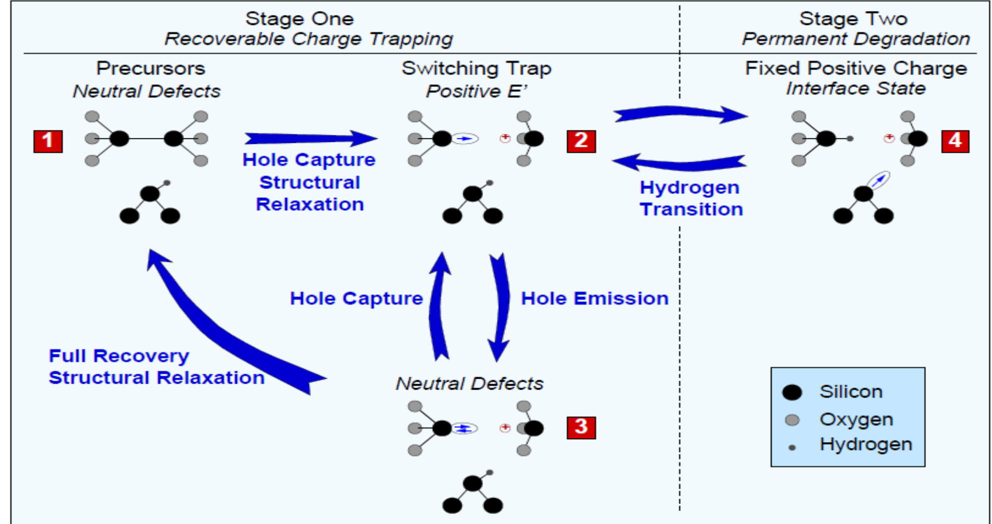


Figure I.21: Schematic of switching traps representing the HDL model for switching trap coupled to the dangling bond at the interface. It illustrates the states of two stage model. State (1) depicts the precursor defect, state (2) is the positively charged *E'* center, state (3) represents *E'* center annihilation by electron capture, and state (4) shows the locking of *E'* center in positive charge by hydrogen coming from passivated silicon dangling bond at the interface and subsequently interface trap creation **[29]**.

state two to state three, where the $E_{\gamma}^{'}$ defect is neutral at state three. The switching back and forth between state two and three explain the fast recoverable component of NBTI. Being in its neutral charge state (state three), the $E_{\gamma}^{'}$ defect also may return back to its initial configuration of precursor (neutral defect). Alternatively, the $E_{\gamma}^{'}$ defect in state two may undergo a reaction with P_b-H and attract its hydrogen. When this happens, the E'-P_bH complex moves to state four. This step locks in the positive charge at the $E_{\gamma}^{'}$ and induces a dangling bond creation at the interface.

The trapping/detrapping dynamic describing the steps of two-stage model are given by the following set of rate equations:

First stage

$$\frac{df_1}{dt} = f_3 K_{31} - f_1 K_{12} \tag{I.71}$$

$$\frac{df_2}{dt} = f_1 K_{12} + f_3 K_{32} - f_2 K_{23} + f_4 K_{42} \tag{I.72}$$

$$\frac{df_3}{dt} = f_2 K_{23} - f_3 K_{32} - f_3 K_{31} \tag{I.73}$$

Second stage

$$\frac{df_4}{dt} = f_2 K_{24} - f_4 K_{42} \tag{I.74}$$

where, f_i is the occupation of the state i, K_{ij} denotes the transition rates from state f_i to state f_j. Since the defect has to be in one of its four states, therefore the constraint $f_1 + f_2 + f_3 + f_4 = 1$ has to be satisfied.

The transition rates describing the tunneling processes of electrons (holes) from conduction (valence) band into the trap and vice versa read as follows:

First stage

$$K_{12} = k_p^c\left(E_T, \Delta E_B, E_{ref}\right) + k_n^e\left(E_T, \Delta E_B, E_{ref}\right) \tag{I.75}$$

$$K_{23} = k_p^e\left(E_T', \Delta E_C, 0\right) + k_n^c\left(E_T', \Delta E_C, 0\right) \tag{I.76}$$

$$K_{32} = k_p^c\left(E_T', \Delta E_C, 0\right) + k_n^e\left(E_T', \Delta E_C, 0\right) \tag{I.77}$$

$$K_{31} = \upsilon_1 \exp\left(-\beta \Delta E_A\right) \tag{I.78}$$

Second stage

$$K_{42} = \upsilon_2 \exp - \beta\left(\Delta E_D - E_2 - a_{eff} E_{OX}\right) \tag{I.79}$$

$$K_{42} = \upsilon_3 \exp - \beta\left(\Delta E_D - E_4 + a_{eff} E_{OX}\right) \tag{I.80}$$

where the shorthand k (trap level energy, MPE barrier, MPFAT reference field) is used for the emission and capture tunneling process. υ_i and ΔE_i are the attempt frequencies and energy barriers, respectively. The term $a_{eff}E_{OX}$ represents the rise or the lowering of the barrier due to the applied electric field. Indeed, since the interfacial Si-H bonds are associated with a dipole moment, the shift of the energy minima depends linearly on the oxide field with a proportionality constant of a_{eff} (effective dipole moment).

The hole and electron capture and emission rates k are given by:

$$k_p^c = p v_{thp} \sigma_p e^{-x/x_{p0}} e^{-\beta \Delta E} \theta\left(E_{VT}, e^{-\beta E_{VT}}, 1\right) e^{E_{OX}^2 / E_{ref}^2} \tag{I.81}$$

$$k_p^e = p v_{thp} \sigma_p e^{-x/x_{p0}} e^{-\beta \Delta E} \theta\left(E_{VT}, e^{-\beta E_{VF}}, e^{-\beta E_{TF}}\right) \tag{I.82}$$

$$k_n^c = n v_{thn} \sigma_n e^{-x/x_{n0}} e^{-\beta \Delta E} \theta\left(E_{TC}, e^{-\beta E_{TC}}, 1\right) \tag{I.83}$$

$$k_n^e = n v_{thn} \sigma_n e^{-x/x_{n0}} e^{-\beta \Delta E} \theta\left(E_{TC}, e^{-\beta E_{FC}}, e^{\beta E_{TF}}\right) \tag{I.84}$$

where n and p are electron and hole concentrations in the channel, v_{thn} and v_{thp} are their thermal velocities, σ_n and σ_p their capture cross sections. E_F is the Fermi level, E_V and E_C the valence and conduction bands at the interface. ΔE is MPE barrier, and $\beta = 1/KT$. E_{ref} is the reference electric field for MPFAT. θ is an auxiliary function and writes as:

$$\theta\left(E_{switch}, a, b\right) = \begin{cases} a & E_{switch} \geq 0 \\ b & E_{switch} < 0 \end{cases} \tag{I.85}$$

The shorthand relation $E_{switch} = E_{AB} = E_A - E_B$ describes the thermal activation energy needed for hole capture into traps below E_V, while capture above E_V proceeds without activation energy, and vice versa for electrons. More details are given in **appendix (B).**

The two-stage four-well model with various energies is represented in **Fig. I.22**. The energy levels are assumed related to a neutral precursor well (E_1). The rate is calculated solving rate equations between pairs of wells (E_1−E_2, E_2−E_3, E_1−E_3, and E_2−E_4) to determine the time-dependent occupancies f_1–f_4 of wells E_1–E_4. Barrier ΔE_B between E_1 and E_2 determines the oxide trap density, ΔN_{ot} during stress, barrier ΔE_A between E_1 and E_3 resolves ΔN_{ot} during recovery, and ΔE_A is assumed equal to ΔE_B since wells 1 and 3 are in thermal equilibrium **[29]**. Generation and recovery of interface trap density, ΔN_{it} are determined by the barrier ΔE_D between E_2 and E_4. The time-dependent well occupancy probabilities are calculated during stress and recovery, and the total NBTI-induced charge is thus given by:

$$\Delta Q_{Total} = \Delta Q_{it} + \Delta Q_{ot} \tag{I.86}$$

The amount of positive charge stored in the oxide is given by all the defects being either in state 2 *or* 4 and not in state 1 (the precursor state) and writes as:

$$\Delta Q_{ot} = qN_0^{ot}\left(1-\frac{x}{T_{ox}}\right)\left(f_2+f_4\right) \tag{I.87}$$

The amount of positive charge stored in the interface states is given by the average of the probability of having depassivated bonds $\left(f_4\right)$ times the probability that the created electrical level is unoccupied $\left(1-f_{it}\right)$ and for E_{it} within the lower-half of the silicon bandgap (the donor-like states). It reads as:

$$\Delta Q_{it} = qN_0\left(1-f_{it}\right)f_4 \tag{I.88}$$

As the degradation and recovery in thick and thin oxides looks basically the same, Grasser *et al.* **[29]** have concluded that the observed dispersion in time constants is primarily a property of the Si/SiO_2 interface. Consequently, the depth dispersion will be neglected ($x \approx 0$). Further, the occupancy of the created interface states is of minor relevance since normally both during stress and

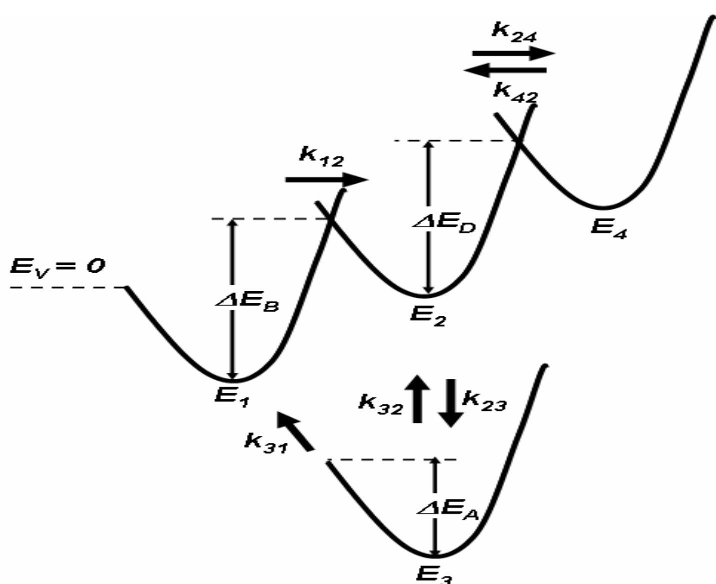


Figure I.22: Two stage four well model with different trap levels and energy barriers.

recovery the Fermi-level is close to the silicon valence band ($f_{it} \approx 0$) and consequently most interface states will be positively charged. Therefore, **Eqs. (I.87) and (I.88)** can be simplified and the total threshold voltage shift ΔV_{th} writes:

$$\Delta V_{th} = -\frac{q}{C_{OX}}\left[N_0^{ot}\left(f_2 + f_4 \right) + N_0 f_4 \right] \tag{I.89}$$

I.8- NBTI Gate Oxide Thickness Dependence

Even though one can think that the gate thickness and the nature of the gate dielectric (SiO_2, high-k) can affect the NBTI degradation, several studies have shown that NBTI effect is independent of gate oxide thickness **[29,40,46,124,125]**. In fact, to avoid polluting CP current with parasitic leakage current, thick gate oxide devices are more appropriate to extract NBTI-induced interface-trap. However, the exact location and type of defects created under negative bias temperature (NBT) stress in p-MOS transistors are still a highly debated topic. Grasser et *al.* **[29,46]** have found an excellent agreement with measurements from three different technologies (SiO_2, SiON, and HK) with different thicknesses, underlying that NBTI is driven by a technology-independent mechanism primarily related to the chemistry of the silicon/silicon-dioxide interface and the near-interfacial layer (see **Fig. I.23**). They investigated two extreme technologies, one with an ultra-thick 30 nm SiO_2 layer and the other with a SiO_2/HfO_2 (HK) gate stack. Amazingly, the same scalability is observed and all devices show qualitatively the same stress and recovery behavior, quite contrary to the opinion that NBTI in devices with ultra-thick oxides is understood and complications arise only due to the introduction of nitrogen or alternative gate stacks. This supports the view that NBTI is primarily determined by the Si/SiO_2 interface and interfacial layer properties rather than the oxide bulk.

Pobegen et *al.* **[124,125]** have presented a detailed study on equivalent devices with different oxide thicknesses (5 to 30 nm) where they have experimentally shown that the basic mechanisms behind the NBTI are the same in thin and thick oxide technologies. They have also shown that defects

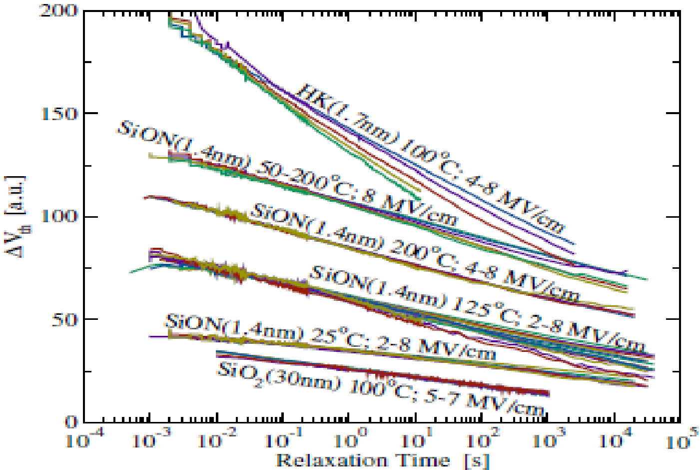


Figure I.23: Recovery of the threshold voltage shift at different temperatures, voltages, and stress times, for three completely different gate stacks, thick SiO_2, ultra-thin SiON, and HK. A similar scalability as during recovery is observed during stress for all technologies. All data sets show good temperature and field scalability and thus do not support the idea that NBTI is a consequence of two independent mechanisms. underlying that NBTI is driven by a technology-independent mechanism primarily related to the chemistry of the silicon/silicon-dioxide interface and near-interfacial layer **[46]**.

created under NBTI stress are not solely located at the interface but extend a few nanometers into the oxide. They have found that the equivalent oxide thickness normalized V_{th} shift and the change of the I_{CP} after BTS as a function of the EOT are depicted for the p++ gated and n++ gated p-MOS devices, respectively [see **Figs. I.24 (a) and (b)**]. The NBTI in either p++ or n++ poly gated devices is nearly independent of the equivalent oxide thickness, regarding both V_{th} shift and I_{CP} change. However, The PBTI showed a complex picture in two regards. First, vastly different dependences on the EOT for devices with different gate poly doping are observed. While the degradation in n++/p-MOS devices is independent of the oxide thickness, it increases strongly with decreasing oxide thickness in p++/p-MOS devices. ΔV_{th} even changes its sign with decreasing EOT, such that a very small net negative charge is built up for the device with 26 nm equivalent gate oxide thickness, and a net positive charge for devices with thinner dielectrics. Noting that in our experiments we studied NBTI stress in n+/p-MOSFET.

Finally, Based on vast experimental data set obtained from different technologies (pure SiO_2, nitrided SiO_2, and HK), Huard **[40]** has suggested that NBTI is made of two independent components, presenting different voltage and temperature acceleration factors as well as process dependences. The recoverable part, subjected to fast transient effects, is shown to obey field-assisted hole trapping/detrapping processes. The permanent part is shown to be made of an equal number of interface traps. The permanent part is found independent of the nitrogen content, gate stack process, and thickness for different gate stacks: pure SiO_2, SiON (thermally- or plasma nitrided) and HfSiON gate stacks, while the recoverable part is impacted by nitrogen incorporation into gate stack [see **Figs. I.25** (a) and (b)]. In our study, we are concerned by the permanent part.

I.9- Discussion

Although subject to thorough modeling and analysis, NBTI is still under intensive investigation. Efforts have been deployed towards physical basic mechanisms leading to two protagonist models i.e. reaction-diffusion **[17,119]** and two-stage models **[29,49]**. None of them is able to describe all experimental NBTI key features. The fundamental criticisms of R-D model arise from its inability to predict the bias dependence of recovery and long tail of transient recovery. These features have inspired the energy wells based models **[28,29,62,126]**, especially two-stage model **[29]**. The supporters of R-D model claim that it is important to clean experimental data from hole detrapping in pre-existing and generated bulk traps before comparison with R-D theory is made **[17]**, and that mobility correction is also important for NBTI relaxation analysis **[127]**. However, Grasser *et al.* **[62]** have shown that superposition of elastic hole trapping, which saturates within about a second, followed by the "classic" H_2 diffusion-limited creation of interface traps, leads to unnatural "bumps" in the recovery characteristics. No such bumps have ever been observed experimentally. In addition, the fact that recovery in R-D is predicted by only the back diffusion of neutral H_2 leads to recovery bias independent. Nevertheless, experimental recovery is shown strongly bias dependent when V_{GS} is switched toward accumulation **[62]**. This bias dependence occurs well beyond the assumed saturation of the hole-trapping component of about 1 s and thus must be an intrinsic feature of the dominant recoverable component.

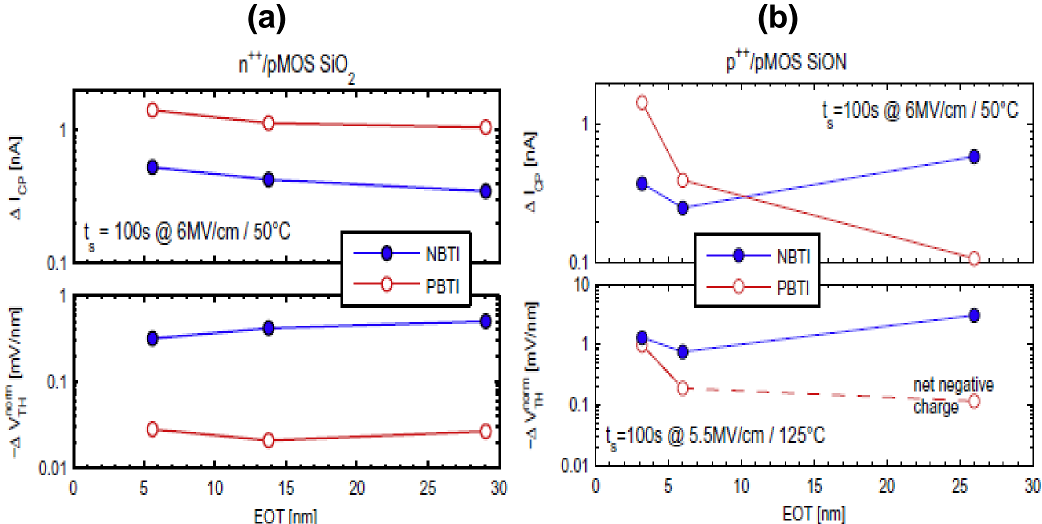


Figure I.24: (a) The degradation of ΔI_{CP} and normalized V_{th} ($\Delta V_{th}/EOT$) following NBTI and PBTI in n++/p-MOS device is independent of the oxide thickness. This indicates that the electric field is the only relevant parameter for the NBTI and PBTI in n++ poly gated devices. (b) Variation of ΔI_{CP} and $\Delta V_{th}/EOT$ with oxide thickness. An increase of ΔI_{CP} following PBTI with decreasing oxide thickness suggests that holes tunneling from the p++ poly gate may contribute to the degradation in thin dielectric devices **[125]**.

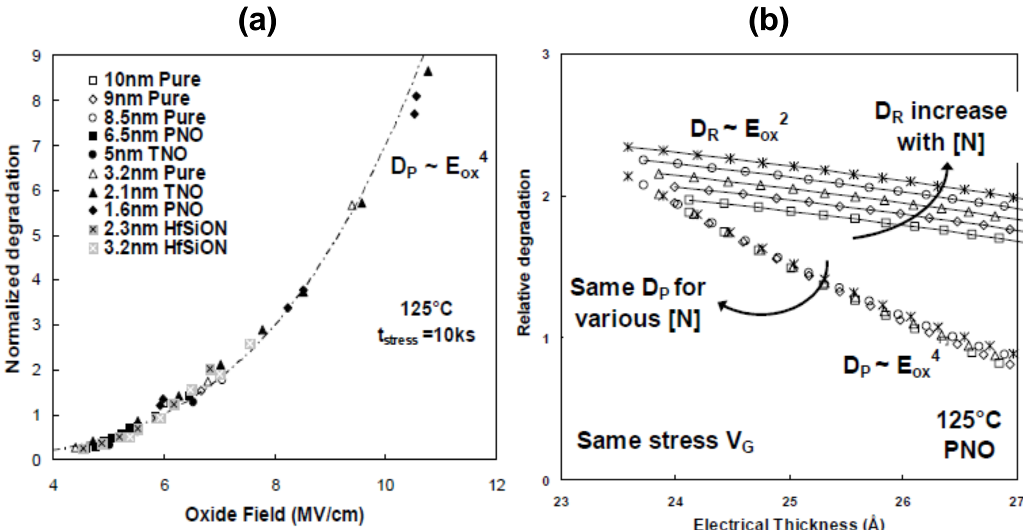


Figure I.25: (a) The independence of the permanent component (D_P) of the gate stack process and thickness pure SiO_2, SiON and HfSiON. All D_P degradations were normalized to 6 MV/cm vertical oxide field. (b) The independence of D_P of the nitrogen content/process and thickness of oxide, while the recoverable component (D_R) shows strong nitrogen dose dependence **[40]**.

Another disagreement between both models is the duty-factor (DF) dependence degradation. R-D model predicts $(DF)^{1/3}$ dependence of degradation, but experiments show a step-shaped curve with an abrupt drop of the degradation at DF = 100% (DC) **[62]**. Furthermore, R-D predicts 80% of the DC degradation at DF = 50% (AC), while degradation smaller than 40% is experimentally observed **[62]**. Recently, Mahapatra *et al.* **[48]** have suggested that the sharp increase is caused by the elastic tunnelling of holes into the pre-existing hole traps (ΔN_{ht}). This argument has been deduced from normalized degradation to the DF = 50% (AC) rather to DF = 100% (DC). Indeed, the curves have revealed a universal relation for up to 80% (AC), which is well fitted by the R-D model, and large spread has only been observed for DF closer to DC. This point of view is disagreed by Grasser *et al.*

[62], because the peak at DF = 100% (DC) decreases but doesn't disappear with increasing recovery time, even after 30 ks of recovery, where any elastic hole trapping component would have vanished by this relaxation time. They have concluded that the peak is an intrinsic part of the degradation.

On the other side, the two-stage model has been severely criticized **[47]**, because it has extremely been used to fit NBTI for very short stress time **[29]**. In fact, when the model is examined for long stress time, its prediction tends to diverge from experimental data, facing two-stage model to significant challenges to predict stress over longer time **[47]**. Moreover, since barrier E_A (= E_B) controls recovery in two-stage model, a lower value increases recovery flux from well 3 to well 1 and results in early start of recovery and vice versa. However, barrier E_B controls stress, a lower value would increase the forward reaction, and the degradation would tend to saturate early and would result in a lower exponent n at long stress time and vice versa. This indeed is a fundamental limitation of the two-stage model, as it cannot simultaneously predict experimental stress and recovery trends for the same set of parameters **[48]**.

Finally, pros and cons of the R-D and two-stage models can be summarized as follows:

- R-D data **[17]** are usually obtained with typically ms measurement delay, which however has insignificant effect since the stress time is very long. In spite of disparate sources, all devices show power law time dependence with exponent n = 1/6, a feature of DC NBTI that is readily predicted by H_2 based framework **[17]**. It is important to note that the prediction of such power law time exponent is inherent to H_2 based R-D framework and is obtained without adjustable parameters.
- The R-D model is unable to predict bias dependence of recovery and long tail of recovery features.
- The two-stage model or four-energy well model prediction tends to diverge from experimental data for long stress time stress.
- The two-stage model uses a pre-stress stabilization step that equilibrates the occupancy of different wells. Otherwise, all wells, except the first well, would be empty at the beginning of stress.
- The two-stage model cannot simultaneously predict experimental stress and recovery trends using the same Physical set of parameters.
- R-D model predicts recovery by the back diffusion of neutral H_2 and is bias independent.

I.10- Conclusion

In this **Chapter**, we have presented several models intended to describe NBTI degradation as well as the defects behind it. Despite their quantitative number, none of the NBTI models proposed so far could fully explain all the experimental findings. This holds true either for the R-D model along with all its variants and two-stage model. This reflects the complexity of the microscopic nature of the defects at the origin of NBTI and their exchange charge mechanisms. This fact has engendered a great confusion, inciting researchers to develop new and more sophisticated electrical measurement methods to get insight into NBTI underlying physical processes. This point will be treated in the next **Chapter**.

As the situation gets complicated, it is worth exploring new explanations for the experimental observations and upgrading our understanding of NBTI. That is what we will try to do in the last **Chapters**.

CHAPTER II

NBTI CHARACTERIZATION METHODS

II.1- Introduction

II.2- Charge-Pumping (*C-P*) Technique

II.3- Transistor Drain Current for Different Modes

II.4- Classical Measure-Stress-Measure (MSM)

II.5- Parameter Extraction of MSM Methods

II.6- On The Fly V_{th} (OTF-V_{th}) Methods

II.7- On The Fly Interface Trap (OTFIT)

II.8- Conclusion

CHAPTER II

NBTI CHARACTERIZATION METHODS

II.1- Introduction

Negative bias temperature instability is used to be characterized following the traditional paradigm, which consists of conventional measure/stress/measure cycles. The stress is interrupted to measure the linear-region transfer characteristics, I_{DS}-V_{GS} of stressed devices. These curves are used to estimate the degradation from the extracted parameters such as the threshold voltage V_{th}, the subthreshold swing *SS*, the transconductance, and the interface trap D_{it}. The latter is usually obtained using $log(I_{DS})$–V_{GS} subthreshold swing measurements **[63]**, charge pumping technique **[56],** and DCIV measurement **[128]**. Techniques were since then developed to minimize and optimize the delay between stress and measure **[55,57]**. Denais et *al*. **[22,57,129]** proposed on the fly threshold voltage (OTF-V_{th}) to extract V_{th} using a low drain voltage of about 25-50 mV and record the drain current at the end of the stress period, without stress interruption. Some authors **[55,130]** proposed on the fly interface-trap (OTFIT) to extract the interface-trap N_{it} without any recovery between stress and measure.

In this **Chapter**, we start by describing the standard charge pumping (*C-P*) technique as well as its ability to extract trap density distribution as a function of gate length, depth into the oxide near the interface and energy. Then after, we relate methods and techniques based on *I-V* and *C-P* to extract the NBTI degradation.

II.2- Charge-Pumping (*C-P*) Technique

Since the publication of a modeling approach by Groeseneken et *al.* in 1984 **[56]**, the charge pumping technique has became the most widely used technique for electrical characterization of Si/SiO_2 interface trap. It is based on measurement of the DC current resulting from applying pulses onto the gate of a MOSFET, while keeping source and drain grounded or under reverse polarization as illustrated in **Fig. II.1.** They showed that the current originates from recombination of minority and majority carriers at traps located at the Si/SiO_2 interface. For this reason, the technique can be used for estimation of the interface trap density in MOSFETs and the evaluation of MOSFET degradation. The current is found to be proportional to the gate area and the frequency of the applied gate pulses. It flows in the opposite direction of the leakage current of the source/substrate and drain/substrate diodes. When the pulse is switched from accumulation to inversion modes while the amplitude is kept constant **[131]**, five phases are observed as illustrated by **Fig. II.2** for p-MOS transistor (used in this work)**:**

Phase 1: The pulse is totally above the flatband voltage and the substrate is in accumulation. The interface traps are permanently filled with electrons and therefore no recombination current is measured.

Phase 2: The pulse low level (V_L) reaches the region between the flatband and the threshold voltages. In this phase the channel is moved into strong depletion up to weak inversion and the charge pumping current starts to increase. The rising I_{CP} current could be induced by the recombination

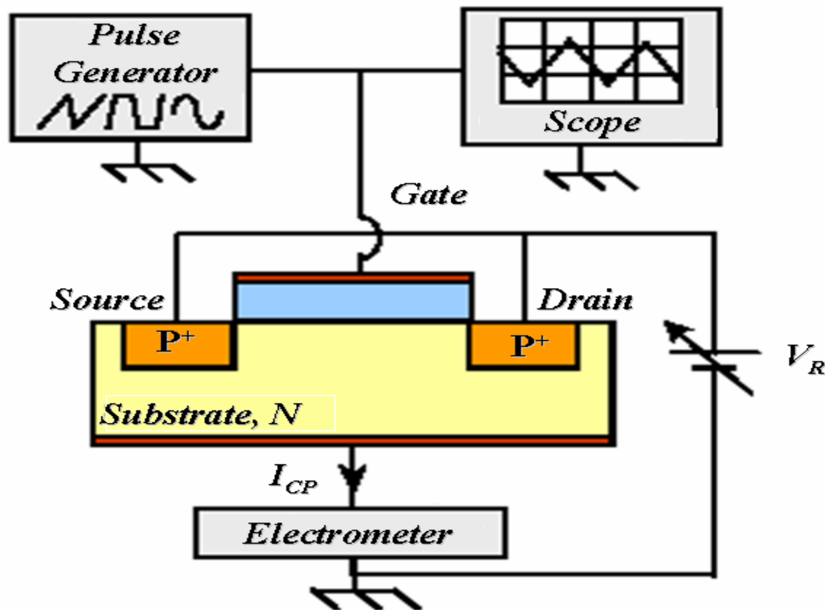


Figure II.1: Setup for charge pumping measurement. The gate is pulsed between inversion and accumulation conditions. The source- and drain-substrate are reversely polarizated or grouded. The DC substrate current is measured as the charge pumping current, I_{CP}.

process in weak inversion. Furthermore, it has been shown, though, that other mechanisms may have an important influence. These can be surface potential fluctuations because of non-uniformly spatial distribution of oxide charges **[132]**, or variations in the vicinity of the source and drain regions **[133]**.

Phase 3: The low level of the pulse is below the threshold voltage and the high level is above the flatband voltage, $V_H > V_{fb} > V_{th} > V_L$. The pulse sweeps the substrate in the channel area from accumulation to complete inversion. The electrons and holes fill alternatively the interface traps, where they recombine and induce I_{CP} current.

Phase 4: The high level resides between the threshold voltages and flatband. The transistor only reaches weak accumulation. The interface traps are mainly positively charged and are no longer flooded with electrons, thus recombination is reduced and the charge pumping current dropdown. The falling side of the Elliot curve could be shaped by the LOCOS region **[134]**.

Phase 5: The high level is below the threshold voltage and the transistor is in strong inversion. The traps are filled with holes and no electrons reach the channel at any time. The measured substrate current only consists of the source and drain leakage currents.

II.2.1- Charge-pumping current model

The Groeseneken's model **[56]** has been developped to capture the maximum I_{CP} current which is obtained when the low level of the gate voltage pulse is below the flatband voltage, and the high level is above the threshold voltage,($V_L < V_{fb} < V_{th} < V_H$) in n-MOS transistor. In this case, the transistor channel is swept from accumulation to inversion repeatedly inducing interface traps filling with holes and electrons, respectively. The latter recombine at the interface trap leading to I_{CP} current. The I_{CP} current measured at the substrate is given by:

$$I_{CP} = qfA_G \overline{D_{it}} \left(E_{em,h} - E_{em,e} \right) \tag{II.1}$$

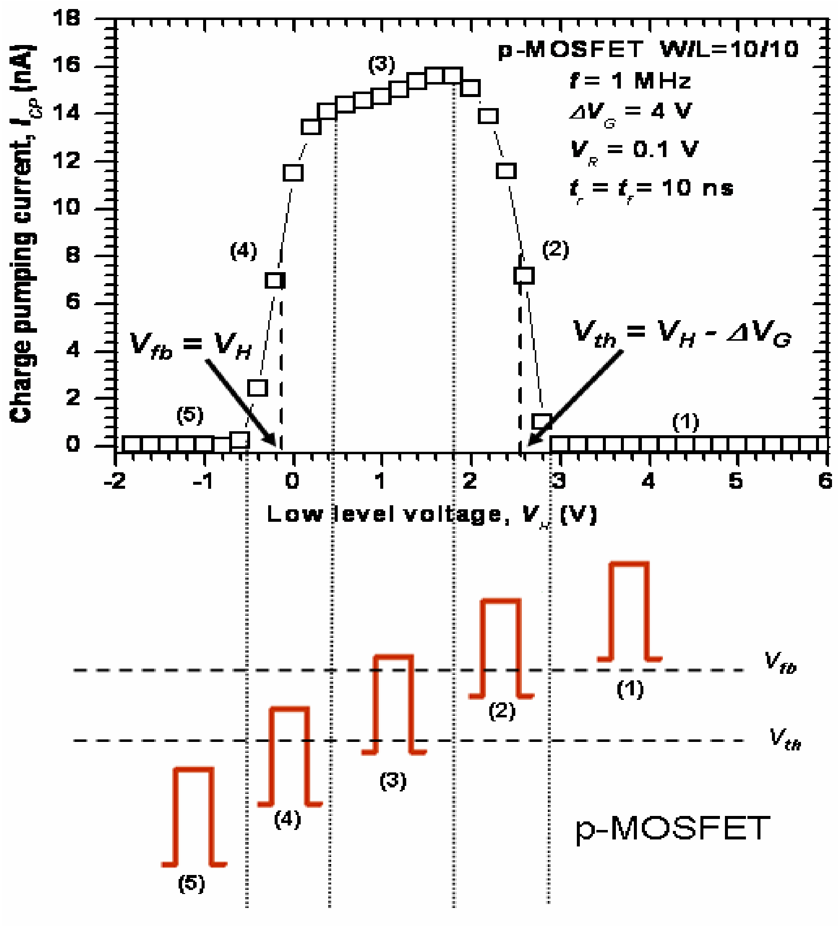


Figure II.2: Charge pumping current curves performed with constant amplitude method on one of transistors used in the present work. As the pulse with constant amplitude is moved from accumulation to inversion, five phases can be depicted.

where

$$E_{em,e} = E_i - KT\ln\left(v_{th}n_i\sigma_n t_{em,e}\right) \;\; E_{em,h} = E_i + KT\ln\left(v_{th}n_i\sigma_p t_{em,h}\right), \tag{II.2}$$

and

$$t_{em,e} = \frac{\left|V_{th} - V_{fb}\right|}{\Delta V_G} t_f \; , \; t_{em,h} = \frac{\left|V_{th} - V_{fb}\right|}{\Delta V_G} t_r \tag{II.3}$$

Hence, the scanned energy window writes:

$$\Delta E = E_{em,h} - E_{em,e} = 2KT\ln\left(v_{th}n_i \frac{\left|V_{th} - V_{fb}\right|}{\Delta V_G} \sqrt{\sigma_n\sigma_p}\sqrt{t_f t_r} \right) \tag{II.4}$$

where f is the frequency, A_G is the gate area, D_{it} is the surface density of the interface trap (cm^{-2} eV^{-1}). $E_{em,e}$, $E_{em,h}$, and E_i are the electron emission energy level, the hole emission energy level, and the intrinsic energy level, respectively. v_{th}, σ_n, σ_n, n_i, V_{fb}, V_{th}, and ΔV_G, are the thermal velocity, electron capture cross section, hole capture cross section, intrinsic carrier density, flatband voltage, threshold voltage, and pulse amplitude, respectively.

The threshold voltage and flatband voltage can be extracted from charge pumping curve of **Fig. II.2** using the following relations:

$$V_{th} = V_H - \Delta V_G \text{ and } V_{fb} = V_H \quad \text{(II.5)}$$

II.2.2- Trap profiling by charge-pumping technique

Besides its capability to study the interface traps, charge pumping technique, through multi-frequency variant, it can be used to characterize the depth profiling of the bulk trap density. In fact, some authors have proposed to evaluate the depth profile of border traps situated in the SiO_2 gate oxide **[135,136]** and High-k gate dielectric **[137,138]** of MOS transistors. Fixing the pulse amplitude around threshold and flatband voltages and varing the frequency allows charging and discharging traps located farther away from the Si/SiO_2 interface. For simplicity, we consider the filling probability, ΔF equal 1, the maximum CP-current can be defined as:

$$I_{CP} = qA_G f.\left[\int_{E_{em,e}}^{E_{em,h}} D_{it}(E)dE + \int_{Z_{min}}^{Z_{max}}\int_{E_{inv}}^{E_{acc}} n_T(E,Z)dEdZ\right] \quad \text{(II.6)}$$

where E_{inv} and E_{acc} are the lower and the upper energy bounds of the examined CP measurement, respectively. n_T is the volume density of the oxide traps ($cm^{-3}.eV^{-1}$). The maximum tunneling distance Z_{max} is the maximum depth in the gate oxide from the Si/SiO_2 interface that can be probed at a given CP frequency. The lower limit Z_{min} is the minimum distance from which near interfacial oxide traps are discernible from interface trap **[136]**.

Applying fixed square pulses at $V_H > V_{fb} > V_{th} > V_L$ (see **Fig. II.3**) with constant fall and rise times, **Eq. (II.6)** can be written as:

$$I_{CP} = qA_G f.\left[D_{it}(E)\Delta E + \Delta E^* \int_{Z_{min}}^{Z_{max}} n_T(E,Z)dZ\right] \quad \text{(II.7)}$$

By differentiating **Eq. (II.7)** with respect to Z, we can easily obtain:

$$n_T(E,Z) = \frac{1}{qA_G f\Delta E^*}\frac{dI_{CP}}{dZ} = \frac{1}{\Delta E^*}\frac{dN_T}{dZ} \quad \text{(II.8)}$$

ΔE^* is the band energy scanned in the oxide between inversion and accumulation regimes. As illustrated in **Fig. II.4**, traps outside this band cannot contribute to the current as the trapped charge becomes de-trapped instantly through thermal emission when the Fermi-level moves beyond the trap level for trapped electrons, or above the trap level for trapped holes. By introducing the spatial dependence of electron (hole) emission energy level, ΔE^* can be determined as described below in section **§ II.2.2.1**.

II.2.2.1- Trap depth and energy Profiling

During inversion of p-channel MOS transistors, holes fill not only the traps at the interface, but also traps with an energy higher than the Fermi level in inversion and located few angstroms within the

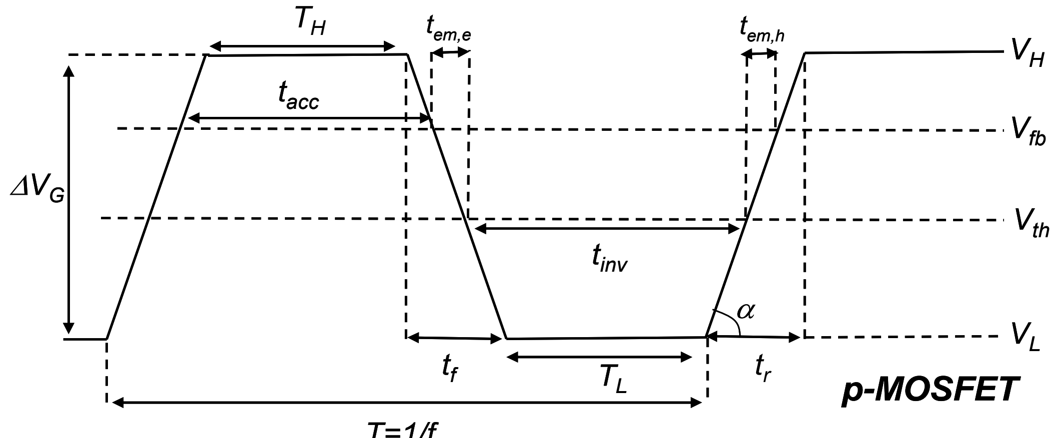


Figure II.3: Gate voltage signal. The signal is characterized by the amplitude (ΔV_G), the rise time (t_r) and fall time (t_f). t_{acc} and t_{inv} times correspond to electrons and holes capture times in p-MOS transistors. The emission times for electrons and holes are $t_{em,e}$ and $t_{em,h}$, respectively. α is the rising and falling slope.

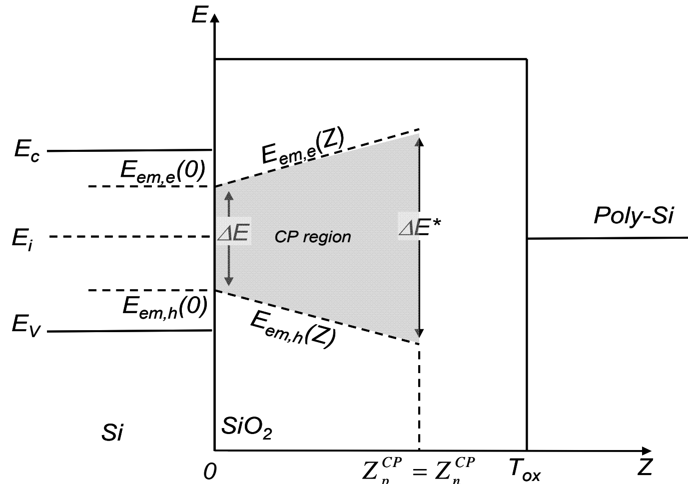


Figure II.4: Illustration of the energy and depth regions sensed by charge pumping technique during the fixed amplitude (ΔV_G) around V_{fb}-V_{th} and varied frequency. $E_{em,e}(0)$ and $E_{em.h}(0)$ are emission energy level of electrons and holes at the interface, respectively. $E_{em,e}(Z)$ and $E_{em.h}Z)$ are emission energy levels as a function of depth for electrons and holes into the oxide, respectively.

oxide. The maximum penetration depth, reached by the holes during the inversion phase of the gate signal, defines the location of the hole capture. During accumulation, electrons of p-MOSFET fill traps lower than the Fermi level. To resolve the dependence of defects on the distance, the effective capture cross section model developed by Heiman and Warfield **[139]** is used. In this model, the effective capture cross sections for holes and electrons exponentially decrease with increasing distance from the interface as:

$$\sigma_{n(p)}(Z) = \sigma_{n(p)}(0) e^{-Z/\lambda_{n(p)}} \qquad \text{(II.9)}$$

where $\sigma_{n(p})(0)$ is the capture cross section for electrons (holes) at the interface, and $\lambda_{n(p)}$ is the attenuation coefficient for electrons (holes), which is defined as:

$$\lambda_{n(p)} = \frac{\hbar}{2\sqrt{2 m_{n(p)} \phi_{n(p)}}} \qquad \text{(II.10)}$$

where $m_{n(p)}$ and $\phi_{n(p)}$ are the effective mass of electrons (holes) in the dielectric and the Si-dielectric barrier height for electrons (holes), respectively.

As charge pumping is dominated by capture processes in inversion and accumulation period, the capture rate $c_{n(p)}$ of electrons (holes) for traps at position *Z* can be defined as:

$$c_{n(p)}\left(Z\right) = n_s\left(p_s\right)v_{th}\sigma_{n(p)}\left(Z\right) = 1/t_{acc(inv)} \tag{II.11}$$

where $n_s\left(p_s\right)$ is the surface concentration of electrons (holes) during accumulation and inversion for p-MOS transistor. $t_{acc(inv)}$ is the accumulation (inversion) time of electrons (holes) in p-MOSFET, as illustrated by **Fig. II.3**. v_{th} is the thermal velocity.

Using **Eqs. (II.9)-(II.11)**, the maximum CP tunneling depth ($Z_{n(p)}^{CP}$), reached by the accumulation and inversion carriers, can be estimated as:

$$Z_{n(p)}^{CP} = \frac{\hbar}{2\sqrt{2m_{n(p)}\varphi_{n(p)}}}\ln\left[\sigma_{n(p)}\left(0\right)v_{th}n_s\left(p_s\right)t_{acc(inv)}\right] \tag{II.12}$$

Since the recombination occurs when both types of carriers are captured by the same trap, the maximum depth is defined by the carrier type that has the minimum tunneling distance in the oxide. Example, in the case $Z_n^{CP} > Z_p^{CP}$, the maximum depth in the oxide for CP is Z_p^{CP} and vice versa **[135]**.

The time during inversion, calculated as a function of signal parameters (see **Fig. II.3)**, is:

$$t_{inv} = \frac{1}{2f} + \left(2\frac{\left|V_{th} - V_L\right|}{\Delta V_G} - 1\right)\cdot t_f \tag{II.13}$$

Substituting **Eqs. (II.12) and (II.13) in Eq. (II.8)**, we find:

$$n_T = \frac{1}{\Delta E^*}\frac{\Delta N_T}{\Delta Z_p^{CP}} = -\frac{1}{qA_G f\lambda\Delta E^*}\frac{\Delta I_{CP}}{\Delta \ln f} \tag{II.14}$$

During the inversion period, all the traps having energy higher than the Fermi level and located at $Z < Z_p^{CP}$ are filled by holes. When the gate bias is reversed, bringing the device into depletion, some of the traps lose holes by emission. Only those traps with energy higher than $E_{inv} = E_{em,h}\left(Z\right)$ and holding the captured holes until the accumulation phase may contribute to the CP-current. Such traps have a hole emission time constant longer than the transition time from inversion to accumulation. Similarly, the electrons reach a distance from interface into the oxide during the accumulation. Only traps having energy lower than $E_{acc} = E_{em,e}\left(Z\right)$ and located at $Z < Z_n^{CP}$ remain filled by electrons until the arrival of the inversion holes that contribute to CP-current. Taking $t_{em,h} = t_{em,e}$ and $Z^{CP} = Z_p^{CP} = Z_n^{CP}$, we schematize in **Fig. II.4** the energetic band and depth regions, where CP-

current is probed from the interface to a given distance Z^{CP} into the oxide. By introducing spatial dependence of electron (hole) emission energy, through the capture cross section, $E_{em,e(h)}(Z)$ writes:

$$E_{em,e(h)}(Z) = E_i \mp KT \ln\left(v_{th} n_i \sigma_{n(p)}(Z) t_{em,e(h)}\right) \quad \text{(II.15)}$$

Substituting **Eq. (II.9) in Eq. (II.15)** yields:

$$E_{em,e(h)}(Z) = E_i \mp KT \left[\ln\left(v_{th} n_i \sigma_{n(p)}(0) t_{em,e(h)}\right) - \frac{Z_{n(p)}^{CP}}{\lambda_{n(p)}} \right] \quad \text{(II.16)}$$

Combining **Eqs (II.12) and (II.16**), we can write:

$$\Delta E^*(Z) = E_{em,e}(Z) - E_{em,h}(Z) = 2KT \left[\ln \frac{\sqrt{n_s \cdot p_s}\sqrt{t_{acc} \cdot t_{inv}}}{n_i \sqrt{t_{em,h} \cdot t_{em,e}}} \right] \quad \text{(II.17)}$$

II.2.2.2- Trap horizontal profiling

As illustrated in **Fig. II.1**, V_R is the reverse voltage applied onto the source and drain terminals. When V_R increases, the depletion region at source/substrate and drain/substrate junctions increases toward to the middle of the channel **[56]**. As a result, the effective channel length (L_{eff}) decreases permitting CP-current measurement from a small area. Therefore, the V_R-interface trap profiling consists of reducing the contribution of the channel length to the CP-current by increasing the depletion area. Channel length dependence of I_{CP} current can be expressed as follows:

$$I_{CP} = qN_{it} f \, . \, W_G \, . \, L_{eff} \quad \text{(II.18)}$$

where L_{eff} is given by:

$$L_{eff} = L_G - 2\Delta L - 2\sqrt{\frac{2\varepsilon_{si}}{qN_D}\left(2\phi_F(T) - V_R\right)} \quad \text{(II.19)}$$

It is clear that when V_R is gradually increased in absolute value (V_R is negative in the case of p-MOSFET), the area participating to CP-current decreases accordingly, which permits to profile the interface trap along the channel length. So, combining **Eqs. II.18 and II.19**, δN_{it} for each small area $W \cdot \delta L_{eff}$ in the channel can be written as:

$$\delta N_{it} = \frac{\delta I_{CP}}{2qWf\sqrt{\frac{2\varepsilon_{si}}{qN_D}}\left(\sqrt{2\phi_F - V_{R2}} - \sqrt{2\phi_F - V_{R1}}\right)} \quad \text{(II.20)}$$

where $V_{R1} < V_{R2}$. δI_{CP} (A) and δN_{it} (cm^{-2}) correspond to CP-current and interface-trap density of $W_G \cdot \delta L_{eff}$ area, respectively. q (C) is the electron charge, L_G (μm) is the designed gate length, L_{eff} (μm) is the effective channel length, ΔL (μm) is the LDD overlap, W (μm) is the gate width, ε_{Si} ($F.cm^{-1}$)

is the permittivity of the Silicon, N_D (cm^{-3}) is the substrate doping, ϕ_F (V) is the Fermi level, V_R (V) is the reverse voltage, f (Hz) is the frequency.

II.3- Transistor Drain Current for Different Modes

II.3.1- Drain current in linear mode

We recall that the drain current is proportional to the mobile charge of the inversion layer (Q_{inv}) and to the electron transit time from source to drain (τ). To create the inversion layer, the gate voltage has to reach the threshold voltage (V_{th}). The transit time is the ratio of channel length (L_G) and the electron velocity (v_e):

$$I_{DS} = \frac{Q_{inv}}{\tau} \tag{II.21}$$

where Q_{inv} and τ are given by:

$$Q_{inv} = C_{OX} W_G L_G (V_{GS} - V_{th}) \tag{II.22}$$

$$\tau = \frac{L_G}{v_e} = \frac{L_G}{\mu_{eff} E_L} = \frac{L_G}{\mu_{eff} \frac{V_{DS}}{L_G}} \tag{II.23}$$

Substituting **Eqs (II.22) and (II.23) in Eq. (II.21)** yields:

$$I_{DS} = \frac{\mu_{eff} C_{OX} W_G}{L_G} (V_{GS} - V_{th}) V_{DS} \tag{II.24}$$

where μ_{eff} (cm^2/ V.s) is the carrier mobility, C_{OX} (F/cm^2) is the oxide capacitance, E_L (V/cm) is the lateral electric field, V_{GS} (V) is the gate/source voltage, V_{DS} (V) is the drain/source voltage, L_G (cm) is the gate length, and W_G (cm) is the gate width.

Eq. (II.24) describes drain current in linear region (for $V_{DS} << V_{GS}-V_{th}$) as well as for negligible body effect **[93]**. It is given for p-MOS transistor in the mobility-dominated regime, while in the velocity saturation limited regime, it follows:

$$I_{DS} = \frac{C_{OX} W_G}{L_G} \frac{\mu_{eff}}{1 + \mu_{eff} \frac{V_{DS}}{L_G v_{sat}}} (V_{GS} - V_{th}) V_{DS} \tag{II.25}$$

The effective mobility, μ_{eff} is given by:

$$\mu_{eff} = \frac{\mu_0}{1 + \theta (V_{GS} - V_{th})} \tag{II.26}$$

where μ_0 is the low vertical electric field mobility, θ the mobility degradation factor due to vertical electric field, and v_{sat} the saturation velocity. All voltages are negative for p-channel MOSFETs and given as absolute values.

II.3.2- Drain current in saturation mode

In the case where $V_{DS} >> V_{GS}-V_{th}$, the drain current saturates and **Eq. (II.24**) becomes:

$$I_{DS} = \frac{\mu_{eff} C_{OX} W_G}{2L_G} \left(V_{GS} - V_{th}\right)^2 \quad \text{(II.27)}$$

II.3.3- Drain current in subthreshold mode

The drain current of MOSFET at gate voltage below the threshold voltage corresponds to weak inversion regime, i.e. $V_{GS} < V_{th}$. This current is induced by the diffusion of the carriers and it is given for long channel transistor as:

$$I_{DS} = \frac{\mu_{eff} C_{OX} W_G}{L_G} \phi_t^2 \exp\left(\frac{V_{GS} - V_{th}}{n\phi_t}\right)\left(1 - \exp - \frac{V_{DS}}{\phi_t}\right) \quad \text{(II.28)}$$

where

$\phi_t = \frac{KT}{q}$ and $n = 1 + \frac{C_{Dep}}{C_{OX}}$, C_{Dep} is the capacitance of the depletion layer and n is the ideality factor. It accounts for the charge placed on the gate that does not result in inversion layer charge. Some gate charges are imaged as space-charge region charge and some as interface trap charge. Typically, n equal 1.

II.4- Classical Measure-Stress-Measure (MSM)

The classical MSM procedure is illustrated in **Fig. II.5**. Conventionally, V_{th} degradation is typically evaluated by measuring I_{DS}-V_{GS} characteristics after stress interruption. In this procedure, full I_{DS}-V_{GS} characteristics are performed either in linear regime or saturation regime and all relevant transistor degradation parameters can be extracted. An example of I_{DS}-V_{GS} and g_m-V_{GS} characteristics of transistors used in this work is given in **Fig. II.6** after NBTI stresses using the classical MSM protocol. The NBTI impact is clearly shown on both I_{DS}-V_{GS} and g_m-V_{GS} characteristics. The most important parameters of the transistor are degraded, such as increasing absolute value of the threshold voltage (V_{th}), decreasing the maximum transconductance (g_m) (defined as $dI_{D,lin}/dV_{Gs}$ at fixed V_{DS}), decreasing channel mobility (μ_{eff}), decreasing linear drain current ($I_{D,lin}$), saturation current ($I_{D,sat}$), increasing off current (I_{off}), and decreasing subthreshold slope (S).

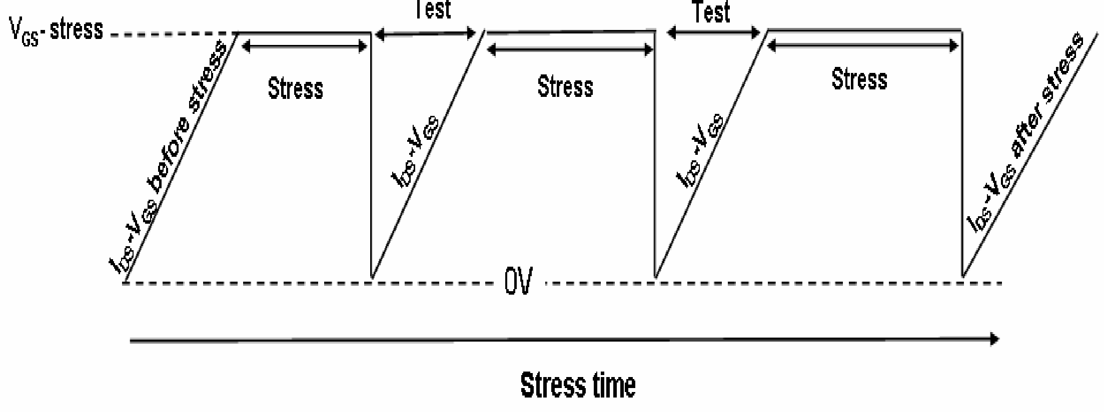


Figure II.5: Illustrative schematic of gate-source voltage cycle of full I_{DS}-V_{GS} characteristics measurement for NBTI characterization. Note that the drain can either be biased in the linear regime or saturation regime during the measurement.

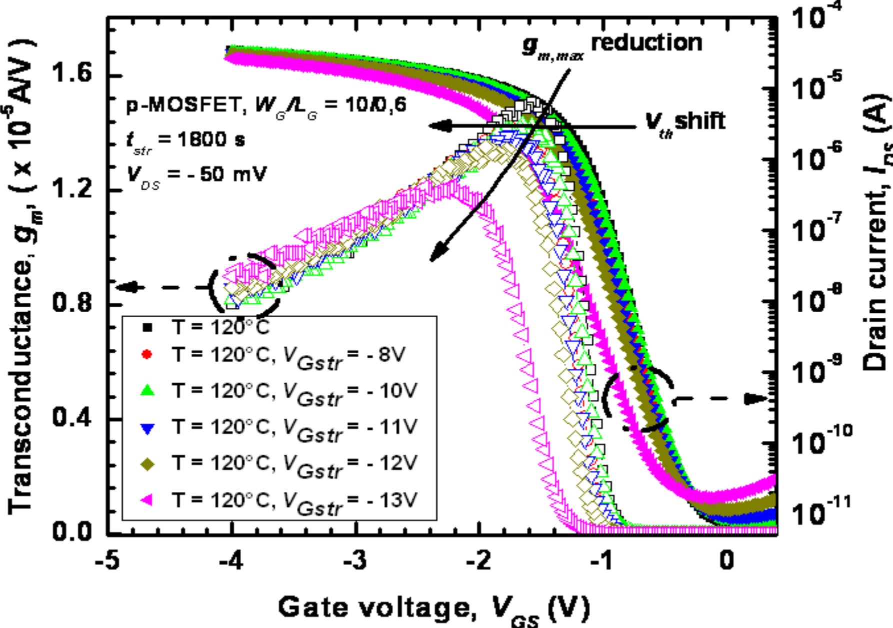


Figure II.6: Transfer characteristics plotted in logarithmic-scale (right ordinate axis) and transconductance (left ordinate axis). Both maximum of g_m and V_{th} are degraded after 1800 s (30 min) of NBTI stress for different stress temperatures and voltages.

However, the classical MSM cycle is time consuming taking several minutes to achieve, which induces recovery effect. In order to avoid unintentional recovery during measurement, Rangan et *al.* **[103]** have changed the I_{DS}-V_{GS} measurement by lowering gate voltage to a constant value V_{GS} around V_{th} to perform just a single drain current measurement. During the monitoring of the linear drain current (I_{Dlin}), V_{DS} is kept at 50mV, as shown on **Fig. II.7 (a).** Doing so, the measurement delay during intermittent characterization is reduced. After each stress time step, the gate voltage switches from the stress level to the sense voltage level and the linear drain current is measured before the gate voltage switches back to the stress level. The measured current is translated to V_{th} shift.

II.5- Parameter Extraction of MSM Methods

II.5.1- Measure around V_{th} methods

After stress, any change in drain current can be linked to threshold voltage. Hence, the fractional change of drain current due to voltage change is given by:

$$\frac{\Delta I_{Dlin}}{I_{Dlin0}} = -\frac{\Delta V_{th}}{V_{GS} - V_{th0}} \Rightarrow \Delta V_{th} = -(V_{GS} - V_{th0})\frac{\Delta I_{Dlin}}{I_{Dlin0}} \tag{II.29}$$

for MOSFET in linear regime and

$$\frac{\Delta I_{Dsat}}{I_{Dsat0}} = -2\frac{\Delta V_{th}}{V_{GS} - V_{th0}} \Rightarrow \Delta V_{th} = -2(V_{GS} - V_{th0})\frac{\Delta I_{Dsat}}{I_{Dsat0}} \tag{II.30}$$

in saturation regime. Where V_{th0} is the unstressed threshold voltage (neglecting any change in mobility). The degradation in saturation regime is two times greater than that in linear regime, as observed experimentally **[140]**.

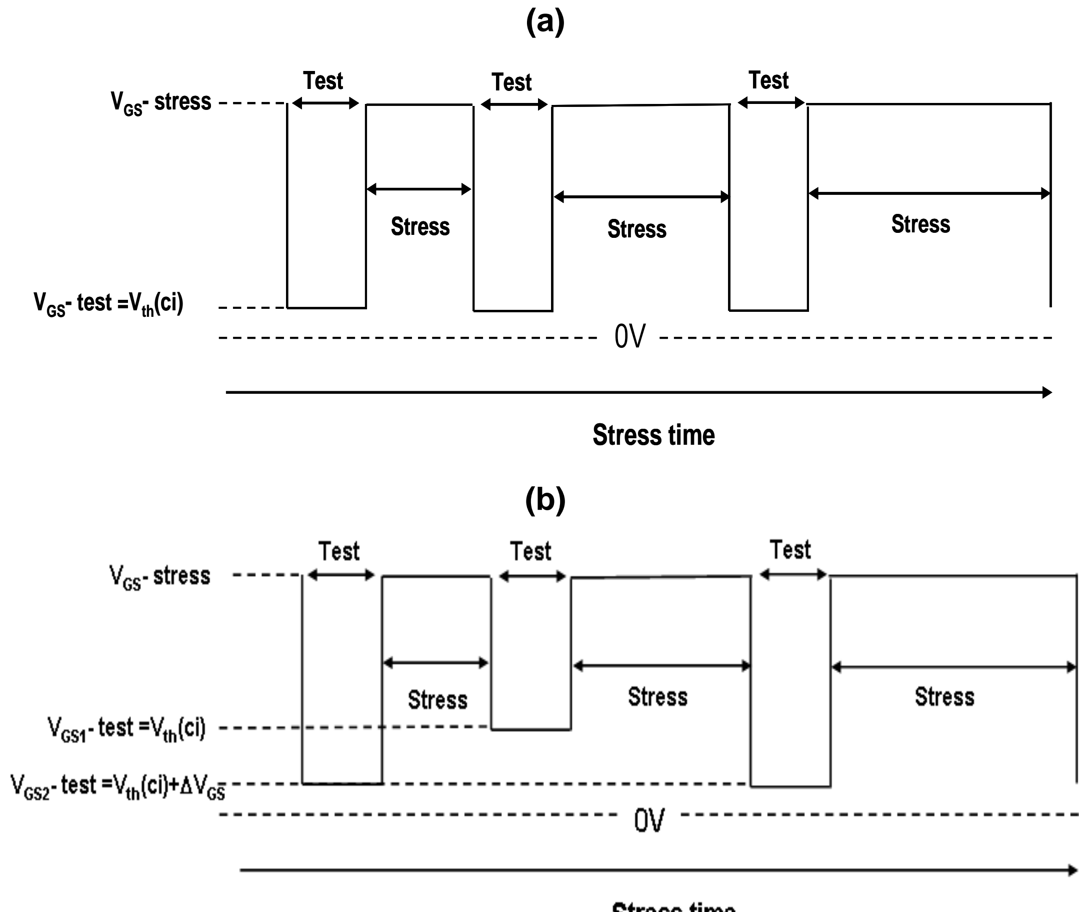


Figure II.7: Schematic of V_{GS} switching to measure (a) single linear current drain around threshold voltage and (b) two point measurements at V_{GS1} and V_{GS2}.

In this procedure, the stress is interrupted for a while to get I_{Dlin} around V_{th}, which induces measurement delay and therefore a significant recovery of threshold voltage shift ΔV_{th}. This limits the use of direct ΔV_{th} as a monitoring parameter.

II.5.2- Subthreshold Swing (SS) method

The usual parameter used at that regime is the subthreshold swing (SS), which is the inverse of the plot log(I_{DS}) versus V_{GS} slope (S) of **Eq. (II.28),** given by:

$$SS = \frac{1}{S} = \frac{dV_{GS}}{d\log\left(I_{DS}\right)} = \frac{\ln\left(10\right)nKT}{q} \text{ (V/decade)} \qquad \text{(II.31)}$$

During NBTI stress, the V_{DS} is typically about 50mV. After each stress time, V_{GS} is reduced to a fixed test value that is equal to the initial V_{th0} [see **Fig. II.7 (a)**], and the drain current $I_{DS}(t_{Str})$ is measured. V_{th} degradation with stress time (t_{Str}) is determined using:

$$\Delta V_{th} = SS_0 \log\left(\frac{I_{DS0}}{I_{DS}}\right) \qquad \text{(II.32)}$$

I_{DS0} is the initial drain current at V_{th0}. **Eq. (II.32)** is derived assuming that SS_0 is constant during stress. In **Fig. II.8**, we illustrate the NBTI effect on the subthreshold I_{DS}-V_{GS} characteristics as well as subthreshold swing extracted from our devices. The curves show pre- and post-NBTI stress of p-MOS transistor stressed for 1 hour at 100 °C and -13 V. V_{th} increases in absolute value at constant current

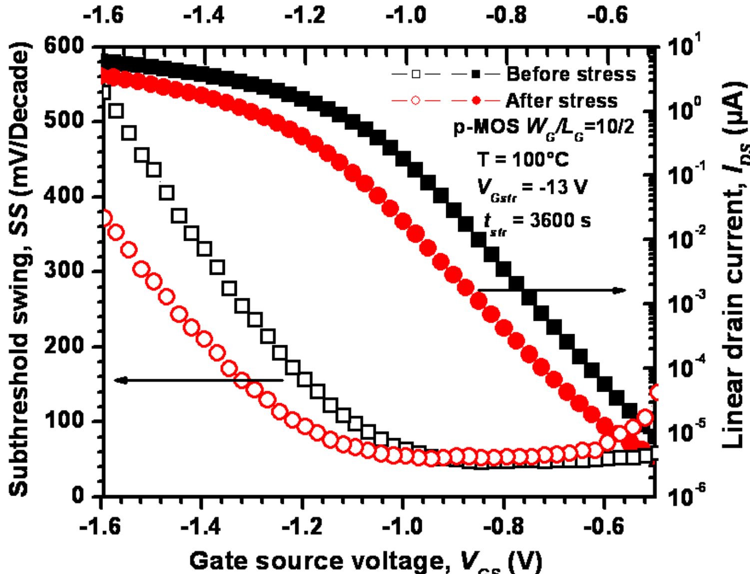


Figure II.8: Pre- and post-NBTI stress of drain current, I_{DS} (right ordinate axis) and subthreshold swing, *SS* (left ordinate axis) performed on our devices. Results show V_{th} increase at constant current (~1µA) and SS decrease (improve) in p-MOS transistor.

(~1µA) and *SS* decreases (improves). Moreover, it is clear that SS is not constant with respect to V_{GS} during stress, as assumed by **Eq. (II.32)**, but decreases with decreased V_{GS}. Indeed, it has been pointed out that assuming SS_0 constant may not be valid **[127,141,142]**. Therefore, ΔV_{th} determined by the standard technique (JEDEC) **[143]** may be incorrect.

Unfortunately, making multiple I_{DS} measurements to extract the actual *SS* after any stress time interval is not accurate because of NBTI relaxation. In order to obtain the variation of SS with stress, several options are possible. Brisbin et *al.* **[144]** have proposed to measure I_D currents at two different V_{GS} values. The latter are applied by alternating stress intervals, as shown in **Fig. II.7 (b)**. The first point is V_{GS1} taken at V_{th0}, while the second one is V_{GS2} taken at V_{th0} + 50 mV. The incremented degradation of V_{th} is calculated using:

$$\Delta V_{th}\left(t_{str}\right) = SS\left(t_{str}\right) * \log\left(\frac{I_D\left(t_{strprev}\right)}{I_D\left(t_{str}\right)}\right) \tag{II.33}$$

where $I_D(t_{strprev})$ is the measured I_D at the previous stress time for V_{GS1} and $SS(t_{str})$ is determined for each stress time using :

$$SS\left(t_{str}\right) = \frac{\Delta V_{GS}}{\log\left(\frac{I_{D1}\left(t_{str}\right)}{I_{D2}\left(t_{str}\right)}\right)} \tag{II.34}$$

where I_{D1} (t_{str}) and I_{D2} (t_{str}) are the measured and interpolated I_D values at stress time (t_{str}), respectively. However, in this method, $SS(t_{str})$ is considered the same in $I_D(t_{strprev})$ and I_D (t_{str}). The second option is described below in section **§ II.5.3**.

II.5.3- ΔV_{th} and ΔSS extraction

Considering $SS_1 \neq SS_0$ and using **Eq. (II.28)**, we can write:

$$\log\left(I^1_{DS1}\right) - \log\left(I^1_{DS0}\right) = \frac{V_{GS1} - V_{th1}}{SS_1} - \frac{V_{GS1} - V_{th0}}{SS_0} \tag{II.35}$$

where I^1_{DS0} and I^1_{DS1} are currents measured at V_{GS1} before and after stress, respectively. In the case of $SS_1 = SS_0$, we find **Eq. (II.32).**

Since $V_{th1} = V_{th0} + \Delta V_{th}$, **Eq. (II.35)** yields:

$$\frac{SS_0 \log\left(I^1_{DS1} / I^1_{DS0}\right)}{V_{GS1} - V_{th0}} = \frac{SS_0}{SS_1}\left(1 - \frac{\Delta V_{th}}{V_{GS1} - V_{th0}}\right) - 1 \quad \text{(II.36)}$$

Therefore, ΔV_{th} is obtained as:

$$\Delta V_{th} = \left[1 - \frac{SS_1}{SS_0}\left(\frac{SS_0 \log\left(I^1_{DS1} / I^1_{DS0}\right)}{V_{GS1} - V_{th0}} + 1\right)\right]\left(V_{GS1} - V_{th0}\right) \quad \text{(II.37)}$$

Using $SS_1 = \Delta SS + SS_0$ in **Eq. (II.37)**, ΔV_{th} writes:

$$\Delta V_{th} = \left[1 - \left(\frac{\Delta SS}{SS_0} + 1\right)\left(\frac{SS_0 \log\left(I^1_{DS1} / I^1_{DS0}\right)}{V_{GS1} - V_{th0}} + 1\right)\right]\left(V_{GS1} - V_{th0}\right) \quad \text{(II.38)}$$

On the other side, *SS₁ and SS₀* are given by:

$SS_1 = \Delta V_{GS} / \log\left(I^1_{DS1} / I^2_{DS1}\right)$ and $SS_0 = \Delta V_{GS} / \log\left(I^1_{DS0} / I^2_{DS0}\right)$, respectively.

Then ΔSS is as follows:

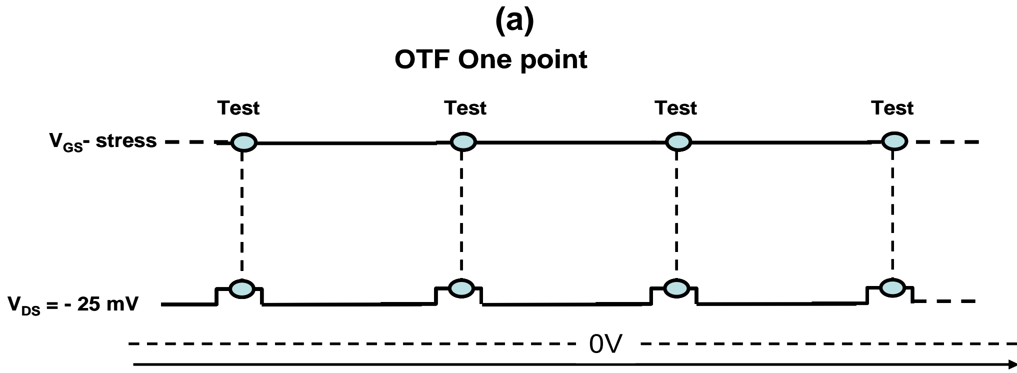
$$\Delta SS = SS_0\left(\frac{\log\left(I^1_{DS0} / I^2_{DS0}\right)}{\log\left(I^1_{DS1} / I^2_{DS1}\right)}\right) \quad \text{(II.39)}$$

$$\Delta V_{th} = \left[1 - \left(\left(\frac{\log\left(I^1_{DS0} / I^2_{DS0}\right)}{\log\left(I^1_{DS1} / I^2_{DS1}\right)}\right) + 1\right)\left(\frac{SS_0 \log\left(I^1_{DS1} / I^1_{DS0}\right)}{V_{GS1} - V_{th0}} + 1\right)\right]\left(V_{GS1} - V_{th0}\right) \quad \text{(II.40)}$$

The *SS*-based methods face the same recovery issue as V_{th} measure (due to stress interruption), described in section **§ II.5.1**. That is why, the need for alternative methods becomes mandatory to capture the actual NBTI degradation. Some of these methods are explored in the following sections.

II.6- On The Fly V_{th} (OTF-V_{th}) Methods

The OTF measure/stress/measure methodology was introduced for the first time by Denais and Huard **[22,57]**. The main objective of this approach it to capture the total device degradation activated during the NBTI stress. This is accomplished by monitoring the linear drain current (I_{Dlin}) without interrupting the NBTI stress (no delays) for the whole duration of the experiment. The applied V_{DS} is small enough to not disturb the gate oxide field at a given V_{Gstr} along the channel. By applying a small V_{DS}, it is then possible to monitor the degradation of the linear drain current I_{Dlin} without any unintentional recovery [see **Fig. II.9 (a)**]. This approach, referred to as one point OTF, fulfils the limitation that no recovery occurs during the stress/measurement phase, because the stress is never interrupted. But it is not fully satisfying since only one device parameter is accessible. Since the current depends on threshold voltage, mobility and other device parameters, it is not possible to



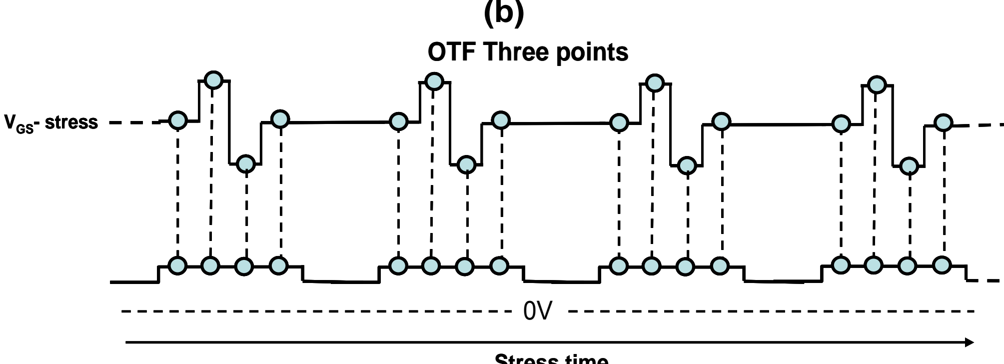


Figure II.9: On the fly protocol of V_{GS} switching to measure (a) one point I_{DS} current (b) three points I_{DS} current. V_{DS} voltage can be set at 25mV only during the pulse measurement or set at 25 mV for whole stress/ measure cycle. The fourth point in (b) is used to check if the added pulse induces recovery.

accurately extract ΔV_{th}. Therefore, an alternative method, named three points OTF, was proposed as shown in **Fig. II.9 (b).** In this method, small gate pulse voltage around the DC gate stress voltage is required for every time measurement. By this way, not only ΔV_{th} at stress voltage is measured but also the transconductance degradation (Δg_m).

II.6.1- One point on the fly method

Assuming mobility constant during stress, the change in drain current can, compared to the unstressed (I_{Dlin0}), be extrapolated to ΔV_{th} using **Eq. (II.29)**, which is given in section **§II.5.1**. This is an approximation since we know that traps generated during NBTI stress degrade the mobility by introducing scattering centers. Moreover, the mobility dependence on gate voltage decreases at higher gate voltages. The mobility dependence can be eliminated by measuring the transconductance, as shown in the following section **§ II.6.2**.

II.6.2- Three points on the fly method

To take account for mobility variation, resulting from traps creation and also from enhanced scattering of the inversion carriers at the dielectric/semiconductor interface **[63]**, the three points OTF method was proposed **[57,129]**. The MSM protocol is illustrated in **Fig. II.9 (b).** The fourth point measurement is performed to show that the added gate pulse does not introduce any relaxation. In fact, **Fig. II.10** shows the four points, I_{D1}, I_{D2}, I_{D3}, and I_{D4} measured at V_{Gstr} measured on our transistors

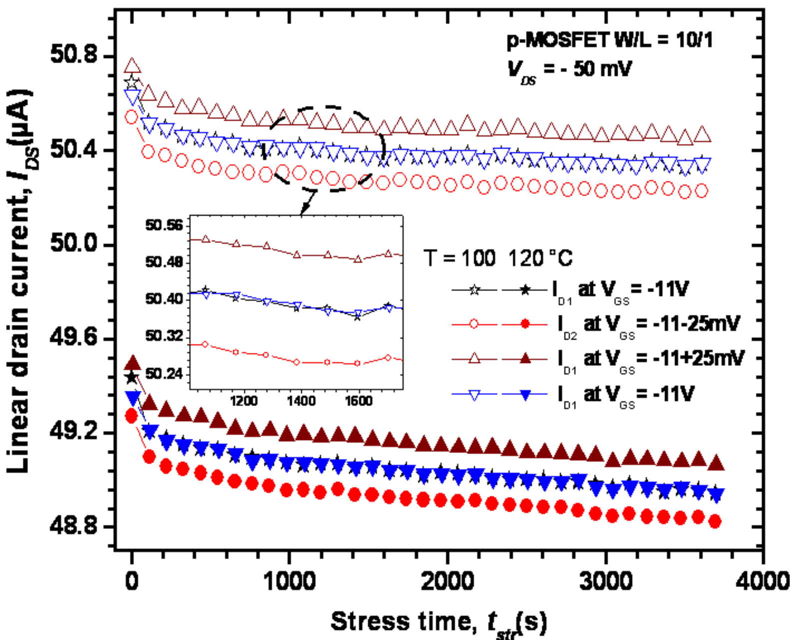


Figure II.10: On the fly three points measured as a function of stress time at stress voltage of – 11V and stress temperature of 100 °C and 120 °C. The first and the fourth points are roughly the same indicating that the gate pulse does not cause any relaxation.

during and after gate pulse, respectively. I_{D4} is identical to I_{D1} indicating no difference between before and after V_G pulses, subsequently no relaxation during pulse measurement **[129]**.

In mobility-dominated regime, g_m can easily be deduced, from **Eq. (II.24)** and taking account of **Eq. (II.26)**, as follows:

$$g_m = \frac{dI_{DS}}{dV_{GS}} = \frac{C_{OX}W_G}{L_G}\frac{\mu_0}{\left[1+\theta(V_{GS}-V_{th}\right]^2}V_{DS} \tag{II.41}$$

then,

$$\frac{I_{DS}}{\sqrt{g_m}} = \sqrt{\frac{C_{OX}W_G}{L_G}\mu_0 V_{DS}}(V_{GS}-V_{th}) \tag{II.42}$$

In velocity saturation limited regime, g_m can be obtained, using **Eqs (II.24), (II.25), and (II.26)**, as:

$$g_m = \frac{C_{OX}W_G}{L_G}\frac{\mu_0(1+\mu_0 V_{DS}/L_G\upsilon_{sat})}{\left[1+\theta(V_{GS}-V_{th})+\mu_0 V_{DS}/L_G\upsilon_{sat}\right]^2}V_{DS} \tag{II.43}$$

then

$$\frac{I_{DS}}{\sqrt{g_m}} = \sqrt{\frac{C_{OX}W_G}{L_G}\mu_0 V_{DS}}\frac{V_{GS}-V_{th}}{\sqrt{1+\mu_0 V_{DS}/L_G\upsilon_{sat}}} \tag{II.44}$$

In **Eqs (II.42) and (II.44),** the mobility degradation factor, θ is eliminated, but they still hold the low field mobility, μ_0. The detailed extraction of μ_0 is given in **[22]**. For simplicity, we assume μ_0 constant with stress time in both cases (i.e. mobility-dominated regime and velocity saturation limited regime). This yields to ΔV_{th}:

$$\Delta V_{th} = \left(1 - \frac{I_1\sqrt{g_{m0}}}{I_0\sqrt{g_{m1}}}\right)\left(V_{GS} - V_{th0}\right) \quad \text{(II.46)}$$

where I_0, g_{m0}, V_{th0} (are extracted from virgin characteristics) $g_{m1} = (I_3 - I_2)/2V_P = \Delta I_P/2V_P$, and V_P is the pulse amplitude.

Compared to the classical MSM methods, the advantage of OTF methods is their delay-free between stress and measurement, because they do not interrupt stress (does only a modulation of the stress voltage in three points OTF) during measurement **[57,103,145]**. Nevertheless, OTF methods suffer from the delay inherent in the first measurement point. In fact, Shen et *al.* **[53]** pointed out that the initial I_{D0} influences the shape of the ΔV_{th} shift curve and strongly distorts the data, because it is extracted at stress phase, while the corresponding V_{th0} is measured using pre-stress standard I_{DS}-V_{GS}. More precisely the initial pre-stress measure of I_{D0} takes 10-100 ms with a typical setup on HP4156C during which some V_{th}. degradation occurs under the high gate voltage (V_{Gstr}). Therefore, the measured I_{D0} is lower than the actual value, thus the V_{th} shift after the subsequent stress is underestimated. To overcome this slow initial measurement, the pre-stress I_{D0} and V_{th0} are measured using the fast I_{DS}-V_{GS} technique **[146]** within 1µs to minimize I_{D0} degradation. The initial first value is obtained using special setup connected to digital scope (DSO), then after the setup is switched to parameter analyzer for OTF one point extraction. In contrast to standard (slow) OTF methods **[22,57,129]**, fast OTF method **[146,147]** cannot be performed with Agilent 4156C equipment and needs a special setup. Although, both slow and fast OTF are recovery free, their drawback is that the ΔV_{th} is determined at a gate voltage higher than operating voltage. Therefore some states could be occupied which are not occupied at operating voltage leading to a different ΔV_{th}. Moreover, these methods determine ΔV_{th} indirectly from an analysis of the change in the measured current by means of a mathematical equation of MOSFET model. Reisinger et *al.* **[148]** have proposed another setup to directly measure V_{th} (using constant current method) in operating conditions relevant in the circuit within 0.5 µs. This method is named “fast V_{th}” method. Its setup basically consists of a feedback loop forcing a constant current across source drain of the MOSFET under test by applying an appropriate gate voltage to the MOSFET. The operational amplifier tries to zero the difference between actual current and current set point (70nA*W/L, in their case). V_{th} is recorded after the setting time of the feedback loop, which is about 0.5 μs after stress.

Moreover, there are other types of measurement based on pulsed I_{DS}-V_{GS} methods **[53,146,149,150]**. The setup of pulsed I_{DS}-V_{GS} was originally developed by Kerber et *al.* **[149]** to extract the pre-existing defects in high-k insulator (SiO_2/HfO_2 dual layer stacks) and identify their charging impact on V_{th} instability and its measurement accuracy, they also studied the impact of various experimental conditions on the charge trapping in high-k insulator. The proposed setup allows measuring I_{DS}-V_{GS} in the microseconds to milliseconds time range (see details in **[149]**. Later, Shen et *al*. **[150]** have improved the measurement time of pulsed I_{DS}-V_{GS} to 1µs, and further it is reduced to 100 ns **[53,146]** to study NBTI degradation with minimum recovery.

All aforementioned methods either slow or fast are not able to distinguish and separate the interface and oxide traps in NBTI degradation. In order to differentiate between oxide and interface traps, specialized measurement techniques such as *C-P* and *DCIV* techniques are used **[56,128]**.

II.7- On The Fly Interface Trap (OTFIT)

Before OTFIT, the interface traps have been measured using *DCIV* **[128]** and the charge pumping **[56]** methods. In these methods, the stress has been interrupted during measurement inducing relaxation and error on the N_{it} measurement. In conventional CP (CCP), as illustrated by **Fig. II.11 (a)**, the stress voltage is interrupted during CP measurement. In that case, a significant relaxation may occur. Consequently, Lui et *al*. **[55]** have proposed On The Fly Interface Trap (OTFIT) method to measure the interface trap degradation without delay between stress and measurement.

The basic difference between CCP and OTFIT is that the low signal level is simultaneously used as a stress voltage condition (for NBTI). **Figure II.11 (b)** shows the schematic of measure/stress/measure of the OTFIT method. During stress phase, stress voltage is always on and to make measurement almost on the fly, the low voltage level of the gate pulse is set to stress voltage (V_L=V_{Gstr}), while high level is set at flatband voltage or above. In addition to stress phase, the gate bias and pulses used during relaxation measurement phase are also presented. However, the issue with OFIT method **[55]**

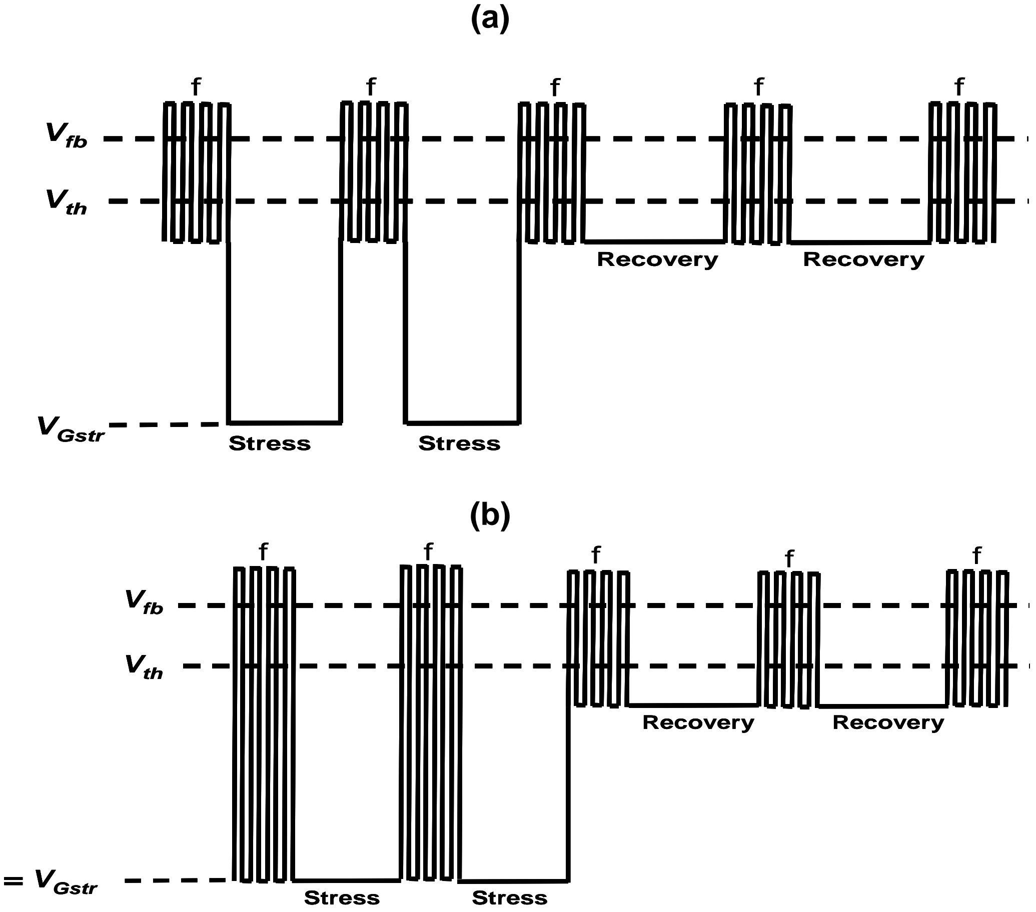


Figure II.11: Schematic stress and sense protocol of interface trap. It shows the time evolution of V_{GS} and pulses applied for CP measurements, including both stress and recovery phases. (a) Conventional CP measurements and (b) on the fly CP measurement.

is using different low signal levels during stress and relaxation, the later is taken as measurement reference. In fact, it has been shown **[117]** that increasing V_L induces additional charge contribution to I_{CP} current. This contribution is absent during the initial reference measurements and during the OFIT relaxation measurements both taken at $V_L = V_{relaxation}$. This has fundamental consequences on OFIT measurements. Indeed, much larger ΔV_G increases band energy of both interface and oxide traps contributing to CP-current. To overcome this issue, Djezzar et *al.* **[151]** have taken the first measured point at stress phase as reference point for a meaningful assessment of NBTI degradation, which will be presented later in **Chapter IV**.

II.8- Conclusion

In this **Chapter**, pros and cons of conventional and special measure/stress/measure (MSM) protocols for NBTI investigation have been reviewed. The mostly used method is I_{DS} point measurement methods to extract V_{th}, because they can be achieved rather easily with commercial measurement instrumentation with sense delay around 1 ms. Further efforts are being made to push the measurement delay below the µs time domain, but these fast measurements require tool upgrades.

The fast measurement methods are out of the scope of this thesis, because they are not implemented in our experimental setup based on Agilent 4156C equipment, on one hand, on the other hand, the commercial equipments (last generation of Agilent B1500A test parametric and Keithley 4200-SCS) integrating these fast methods are very expensive. Despite these ultra-rapid methods to capture the fast switching component, NBTI is still unclear and ambiguous. Finally, as we stated in **Chapter I**, we are interested by the permanent (or quasi permanent) component, which is the solely component affecting the circuits in working conditions.

CHAPTER III

EXPERIMENT DETAILS

III.1- Introduction

III.2- Devices and Process Details

III.3- Measurement Setup Details

III.4- Characterization before NBTI Stress

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CHAPTER III
EXPERIMENT DETAILS

III.1- Introduction

Part of this thesis concerns the different experimental setups used to carry out the bias temperature stress (BTS) experiments. These setups include *I-V*, *C-V*, and *C-P* based methods. The first section of this **Chapter** is aimed to describe the devices and their process. The second section is dedicated to the experiment as well as the instrumentation used for stress and test protocols. The third section deals with device test and characterization before NBTI stress at both ambient and high temperatures.

III.2- Devices and Process Details

The Device Under Test (DUT) used in this work are part of test structure chip provided by ISiT (Institut SiliziumTechnologie) of Fraunhofer, Germany in the framework of 1 µm CMOS technology platform (clean room) project at CDTA (ongoing project). The chips are duplicated on test wafer, named Process Evaluation Vehicle (PEV). **Figure III.1** shows a global view of the PEV wafer (a), Process And Reliability Evaluation Structures (PARES) chip (b), and the DUT (c). In addition to MOSFET and capacitor devices, the PARES includes resistors, diodes, inverters, ring-oscillators …etc.

The PEV was fabricated at ISiT using a conventional 1 µm-CMOS twin-well technology on p-type 12 µm-epi-layer on silicon <100> substrate with dual layer metal, Lightly Doped Drain (LDD) structure,

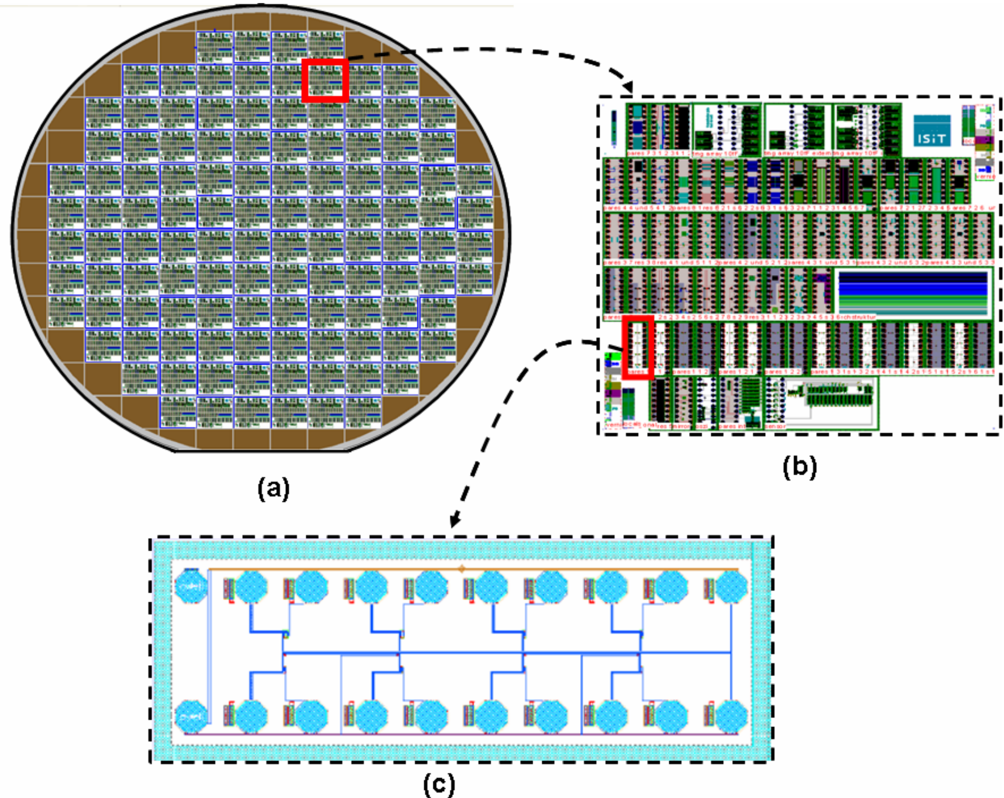


Figure III.1: (a) Process evaluation vehicle (PEV) wafer including duplicated test structure chip. (b) Layout process and reliability evaluation structures (PARES). (c) Layout of MOS transistor series.

and 20 nm thick gate oxide layer grown in dry O_2. The gate capacitance per unit area (C_{ox}) is about 2.12 x 10^{-7} F.cm^{-2}. More details on the main steps of the process and the technological parameters are given in **appendix (C.1)**. The investigated DUTs include two series of non-packaged n- and p-MOS transistors with gate length ranging from 0.5 to 10 µm and fixed gate width at 10 µm (see **Fig. III.2**). Moreover, characterization was also performed on p- and n-substrate MOS capacitors with area of 0.001 cm^2 [see **Fig. III.2 (b)**].

In the ISiT process, after low pressure chemical vapour deposition (LPCVD) of poly-silicon and phosphorous oxychloride ($POCL_3$) doping, the gate dimension was defined by reactive ion etching (RIE) using hydrogen bromide (HBr) with high selectivity with respect to gate oxide. The LDD regions were formed using conventional boron (B) implantation. The gate edges were covered using tetra-ethyl-ortho-silicate (TEOS) spacer deposited by LPCVD process. All devices were annealed at 925 °C in forming N_2/O_2 atmosphere for TEOS spacer densification. Finally, p-MOSFET source and drain were formed by BF_2 implantation.

III.3- Measurement Setup Details

All experiments were done at CDTA using above-mentioned non-packaged devices. In order to perform electrical tests, the probe station is used together with an alignment optical microscope to access the device and get electrical contacts with pads via probe micromanipulators. **Figure III.3** gives an overall view on the soft/hard platform used in this work. The electrical test benches are built around a Karl-Süss AP4 micro-manipulator probe station which is housed in a grounded Faraday box to avoid both RF and light effects. BNC connectors are mounted on the Faraday cage. The benches include:

- _Precision semiconductor parameter analyzer, model Agilent 4156C_: its measurement capabilities

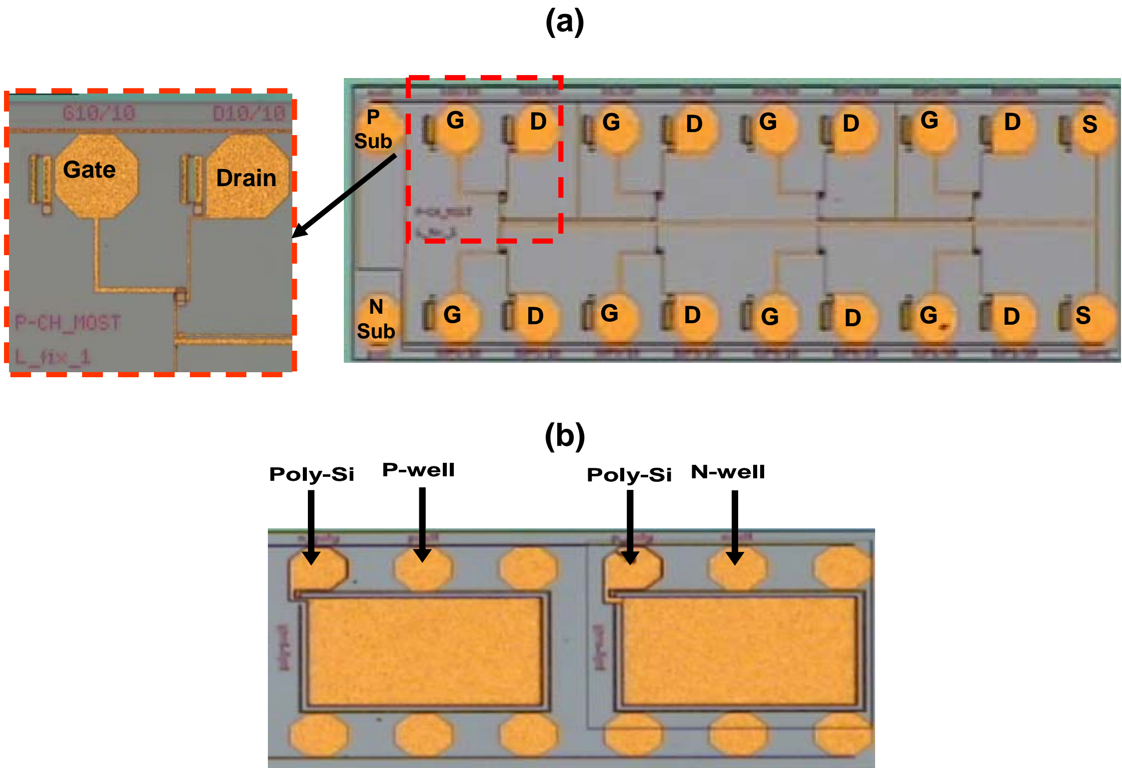


Figure III.2: Devices under test. (a) Battery of p-MOSFET devices. (b) p- and n-substrate MOS capacitors

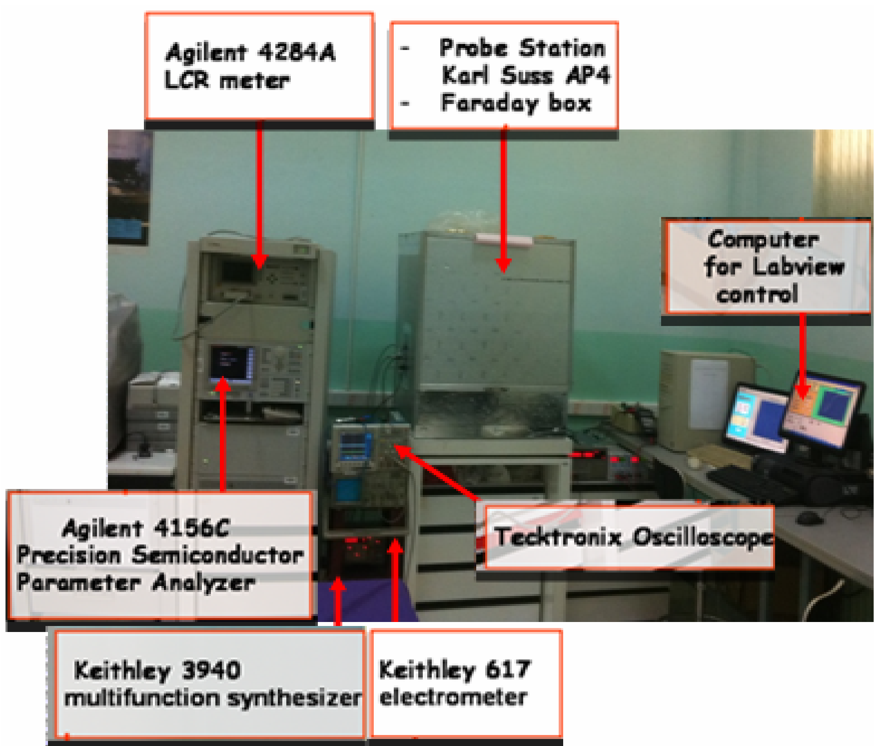


Figure III.3: Global view on soft/hard electrical test platform used for NBTI experiments.

include device parameter extraction and current-voltage (*I-V*) as well as charge-pumping (*C-P*) characteristic measurements via Four (4) Source Monitor Units SMU with high resolution (1fA/2µV to 100mA/100V), two (2) Voltage Monitor Units (VMU) (± 20 V, minimal value 0.2µV), two (2) Voltage Source Units (VSU) (± 20 V, minimal value 1 mV). It is extended by SMU and Pulse Generator Expander (Agilent 41501B) to high power measurements using HPSMU: High Power SMU (10fA/2µV to 1A/200V). It also comprises one (1) Pulse Generator Unit (PGU) that allows the control of the signal rise and fall times up to a frequency of 500 kHz.

- *LCR meter Agilent 4284A* : measures the impedance and performs capacitance-voltage characteristics. It has a frequency range from 20Hz to 1MHz.
- *Multifunction synthesizer (function generator), model Keithley 3940:* generates different types of signals (sinusoidal, square, triangular and arbitrary) with frequency ranging from 0Hz to 20MHz (resolution 0.1mHz) and voltage amplitude, Vp-p (peak to peak) of 20 V at offset voltage 0. It is possible to add an external signal to the principal generator.
- *Programmable Electrometer, model Keithley 617:* can measure currents with high sensitivity, voltages, charges, and resistance with range of 0.1fA-20mA, 10µV-200V, 10fC-20nC, and 0.1Ω-200MΩ, respectively. Moreover, it incorporates a programmable DC voltage source (± 100 V, max 2mA).
- *Digital oscilloscope, model Tektronix TDS 3054B:* has four (4) input channels, 500MHz bandwidth, base time of 1 ns – 20 s, and a sampling rate of 5 GSa/s on all channels. It is used to display signals and voltage applied on DUT pads (for example measure/stress/measure protocols).
- Computer for measurement control using LabVIEW (Laboratory Virtual Instrument Engineering Workbench) software.

- GPIB cards and triax and coax cables.
- Faraday box.

These instruments have remote access for control and data acquisition via GPIB (General Purpose Interface Bus) interface with IEEE 488.2 standard. All measurements are fully automated.

III.3.1- Hot plate

As our probe station is not equipped with hot chuck to heat DUT for NBTI experiments, an in-house hot plate was designed and fabricated at CDTA. The integration of the hot plate in our probe station required optimization of its geometry to minimize heat dissipation. The geometry and the corresponding heated surface (2.3 cm x 2 cm x 0.9 cm) are chosen to avoid any alteration of the intrinsic probe station characteristics by heat dissipation, especially the optical characteristics of the probe station microscope. The heat monitoring is carried out with a passive Platinum resistance sensor (Pt100) housed in the chuck to read its temperature. Special care has been taken to the reading of the temperature as the thermal heating losses, thermoelectric effect, and the cables used to connect the Pt100 induce parasitic errors on the measurement itself due to their influence on the resistance. Therefore, appropriate corrections have been brought. The Pt100 sensor surface is 2.3x2 mm^2, the small area is chosen to significantly reduce thermal errors. To read the temperature of the chip (DUT), a calibration between plate and chip temperatures has been performed, as shown on **Fig. III.4 (b)**, and introduced in the acquisition program. The temperature control is done by a Proportional Integral Derivative (PID) algorithm. The heat system is automated using a labview program. This system is able to heat up to 260 °C in 100 s with a precision of 0.2 °C.

III.3.2- Standard electrical techniques

III.3.2.1- Drain current versus gate voltage (I-V) setup

For all benches, the following is adopted: SMU1 is connected to drain terminal, SMU2 to gate terminal, SMU3 to source terminal, and SMU4 to substrate terminal, except if otherwise specified. **Figure III.5 (a)** illustrates the *I-V* setup using SMUs of Agilent 4156C. SMU2 applies a variable voltage on the gate, SMU3 and SMU4 connect source and substrate to the ground, respectively, while SMU1 forces a voltage on the drain and senses the current. This setup allows measuring I_{DS}-V_{GS} as well as I_{DS}-V_{DS} characteristics.

III.3.2.2- Charge-pumping (C-P) setup

The experimental setup of the *C-P* technique is illustrated on **Fig. III.5 (b)**. To sweep the channel state of the MOS transistor from accumulation to inversion, a gate voltage signal is applied using Keithley 3940 function. The latter can generate waveforms with frequencies higher than 1 MHz. Alternatively, PGU of Agilent 4156C can also be used to apply gate signal, but with frequency below 500 kHz. The drain and source are connected to SMU1 and SMU3, respectively. Both SMUs are either forced to the ground voltage or to a small reversed-bias voltage (V_R). Finally, SMU4 is connected to the substrate to measure the resulting recombination DC current, commonly named CP-current (I_{CP}).

III.3.2.3- Capacitance versus voltage (C-V) setup

The C-V technique is easy to setup using Agilent 4284A LCR meter, as shown on **Fig. III.5 (c).** It consists in connecting V_{low} and V_{high} cables of LCR meter to the gate and substrate terminals of

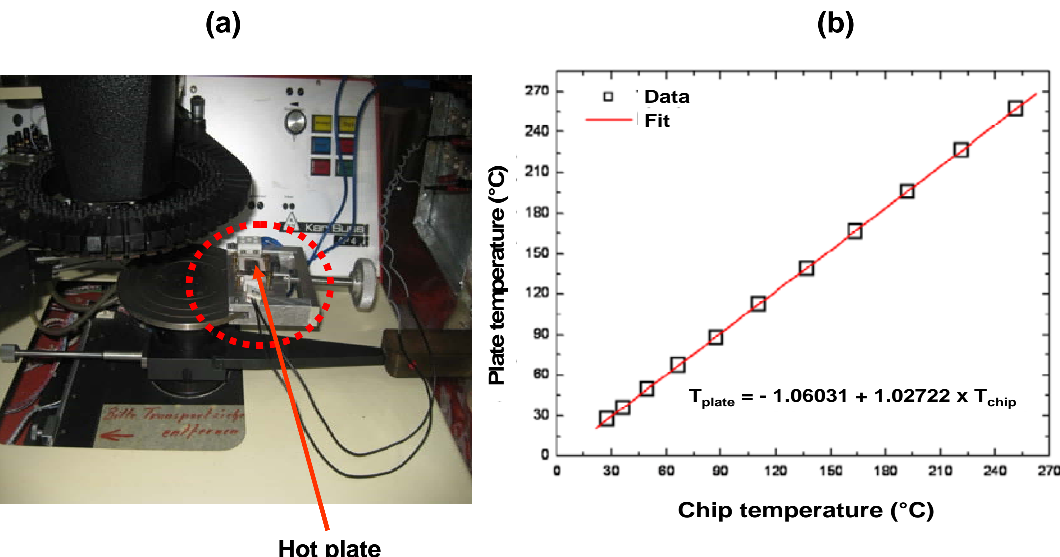


Figure III.4: (a) In-house hot plate into probe station as indicated by arrow. (b) Calibration curve for plate and chip temperatures.

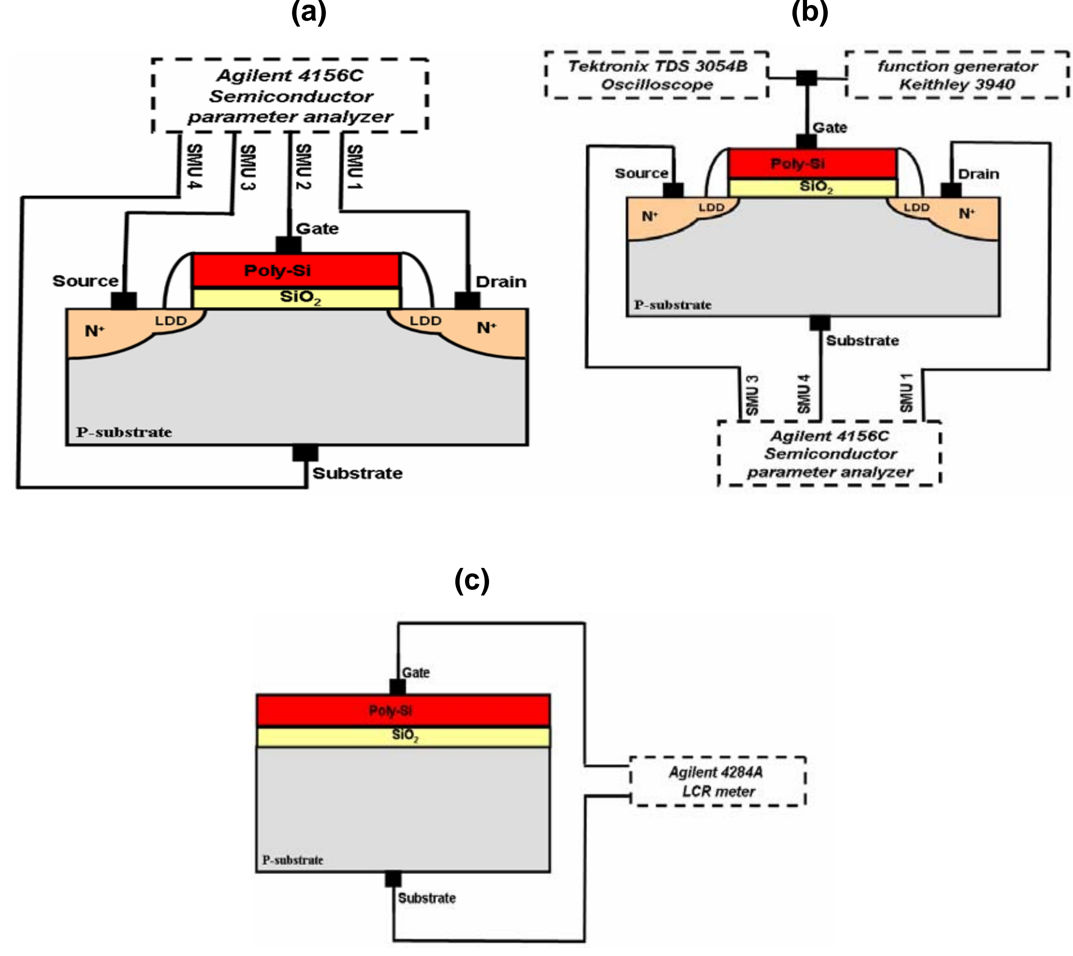


Figure III.5: Illustrative technique setups for (a) current-voltage (*I-V*) (b) charge pumping (*C-P*) and (c) capacitance-voltage (*C-V*).

the capacitor. Superposing a small signal of variable frequency to a DC voltage, can lead to *C-V* characteristics at high (1 MHz) and low (1 kHz) frequency.

III.3.3- Special setup

Several specific setups were mounted in our laboratory including on the fly (OTF) one and three points **[22,57,129]**, OTFIT **[55,130]**, OTFBT **[152]**, TPCV **[153]**, and OTFOT **[151,154]**. Additional details on the OTFOT method: concept and results are addressed in **Chapter IV**. In this section, we focus on its setup, which is illustrated on **Fig. III.6**. The bench is fully automated to perform OTFOT measure/stress/measure (MSM) sequences. When the protocol switches from stress to measurement phases, all SMUs and PGU of Agilent HP 4156C are biased to 0 voltage, causing delay time before measurement. To overcome this limitation, we have used Agilent HP 4156C to measure the CP-current and trigger Keithley 3940 to generate signal during measurement, as illustrated in **Fig. III.6**. Furthermore, it generates a trapezoidal signal of 1 MHz, contrarily to Agilent HP 4156C which is limited to a signal frequency of 500 kHz. Regarding the stress voltage, we have used the voltage source of Keithley 617 added (it is injected as external voltage in Keithley 3940) to the offset voltage of Keithley 3940,. The voltage source is also superposed in series with SMU2 to composite the trigger voltage during measurement. This configuration allows to carry out a gate measure/stress signal, as

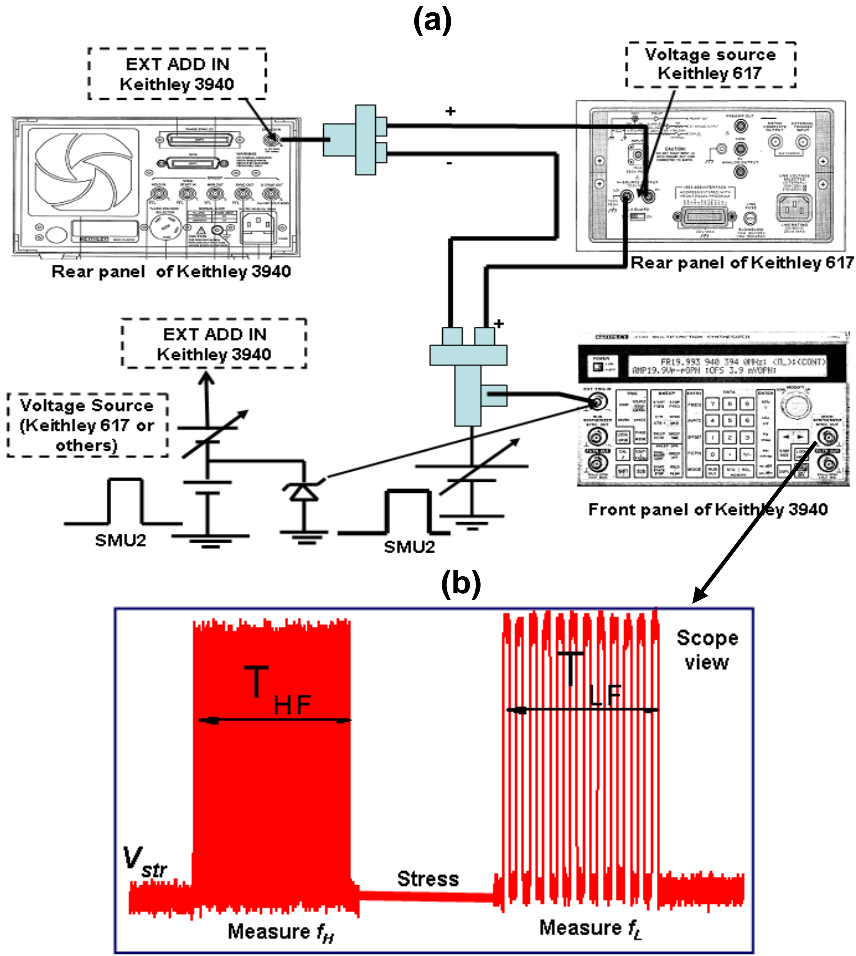


Figure III.6: (a) Illustrative instrumental setup of OTFOT method, showing instrumentations used for (b) the output measure/stress/measure signal applied on the transistor gate.

shown in **Fig. III.6 (b)** (where CP signal is generated with alternate low and high frequencies). The low voltage of the CP (V_L) is set to the stress bias (V_{GStr}) (i.e., V_L = V_{GStr}). During the stress interval, V_{Gstr} is applied, through a DC voltage, onto the gate of the device. After each stress time, a gate pulse train is applied without modifying the experimental setup. In this case, the gate trapezoidal signal of amplitude $\Delta V_G = V_H - V_{Gstr}$ and two different frequencies [high (f_H) and low (f_L)] are applied alternatively to measure the maximum CP-currents, I_{CPH} and I_{CPL}. **Figure III.7** schematically summarizes the electrical setup of OTFOT method **[151,154]**.

III.4- Characterization before NBTI Stress

Before starting NBTI experiments, we have extracted the characteristics of the transistors used in our experiments at virgin state (before applying any stress). The characteristics concern *I-V*, *C-V,* and *C-P*.

III.4.1- Current-Voltage (I_{DS}-V_{GS}) characteristics

Figure III.8 shows the drain current versus gate voltage transfer characteristics (I_{DS}-V_{GS}) [see **Fig. III.8 (a) and (b)**] and the transconductance (g_m-V_{GS}) [see **Fig. III.8 (c) and (d)**] characteristics of p-MOS and n-MOS transistors of different gate lengths and fixed width at 10 µm, respectively. To avoid the lateral electric field effect on mobility, the linear I_{DS}-V_{GS} curve were measured at a drain voltage of V_{DS} = 0.05 V for n-MOSFET and -0.05 V for p-MOSFET. The short transistors exhibit higher drain current as well as higher transconduction compared to longer ones, because they are inversely proportional to gate length [see **Eqs. (II.24)** and **(II.41)** in **Chapter II**].

There are several ways to extract the threshold voltage. The most used one is the linear threshold-voltage extraction method. It consists of finding the gate-voltage axis intercept of the linear extrapolation of the I_{DS}–V_{GS} curve at the maximum of its first derivative (slope) [i.e. the point of maximum transconductance, (g_m)] **[155]**, as illustrated in **Fig. III.9 (a).** The extracted V_{th} is presented in **Fig. III.9 (b)** for n- and p-MOS transistors as a function of gate length. All transistors show threshold

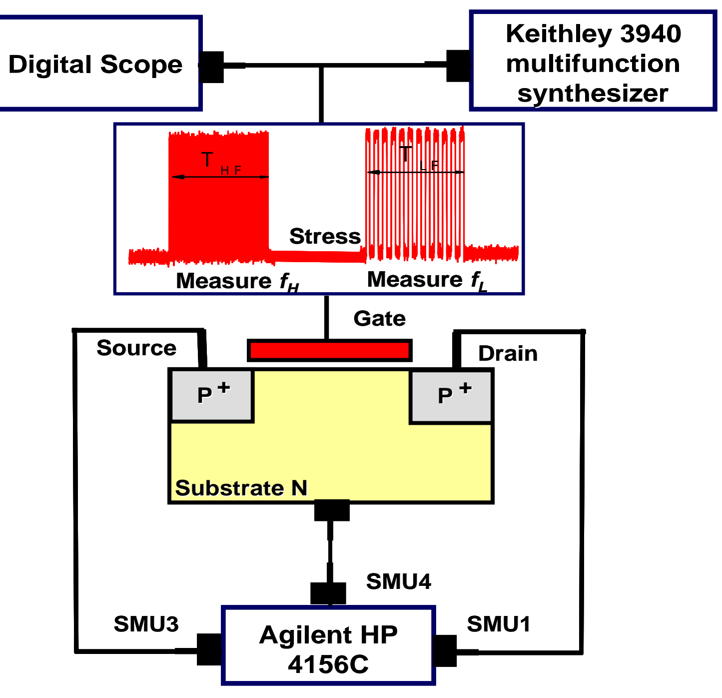


Figure III.7: Schematic representation of OTFOT setup.

voltages within the specification given by ISiT (see **appendix (C.2)** as shown by dashed lines on **Fig. III.9 (b)**. n-MOSFET threshold voltages are comprised between 0.56 and 0.9 V, while those of p-MOSFET are between -1.2 and -0.9 V.

Due to these differences in V_{th}, care has been taken to quantify NBTI degradation by comparing each degraded transistor to its own virgin (non-degraded) state threshold voltage.

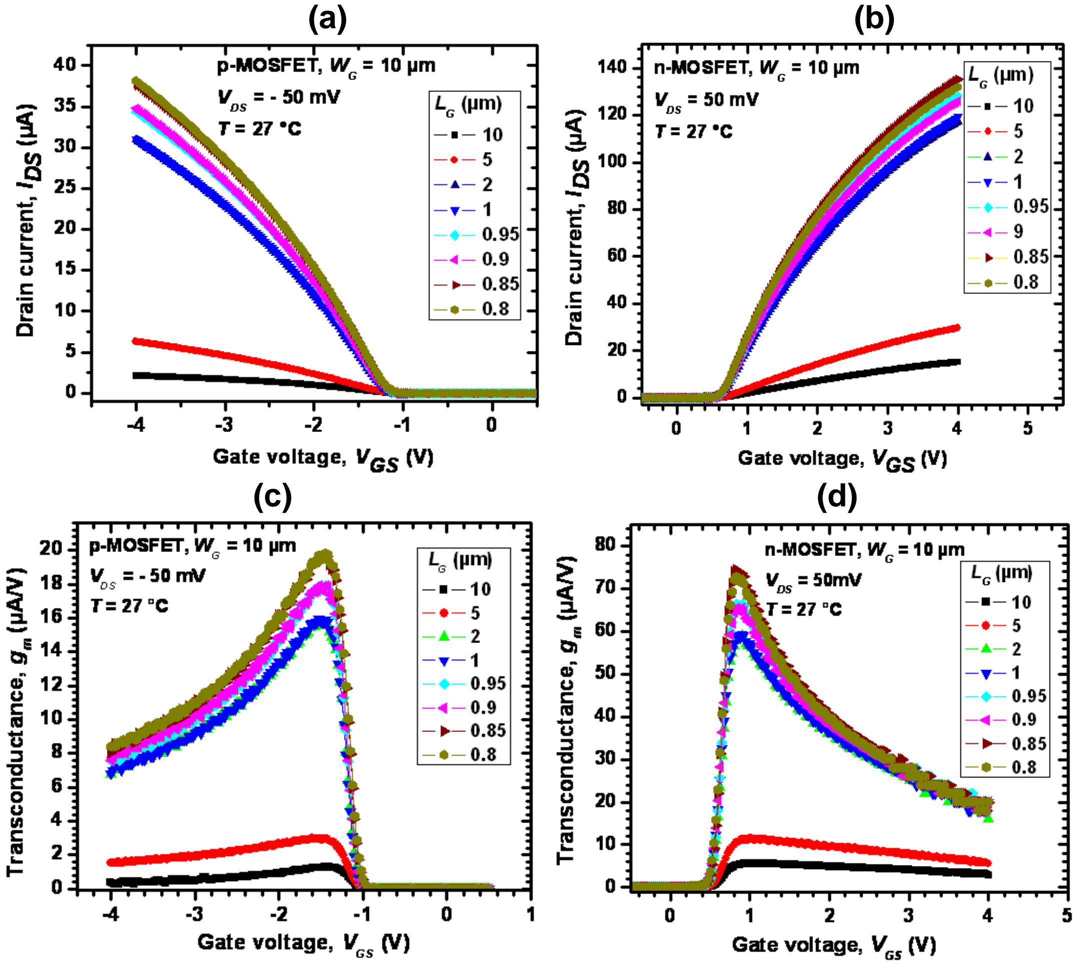


Figure III.8: (a) and (b) present I_{DS}-V_{GS} characteristics of p- and n-MOSFET, respectively. (c) and (d) trans-conductance of p- and n-MOSFET, respectively.

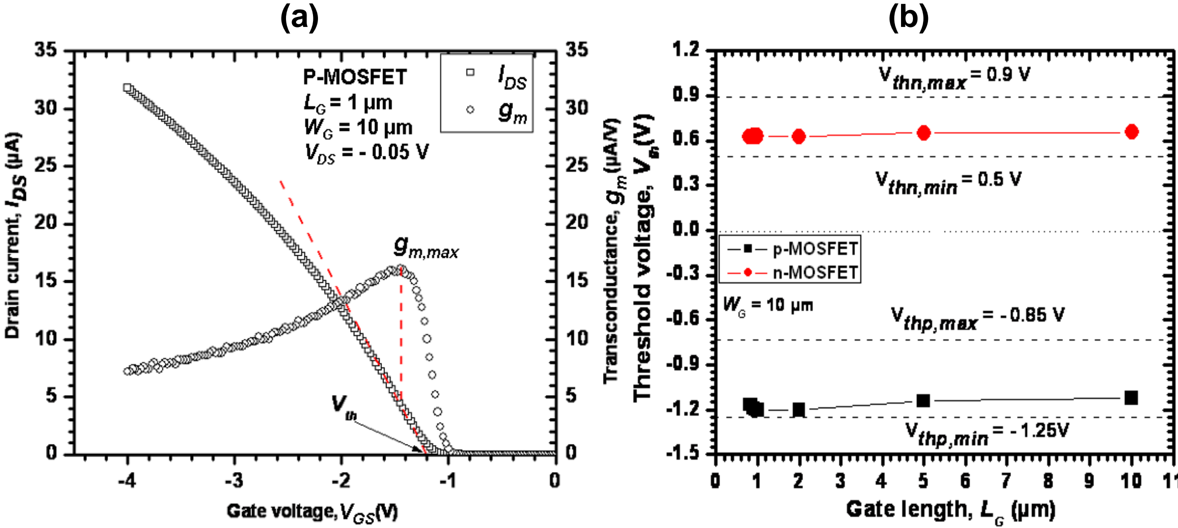


Figure III.9: (a) Threshold voltage extraction using linear extrapolation of the I_{DS}–V_{GS} curve at the maximum of its first derivative ($g_{m,max}$). (b) Threshold voltage of transistors used in the NBTI experiments. V_{th} given by ISiT are also presented by dashed lines.

III.4.2- Capacitance-Voltage (C-V) characteristics

The capacitance-voltage (*C-V*) measurement can be used to determine the NBTI degradation. During the *C-V* measurement, the device is swept from accumulation to inversion while constantly measuring the capacitance as depicted in **Fig. III.10 (a) and (b)** for n-and p-substrate MOS capacitors at room temperature, respectively. The shift and stretch out of the *C-V* characteristics are directly related to the oxide and interface traps generation **[63,76]**. The flatband voltage is extracted at the flatband capacitance (C_{fb}), which is determined, as **[93]**:

$$C_{fb} = \frac{C_{ox} C_{sfb}}{C_{ox} + C_{sfb}} \tag{III.1}$$

where C_{Sfb} is the semiconductor capacitance at flatband conditions, given by

$$C_{sfb} = \frac{A_g \varepsilon_0 \varepsilon_{sc}}{\lambda} \tag{III.2}$$

where λ is the Debye length defined by

$$\lambda = \left(\frac{\varepsilon_0 \varepsilon_{sc} KT}{q^2 N_{d,a}} \right)^{1/2} \tag{III.3}$$

C_{OX} is the oxide capacitance, $\varepsilon_0 \varepsilon_{sc}$ the permittivity of substrate. The constant values are $\varepsilon_0 \varepsilon_{sc} = 1{,}062510^{-12}$ (F/cm), $KT/q = 0.02585$ (V), $q = 1.602x10^{-19}$ (C), and the gate area A_G = 0.001 (cm^2).

III.4.3- Charge-Pumping (C-P) characteristics

The CP-current (I_{CP}) curves of virgin transistors with different gate lengths are presented in **Fig. III.11 (a) and (b)** for p- and n-MOSFET. As expected by **Eq. (II.1)**, the I_{CP} is proportional to gate length area, smaller I_{CP} corresponds to shorter gate length transistors. In order to show I_{CP} curves of all transistors, we have plotted I_{CP} data in semi logarithm in **Fig. III.11 (c) and (d)**.

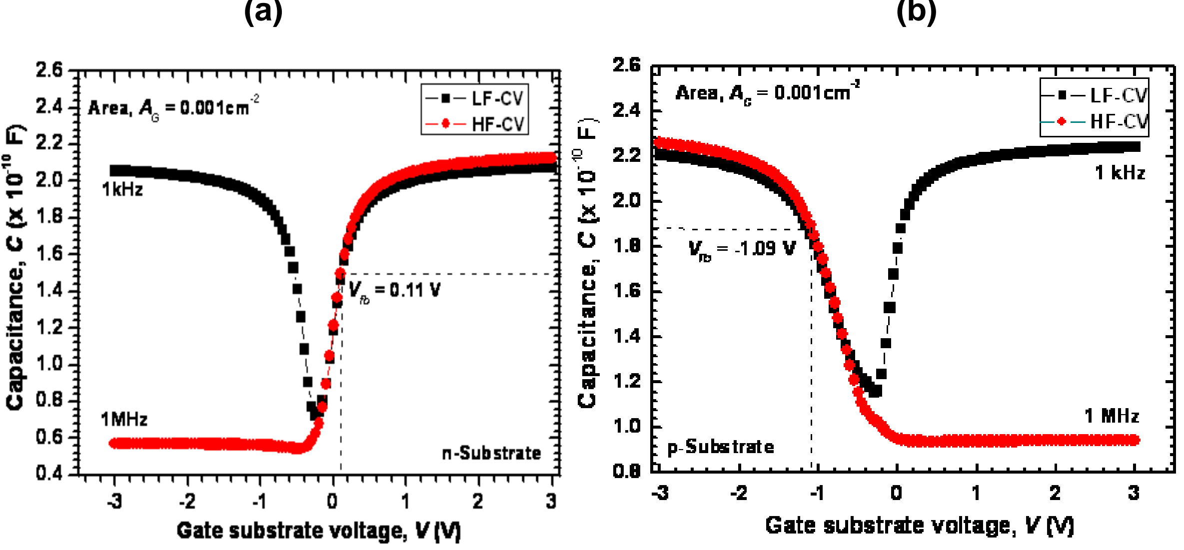


Figure III.10: Capacitance versus gate-substrate voltage for (a) n-substrate capacitor and (b) p-substrate capacitor.

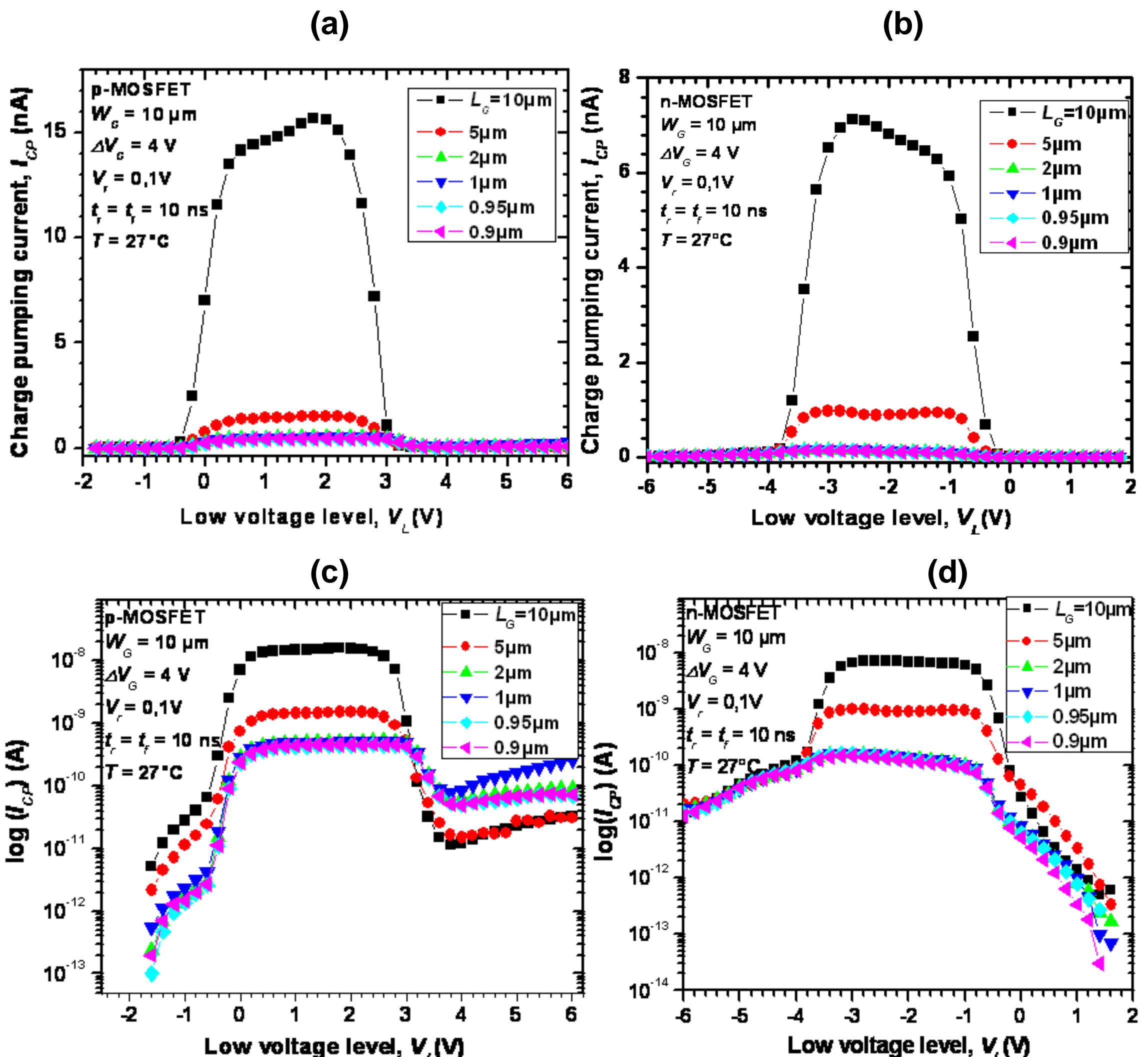


Figure III.11: CP-current, I_{CP} as a function of low voltage, V_L. (a) and (c) for p-MOSFET in linear and log scale, respectively. (b) and (d) for n-MOSFET in linear and log scale, respectively.

Finally, I_{DS}-V_{GS}, *C-V*, and *C-P* characteristics exhibit the well known behaviour that characterizes MOS transistors and capacitors in fresh state.

III.5- Temperature Effect on MOS Device Characteristics

Our focus in this section will be on the effect of the temperature without stress voltage on MOS device characteristics, such as I_{DS}-V_{GS}, *C-V*, and *C-P* and their principal parameters.

III.5.1- Temperature effect on I_{DS}-V_{GS} characteristics

It is well established that temperature influences the MOS device characteristics and consequently its working conditions. In fact, temperature reduces the magnitude of V_{th} in absolute value, decreases carrier mobility and the transconductance, while it increases the junction leakage current. **Figure III.12** illustrates those effects on both p- and n-MOSFET. In addition, I_{DS}-V_{GS} characteristics show the well known coefficient, commonly called Zero Temperature Coefficient (ZTC) ($dI_{DS}/dT = 0$) **[156,157]**. ZTC appears in both linear and saturation regions for temperatures between 27 and 200°C and it relies on the mutual cancellation of the threshold voltage and the channel mobility temperature

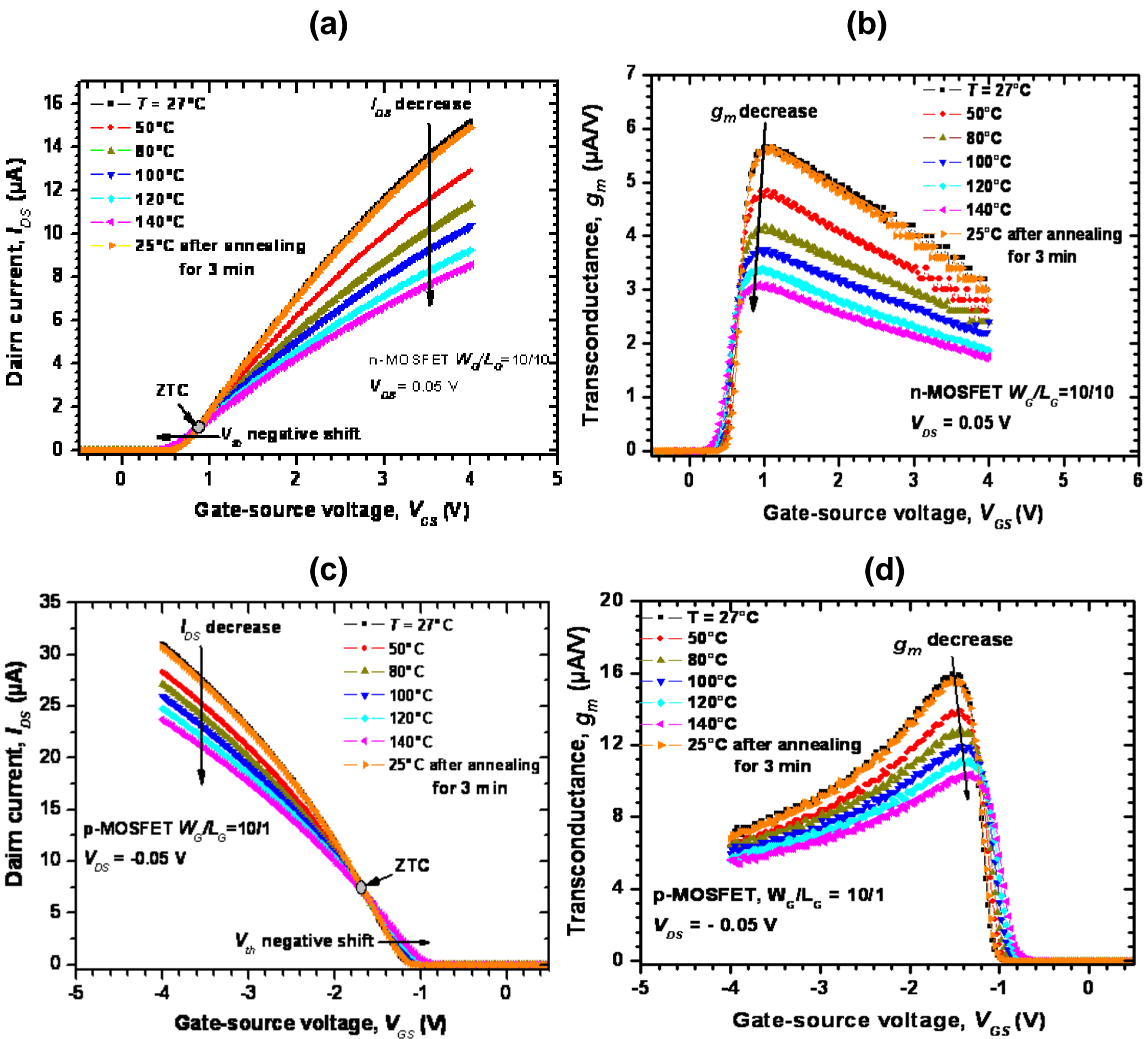


Figure III.12: Current-voltage characteristics as a function of temperature for n-MOSFET (a) and p-MOSFET (c). The influence of the temperature on transconductance of n-MOSFET (b) and p-MOSFET (d).

derivatives, over a specified temperature range **[156,157]**. In other words, ZTC is due to several competing temperature dependent physical parameters of the MOS transistor, such as temperature dependence of mobility, surface potential, intrinsic doping, threshold voltage, and source/substrate and drain/substrate junction leakage current. This effect is often used to design analog circuits to avoid temperature effect.

To understand how high temperature affects the performance of the transistors, in particular threshold voltage and transconductance characteristics, we analyze their relation to temperature. Effective mobility in inversion layer depends on the interactions between electrons/phonons and impurities. Therefore, high temperature increases scattering of electrons by phonons which yields the mobility dependence on temperature by a nearly $1/T^2$ at gate biases corresponding to strong inversion **[63]**. This leads to lower I_{DS} current and lower g_m at higher temperature.

Regarding the temperature dependence of threshold voltage, it depends on several device parameters which are described by **[63]**:

$$V_{th} = V_{fb} \pm 2\phi_F \pm \frac{\sqrt{4\varepsilon_{Si} N_{A(D)} \phi_F}}{C_{OX}} \tag{III.4}$$

where V_{fb} (V) is the flatband voltage, ϕ_F (eV) is the Fermi level, $N_{A(D)}$ (cm^{-3}) is the substrate acceptor (donor) impurity concentration of n- and p-MOS transistors, ε_{Si} (F/cm) is the permittivity of silicon, and C_{OX} (F/cm^{-2}) is the gate MOS capacitance. The upper sign refers to the n-MOS transistor whereas the lower sign refers to the p-MOS transistor.

The flatband voltage depends on the metal-semiconductor work function, ϕ_{ms} and on the total charge in Si/SiO_2 system as described in section **§ I.4** of **Chapter I**. The effect of temperature on ϕ_{ms} and charges is often neglected in the literature **[63]**. However, this approximation is questionable, since it has shown that the temperature influences ϕ_{ms} and the interface charges (Q_{it}) **[158,159]**. We will return to this point in the sequel.

Considering that the temperature has no significant influence on V_{fb}, the temperature dependence of V_{th} is driven by ϕ_F. In fact, ϕ_F is given by:

$$\phi_F = \frac{KT}{q}\ln\left(\frac{N_A}{n_i}\right) \quad \text{(III.5)}$$

The temperature dependence of the silicon intrinsic carrier concentration n_i is approximated by the well-known expression **[63]**:

$$n_i(T) = AT^{3/2}\exp\left(-\frac{E_{g0}}{2KT}\right) \quad \text{(III.6)}$$

where E_{g0} (eV) is the energy bandgap at $T = 0\ K$. A is a constant equal to 3.9 x10^{16} cm^{-3} $K^{-3/2}$. It is clear from **Eqs (III.5) and (III.6)** that n_i increases and ϕ_F decreases with T. That is why around V_{th}, the I_{DS}-V_{GS} characteristics of both n- and p-MOSFET shift toward zero.

In summary, the main effect on the I_{DS}-V_{GS} characteristics when temperature increases, the mobility and the absolute value of the threshold voltage for both n- and p-MOS transistors decrease. V_{th}, extracted from **Fig. III.12** as a function of temperature is potted in **Fig. III.13**. It varies rather linearly with temperature as observed elsewhere **[160]** following:

$$V_{th}(T) = V_{th}(T_0) + \alpha(T - T_0) \quad \text{(III.7)}$$

where α (V/°K) is the threshold voltage temperature coefficient. T_0 (°K) is the reference temperature. However, temperature dependence of the mobility is assumed in the following form:

$$\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{-k} \quad \text{(III.8)}$$

where the exponent k varies between 1.5 and 2 **[160]**. This behaviour is illustrated by **Fig. III.14 (b)** which represents the mobility data, extracted using the maximum transconductance, $g_{m,max}$ relation. The mobility, μ is given by the slope of **Eq (III.9):**

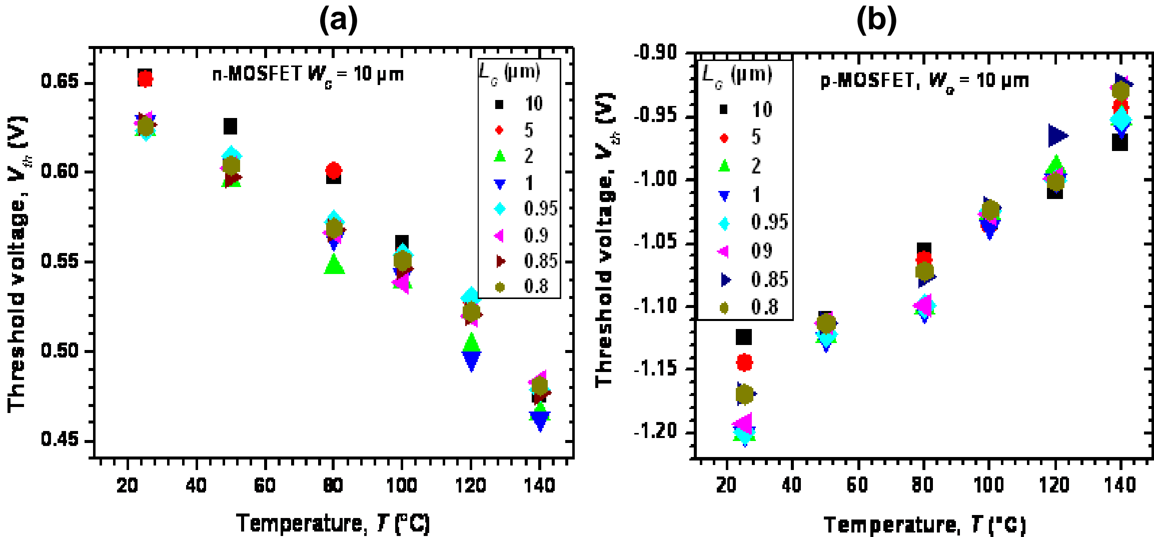


Figure III.13: Temperature dependence of the threshold voltage for n-MOSFET (a) and p-MOSFET (b) with different gate lengths

$$\frac{1}{g_{m,\max}} = \frac{1}{\mu \ C_{OX} \ W \ V_{DS}} (L - \Delta L) \qquad \text{(III.9)}$$

ΔL (µm) is the lateral diffusion of LDD underneath the poly-Si gate. It can also be extracted easily from **Eq (III.9)** [see **Fig. III.14 (a)]**. It is not affected by the temperature at least up to 140°C.

It is worth noting that if the temperature is reduced to room temperature, the I_{DS}-V_{GS} characteristics return back to values measured before annealing at 27°C (see **Fig. III.12**), indicating that the temperature, alone, affects only the MOS transistor physical parameters that are temperature dependent without any degradation of transistor (up to 140°C for 3 to 5 min of annealing).

III.5.2- Temperature effect on C-V characteristics

In addition to temperature dependence of I_{DS}-V_{GS}, the effect of temperature on *C-V* at high frequency (1MHz) for both n- and p-type substrates are plotted in **Fig. III.15**. At first glance, it appears that there is no significant change in *C-V* characteristics with elevated temperature. However, a slightly variation and stretch-out of the *C-V* characteristics can be observed with temperature (see insert **Fig. III.15**). It is clear that the flatband voltage is shifted positively and negatively for p- and n-substrate MOS capacitance, respectively. The stretch-out of the characteristics indicates contribution of the interface charges **[161]**. For further analysis, we express V_{fb} as a function of its principal components:

$$V_{fb} = \phi_{ms} + \frac{Q_T}{C_{OX}} \qquad \text{(III.10)}$$

Q_T is the total charge in the Si/SiO$_2$ system as defined in **Chapter I**, section **§ I.4**. $Q_T = Q_f + Q_m + Q_{ot} + Q_{it} + Q_{bt}$. Q_f, Q_m, Q_{bt}, and Q_{ot} can be assumed constant with temperature variation (without stress voltage) **[159]**. However, Q_{it} charges change because they are distributed in the band gap energy, thus they are affected by the surface potential φ_s variations with temperature. Considered as amphoteric defects, interface traps can be charged either positively or negatively. As a consequence, Q_{it} charges can be positive or negative, depending on the surface potential **[162]**. At

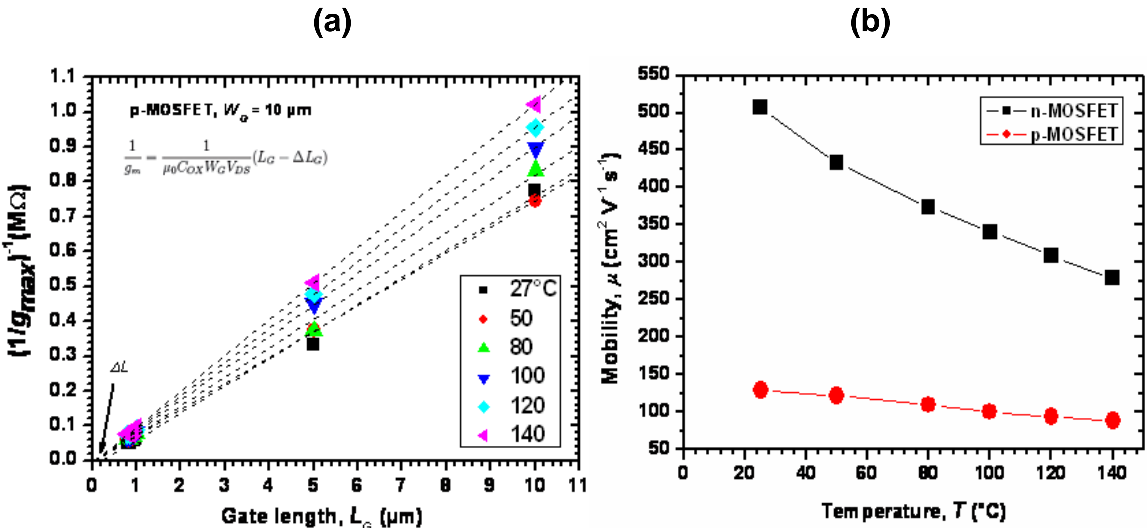


Figure III.14: (a) $1/g_{m,max}$ as a function of gate length for different temperatures. (b) Mobility degradation as a function of temperature for n- and p-MOSFET.

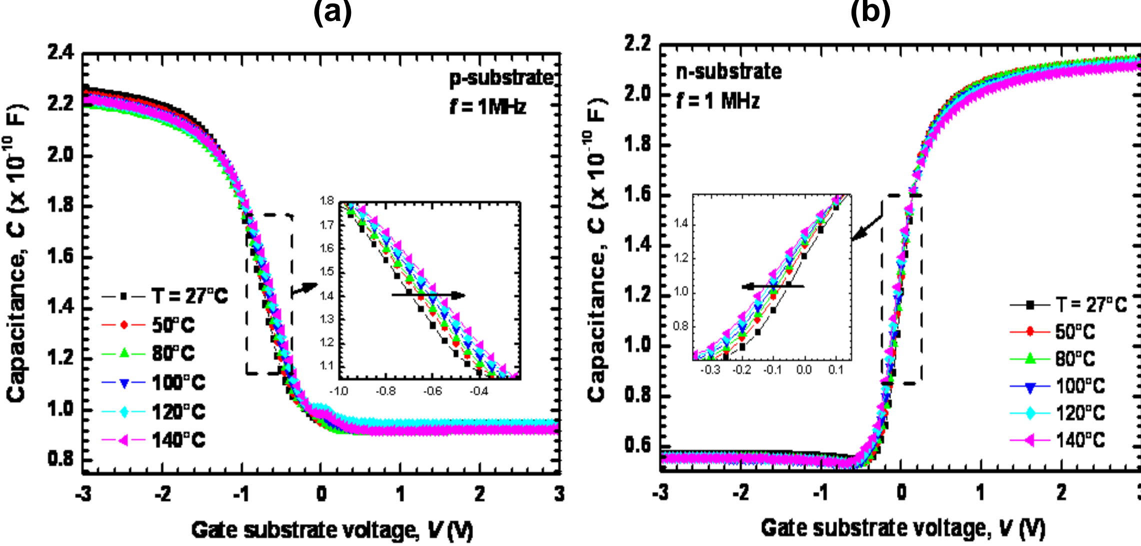


Figure III.15: The effect of temperature on the capacitance-voltage characteristics at high frequency for p- and n-substrate MOS capacitor

flatband position ($\varphi_s = 0$), they are positive in p-substrate MOS capacitor (inducing negative voltage) and negative in n-substrate capacitor (inducing positive voltage):

$$V_{it} = \frac{qD_{it}(E)\Delta\varphi_S}{C_{OX}} = \frac{qD_{it}(E)\phi_F}{C_{OX}} \quad \text{for n-substrate}$$
$$V_{it} = \frac{qD_{it}(E)\Delta\varphi_S}{C_{OX}} = -\frac{qD_{it}(E)\phi_F}{C_{OX}} \quad \text{for p-substrate} \qquad \text{(III.11)}$$

As ϕ_F decreases with increasing temperature, the absolute value of V_{it} decreases for both p- and n-substrate. Moreover, temperature dependence of ϕ_{ms} is directly influenced by the temperature dependence of n_i **[66,159]**. Thus increasing *T*, n_i increases inducing ϕ_F and ϕ_{ms} decrease with temperature. In summary, both interface charges and work function behaviors with temperature

contribute to the shift of *C-V* curves toward positive and negative voltages for p- and n-substrate, respectively, as shown in **Fig. III.15**.

III.5.3- Temperature effect on C-P characteristics

In this section, we investigate the temperature effect on Elliot *C-P* curves. **Figure III.16** shows I_{CP} as a function of the low level gate signal for p-MOS transistor with temperature as a parameter. When the temperature is increased, the maximum of I_{CP} current decreases because of the reduction of the energy window contributing to I_{CP}. In fact, I_{CP} depends on the temperature as described in **Chapter II** following **Eqs. (II.1) and (II.4)** via thermal velocity and the intrinsic carrier density. Therefore, using **Eqs. (II.1) and (II.4)** and taking into account **Eq. (III.6)**, as well as the thermal velocity expression $v_{th} = \sqrt{3KT/m}$ **[63]**, I_{CP} can be expressed for p-MOSFET as:

$$I_{CP} = -a \cdot T - b \cdot T \ln(T) + c \tag{III.12}$$

Where

$$a = 2qL_G W_G fK\,\overline{D_{it}} \ln\left(A\sqrt{\frac{3\sigma_n \sigma_p K}{m}} * \frac{|V_{th} - V_{fb}|}{\Delta V_G} \sqrt{t_r t_f} \right)$$

$$b = 4qW_G L_G fK\overline{D_{it}}$$

$$c = qW_G L_G fE_{g0}\,\overline{D}_{it}$$

Shifts observed on the *C-P* edges [see insert **Fig. III.16 (a)**] are directly related to the temperature dependence of the threshold and flatband voltages, as shown previously. *CP*-V_{th} and *CP*-V_{fb} present the same temperature dependence as *IV*-V_{th} and *CV*-V_{fb}, respectively. In **Fig. III.16 (b)**, the maximum CP-current decreases with temperature as stated by **Eq. (III.12)**.

Regarding the above-cited temperature dependence of MOS device characteristics and parameters, care has to be taken to avoid any artefact in BTI investigation. That is why; we have carried out the measurement phase at the same temperature as that of stress phase to take only account of degradation induced by NBTI. Besides, the influence of using high amplitude (ΔV_G) to stress devices on CP curves is given in **appendix (C.3)**.

III.6- Bias Temperature Combined Stress on MOS Devices

The BTI degradation is usually accelerated by combining elevated temperature and high voltage to get a reasonable parameter drift within short stress duration. To characterize pure BTI, a stress field less than 8 MV/cm (stress voltage, in our case, less than 16 V) should be applied on the gate **[67]** while source, drain, and substrate remain grounded. In fact, higher V_{GS} stress can induce other unwanted transistor degradation like time dependent dielectric breakdown (TDDB). Other terminals are grounded (or V_{DS} = 50mV in OTF methods) to stress transistor in an uniform inverted channel condition to prevent hot carrier damage. However, in the past, the same stress conditions were associated with the drift of mobile ionic charge such as Na^+, Li^+, and K^+. Therefore, what are the differences between BTI and mobile ion effect? The answer is given in the next section **§ *III.6.1***, but the fundamental difference is the nature of the defects involved: mobile ions are extrinsic defects, while BTI deals with intrinsic defects. On the other hand, bias could either be positive or negative and devices either p-MOS or n-MOS devices. Thus why is NBTI in p-MOSFET the well-known one?

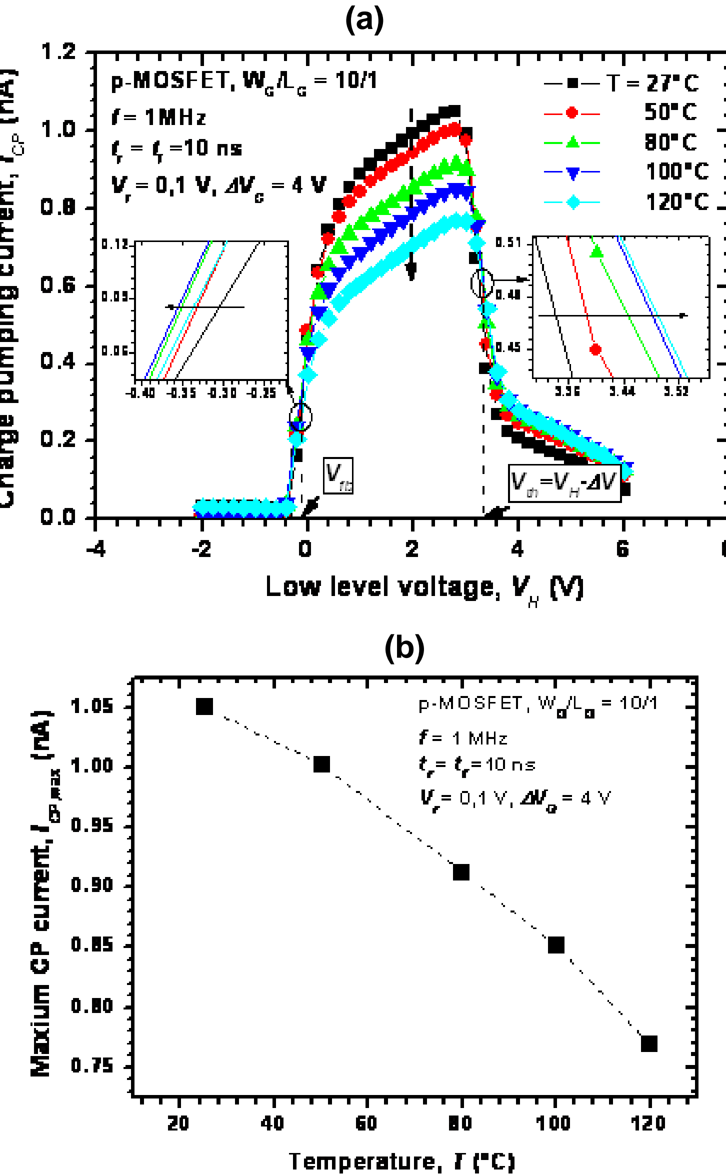


Figure III.16: (a) Temperature influence on Elliot *C-P* curve for p-MOSFET. (b) Temperature effect on maximum CP-current ($I_{CP,max}$).

III.6.1- BTI and Mobile ionic charge

Commonly, the mobile ions are associated with the cleanness of the technological process. In the past, ionic impurities were inherent to the process recipes and equipments of that time. With continuous improvement of the processes, the ionic contamination has been considerably reduced and is considered as a quality problem, while BTI is a reliability/wearout issue. Now, it is well accepted **[43,67,92]**, that mobile ions do not play an important role under BTI conditions. Indeed, **Fig. III.17** depicts shifts induced by NBTI stress in p-MOS transistor and n-substrate capacitor. p-MOSFET was stressed for 30 min at 80°C with stress voltage of – 13 V and the MOS capacitor for 1 hour at 100°C and – 13 V. It is clear that under negative gate voltage stress at elevated temperature, both *C-V* and I_{DS}-V_{GS} characteristics shift to the negative voltage indicating an increase in the net positive charge at the interface. This observation suggests that the mobile charges have insignificant influence on the NBTI shift. In fact, if positive ions are present in the gate oxide they will be accumulating toward the

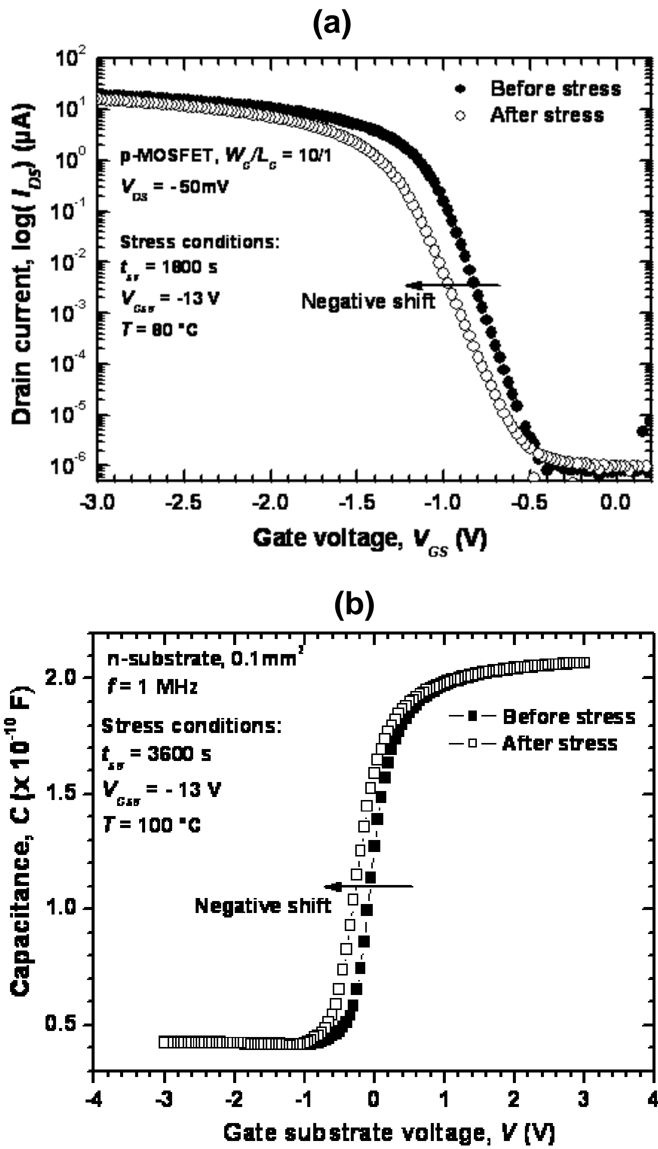


Figure III.17: NBTI-induced shift of I_{DS}-V_{GS} curve (a) and *C-V* curve (b). It is clear that negative bias stress causes negative voltage shift in both p-MOSFET and n-substrate capacitor, which is opposite to the mobile ion effect.

poly-Si/SiO_2 interface during NBTI stress condition, which will cause a reduction in the net amount of positive charge near the Si/SiO_2 interface and will result in a positive shift of flatband and threshold voltages contrarily to NBTI effect. The latter is explained by the creation of positive oxide traps near the Si/SiO_2 interface and/or hole trapping or electron detrapping. This fact is confirmed elsewhere **[163]** by performing NBTI and PBTI in silicon carbide capacitors, p- and n-substrate/4H-SiC. They have obtained an opposite behaviour of *C-V* curves compared to the case of ionic mobile contamination influence.

III.6.2- NBTI versus PBTI in p-MOS and n-MOS transistors

In R-D based models, it is assumed that holes are necessary for Si-H dissociation, therefore one can expect that n-MOSFET biased in accumulation should show similar degradation as p-MOSFET in inversion. But they do not, as shown in **Fig. III.18**.The latter is depicted for n- and p-MOSFET with different gate lengths. Both transistor types are stressed with negative voltage to bring holes at the

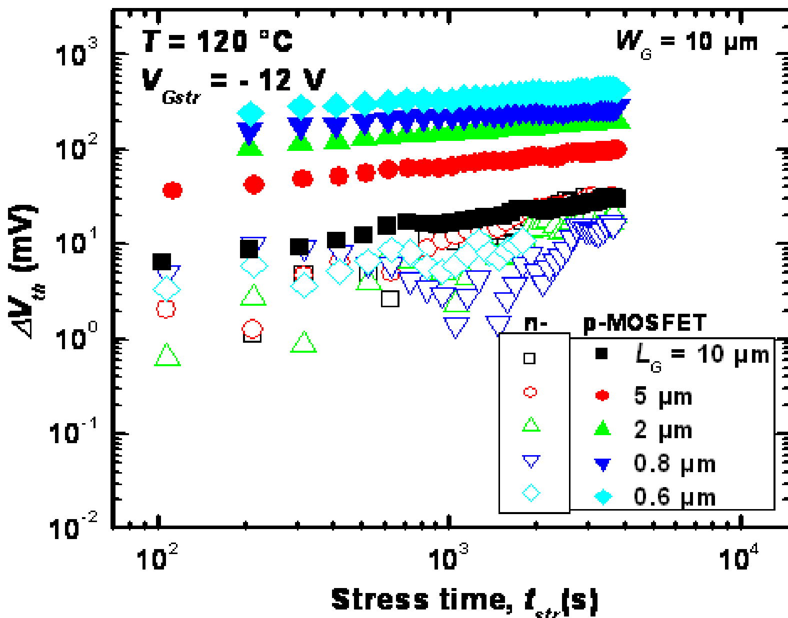


Figure III.18: NBTI-induced threshold voltage shift (ΔV_{th}) as a function of stress time in p-MOS and n-MOS transistors at stress voltage of – 12 V and temperature of 120 °C.

surface. The n-MOS transistor is in accumulation regime, while p-MOS transistor is in inversion regime. Obviously, it is clear that NBTI degradation affects more severely p-MOS transistor than n-MOS transistor, although the presence of holes at the surface of n-MOSFET in accumulation. We have found the same behavior for interface trap creation (ΔN_{it}) under NBTI/PBTI on p-MOSFET and n-MOSFET conditions, as illustrated in **Fig. III.19.** BTI-induced ΔN_{it} are extracted using OTFIT method **[55]** for the same stress conditions of electric field and temperature. It is clear, from **Fig. III.19,** that the worst case is associated with NBTI in p-MOSFET. Similar observations were found elsewhere **[22,25,164]** for NBTI/PBTI degradation in p- and n-MOSFET. As a consequence, the lack of holes can not be the only cause for the different degradation behaviors.

One possible explanation of discrepancies between different types of degradation has been given by Tsetseris et *al.* **[24,25]**. As mentioned in **Chapter I**, section **§ I.4.6**, they have shown, using first-principle calculations, the importance of positively charged atomic hydrogen (H^+), instead the hole carriers, for weakening and breaking Si-H band at the interface. These protons are assumed to originate from phosphorus-hydrogen bonds (P-H) in n-substrate and from boron-hydrogen bonds (B-H) in p-substrate. Both B-H and P-H bonds dissociate and liberate H which diffuses to the Si/SiO_2 interface. On their way to the interface, H captures a hole and becomes H^+, then reacts with Si-H to form Si dangling bond and hydrogen molecule (H_2). H_2 diffuses from the interface into the oxide or poly-Si, it can later diffuse back and passivate the dangling bond. Therefore, following this model, the raison for less degradation of NBTI in n-MOSFET, lies in the difficulty to break B-H bonds in p-substrate compared to P-H bonds in n-substrate. The difference between the two processes is mainly in their activation energies.

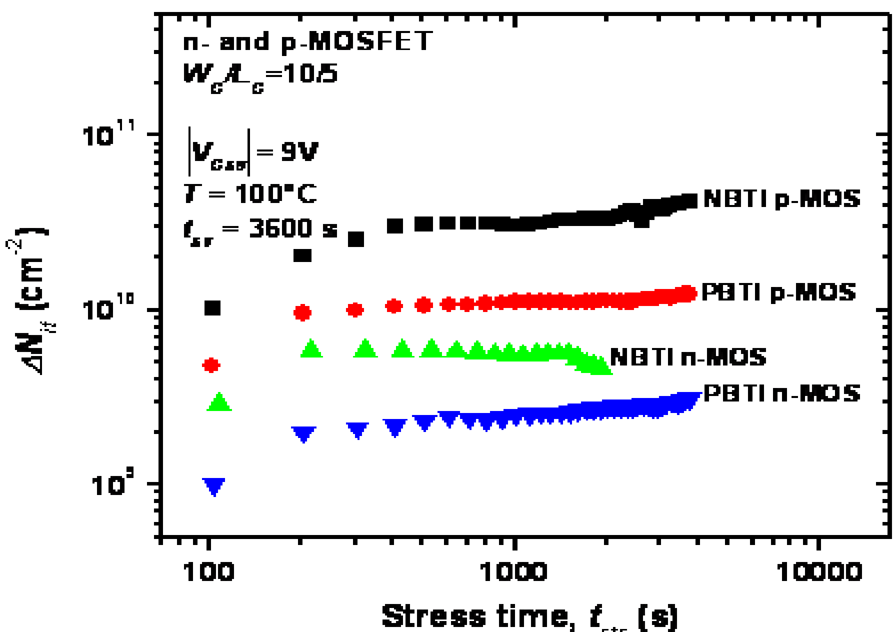


Figure III.19: BTI-family degradations in both p- and n-MOS transistors. The four combinations are presented as function of stress time at stress voltage of 9 V in absolute value and stress temperature of 100 °C.

Actually, the activation energy for dissociation of P-H bonds is usually very high (1.13 eV **[24]**). But, this energy is calculated for n-substrate silicon at accumulation conditions (or PBTI in p-MOSFET) where hydrogen exists as H^-, which is in good agreement with an experimental value of 1.18 eV **[165]**. In the inversion regime (NBTI in p-MOSFET), the activation energy is related to the reduction of the P–H dissociation energy in the depletion region. In this regime, the charge state of hydrogen changes from negative to neutral (*H*), resulting in a much lower dissociation activation energy for a P-H complex of only 0.3–0.4 eV **[24,166]**. For a given period of time the hydrogen atom located in the inversion layer remains neutral and then transforms into a positively charged proton (H^+), after picking up a hole.

This model partly explains the different susceptibility of MOSFETs to positive and negative bias stress. Indeed, as the substrate of n-MOSFET is typically doped with boron, hydrogen can only be supplied from B-H bonds. The activation energy for B–H complexes is 1.28 eV **[167]**, which is larger than that of the P–H. The release of H is thus more difficult in B-doped Si, leading to a less pronounced BTI degradation in n-MOS transistors. There is another explanation based on work function difference between n-poly/n-substrate and n-poly/p-substrate. Due to this difference, the oxide electric fields are not equal for a given gate voltage. This has to be considered when comparing the two types of transistors.

Unlike MOSFET devices, capacitor devices show more NBTI degradation in p-substrate type than in n-substrate. In fact, Benabdelmoune et *al.* **[168]** have depicted, in **Fig. III.20,** that NBTI-induced flatband shifts (ΔV_{fb}) in both capacitors under stress electric field of 6 MV/cm and different temperatures. Here ΔV_{fb} of p-substrate is more important than that of n-substrate. Another possible explanation, based on the amphoteric nature of interface traps, and positive charge oxide traps is also accepted **[26]**. Indeed, being positively charged, oxide trap generation (ΔV_{ot}) always induces negative shift of ΔV_{th} and ΔV_{fb} in MOS transistors and capacitors, respectively. However, the voltage shift

induced by the interface trap generation (ΔN_{it}) depends on the energetic location of the traps and the position of the Fermi level in the bandgap at the surface. As discussed in **Chapter I** section **§ I.4.2**, interface traps are acceptors in the upper half of the band gap and donors in the lower half. This fact influences ΔV_{th} and ΔV_{fb} of p- and n-MOS devices differently. At the inversion regime ($\psi_s = 2\phi_f$), ΔN_{it} induces negative and positive shift of ΔV_{th} in p- and n-MOSFET, respectively. Inversely, at the flatband (($\psi_s = 0$), it causes positive and negative shift of ΔV_{fb} in p- and n-MOSFET, respectively. **Table III.1** summarizes the different shifts of flatband and threshold voltages. For this reason, NBTI affects more

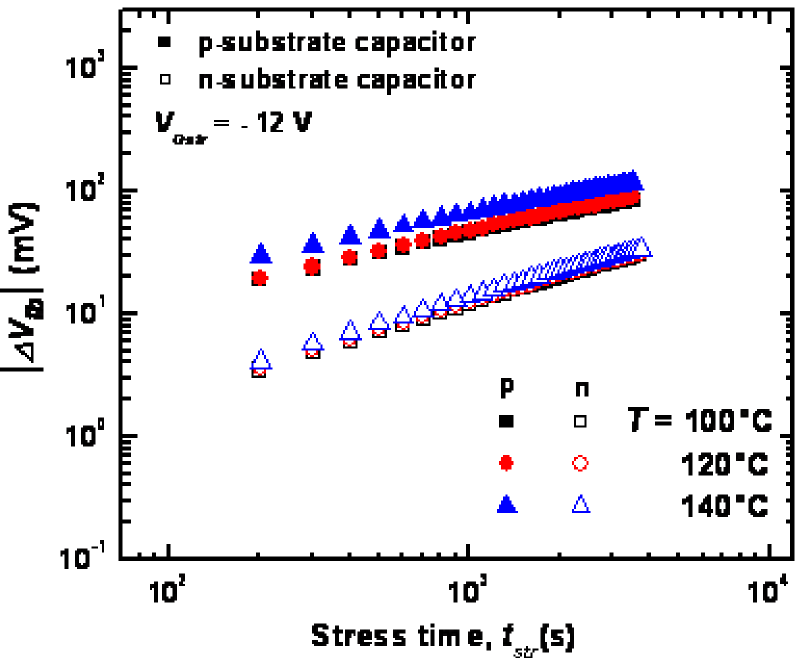


Figure III.20: NBTI-induced flatband shift (V_{fb}) as a function of stress time in p- and n-substrate capacitors at stress voltage of -12 V for different temperatures 100, 120, and 140 °C **[168]**.

Table III.1: Different voltage shifts.

Regime	Voltage shift	n-substrate	p-substrate
At flat-band	ΔV_{it}	$\frac{\Delta Q_{it}}{C_{OX}}$	$-\frac{\Delta Q_{it}}{C_{OX}}$
	ΔV_{ot}	$-\frac{\Delta Q_{ot}}{C_{OX}}$	$-\frac{\Delta Q_{ot}}{C_{OX}}$
At inversion	ΔV_{it}	$-\frac{\Delta Q_{it}}{C_{OX}}$	$\frac{\Delta Q_{it}}{C_{OX}}$
	ΔV_{ot}	$-\frac{\Delta Q_{ot}}{C_{OX}}$	$-\frac{\Delta Q_{ot}}{C_{OX}}$

severely ΔV_{fb} in p-substrate capacitors and ΔV_{th} in p-MOSFET (n-substrate). This is a reasonable reconciliation between aforementioned results **of Figs. III.18, III.19, and III.20.**

III.7- Conclusion

In this **Chapter**, we have given an overview of the experimental methods that we have used in this work to characterize the BTI phenomena in p-MOS and n-MOS transistors and capacitors of 20 nm SiO_2 gate oxide. At the beginning, we have tested the functionality of devices before any stress. The results are in accordance with those given by the supplier. Then the devices have been characterized at elevated temperature. All of them have shown a conventional behaviour with temperature. We point out here that all BTI measurements have been taken at the same temperature as in the stress phase to avoid any potential artefact caused by temperature-dependent parameters. Furthermore, we have shown that NBTI induces an opposite shifts as expected by mobile ion model. Finally, we have shown that, among all BTI degradations, NBTI in p-MOS transistor is the worst one. It is the mostly studied phenomenon in BTI-family effects. That is why; we focus, in the next chapters, on the NBTI degradation in p-MOS devices.

Chapter IV

ON THE FLY OXIDE TRAP METHOD (OTFOT): EXTRACTION AND ANALYSIS OF NBTI DEGRADATION PARAMETERS

IV.1- Introduction

IV.2- Theory and Concept of OTFOT Method

IV.3- Experimental Conditions

IV.4- NBTI-Induced Interface and Oxide Traps

IV.5- Time, Temperature, and Electric Field Dependence

IV.6- Empirical Life Time Estimation

IV.7- Gate Length Dependence of NBTI

IV.8- Geometric Component Effect in OTF CP-Based Methods

IV.9- NBTI Effect in LDD Region

IV.10- Discussion

IV.11- Conclusion

CHAPTER IV

ON THE FLY OXIDE TRAP METHOD (OTFOT): EXTRACTION AND ANALYSIS OF NBTI DEGRADATION PARAMETERS

IV.1- Introduction

As NBTI degradation issue is getting more critical for microelectronic devices, the need for an in-depth understanding of the NBTI basic mechanisms becomes crucial for the development of accurate models. Nowadays, it is more evident and widely accepted that NBTI effect on threshold voltage originates from two components; namely the interface-trap and the oxide-trap **[54,169-171]**. The relative contribution of interface and oxide traps to the threshold voltage shift after NBTI stress and recovery requires more experimental and theoretical investigation.

The classical methods have exclusively focused on the rapidity of the switching trap measurement **[50,54]**. The course toward the faster methods has led researchers to develop several models to explain their own data **[40,51,106,126,172]**. This situation creates a strong confusion regarding the NBTI behavior. However, in the actual working conditions, the device degradation is driven by the permanent component **[48]**.

Experimental separation between oxide- and interface-trap contributions is challenging due to the rapid recovery of the degradation. This relaxation has been explained by hole trapping in pre-existing switching oxide-trap and/or oxide-trap creation near Si/SiO_2 interface, while interface-trap does not relax **[22,35]**. However, Li et *al.* **[53,54]** have proposed that both components recover through a fast recovery component which is attributed to oxide-trap and a slow recovery attributed to the interface-trap. Nevertheless, the microscopic nature of defects behind these components and also which component dominates the NBTI stress and relaxation effects are still under debate.

To obtain the relative contribution of interface- and oxide-trap to the threshold voltage shift after NBTI stress and recovery, researchers combine on-the-fly interface-trap (OTFIT) **[55,130]** using charge pumping measurements to extract ΔV_{it} (induced by interface-trap increase) and on-the-fly V_{th} (OTF-V_{th}) **[57,103]** to extract ΔV_{th}. Subsequently, ΔV_{ot} (induced by oxide-trap increase) is found by subtracting ΔV_{it} from the amount of ΔV_{th}.

Despite the advantages of OTFIT and OTF-V_{th}, their combination can not directly provide information on the interface- and oxide-trap independently. The problem with this approach is not only due to the use of two methods, which causes more recovery, but also to the difference in band energy scanned by OTFIT and OTF-V_{th}. The extraction of the oxide-trap contribution ΔV_{ot} is indirect and depends on ΔV_{it} and ΔV_{th}.

Therefore, it is advantageous to develop methods that can measure both components separately. For this purpose, we suggest a new method, named on-the-fly oxide-trap (OTFOT) **[151,154]**. In this method, we propose the extraction of the NBTI-induced interface- and oxide-trap in the same

experimental setup and stress timeframe without changing the setup and devices, hence reducing the errors due to distinct measurements.

IV.2- Theory and Concept of OTFOT Method [151,154]

The OTFOT method is based on charge-pumping technique (*C-P*) **[56]** at low and high frequencies. Using alternatively C-P high and low frequencies, OTFOT method separates the interface-trap (ΔN_{it}) and border-trap (ΔN_{bt}) (switching oxide-trap) densities independently and also their contributions to the threshold voltage shift (ΔV_{th}), without the need for any additional methods. This method is derived from oxide-trap C-P (OTCP) method, developed for radiation effect **[68,173,174]**. It can give additional information on the behaviour of NBTI-induced interface- and oxide-trap.

IV.2.1- Charge recombined per cycle, $Q_{CP} = I_{CP} / f$ Characteristics

Before introducing OTFOT method, it is worth recalling the characteristics of charge recombined per cycle (Q_{CP}) as a function of frequency, as illustrated in **Fig. IV.1**. In practice, there is no abrupt variation between high and low frequencies. That is why we take 10 % of variation in I_{CP} as a criterion **[173]**. When the I_{CP} current reaches 10% of high frequency background I_{CP} signal, the additional current coming from border traps is considered. In our devices, 10% of variation corresponds to a frequency of about 10 kHz at room temperature and ΔV_G = 4 V **[174]**, as illustrated in **Fig. IV.1**. To measure $Q_{CP}(f)$, we maintain the gate voltage signal in a fixed position, where I_{CP} current reaches a maximum value, (i.e., $V_L < V_{fb}$ and $V_H > V_{th}$ for n-MOSFET and $V_L < V_{th}$ and $V_H > V_{fb}$ for p-MOSFET). V_L and V_H are the low and the high bias levels of the gate voltage signal, respectively. V_{fb} and V_{th} are the respective flatband and threshold voltages. The frequency varies, while ΔV_G, rise time (T_r), and fall time (T_f) and duty cycle parameters remain constant. However, high level and low level durations as well as the number of pulses parameters change with frequency. The Q_{CP} is constant in the absence of oxide-trap closer to Si/SiO_2 interface **[56]**, but in the presence of border-trap, it increases as the frequency is lowered **[136]**.

At low frequencies, the inclination of $Q_{CP}(f)$ shows an explicit and observable contribution of the border-trap. This is explained by conduction band to trap (CB-trap) and/or trap-to-trap tunneling processes **[136]**. The oxide-trap, within tunneling distance of Si/SiO_2 interface, fills and empties along

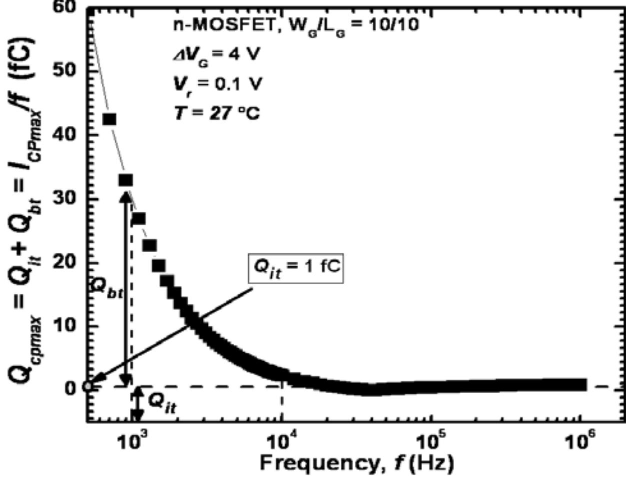


Figure IV. 1: Charge recombined per cycle versus frequency of n-MOS transistor with W_G/L_G = 10/10.

with interface-trap resulting in an increase in Q_{CP}. In fact, when the frequency is decreased, the applied gate voltage drives the device into inversion for longer times; allowing tunneling processes to take place where, not only the interface-trap switches, but also the oxide-trap within a distance appropriate for that particular frequency.

To avoid any ambiguity with metal-insulator-silicon conductance technique **[175]**, it is benefit to make a recall on interface-trap density energetically scanned by *C-P* technique. Indeed, in the metal-insulator-silicon conductance technique, the interface-trap density, contrary to low frequency *C-P* technique, decreases with decreasing frequency and near-midgap interface-traps are very low and known to have time constants able to reach 0.01 s (or 100 Hz in frequency domain). In *C-P* technique **[56]**, the boundaries of the active energy interval of interface-trap density are dependent on rise (t_r) and fall (t_f) times of the signal. Therefore, increasing t_r and t_f gives enough time for carrier emission process from energetically deep interface-trap to occur, thus reducing the number of traps that can contribute to I_{CP}. This fact narrows the scanned energetic band around midgap and reduces the I_{CP}. As the I_{CP} current is proportional to the density of interface traps, averaged across the active energy band, the interface-trap density is lower and located near midgap. This case is the same as the one previously cited **[175]**. However, in this work t_r and t_f are kept the same during frequency variation. Subsequently, the scanned energetic band is the same for different frequencies. To change frequency **[$f = (1/(t_r + t_f + T_H + T_L)$]**, we have varied time of high level (T_H) and time of low level (T_L). Zahid et *al.* **[176]** showed that the classical charge pumping happens during the rise and fall times, while the oxide slow trap (border-trap) charge pumping happens during high and low times (see **Fig. IV.2**). Therefore, the lower the frequency, the deeper the border traps.

IV.2.2- Measure/stress/measure (M/S/M) protocol of OTFOT method

Figure IV.3 shows measure/stress/measure (MSM) protocol of OTFOT method. During the stress interval, the voltage stress (V_{Gstr}) is applied, through a DC voltage, onto the gate of the device. After each stress time, a gate pulse train is applied, without modifying the experimental setup. In this case,

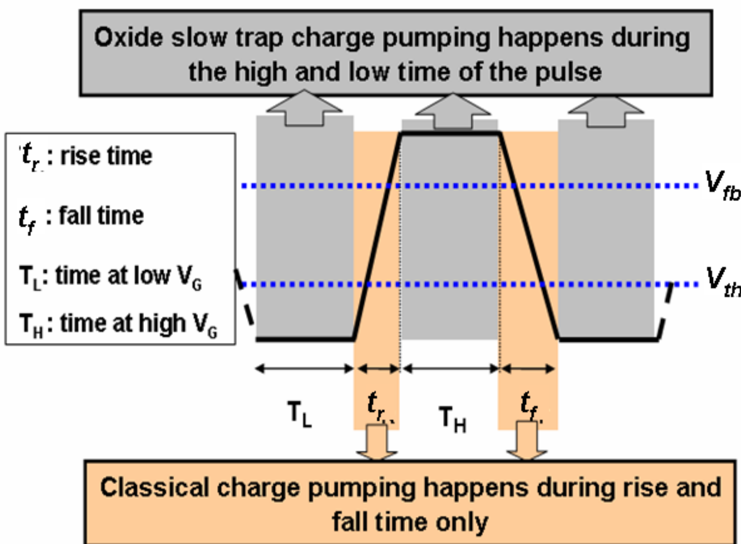


Figure IV.2: Charge pumping (C-P) during signal cycle for p-MOSFET. The classical *C-P* at the interface occurs during rise and fall times, while *C-P* in oxide happens during high and low time.

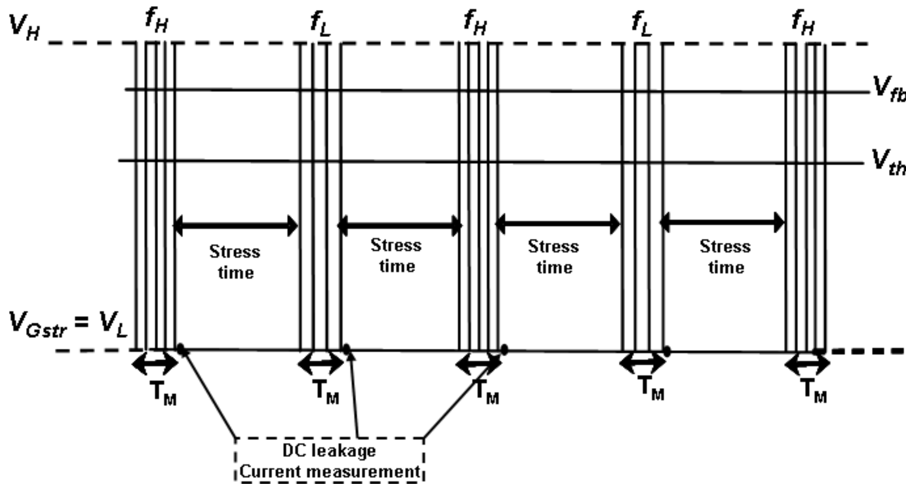


Figure IV.3: Measure/Stress/Measure (MSM) protocol of OTFOT method.

the gate trapezoidal signal of amplitude $\Delta V_G = V_H - V_{GSstr}$, where $V_L = V_{GSstr}$, duty cycle 50%, same rise and fall times, and two different frequencies (high, f_H and low, f_L) are applied alternatively to measure the maximum CP-currents ($I_{CP,H}$) and ($I_{CP,L}$). These currents result from the recombination of electrons and holes at the interface-trap (for high frequency) and at both interface- and border-trap (for low frequency). The low frequency value has to be chosen as low as the CP-current is distinguishable from leakage current. After each CP-current measurement, a DC leakage current is probed. In our transistors, the average DC gate leakage current is found to range between 1 and 5 pA at room temperature, it depends on the gate stress voltages - 2 to – 10 V, respectively. In **Fig. IV.4**, we give an example of as-measured CP-current Elliot curves for different frequencies and DC leakage current. Thus, before calculating Q_{CP} for different fields and temperatures, we first subtracted the DC leakage from the as-measured I_{CP}. **Figure IV.5** illustrates the DC leakage current measured at stress conditions after both high and low frequencies I_{CP} measurement. Obviously, the leakage current limits the scanned depth into the oxide layer when it is in the same order of the as-measured I_{CP}. However, it is not an issue in NBTI degradation since the latter is meanly located very near the interfacial region. In other words, the defects created by pure NBTI are located at the interface of Si/SiO_2 and in the oxide near the interface, of about tens of angstroms depth into the oxide, independently from the oxide nature and its thickness **[46,124]**.

Conventionally, the CP-current should be independent from the signal amplitude, (ΔV_G) when the transistor is in strong inversion **[46]**. However, it has been demonstrated that increasing ΔV_G even when fixing V_H and varying V_L (V_L is used for NBTI voltage stress, in OTFOT method), CP-current increases. This is attributed to stress-induced traps in both interface and oxide **[117,136]**. In fact, this effect has to be taken into account for comparison between recovery and stress phases. But, it does not constitute an issue if comparison is carried out in the same phase i.e. in the stress phase or in the relaxation phase independently. However, in the OTFOT method, the first value of the stress phase is taken as reference value to evaluate the NBTI degradation in stress phase, i.e. the incremented NBTI CP-current degradation is compared to the first value taken in the stress conditions of amplitude, before starting stress in time.

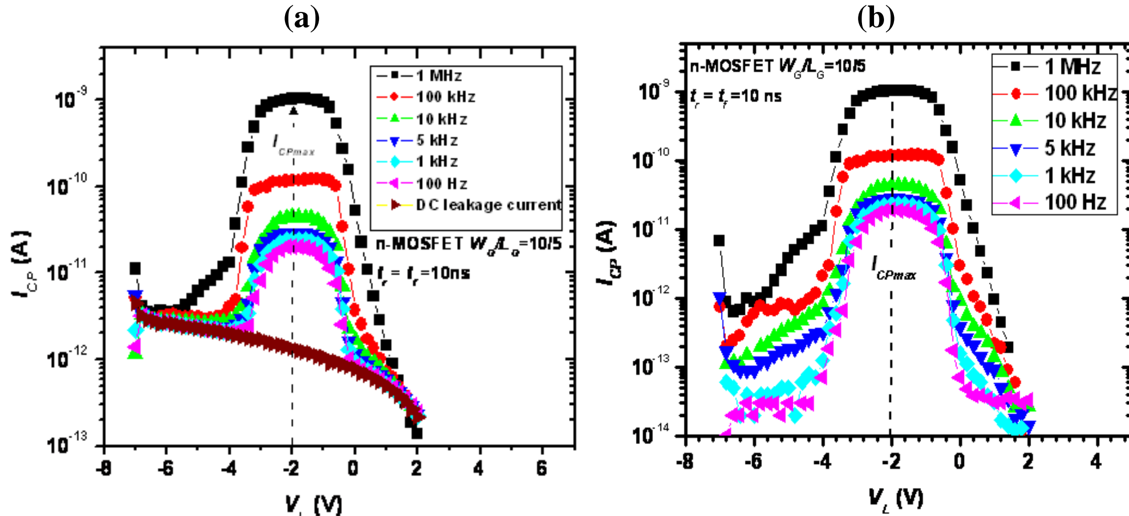


Figure IV.4: (a) As-measured I_{CP} before removing DC leakage current. (b) After removing DC leakage current

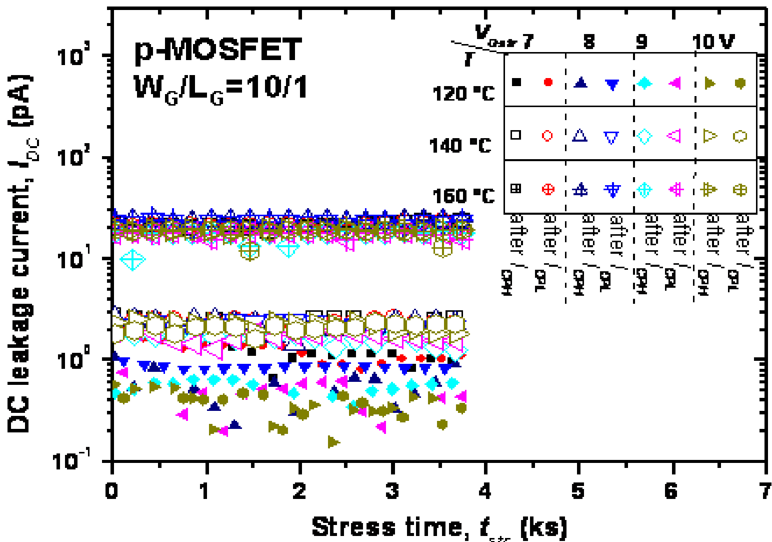


Figure IV.5: DC leakage current measured during NBTI stress using OTFOT method for different stress voltages and temperatures.

IV.2.3- OTFOT method Equations

As shown in **Fig. IV.3**, the proposed method measures the NBTI degradation at two CP frequencies, f_H and f_L applied alternatively on the transistor gate after stress time **[151]**. Both high and low frequency pulse trains have the same duration or delay during measurement. Therefore, the same delay measurement will induce similar relaxation at high and low frequency measurements. Consequently, if there is any relaxation effect on $I_{CP,H}$ and $I_{CP,L}$ measurement (or $Q_{CP,H}$ and $Q_{CP,L}$), it would be the same for both **[154]**.

Figure IV.6 illustrates the graphical approach to determine the contributions of stress-induced interface-trap (ΔN_{it}) and border-trap (ΔN_{bt}). *M* and *I*, in **Fig. IV.6,** denote measurement and intermediate values, respectively. $Q_{CP,L}$ straight line is illustrated higher than that of $Q_{CP,H}$. As previously mentioned, it is widely accepted that a decrease in frequency not only switches the interface-trap but also the border-trap, inducing an increase in Q_{CP}. From data fits, the intermediate values of the maximum of I_{CP} (or Q_{CP}) can be determined by interpolation.

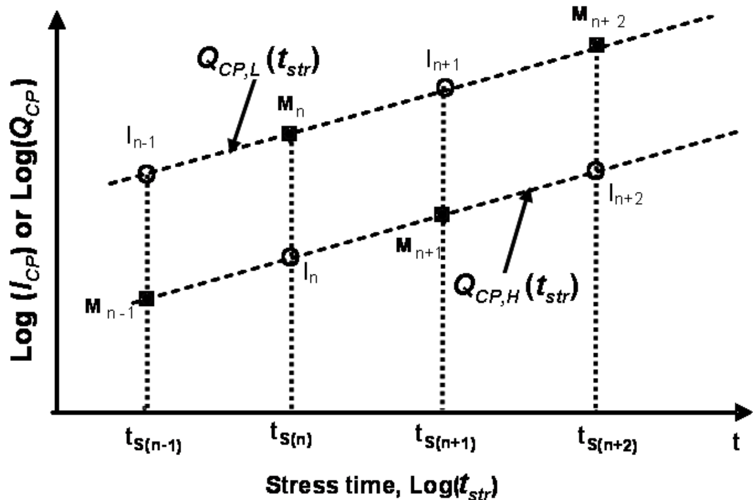


Figure IV.6: Illustrative approach for extracting the contributions of NBTI-induced interface-trap (ΔN_{it}) and border-trap (ΔN_{bt}).

At stress time *n* and *n+1*, the NBTI-induced interface-trap densities are extracted using the following equations **[151]**:

$$N_{it}(t_S)_n = \left|\frac{I_{CP,H}(t_S)_{I_n}}{qf_H A_G}\right| = \left|\frac{Q_{CP,H}(t_S)_{I_n}}{qA_G}\right| \quad \text{(IV.1)}$$

$$N_{it}(t_S)_{n+1} = \left|\frac{I_{CP,H}(t_S)_{M_{n+1}}}{qf_H A_G}\right| = \left|\frac{Q_{CP,H}(t_S)_{M_{n+1}}}{qA_G}\right| \quad \text{(IV.2)}$$

and border-trap densities by

$$N_{bt}(t_S)_n = \left|\frac{I_{CP,L}(t_S)_{M_n}}{qf_L A_G} - \frac{I_{CP,H}(t_S)_{I_n}}{qf_H A_G}\right| = \left|\frac{Q_{CP,L}(t_S)_{M_n}}{qA_G} - \frac{Q_{CP,H}(t_S)_{I_n}}{qA_G}\right| \quad \text{(IV.3)}$$

$$N_{bt}(t_S)_{n+1} = \left|\frac{I_{CP,L}(t_S)_{I_{n+1}}}{qf_L A_G} - \frac{I_{CP,H}(t_S)_{M_{n+1}}}{qf_H A_G}\right| = \left|\frac{Q_{CP,L}(t_S)_{I_{n+1}}}{qA_G} - \frac{Q_{CP,H}(t_S)_{M_{n+1}}}{qA_G}\right| \quad \text{(IV.4)}$$

where q (C) is the electron charge, A_G (cm^2) is the gate area, $I_{CP,H}$ (A) and $I_{CP,L}$ (A) are the maximum CP-current at high, f_H (Hz) and low frequencies, f_L (Hz), respectively, and $Q_{CP,H}$(C) and $Q_{CP,L}$ (C) are the maximum charge recombined by cycle at high, f_H (Hz) and low frequencies, f_L(Hz), respectively. Q_{CP} at points I_n and I_{n+1} are the interpolated values corresponding to the measured ones at points M_n and M_{n+1} and are determined by interpolation as follows:

$$Q_{CP,H}(t_S)_{I_n} = \frac{Q_{CP,H}(t_S)_{M_{n+1}} + Q_{CP,H}(t_S)_{M_{n-1}}}{2} \quad \text{(IV.5)}$$

$$Q_{CP,L}(t_S)_{I_{n+1}} = \frac{Q_{CP,L}(t_S)_{M_{n+2}} + Q_{CP,L}(t_S)_{M_n}}{2} \quad \text{(IV.6)}$$

Under the assumption that interface traps are of amphoteric nature **[26,177]**, they affect V_{th} shifts in n- and p-channel MOSFET differently. As shown in **table III.1** of **chapter III**, ΔV_{it} = - q $\Delta N_{it}/C_{ox}$ and ΔV_{ot}= - q $\Delta N_{ot}/C_{ox}$ for p-channel transistor which is more severely affected than n-channel MOSFET.

Using OTFOT method, the NBTI-induced interface traps are measured in strong inversion of p-MOS transistor. Therefore, the threshold voltage shift is calculated as follows:

$$V_{th}\left(t_S\right)_n = V_{it}\left(t_S\right)_n + V_{bt}\left(t_S\right)_n = -\frac{qN_{it}\left(t_S\right)_n}{C_{ox}} - \frac{qN_{bt}\left(t_S\right)_n}{C_{ox}} \quad \text{(IV.7)}$$

$$\begin{aligned} \left|\Delta V_{th}\left(t_S\right)_n\right| &= V_{th}\left(t_S\right)_n - V_{th}(0) = \frac{q}{C_{ox}}\left(\Delta N_{it}\left(t_S\right)_n + \Delta N_{bt}\left(t_S\right)_n\right) \\ &= \Delta V_{it}\left(t_S\right)_n + \Delta V_{bt}\left(t_S\right)_n \end{aligned} \quad \text{(IV.8)}$$

where ΔV_{th} (V) is the NBTI stress-induced threshold voltage shift, ΔV_{it}(V) and ΔV_{bt} (V) are contributions of NBTI stress-induced interface-trap and border-trap to voltage shift, respectively. Matlab program extraction of OTFOT method parameters is given in **appendix (D.1)**.

IV.3- Experimental Conditions

The detailed experimental hardware setup is given in **Chapter III**, section **§ III.3**. Here, we focus on the MSM protocol conditions. The stress interval is kept the same during all MSM cycle. Taken as an example, the whole stress time cycle is fixed at 3600 s (1 hour). The stress is periodically interrupted after 100 s and a trapezoidal pulse with f_H and f_L have been alternatively applied to measure $I_{CP,H}$ and $I_{CP,L}$, as illustrated by the algorithm shown in **Fig. IV.7**. We use signal of f_L after odd stress interval and f_H after even stress interval. The measurement duration is about 0.4 s. We varied the temperature (T) from room temperature (~27°C) to 200°C and stress voltage ($V_{Gstr} = V_L$) from 2 V to 9 V, while keeping V_H at 2 V in all experiments (the stress field was varied from 2 V/cm to 4.5 V/cm), unless otherwise indicated. We cannot exceed 4.5 V/cm due to equipment limitation **[154]**.

In order to extract the NBTI effect at high and low frequencies, it is important to set the following conditions:

- Signal conditions: the rise and fall times of the trapezoidal signal have to be kept the same to ensure that the upper and lower energy boundaries of band gap active energy remains unchanged. Since the duty cycle affects the NBTI measurements, conditions should be the same for both high and low frequency signals **[57]**. The OTFOT method uses the same V_H (relaxation) and the same $V_L = V_{GSstr}$ (stress) for both high and low frequency measurements.
- Devices: to avoid polluting CP measurements with parasitic leakage current and tunneling current, we use thick gate oxide (20 nm), since the basic mechanisms behind the NBTI are assumed to be the same in both thin and thick oxides **[46,124]**. In other words, the defects created by NBTI are located at the interface of Si/SiO_2 and in the oxide near the interface, of about tens of angstroms depth into the oxide, and they are independent of the oxide nature and its thickness.

To avoid additional charge contribution to CP-current at stress level (i.e. when V_L is increased), OTFOT uses as a reference the first I_{CP0} measured at stress level, $V_{Gstr} = V_L$ during the stress phase. Therefore, OTFOT gives the NBTI stress-induced traps starting from the first measured point at stress phase. However, in OTFIT method, the initial reference measurement is taken at V_L corresponding to relaxation phase, where an additional contribution from interface and oxide traps due to ΔV_G increase is attributed to NBTI. As a consequence, OTFIT-I_{CP} data need correction before NBTI estimation

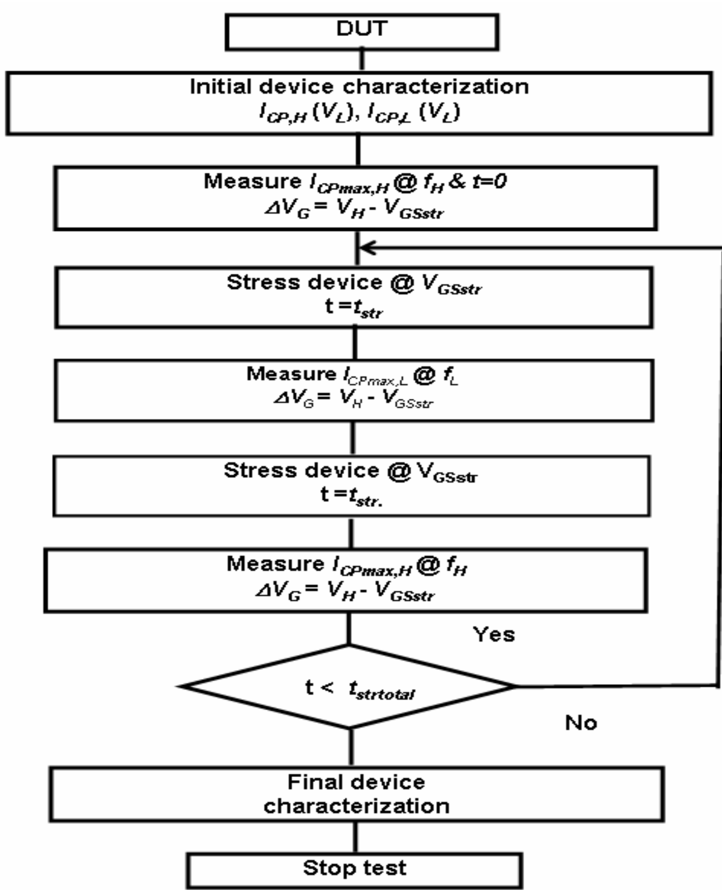


Figure IV.7: Measure/stress/measure (MSM) Protocol sequence Algorithm flow chart of OTFOT method.

[117]. In **table I**, we summarize the pros and cons of OTFOT method compared to OTFIT and OTF-V_{th} methods.

IV.4- NBTI-induced Interface and Oxide Traps

Using the experimental conditions, described in section **§ VI.3,** we have extracted the as-measured NBTI CP-current normalized to the gate area at low (1 kHz) and high (1 MHz) frequencies, unless otherwise specified (see **Fig. IV.8**). The CP-current increases in absolute value with stress voltage, indicating an increase of interface-trap at high frequency **[Fig. IV.8 (a)]**, while at low frequency **[Fig. IV.8 (b)]** both interface- and border-trap are enhanced **[178]**.

Before extracting the contributions of interface-trap and border-trap to the voltage shift, we illustrate in **Fig. IV.9** the extraction of the interpolated points by OTFOT method using **Eqs. IV.5 and IV.6** at high and low frequencies, respectively (see the triangular symbol). **Figure IV.9** clearly shows the succession between low and high frequency measurements for NBTI degradation in p-MOSFET at 100 and 150 °C for V_L = - 9 V.

To understand how the MSM protocol influences NBTI-induced trap dynamic, we have experimented two scenarios. In the first time, all temperature and electric field stresses are successively applied on the same transistor. After each stress of one hour, we characterize the recovery phase of 1 hour duration for each temperature and electric field. The second one consists of using each couple of voltage and temperature stresses on only one transistor without recovery characterization.

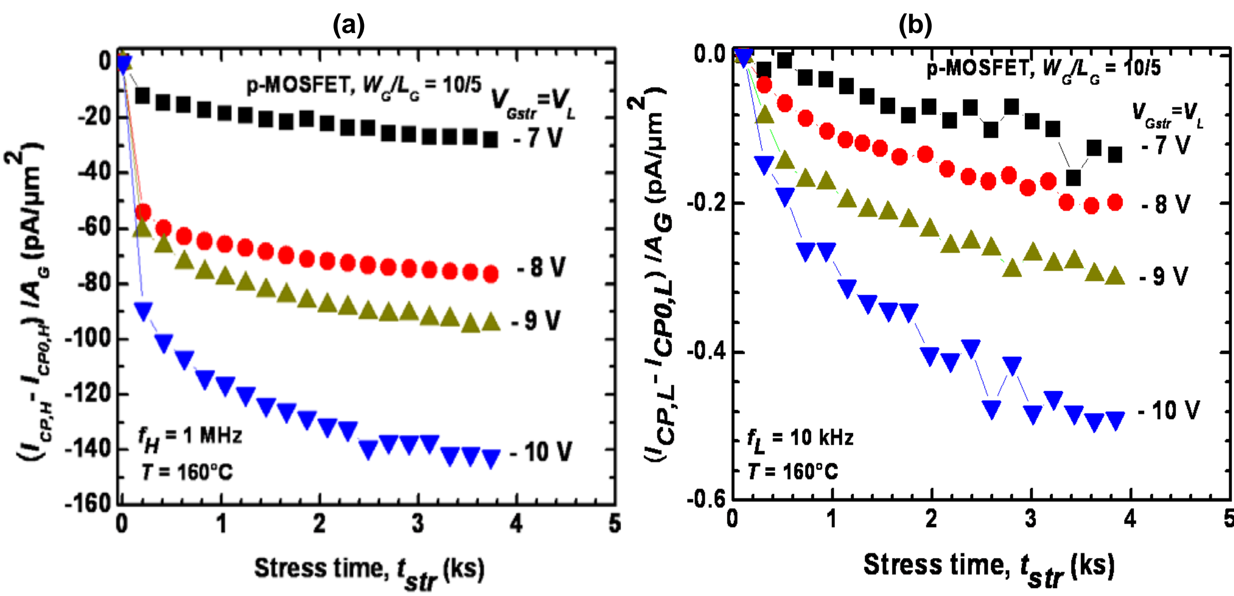


Figure IV.8: As-measured CP-current (a) at high frequency and (b) at low frequency. Data are extracted at 160°C for different stress voltages.

TABLE I: Comparison of OTFOT Method to OTF Methods

Method	ΔV_{it}	ΔV_{bt}	ΔV_{th}	Effect on the measurement
OTF-V_{th} **[57]**			X	- Initial pre-stress I_0 degrades I_{DS}. - Under-estimation of ΔV_{th}.
OTFIT **[55,130]**	X			- Initial pre-stress I_0 corresponds to relaxation phase. - Over-estimation of ΔV_{it}.
OTFOT **[151]**	X	X	X	- Initial pre-stress I_0 corresponds to first point of stress phase. - At f_L only a part of oxide traps is sensed.

First Scenario

Charge pumping current as a function of stress time is presented in **Fig. IV.10** for different temperatures [see **Fig. IV.10 (a)**] and voltages [see **Fig. IV.10 (b)**]. It shows straight lines of I_{CP} increase with respect to stress time in log-log scale at 1 MHz. As mentioned above, only the interface-trap (N_{it}) contributes to CP-current at high frequency, hence the I_{CP} behavior is in good coherence with reaction-diffusion (R-D) model that predicts a linear time dependence of NBTI interface-trap creation in log-log scale. **Figure IV.10 (a)** illustrates power-law time dependence with exponent (n) of about 0.25-0.49 for a temperature range between 25-200 °C and stress voltage of - 8 V. The exponent (n) remains unchanged at T = 100, 150, and 200 °C. In the reaction-diffusion framework model, the interpretation of the NBTI phenomenon is related to the bond breaking of the hydrogen species at the interface. Results of **Fig. IV.10 (a)** plainly show that n of ΔI_{CP} degradation is approximately about n ~ 0.5 and nearly temperature independent, except for T ~ 27 C°, where n ~ 0.25. At low temperature n is about 0.25 which is speculatively corresponding, if we consider the R-D model, to the neutral hydrogenate species (H). However, as temperature increases, n increases to ~ 0.5 which corresponds to ionized hydrogen (H^+). The same fact is observed in **Fig. IV.10 (b)** regarding the influence of the

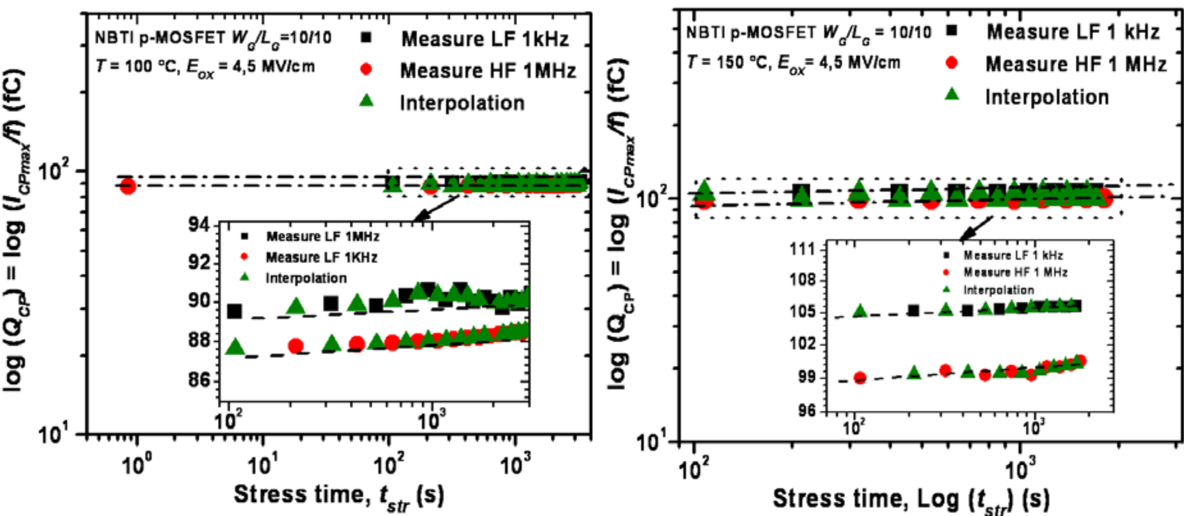


Figure IV.9: Charge recombined per cycle versus stress time extracted by OTFOT method for NBTI degradation in p-MOSFET at V_{Gstr} = - 9 V (a) T = 100 °C and (b) 150 °C. Triangular symbols illustrate the interpolated data.

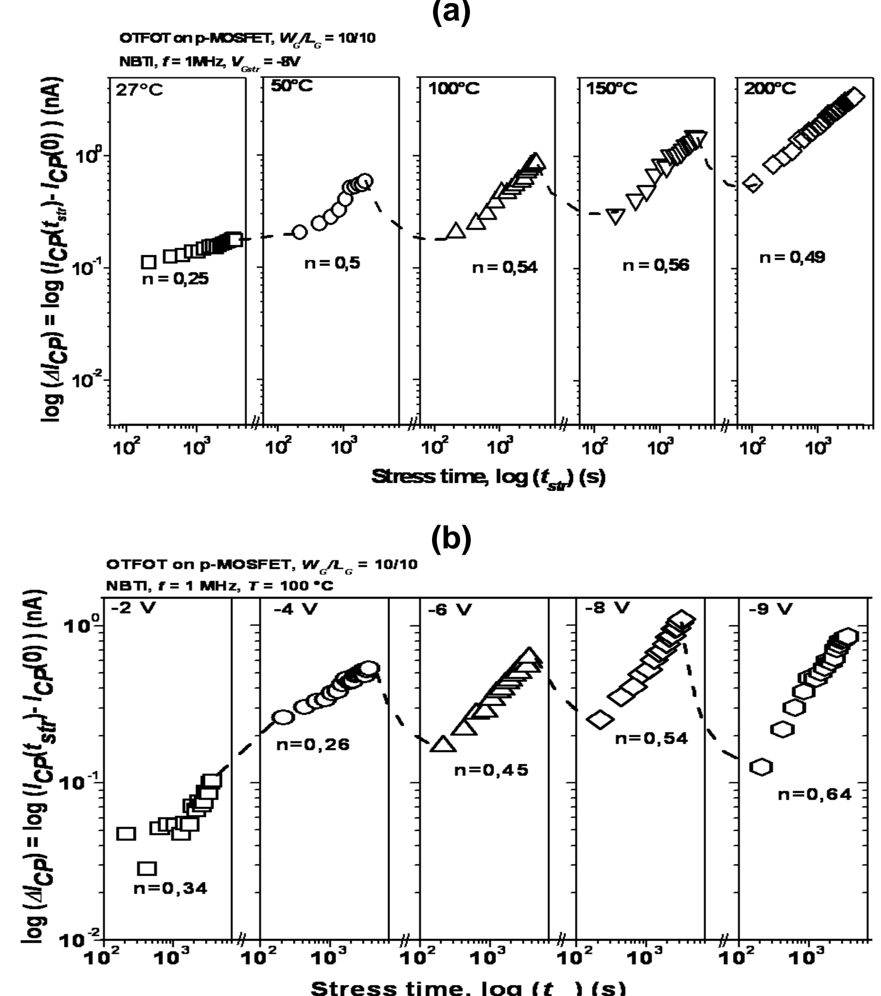


Figure IV.10: p-MOSFET charge pumping current versus stress time. (a) for V_{Gstr} = - 8 V (- 4 MV/cm) and different T from 27 to 200 °C at 1 MHz, in log-log scale. (b) For T = 100 °C and different V_{Gstr} from - 2 to – 9 V at 1 MHz in log-log scale.

electric field on n. For low electric field, n is lower compared to that of high field, where it approaches 0.64. The value of n is larger than that observed in the literature **[55,117]** using OTFIT and OTF-V_{th}. We believe that this value is an artefact induced by the relaxation effect caused by the

protocol of the first scenario, which consists of using all temperature and voltage stresses as well as the recovery on the same transistor. Another source of discrepancies could be also the gate length effect, because it influences the NBTI degradation **[179-181]**, thus it is interesting to use transistors with gate length below 10 µm. This point will be discussed hereafter. On the other side, ΔI_{CP} currents of **Fig. IV.10** are plotted side to side to illustrate the relaxation phenomenon. This latter is indicated by dashed lines and increases with temperature. We think that it is mainly caused by the experimental procedure (i.e. using all stresses on the same device and relaxation after each NBTI stress phase). Despite the protocol used in our experiments, **Fig. IV.10 (a) and (b)** shows the expected R-D relationship between NBTI interface-trap creation and stress time. However, both figures do not show any recovery at low field and low temperature as opposite to high electric field and high temperature cases. The absence of the relaxation at both low temperature and low electric field indicates that the interface-trap creation mechanisms are somehow different from the traditional NBTI R-D mechanism, or there is not enough released hydrogen to re-saturate the dangling bonds that can be detected by our setup.

Nevertheless, the exponent of ΔN_{it} (n-ΔN_{it}) is over estimated if compared to previously published data **[17,50,54,55,117,182]**. In addition, n-ΔN_{it} is field dependent; the higher the field the larger n, while it remains temperature independent. This discrepancy is mainly caused by the experimental procedure (i.e. using the same device for all stresses).

<u>Second scenario</u>

To confirm this statement, we carried out a different scenario of experimental measurements that consists of using each couple of temperature/voltage stress on only one transistor without recovery characterization. The results show a compliance with previous data **[17,50,54,46,117,182]** regarding the exponents of ΔN_{it}, ΔN_{bt}, and ΔV_{th}.

Figure IV.11 illustrates ΔN_{it} and ΔN_{bt} densities as a function of voltage and temperature in log-log scale. On the right axis, we present the voltage shifts induced by interface and border traps. The NBTI stress-induced ΔN_{it} and ΔN_{bt} time characteristics show a power-law time-dependence (t^n) for both interface-trap and border-trap with exponent of 0.16-0.17 and 0.03-0.08, respectively **[151]**. These results are in perfect agreement with those previously published by different groups **[50,54,182]**. The first exponent is often attributed to H_2 diffusion mechanism in the R-D framework **[17]**, while in conventional *C-P*, n is about 0.3 **[54]**. Therefore, n = 0.16 demonstrates reduction of recovery during stress and subsequently the accuracy of the method used in this work. The second exponent is much less than ΔN_{it} exponent indicating two possible processes of NBTI degradation. It is attributed to hole trapping/detrapping process at the pre-existing border-trap, or newly generated hole trapping defects **[183]**. The scattering in n values of trapping/detrapping mechanism at pre-existing border-trap could be explained by the dispersive energetic and spatial distributions of border-trap and/or due to further generated hole trapping sites.

Not only our experimental method shows the same exponents as those found elsewhere **[17,50,54,182]**, but it is easy to use without any pre-assumption and/or additional method. Li *et al.* **[45]** combine two methods OTF-V_{th} and OTFIT to extract ΔN_{bt} from ΔV_{th} and ΔN_{it}. These latter can affect ΔN_{bt}. Other research group **[50,182]** used the cyclic dynamic of NBTI which is assumed to be solely

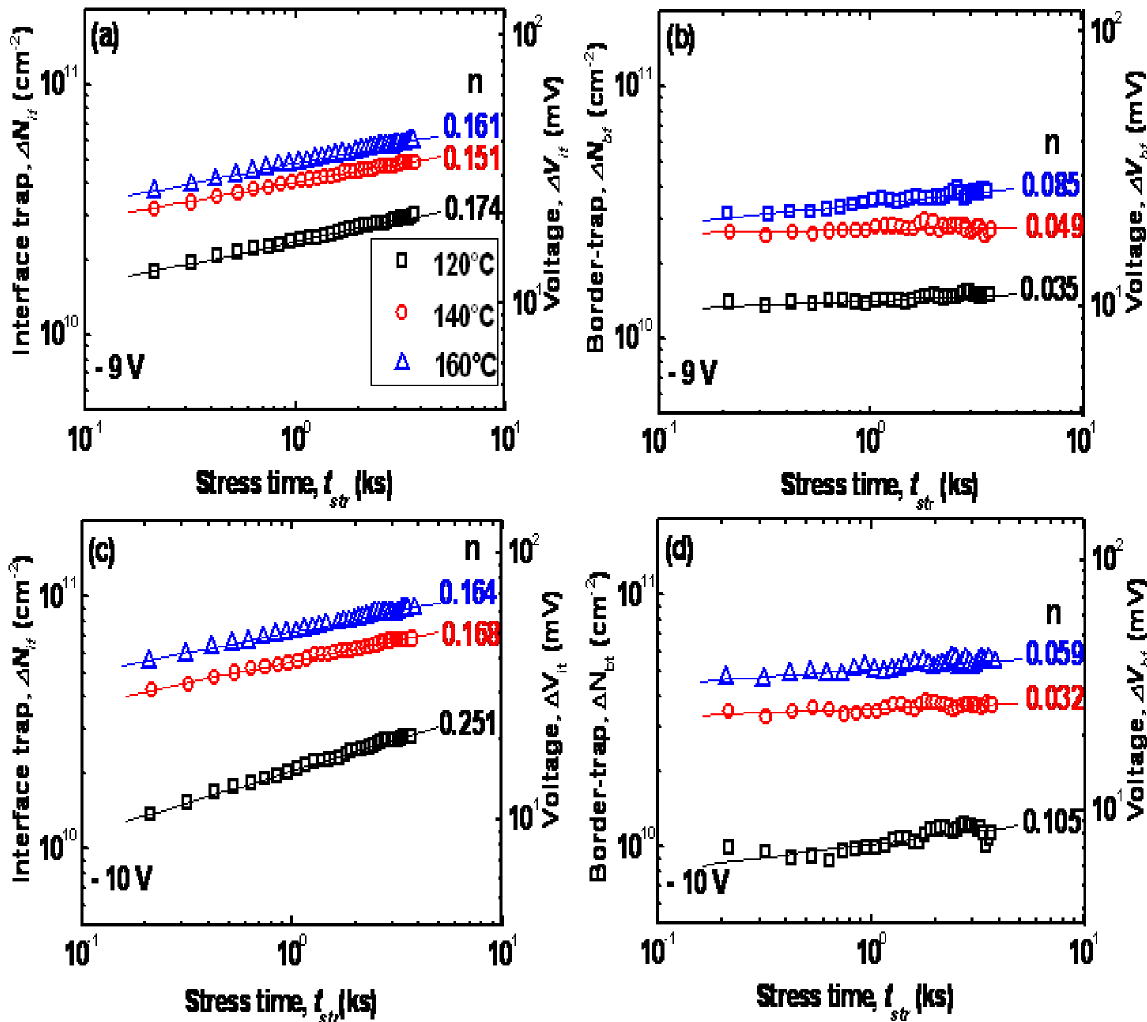


Figure IV.11: NBTI stress-induced interface- and border-trap ΔN_{it} and ΔN_{bt}, (on the left axis) as well as their contribution to voltage shift ΔV_{it} and ΔV_{bt} (on the right axis), respectively.

governed by hole trapping/detrapping mechanism with the assumption that ΔN_{it} is permanent. But, it has been shown that under specific conditions, the permanent component can relax as the recoverable component **[54,58]**. Moreover, the cyclic dynamic method gives a large exponent (0.493) **[50,182]**. To obtain 0.16, the authors assume hole saturation within 1 s. However, our analysis of ΔN_{it} data is only based on as-measured degradation without any pre-assumption, except for low frequency value **[151]**. They show a good agreement with H_2 paradigm.

According to the results, it is clear that the measurement protocol influences the pure NBTI degradation. That is why, in this thesis, we have used one transistor for only one couple of temperature/voltage stress to avoid any artefact due to multi-stresses on one transistor.

IV.5- Time, Temperature, and Electric Field Dependence of NBTI

NBTI degradation in MOSFET devices is often found to depend on temperature, oxide electric field, and power law time. The electrochemical reaction, assisted by field and temperature at the interface induces threshold voltage shift. The later empirically follows the expression given below **[20,26]**:

$$\Delta V_{th} = A\exp(E_{OX} / E_{ref})\exp(-E_a / kT)t^n \quad \text{(IV.9)}$$

where A is the pre-factor constant depending on the process parameters. E_{ref} is the reference electric field ($E_{ref} = 1/\gamma$, γ is the electric field acceleration factor). E_a is the apparent activation energy. n is the time exponent. All these parameters are experimentally fitted parameters. The temperature dependence is modeled to follow Arrhrenius' law. This expression reveals that NBTI degradation can be accelerated by increasing the temperature and increasing the absolute value of the gate voltage in p-MOSFETs. This can be used for setting up NBTI experiments.

It is important to determine the various parameters of this equation to predict NBTI degradation at any given time, temperature and oxide electric field. In fact, all NBTI models face the same challenge to explain the correct electric field acceleration and temperature activation of the ΔV_{th} degradation. On the other hand, n, E_a, and γ constitute indicator parameters of physical mechanisms that govern threshold voltage shift. For example, if the interface-trap generation (ΔN_{it}) is the unique process at the origin of the NBTI-induced ΔV_{th}, therefore both their electric fields and temperature accelerations will be the same.

IV.5.1- NBTI-Time dependence

In addition to ΔV_{it} (V) and ΔV_{bt} (V), we have extracted and plotted ΔV_{th} on **Fig. IV.12.** This latter shows NBTI-induced ΔV_{th} as a function of stress time for different electric fields at 140 and 160 °C. All curves show the same behavior with stress time, electric field, and temperature. They exhibit a power law with exponent of 0.11 in log-log scale **[151]**. Once again, the same ΔV_{th} log-log scale time degradation exponent was depicted in a previous experiment **[50]** using ultra fast *I-V* method and subsequently adds further proof supporting OTFOT method. However, the earlier studies showed a power-law time dependence with an exponent (n) of 0.25 **[12,184]**. Later, when it was pointed out that the relaxation affects n, fast measurement methods have revealed n < 0.25 **[53]**. n depends on the measurement setups. Longer the delay between NBTI stress and its characterization is, larger n is. It

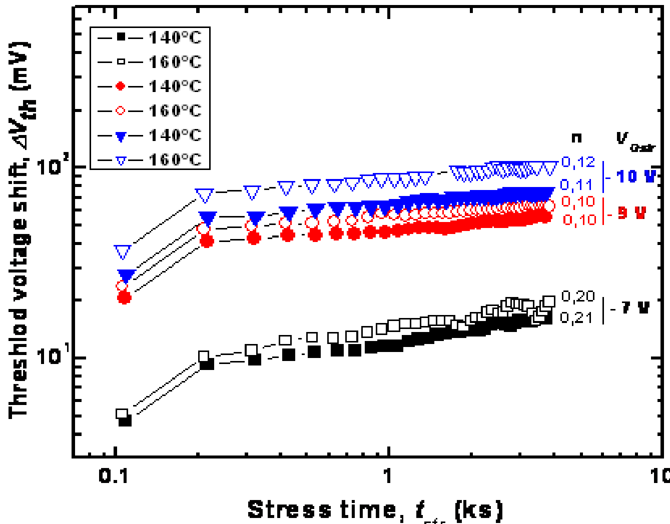


Figure IV.12: NBTI-induced threshold voltage shift, ΔV_{th} for different voltages at 140°C and 160°C versus stress time. ΔV_{th} curves exhibit power law with average exponent of 0.11.

should be noted that even with the improvements brought to the R-D model, it is still suffering from intrinsic limitations regarding the relaxation phase **[62]**, and the exponent (*n*) **[50]**.

IV.5.2- NBTI-Temperature dependence

It is well established that NBTI degradation is a thermally activated process **[185]**. In **Fig. IV.13**, we present ΔV_{th} –OTFOT degradation as a function of temperature at stress voltages of – 8 and -9 V and different stress times. The apparent activation energy of threshold voltage shift in our devices is found to lie between 0.28 and 0.33 eV. These values correspond to the activation energy of H_2 diffusion described by Chakravarthi et *al.* **[20]**. Tsetseri et *al.* **[25]** have shown that the activation energy of dissociation for P-H complex in the depletion region is about 0.3–0.4 eV. For a certain period of time the hydrogen atom located in the inversion layer stays neutral and then changes into proton (H^+), by picking up a hole. At negative bias stress conditions, the free protons drift to the Si/SiO_2 interface. As both dangling bonds and the protons are positively charged, it is very unlikely that proton passivates an interface-trap. It will preferably moves close to Si-H bond which it can break by forming H_2. Others reported activation energy of 0.75 eV and 0.41-0.45 for atomic and molecular hydrogen diffusion in SiO_2, respectively **[186]**.

Very different values are often measured for the apparent E_a and various explanations have been given. Ang et *al.* **[187]** have attributed the non-Arrhenius behavior to the superposition of two defect generation mechanisms with different E_a; hole trapping $E_a \approx$ 0.01-0.02 eV and hydrogen diffusion with $E_a \approx$ 0.25 eV. The exact physical mechanism for the threshold voltage degradation is still unclear. Different types of defects contribute to the total NBTI degradation. The most dominant are interface traps (resulting from *H* de-passivation of Si dangling bonds at the interface) and traps present in the bulk dielectric **[22]**. To increase our understanding on the net apparent activation energy of V_{th} shift (E_a-ΔV_{th}) in our devices, we have plotted ΔN_{it} and ΔN_{bt} as a function of temperature in **Fig. IV.14** from which the apparent activation energy of interface- and border-trap creation, E_a-ΔN_{it} and E_a-ΔN_{bt}, are extracted. E_a-ΔN_{it} and E_a-ΔN_{bt} are in the range of 0.18 eV < E_a < 0.26 eV and 0.31 eV < E_a < 0.43 eV, respectively. The spread in the apparent activation energy suggests different defects with different structures. These defects do not necessarily have the same activation energies. In fact, there will be distribution of activation energies necessary for trap creation. The distribution may be related to Si-

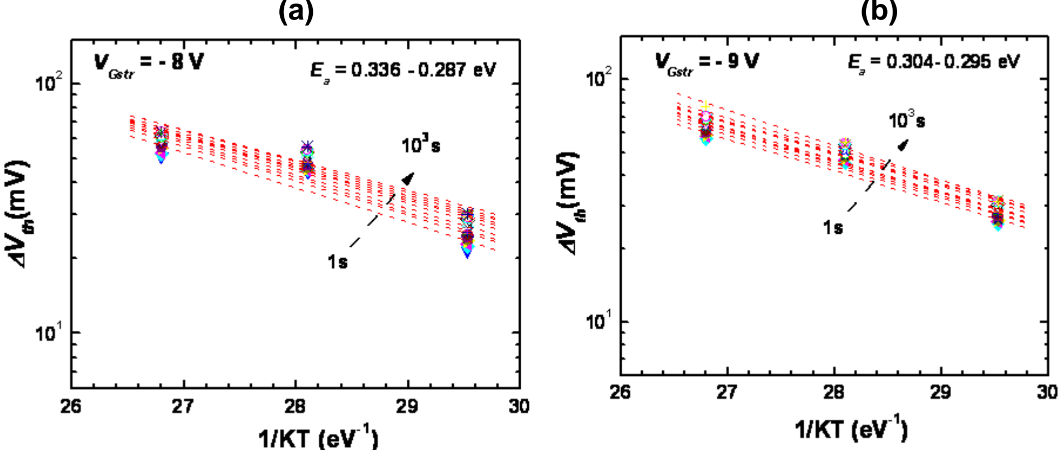


Figure IV.13: NBTI-induced threshold voltage shift as a function of temperature for different stress time and at stress voltage of – 8V (a) and -9 V (b). The apparent activation energy is roughly equal 0.3 eV.

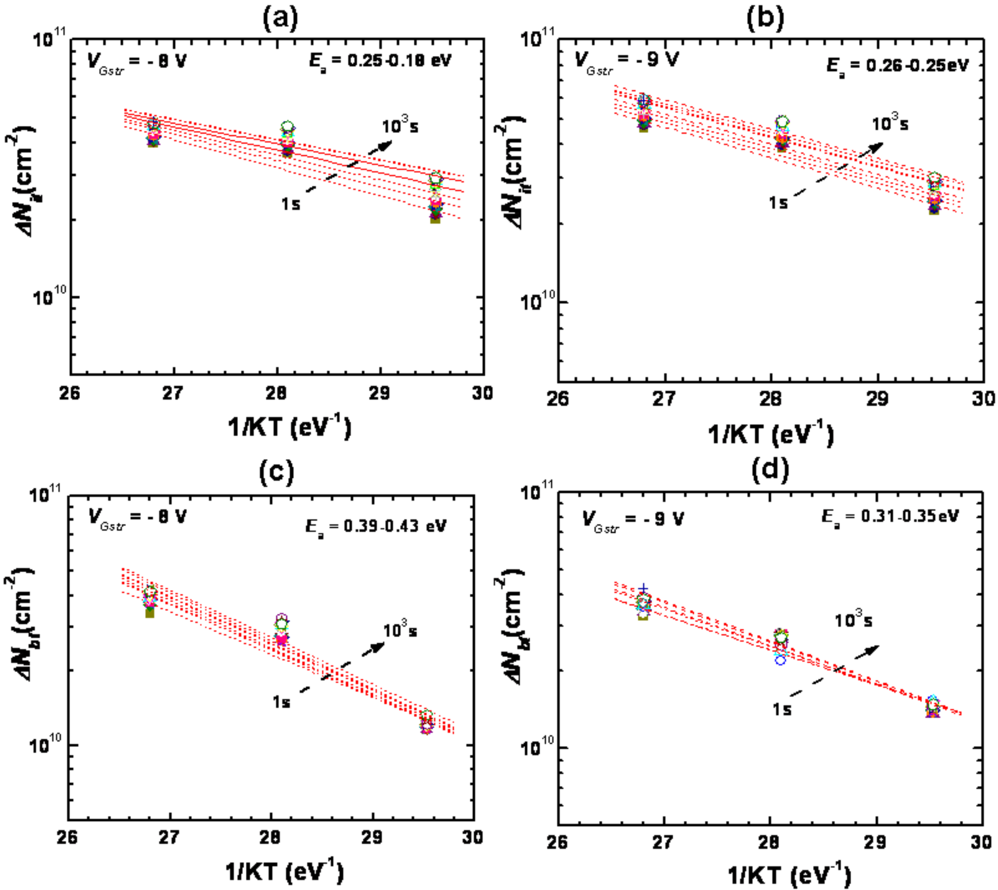


Figure IV.14: NBTI-induced ΔN_{it} and ΔN_{bt} as a function of temperature for different stress time and at stress voltage of – 8V and -9 V. E_a-ΔN_{it} and Ea-ΔN_{bt} equal 0.18-0.26 and 0.31 - 0.43 eV, respectively.

SiO_2 interface and bulk SiO_2 disorders, especially the interfacial region (see **Chapter I** section **§ I.4.4**), where the microstructures of border traps are different with subsequent different activation energies. This dispersion has been pointed out by Schroder et *al.* **[188]** and will be detailed in **Chapter V**. They have reported that E_a appears to be in the range of 0.15 eV < E_a < 0.325 eV, depending on the chemical composition of the dielectric and on which dominates the reaction kinetic and on species involved (for example H_2O, *H, SiH, SiN, SiO, SiF*, etc).

More recently, Mahapatra et *al.* **[48,119]** have experimentally found that 0.6 eV is consistent with molecular (H_2) diffusion at longer stress time and proves that H_2 diffusion governs the long-term temperature dependence of NBTI measurements. On the other hand, it has been suggested that the activation energy for hole trapping in the pre-existing traps is ~ 0.04 eV, which is typically expected in any hole trapping process that involves tunneling and no structural relaxation, while the signature of interface-trap creation is 0.1 eV in nitrided oxides **[50]**. The low apparent activation energy is explained by nitrogen-enhanced NBTI degradation, where nitrided oxide contains more water **[189]**. Moreover, Tan et *al.* **[190]** have shown that the stress-induced oxide traps for pure oxide and rapid thermal-nitrided oxides (RTNO) present E_a of 0.21 eV and 0.15 eV, respectively. Similarly to the oxide traps, the nitrogen incorporation in the interface region reduces the E_a of interface state generation **[190]**. This fact indicates that nitrogen enhances NBTI effect. Nitrided oxides are also reported elsewhere **[102,191]** to have lower power law slopes *n* and lower E_a compared to non-nitrided oxides. At low temperatures and short term stress, ΔV_{th} shift is determined by hole trapping at nitrogen defect

precursors. At the higher temperatures and long term stress, classical hydrogen diffusion takes place. It was proposed that previously published reports of temperature-dependent *n* values in thin SiO_2 may be due to trace amounts of nitrogen in those oxides **[44]**. This mechanism may account for V_{th} recovery being due to ''oxide charges'' and not interface traps **[22]**.

Furthermore, using time-dependent defect spectroscopy (TDDS) method, Grasser et *al.* **[126,192,193]** have shown that the physical microscopic activation energies of the individual trap is about 0.5 – 1.2 eV in small gate area devices. They argued that a small overall macroscopic activation energy (0.1 eV) **[50,119]**, observed in large area devices, is the result of the individual trap energy superposition. Thus the macroscopic activation energy in large area is an apparent activation energy resulting from a large number of defects **[62]**.

IV.5.2- NBTI-field dependence

From empirical **Eq. IV.9**, NBTI-induced ΔV_{th} is exponentially dependent on electric field. The slope of ΔV_{th} versus electric field in semi-log scale is the field acceleration factor (γ). The reference electric field (or critical electric field) is the inverse of γ. **Figure IV.15** depicts NBTI-induced ΔV_{th} in our stressed devices under different stress voltages for one hour at 140 and 160 °C. Our experiments show γ varying from 0.77 to 0.95 cm/MV, roughly the same factor is found elsewhere (0.6-0.86 cm/MV) for SiO_2 **[34,42]**. In order to capture the field dependent mechanisms, we investigated γ of ΔN_{it} and ΔN_{bt}. **Figure IV.16** illustrates ΔV_{th} components which are extracted using OTFOT **[151]**. Both components show almost the same acceleration factor of about 1cm/MV, suggesting the same field dependence mechanism for interface and border traps located in the interfacial oxide region of our devices.

The actual gate oxide field dependence of the NBTI is still a source of very active research. NBTI-induced interface-trap generation has been modeled using various empirical models; exponential model [~ $\exp(\gamma E_{OX})$] **[194]**, power law model (~ E_{OX}^{m}) **[195]**, and mixed model (~ $E_{OX}\exp(\gamma E_{OX})$) **[98,145]**. The physical basis of the field dependence of NBTI phenomena was demonstrated by Alam in the framework of R-D model **[34]**. The presence of holes has been associated to NBTI degradation from the beginning in the earlier studies. Their density at the interface in strong inversion depends on

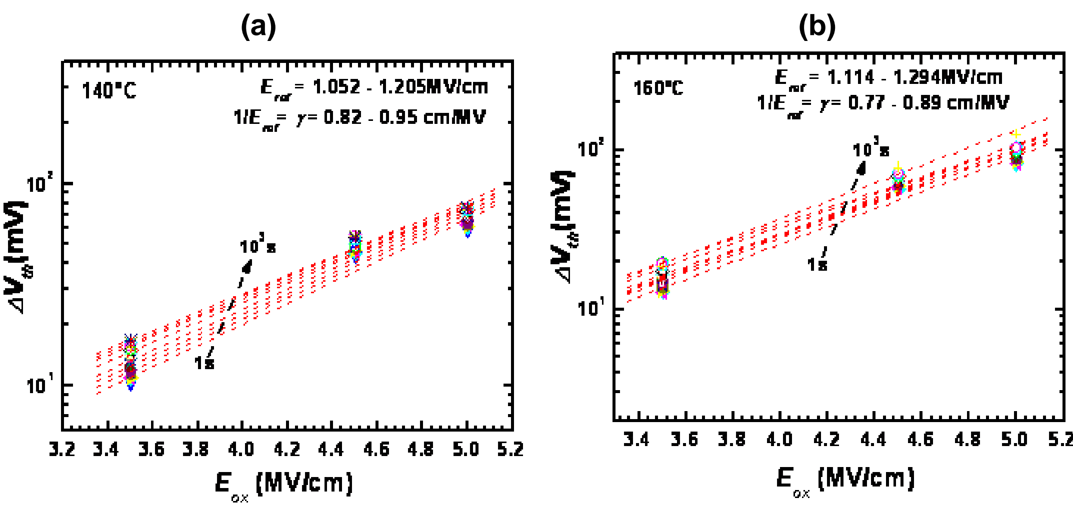


Figure IV.15: NBTI-induced threshold voltage shift as a function of electric field for different stress time and temperature of 140 °C (a) and 160 °C (b). The field acceleration factor is between 0.77-0.95 cm/MV.

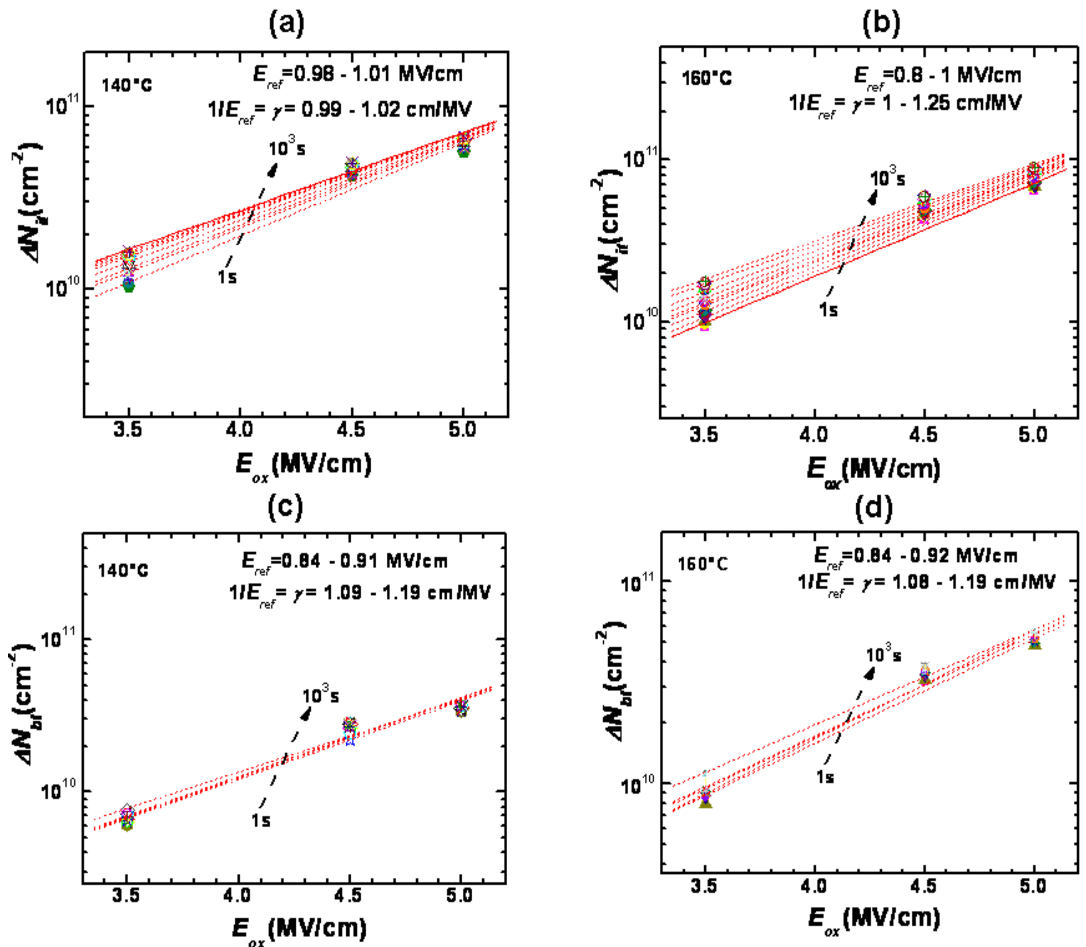


Figure IV.16: NBTI-induced ΔN_{it} and ΔN_{bt} as a function of electric field for different stress time at stress temperature of 140 and 160 °C. γ-ΔN_{it} and γ -ΔN_{bt} are about 0.99-1.25 and 1.08-1.19 cm/MV, respectively.

the gate voltage as (V_G-V_{th}), which is included in the pre-factor A. In addition, in the case of neutral hydrogenated species, the electric field influences the electrochemical reaction of Si-H dissociation by reducing the height of its barrier. It is also involved in hole tunneling process to Si-H bonds with tunnelling coefficient of $[\exp(\gamma E_{OX})]$. In summary, NBTI field dependence is modeled by $[(V_{GS}-V_{th})^{2/3}\exp(2\gamma E_{OX}/3)]$ **[17]** (see **Chapter I**, section **§ I.5.8**). According to Grasser et *al.* **[29]**, NBTI degradation has a quadratic exponent field dependence signature. In fact, based on multiphonon field-assisted tunneling (MPFAT) theory **[120]**, they suggested a field enhancement factor of the form $(\exp(E_{OX}^2/E_{ref}^2))$, which is only introduced for hole capture into oxide-trap in two-stage model **[29,49,62]** (see **Chapter I**, section **§ I.7**).

To better understand the physical mechanisms involved in our NBTI experiments, we have extracted a reference field factor (or acceleration factor) by fitting our data with above-mentioned models via the same procedure as the one used in **Figs IV.15** and **IV.16**. The results are plotted in **Fig. IV.17 (a) and (b)** for interface- and border-trap, respectively. The extracted factor for ΔN_{bt} remains almost constant with stress time and temperature, while that of ΔN_{it} exhibits a slight variation. It presents discrepancies with those calculated using $(V_{GS}-V_{th})^{2/3}\exp(2\gamma E_{OX}/3)$ for Si-H dissociation at the interface in forward rate of R-D model (1.6 MV/cm) **[17]**, whereas it is almost the same as that

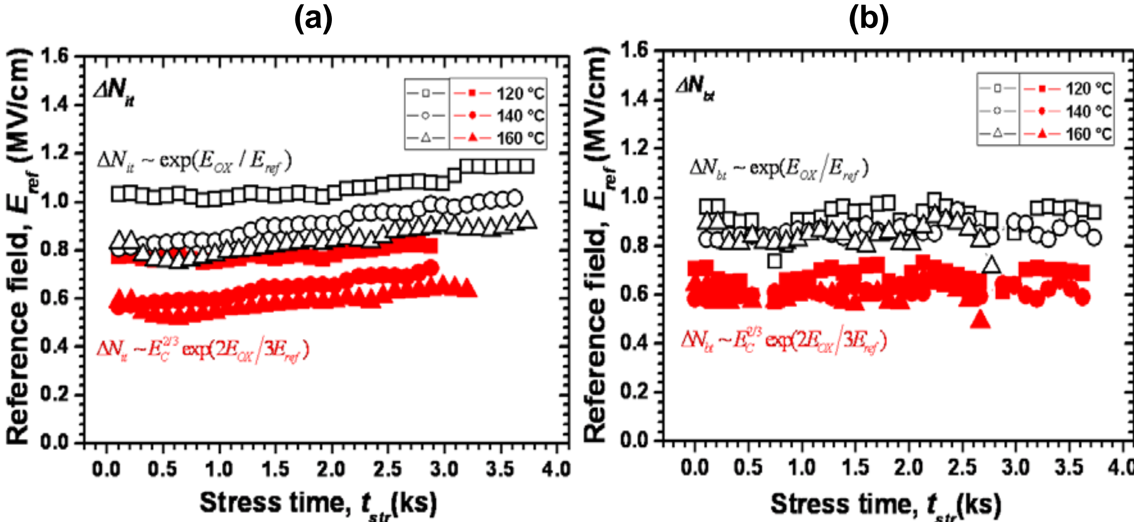


Figure IV.17: Reference field as a function of stress time at different stress temperatures for NBTI-induced ΔN_{it} (a) and ΔN_{bt} (b). E_{ref} is extracted from our data using different fitting models; empirical exponential field dependent (empty symbols), field enhanced Si-H dissociation, k_f in R-D *H-H₂* framework model (solid symbols).

extracted using $\exp(\gamma E_{OX})$ **[34].** Both interface- and border-trap factors exhibit the same values, suggesting that the same physical process might occur for both measurements. These similarities could be explained by the fact that some border traps participate with interface traps to CP-current at high frequency (1 MHz). Indeed, it has been shown that even at high frequency, signal from border traps pollutes that from interface traps **[50,117]**. The border-trap contribution arises from traps located in the interfacial oxide and having a response time within the used gate pulse period. In addition, we have demonstrated that at 1MHz, *C-P* technique scans 4.6 Å into the interfacial oxide region **[197]**. This point is detailed in **Chapter V**.

IV.6- Empirical Life Time Estimation

After describing the usefulness of OTFOT for NBTI-induced interface- and border-trap as well as the threshold voltage shift, we can use ΔV_{th} versus stress time for different voltages and temperatures acceleration to extrapolate (estimate) NBTI lifetime for the devices under investigation. However, the projection lifetime must be performed at circuit normal operation conditions. To do so, we extrapolate ΔV_{th} values obtained at accelerated temperatures, to ambient temperature. **Figure IV.18 (a)** illustrates ΔV_{th} at 27 °C (see grey circle symbol) for different stress times. Results are then extrapolated to operating supply voltage (5 V) and plotted for various stress times. **Figure IV.18 (b)** shows extrapolated data from those extracted after 3600 s of stress. In addition, data for different temperatures are also illustrated.

Finally, the NBTI lifetime projection is given in **Fig IV.19**. In this study, the device lifetime criterion due to NBTI is defined as ΔV_{th} shift equal 10% of the initial value (V_{th0}) (which is equal to -1.2 V). We notice that the NBTI lifetime for these devices exceeds 10 years for ambient temperature (27 °C), but decreases with temperature. For working temperature (80 °C), their lifetime decreases to 5.7 years.

IV.7- Gate Length Dependence of NBTI

Figure IV.20 illustrates NBTI-induced interface-trap in p-MOS transistors as a function of stress time for different gate lengths and fixed gate width. The set of trap densities are extracted at elevated

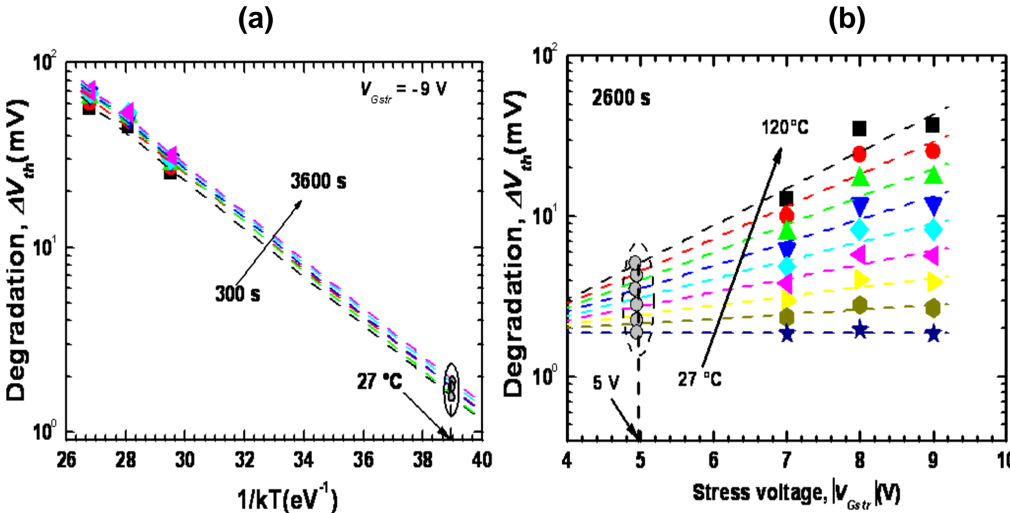


Figure IV.18: Threshold voltage shift under NBTI stress (a) as a function of temperature at - 9 V for different stress times (b) as a function of voltage at 3600 s for different stress temperatures.

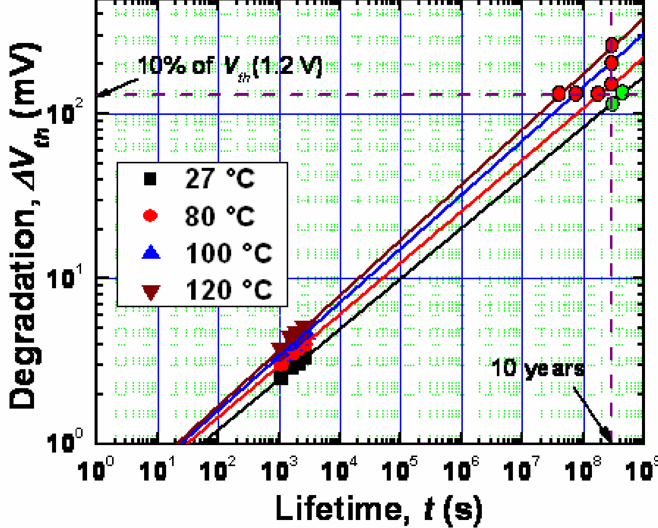


Figure IV.19: Threshold voltage shift vs. projection lifetime for different temperatures. Taking 10% of V_{th} as lifetime rule, our device lifetime exceeds 10 years at 27°C and decreases with temperature. For working temperature (80°C), their lifetime decreases to 5.7 years.

temperature and electric field using OTFOT method **[151,154]**. As observed, ΔN_{it} increases with decreasing gate length. The gate length effect indicates that trap densities, generated along the channel, are non-uniformly distributed. As opposite to long channel devices, NBTI degradation in short ones could have a large contribution from defects located near source/LDD and drain/LDD overlap edges. The possible causes of enhanced defect near the edges could be the ion implant induced damage **[198]**, hydrogen diffusion **[199]**, water **[88]**, and higher concentration of holes near the edge compared to the middle of the channel **[200]**. The same gate length dependence of NBTI degradation has been observed elsewhere **[201]** in devices with SiON gate oxide of 2 nm thick and with boron LDD doping. They proposed that boron enhances ΔN_{it} near the gate edges and consequently worsens NBTI degradation in short devices. In addition, power-law time exponent n of

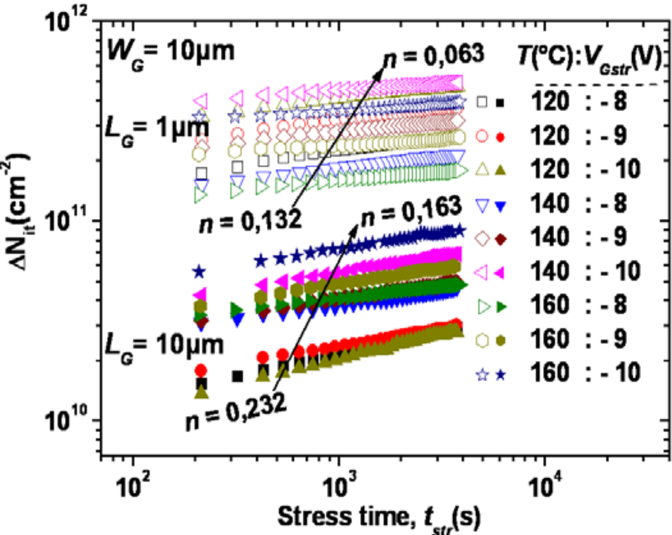


Figure IV.20: NBTI-induced interface-trap as a function of stress time extracted from transistors with gate lengths of 1µm and 10 µm at different electric fields; 4, 4.5, and 5 MV/cm and different temperatures of 120, 140, and 160°C. Shorter gate length transistor shows more degradation than longer one.

ΔN_{it} decreases with decreasing L_G and tends to saturation with stress temperature and voltage for both short and long channels. We will return to this point in the next **Chapter**.

Moreover, NBTI-induced threshold voltage shift, extracted using subthreshold slope method **[144]** described in **Chapter II** (section **§ II.5.2**) and plotted in **Fig. IV.21 [168]**, has revealed the same gate length dependence as discussed above for OTFOT ΔN_{it} and ΔN_{bt}. ΔV_{th} of shorter channel devices is more important than that of longer ones and *n* decreases with decreasing length.

According to the aforementioned gate length dependence of NBTI, it is difficult to predict exactly the NBTI effect on IC's response by simple test structures, because the gate size depends only on circuit layout optimization, done by the integrated circuit designers. In other words, it is impossible to predict the response of IC's to NBTI (which contains many transistors of different gate lengths) from measurements on a transistor with unique gate length.

IV.8- Geometric Component Effect in OTF CP-Based Methods

In the above section, using OTFOT method, we have shown that the NBTI degradation depends on transistor gate length. However, is this dependence due to inhomogeneous distribution of interface- and border-trap creation along the channel or trap creation is exclusively located at the source/LDD and drain/LDD edges? Is it an artefact caused by the measurement since OTFOT is CP-based method, where the geometric component (GC) **[56]** can influence data? To verify these facts, we conducted additional investigation on the GC.

Firstly, we give a short recall on GC. Basically, it is defined as an additional parasitic current which adds to CP-current and appears when some electrons cannot reach the source and drain regions during the transition from inversion to accumulation (see section **§ II.2**). These electrons recombine with incoming holes from the substrate. In an ideal *C-P* measurement, the electrons that were not captured at the interface traps would flow back to the source/drain during the MOSFET switch off. As a result, the presence of GC affects the accuracy of all CP-based methods such as OTFIT **[55]** and OTFOT **[151]**.

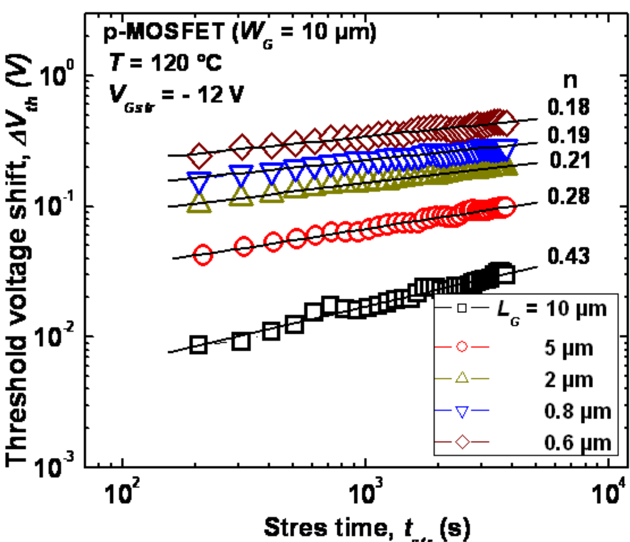


Figure IV.21: NBTI-induced threshold voltage shift, ΔV_{th} versus time evolution. The curves are measured at threshold voltage point, for p-MOSEFT transistors with different channel lengths, at V_{Gstr} = - 12 V and T = 120 °C **[168]**.

We have already shown that the GC affects CP-current of our virgin devices with gate length (L_G > 1 µm) **[202]**. However, as the NBTI degradation induces new traps at the interface and in the oxide, the effective electric field and the mobility carriers are affected, and subsequently the GC by Coulomb scattering **[130,203]**. Therefore, it is clear that the GC plays an important role in the reliability evaluation when using *C-P* methods to measure the interface traps. That is why, it must be properly accounted for NBTI degradation. In this sense, Tahi et *al.* **[204]** have developed a method that allows the evaluation of GC in virgin and degraded devices by radiation and NBTI. It uses an empirical model, which is obtained from *C-P* data using at least three transistors with different gate lengths. The GC evolution with stress time during the NBTI stress at V_{Gstr} = - 9 V and 120 °C for p-MOS transistors is shown in **Fig. IV.22 [204]**. The GC shows an increase (ΔI_{Geo}) with NBTI stress conditions, confirming the influence of NBTI-induced traps on GC by Coulomb scattering **[130,203]**. It also shows that ΔI_{Geo} is mostly the same and below 10 pA for transistors with gate length below 1µm. However, it exhibits a net increase when the gate length is increased.

In **Figs. IV.23 (a) and (b) [204]**, we present NBTI-induced I_{CP} current degradation (ΔI_{CP}) before and after GC removal, respectively. Not only the shorter transistors degrade more severely than the longer ones, but also the exponent (*n*) decreases with the gate length [see **Fig. IV.23 (a)**]. However, after GC current removal, ΔI_{CP} shows the same behaviour with stress time for all transistors and has the same amount of degradation. That means that the degradation sources could be the same for all devices. The LDD/channel edges could be the main cause of this behavior. Indeed, the LDD regions are the same for all transistors, because they are fabricated by the same process in the same production line at the same time. Moreover, these regions are more affected than the middle of the channel by the technological process steps such as source/drain process etching and ion implantation/doping. As a result, they are weaker than the middle of the channel **[205]**. For this reason, we suggest that up to 1 hour of stress, the NBTI-induced interface degradation is most probably located at the vicinity of the LDD regions. More details are given in **Chapter V**. All ΔI_{CP} curves exhibit the same *n* of about 0.12 for different L_G [see **Fig. IV.23 (b)**]. This implies that GC plays a key role in the assessment of the NBTI

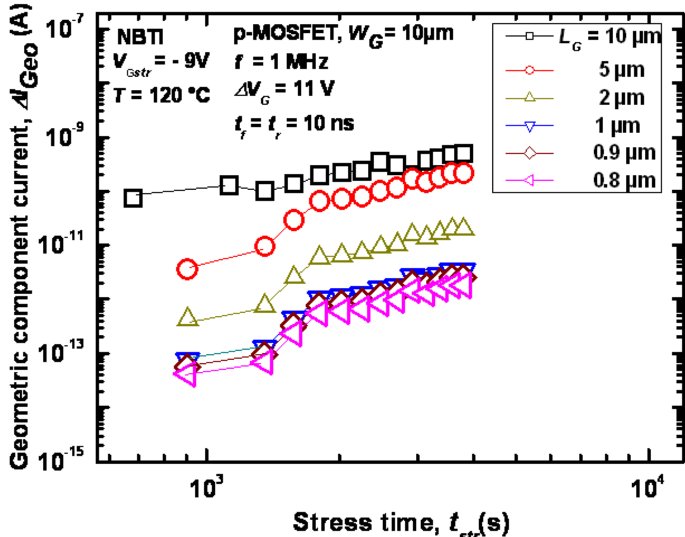


Figure IV.22: Geometric component current as a function of stress time during NBTI stress for transistors PMOS with different gate lengths and fixed width **[204]**.

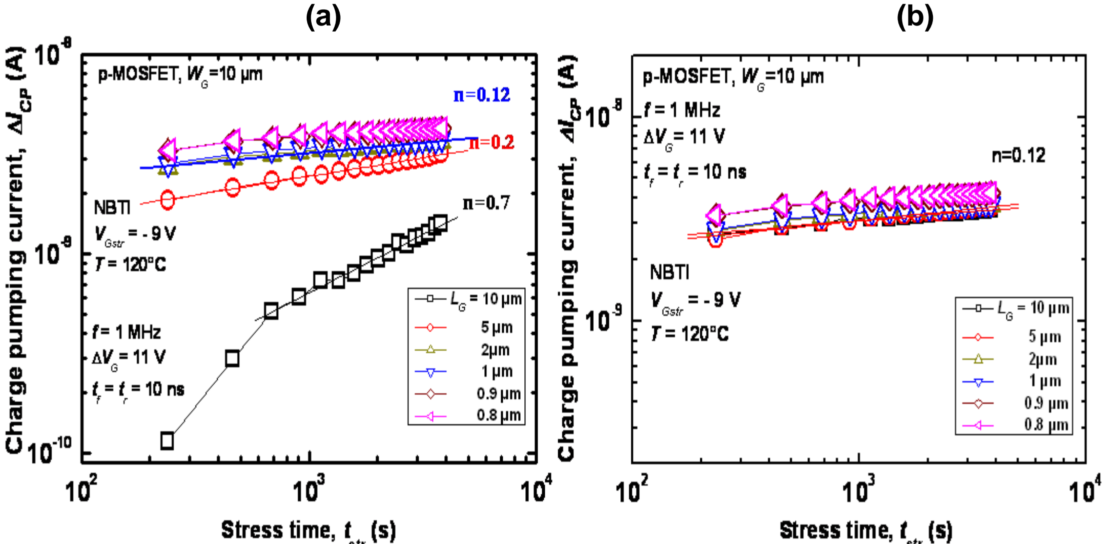


Figure IV.23: Charge pumping current as a function of stress time during NBTI stress for transistors PMOS with different gate lengths and fixed width. (a) with GC and (b) without GC **[204]**.

degradation; i.e. determination of *n* and estimation of device lifetime. This result means that the variation of *n* with L_G [observed in **Fig. IV.23 (a)**] is an artefact and a consequence of the superposition of two mechanisms, i.e. the recombination at the interface, giving information on interface-trap and recombination in the Si bulk, generating GC.

IV.9- NBTI Effect in LDD Region

In order to confirm that the LDD regions are at the origin of the gate length dependence of NBTI, we have looked into the NBTI effect on the edges of the Gaussian-like CP-current curve (I_{CP}–V_L). We have previously shown that the edges of CP-curves can provide useful information on the LDD and LOCOS regions **[133,134,206]**. These later cause humps at CP-edges. **Figure IV.24** shows full CP-curves in semi logarithmic scale to emphasize better the humps. The curves are measured before (solid symbols) and after 1 hour of stress (open symbols) at - 9 V and 120 °C on transistors of different

gate lengths and fixed gate width and vice versa. The LOCOS and LDD regions are as indicated on **Figs. IV.24 (a)-(d)**. Obviously, before stress, the same hump is observed for transistors with different L_G in both types of transistors. That means that LDD regions are the same for all transistors of L_G-variable group. For W_G-variable, LDD region increases with W_G and subsequently the NBTI effect also increases as illustrated in **Figs. IV.24 (c) and (d)**. However, the LOCOS region is still roughly the same even after stress. This is another proof on local NBTI degradation at LDD regions at least up to one hour of stress.

Regarding the CP-curve plateau, which represents the transistor channel, it seems to be insensitive to stress for L_G = 10 µm at least up to one hour under stress temperature of 120 °C and voltage stress of – 9 V. When L_G decreases down to 5µm, the plateau starts increasing with stress [see **Figs. IV.24 (a) and (b)**]. For W_G-variable and L_G fixed at 10 µm [see **Figs. IV.24 (c) and (d)**], the plateau of virgin and stressed curves remains roughly unchanged for each transistor.

From these observations, we can therefore hypothesize that the NBTI degradation starts from LDD

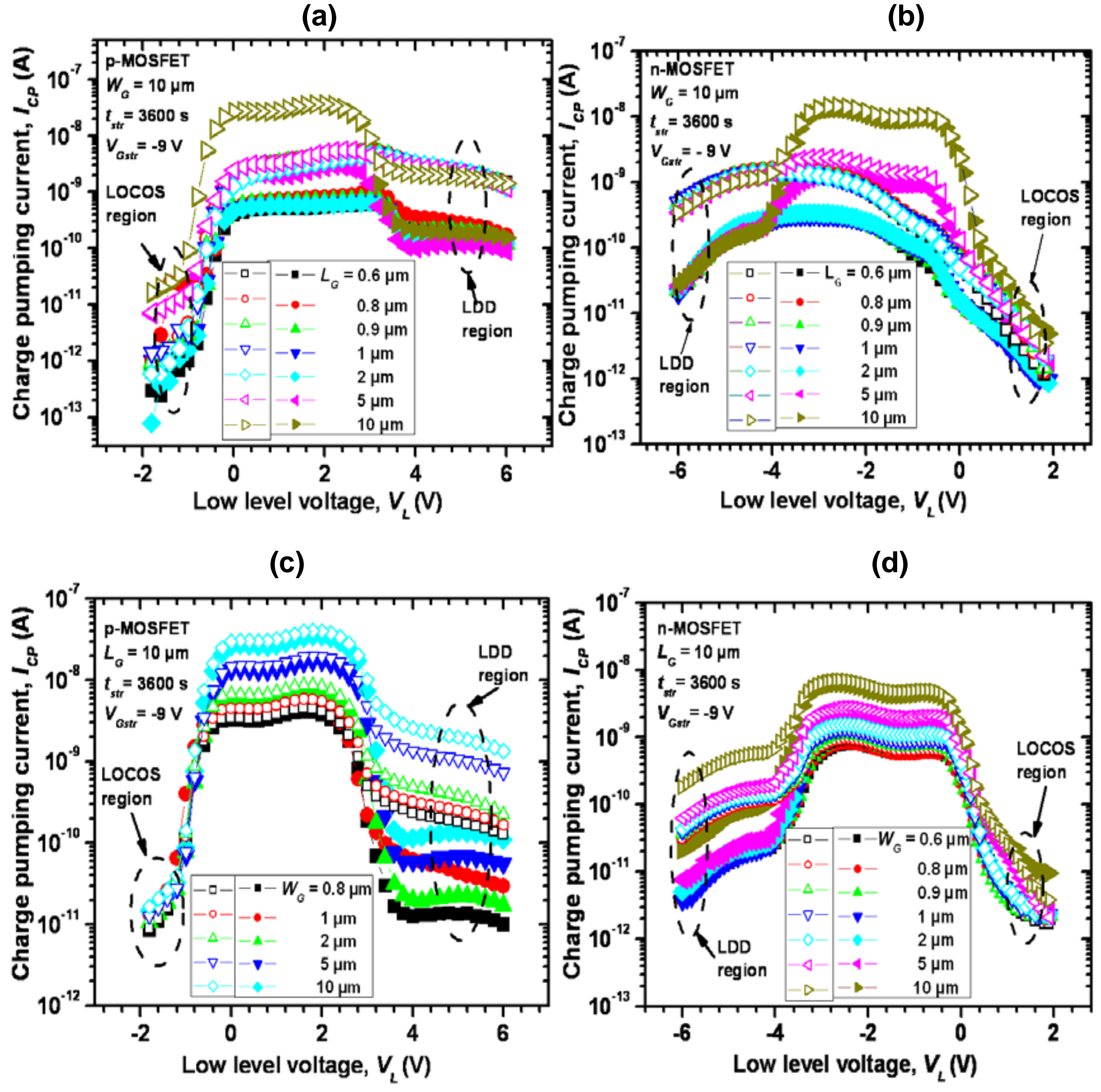


Figure IV.24: NBTI effect on Gaussian-like CP-current curve before and after stress at – 9 V and 120 °C for transistors with different L_G and W_G fix (a) p-MOSFET (b) n-MOSFET and different W_G and L_G fix (c) p-MOSFET and (d) n-MOSFET.

edges at the beginning of stress and propagates towards the middle of the channel. The propagation kinetics depends on stress time, temperature, and field. This hypothesis will be more investigated and deeply analysed in **Chapter V**.

IV.10- Discussion

In this section, we will not focus on OTFOT method since it was largely discussed in previous sections. However, we will treat its results as well as their implication to apprehend the features of the complex NBTI degradation in our devices. First of all, it is important to recall that according to our experiment timescale; only the permanent or quasi-permanent component **[58]** of NBTI degradation is depicted and analyzed. This time is inherent to the *C-P* technique itself, where the necessary pulses to switch between accumulation and inversion induce a measurement delay. The extracted trap densities using the proposed method “OTFOT” have revealed that both interface and border traps have almost comparable dependencies of temperature and field. These similarities between ΔN_{it} and ΔN_{bt} behaviours could result from the fact that defects are located in the interfacial region and their microstructures are controlled by the interfacial layer properties.

The high apparent activation energy measured on our devices is, according to Grasser et *al.* **[126,192,193]**, attributed to border traps. So, why does the apparent activation energy of interface traps look like the one of border traps? Before examining this question, one has to keep in mind that there is no sharp separation between Si/SiO_2 interface and the oxide. That is why it is very difficult from an electrical point of view to sense only the interface. Indeed, even when using very high CP frequencies, there will always be a thin interface layer scanned. At 1 MHz CP measurement, about 4.6 Å of interface layer into the oxide is probed **[197]**. Therefore, signal from interface traps is always convoluted with signal coming from border traps even at high frequency, inducing similar apparent activation energy as that of border traps. Besides, some authors have argued the large exponent *n* of ΔI_{CP} compared to ΔV_{th} observed in SiO_2 gate oxide devices, by a lesser contribution from border traps to CP-current **[50]**. In addition to ΔN_{it}, the CP-method also measures a recombination current arising from the interfacial border traps having a response time within the gate pulse interval **[55,117]**. Border traps whose occupancy does not change during the gate pulse interval are not measured. Hence, the CP-method probes a smaller amount of border traps at high frequency, which explains the larger apparent activation energy E_a.

Furthermore, increasing the low level voltage to the stress voltage in on the fly CP-method enhances contribution from traps with different energy inside the oxide **[56,117]**. If only the interface traps contribute to CP-current, the later should actually become independent of low voltage as soon as the inversion is reached **[56]**. However, it continues to increase at a slower rate **[56]**. This increase is usually attributed to slower oxide traps (border traps) **[136]**. In addition, our devices exhibit dispersion in apparent activation energy of both types of traps, involving several defects with different physical microstructures in NBTI degradation. These defects have different capture times and emission times **[192]**. They are probably related to border traps located in the near interfacial region and microscopically associated with hydrogenated defects **[80,94]**. These defects seem to exhibit different energies and distances inside the oxide near the interface. Further details are provided in **Chapter I** section **§ I.4.5**.

IV.11- Conclusion

In this **Chapter**, we have proposed a conceptual framework of a new method to separately extract NBTI-induced interface- and oxide-trap. Using only *C-P* technique at low and high frequencies, the OTFOT method allows the determination of interface- and border-trap densities without combining other techniques. By adjusting high and low frequency measurement times, we can get a comparable relaxation portion for both interface- and border-trap. In addition, we have presented the experimental results of OTFOT method by showing the NBTI-induced interface- and oxide-trap densities as well as their contributions to the voltage shift. The experiments are based on two different experimental scenarios. The first one consists in performing all stresses on the same transistor with a relaxation period. This scenario shows an apparent higher n. The second one concerns each stress temperature/voltage on only one transistor. This procedure shows a good agreement with literature regarding the power-law exponent. Unlike other existing methods that are more or less complicated, the present method extracts ΔN_{it} and ΔN_{bt} using stress and *C-P* in the same timeframe without changing the experimental setup and without any pre-assumption, except for low and high frequency conditions. ΔV_{th} is obtained from independently extracted ΔV_{it} and ΔV_{bt}. However, low frequency limits the number of border traps probed by OTFOT. In addition, due to the inherent time delay required to switch the channel in CP-based method, OTFOT cannot capture the fast switching traps. Despite these drawbacks, OTFOT can determine the trend of the permanent component, which is the main component affecting the circuits in operating conditions at very long time.

We have also presented the OTFOT results and their analysis. We have showed that NBTI degradation is mainly located at the LDD edges, because of its weak structure compared to the middle. However, this fact is observed for one hour of stress time and low stress electric field (up to 5 MV/cm), therefore it is worth conducting more investigations for long stress time and high electric field to confirm these results.

In summary, the results of the experiments regarding time, temperature, and field NBTI dependence revealed many discrepancies even for those reported in the literature. This could partly explain the complexity of developing a physical model for the observed NBTI effects. Consequently, different concept should be developed to capture the NBTI degradation. In this sense, some interesting ideas, that could explain the origin of these effects, will be developed in the next **Chapter**.

Chapter V

NBTI PERMANENT COMPONENT PROPAGATION CONCEPT

V.1- Introduction

V.2- Lateral Profiling Experiments

V.3- NBTI-Induced Interface-Trap Propagation

V.4- Time, Temperature, and Electric Field Dependence of ΔN_{it}

V.5- ΔN_{it} Propagation Result Analysis and Discussion

V.6- Vertical Profiling Experiments

V.7- Depth Profiling of NBTI-Induced Border-Trap

V.8- Time and Temperature Dependence of ΔN_{bt}

V.9- Possible Defect Precursors Linked to NBTI-Induced ΔN_{bt}

V.10- ΔN_{bt} Profile Result Analysis and Discussion

V.11- Conclusion

CHAPTER V

NBTI PERMANENT COMPONENT PROPAGATION CONCEPT

V.1-Introduction

According to the results obtained in **Chapter IV** and those widely discussed in the literature **[40,48,50,51,62,106,172,192]**, NBTI mechanisms are still not well understood. Discrepancies are closely related to temperature dependence, electric field dependence, and time-law exponent, where frequently, different values of NBTI parameters (such as n, $E_{a,eff,}$ and γ) and different explanations have been reported by different groups **[12,20,22,25,29,34,40,48,185,188,193,207]**. Even though the improvements brought to the R-D model to match experimental data, giving subsequently a steady value of 0.16, disparities regarding the relaxation phase and n have been reported by different groups **[27,50,62]**. In fact, Ang et *al*. **[50]** have shown that T dependence of n arises from the superposition of two mechanisms having different thermal activations in cyclic NBTI. They suggested that the same group of defects with broad spectra of hole trapping and detrapping time constants is responsible of the apparent variation in the power-law exponent for the dynamic NBTI. After accounting for the hole trapping component, a distinct power-law exponent (0.27), independent of temperature, was revealed for the interface state generation **[50]**. More recently, besides the interface traps, two types of NBTI-induced oxide traps (shallow and deep oxide traps) in p-MOSFET have been suggested **[208]**. Taking out the geometric and quasi-geometric components from OTFOT method **[151]** has demonstrated that deep oxide traps are mainly created in the LDD region, while shallow oxide traps are generated in the entire channel.

As a result, a large spread in NBTI experimental features complicates any modeling attempt of the NBTI degradation. These discrepancies suggest that different defects with different structures located at the interfacial region are involved in the degradation. These defects do not necessarily have the same E_a. The defect energy distribution may be related to Si/SiO_2 interface disorder and bulk SiO_2 disorder, especially in the interfacial region. In fact, it has been reported that trap precursors located in this region have different atomic structures **[91]** and different E_a, particularly for the border-trap family precursors ($O_{3-x}Si_xSi$-H), which behave like interface-trap with a longer time constant. NBTI is more likely related to defects at the interface and in the interfacial oxide regions (transition region, SiO_x, $x < 2$). Therefore, different border-trap precursors cannot be ignored and a proper understanding of their behavior with NBTI conditions is necessary to develop a model capable of interpreting a wide number of NBTI experiments. Do these precursors participate at different NBTI stages depending on their position in the interfacial layer? To better understand the NBTI features especially in the interfacial region, we propose to study the depth profiling of the permanent component by investigating the traps lying in the oxide near the interface using the MFCP **[136,209]**.

On the other hand, there have been some papers that showed the influence of the channel length and width on NBTI **[179,180,201]**. However, this issue received much less attention for many years, since it was believed that NBTI should be uniform along the channel and only depends on vertical gate

voltage. Moreover, it is not well understood why NBTI should depends on gate length, since it does not depend on lateral field like hot carriers. Nevertheless, it has been reported **[201]** that enhanced pre-existing damage located near the channel edges is in part responsible for the channel dependence of NBTI. In addition, possible boron diffusion from S/D and lightly doped drain (LDD) into the gate oxide can increase the initial density of electrically active defects at Si/SiO_2 near channel edges. This fact is enhanced for shorter gate length transistors **[201]**.

Our results suggest that defects in the interfacial oxide region as well the gate geometry, especially gate length play an important role in n, E_a, and E_{ref} dispersion. Hence, understanding the channel edges impact as well as the quality of the interfacial region on NBTI features can help developing a reliable model of NBTI degradation.

In this chapter, we will deeply investigate NBTI gate length dependence and its local generation at LDD region by combining on the fly interface-trap (OTFIT) and the reverse voltage variation of source and drain (S/D). In addition, we will scan interfacial traps involved in NBTI degradation using multi-frequency method. The chapter is structured into two parts. The first part describes the lateral propagation of the NBTI degradation, while the second one deals with the vertical propagation.

PART I: LATERAL PROPAGATION OF THE PERMANENT COMPONENT

In this part, we show that NBTI-induced interface traps are not uniform along the channel, not because it depends on lateral electric field but rather on the weakness of the physical structures of the channel edges compared to the middle **[181]**. In addition, we suggest that the NBTI degradation starts at the beginning from the channel edge (S/D) sides and propagates towards the middle of the channel. This propagation is accelerated by temperature and vertical electric field. We should note here that the propagation term does not mean hydrogen diffusion, but describes the time evolution of the lateral distribution of the NBTI-induced interface traps as a function of the stress field, temperature, and time. The proposed NBTI lateral propagation concept allows us to explain the differences in as-measured exponents n shown here **[151,181]** and elsewhere **[12,34,50]**. In addition, it could be one of the explanations of the irrelevance of NBTI effect in micron technologies compared to submicron ones as reported in the past **[188]**. It is indeed, harder to degrade transistors with gate lengths of microns than those with shorter lengths. Furthermore, with shrinking devices, the edge areas take up a higher percentage of the transistor active area, where the local strain in these regions can alter the activation energy/dynamics for NBTI induced trap creation **[188]**. We found that transistors with longer channel exhibit less NBTI degradation. Additionally, the exponent n is lower in smaller channels compared to longer ones for the same stress conditions of temperature, time, and electric field.

V.2- Lateral Profiling Experiments

In these experiments, we have investigated devices with different gate sizes; fixed gate width at 10 µm and gate length shorter than 2 µm to avoid geometric component effect (L_G = 2, 1, 0.8, 0.7, 0.6, and 0.5 µm. The detailed process is given in **Chapter III**, section **§ III.2**. It is worth recalling that thick gate oxide (20 nm) allows avoiding the pollution of CP measurements with parasitic tunneling current **[46,124]**.

V.2.1- Lateral profiling before NBTI stress

Before investigating the NBTI degradation, we first extract the CP-current as well as the distribution of the interface-trap density in the channel before NBTI stress. **Figure V.1 (a)** gives the I_{CP} -V_L standard curves of CP-current as a function of the low voltage for different (S/D) reverse voltages (V_R) (S/D-V_R). They are measured by using a trapezoidal signal with amplitude of 4 V, a fixed rise and fall time of about 10 ns, and a frequency of 1 MHz to minimize the contribution of the border-trap to CP-current. As illustrated in **Fig. V.1 (a)** the maximum of CP-current of the Elliot curves decreases with V_R, due to a reduction of the contributing area to CP-current. **Figure V.1 (b)** illustrates the interface-trap density distribution along the p-channel MOSFET of W/L=10/0.8 at 120 °C before stress voltage (virgin state). They are evaluated using **Eqs. II.18 and II.19** (see **Chapter II** section **§ II.2.2.2**). The virgin state shows that the interface-trap density is not uniform in the vicinity of S/D **[181]**. The extraction program of ΔL (T), L_{eff} (T), and X is given in **appendix (D.2)**.

V.2.2- Lateral profiling After NBTI stress

The NBTI study of degraded transistors is performed by measure/stress/measure (MSM) protocol, as illustrated on **Fig. V.2 (a)**. The measurement phase is performed with on the fly interface-trap (OTFIT) **[130]** at high frequency. During the stress interval, the voltage stress (V_{GStr}) is applied, through a *DC* voltage, onto the gate of the device. After each stress time, a gate pulse train is applied on the fly, without modifying the experimental setup. The gate trapezoidal signal has an amplitude of ΔV_G = V_H-V_{GStr}, where V_L = V_{GStr}, duty cycle 50%, same rise and fall times, and 1 MHz frequency. Unless otherwise indicated, the source and drain voltage (V_S=V_D=V_R) are varied from 0 to 3 V with a step of 0.1 V to screen I_{CP} along the channel. This measurement interval is kept the same (30 s) during all MSM cycle for different temperatures and electric fields. The whole stress time cycle is fixed at 7 hours. During the NBTI stress, we use temperatures of 120, 140, and 160 °C and the electric field is varied from - 6 to - 9 MV/cm with a step of - 0.5 MV/cm while keeping V_H at 1 V in all experiments,

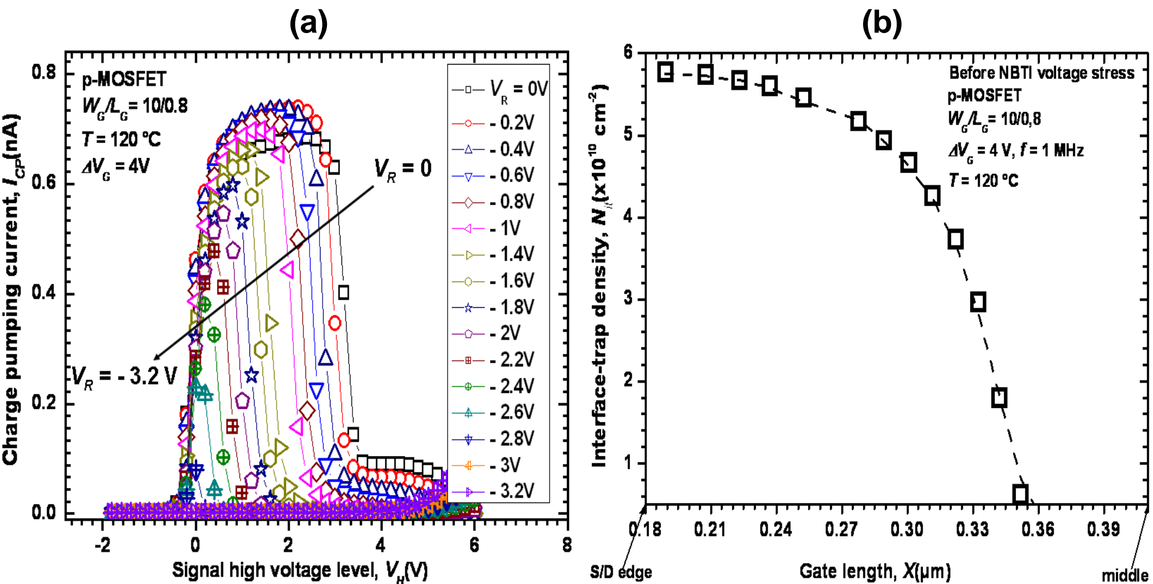


Figure V.1: (a) Elliot curves of CP current as a function of signal low voltage of PMOS transistor before NBTI voltage stress and at 120 °C. (b) Interface-trap density distribution in PMOS transistor channel before NBTI voltage stress and at 120 °C.

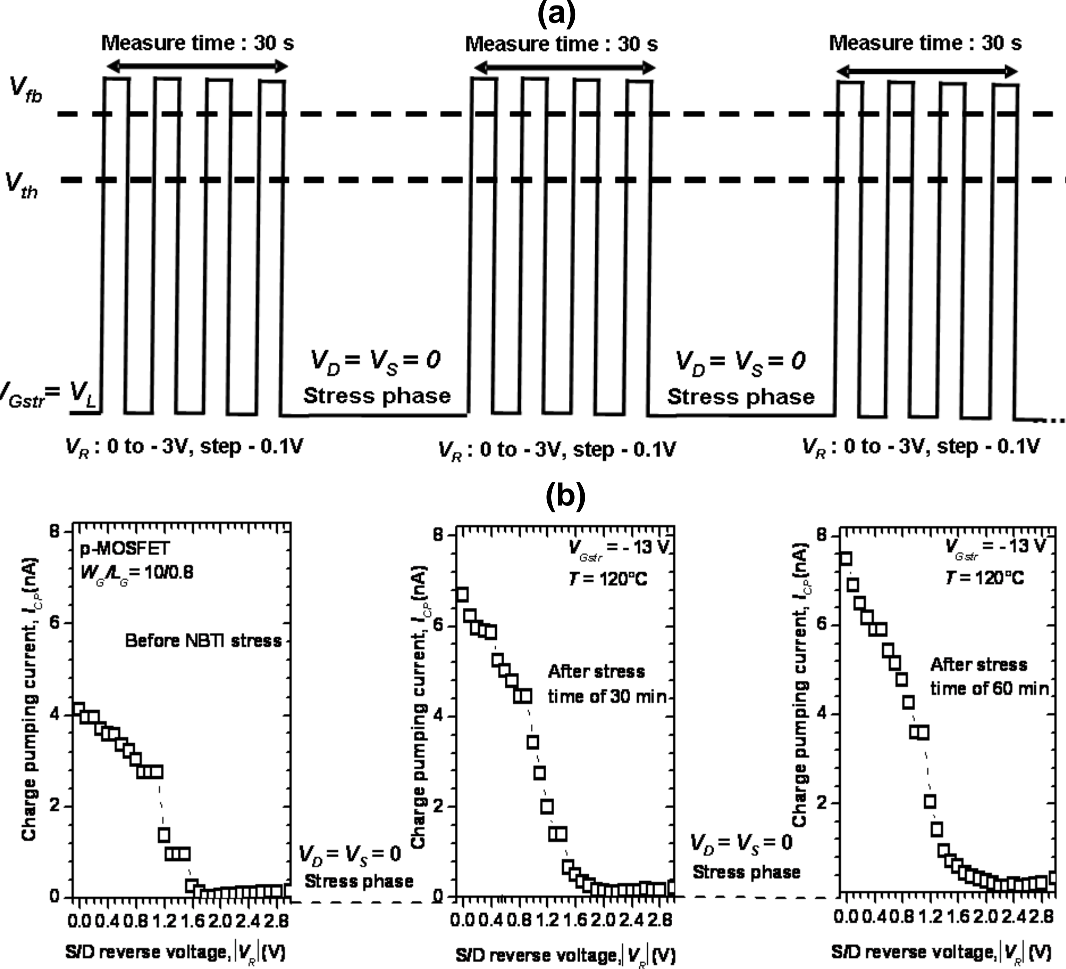


Figure V.2: (a) Mearure/stress/measure (MSM) protocol used to extract the lateral distribution of the NBTI permanent component. (b) As-measured CP-current at 1MHz as a function of S/D reverse voltage, V_R. The CP-current is measured using on the fly interface-trap (OTFIT) method before NBTI stress, after 30 min and 60 min of stress.

except if otherwise specified. The first measure in **Fig. V.2** is done just before starting the stress (at the beginning of the stress phase). This measure is taken as the reference for the degraded state. The MSM sequences are performed using fully automated bench of CDTA, see **Chapter III**.

Figure V.2 (b) shows the as-measured CP-current for different S/D-V_R voltages before and after 30 and 60 min of NBTI stress. The left plot illustrates the current before stress. It decreases as V_R increases. In fact, when V_R is enhanced, L_{eff} should decrease allowing charge pumping in small gate area and hence extracting interface-trap density of that surface. The middle and the right plots show I_{CP} as a function of V_R after NBTI stress at 120°C and – 6.5MV/cm for 30 and 60 min, respectively. We observe that I_{CP} increases with stress time. Moreover, it is more important after stress for the same V_R (i.e. the same region in the channel) **[181]**. This increase indicates that NBTI induces additional interface-trap. However, the NBTI-induced I_{CP} variation is different from V_R to another. The evolution of ΔN_{it} across the channel will be investigated in section **§ V.3**.

V.3- NBTI-Induced Interface-Trap Propagation

As discussed in **Chapter IV** (see sections **§ IV.7-IV.9**), it is believed that the gate length dependence of NBTI degradation takes sources from defects located at the gate edges, see **Fig. V.3**. Therefore, to deeply investigate the gate edge and LDD overlapping influences on interface-trap

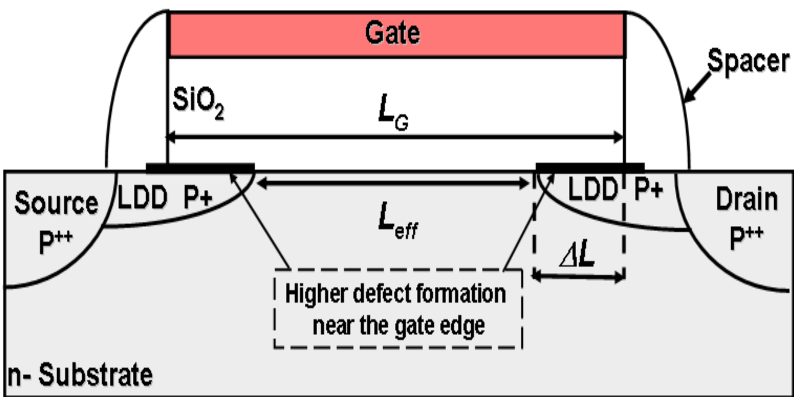


Figure V.3: p-MOSFET device showing LDD structure as well as the LDD sub-diffusion, ΔL underneath the gate indicated by black bold thick line.

generation during NBTI stress, we focus on the lateral distribution of the interface-trap using the above cited MSM protocol [see **Fig. V.2 (a)**]. It should be noted here that the train pulse was applied for 30 s to perform the trap profiling by varying S/D-V_R voltage. Therefore, the extracted data concern traps contributing to the permanent component of NBTI. Using **Eq. II.20**, the evolution of ΔN_{it} can also be tracked with NBTI stress time as:

$$\Delta N_{it}(t_{str}) = \delta N_{it}(t_i) - \delta N_{it}(t_0) \tag{V.1}$$

where $\delta N_{it}(t_0)$ (cm^{-2}) is the localized interface-trap density in the channel before stress, $\delta N_{it}(t_i)$ (cm^{-2}) is the localized interface-trap density in the same area of the channel after different stress times, and $\Delta N_{it}(t_{str})$ (cm^{-2}) is the localized NBTI-induced interface-trap density in the same area of the channel. **Figure V.4** shows ΔN_{it} (t_{str}) evolution with NBTI conditions. **Figure V.4 (a) and (b)** illustrate the variation of ΔN_{it} (t_{str}) as a function of the channel length for different electric fields and temperatures, respectively. These data are extracted during stress time varying from 30 min to 7 hours. In addition, the lateral dynamic of the NBTI evolution with electric field is investigated after 3800s of stress at 120°C [see **Fig. V.4 (c)**]. From the electrical viewpoint, the distribution of ΔN_{it} (t_{str}) over the channel become uniform and saturates at about 2x10^{12} cm^{-2} for stress voltage of -16 and -18 V (or -8 and -9 MV/cm) **[181]**. On the other hand, the saturation is highly field-dependent, but depends slightly on the temperature. In the latter, the saturation is hardly reached even at high temperature (160 °C), especially in the middle of the channel **[181]**. Consequently, the predicted life time would be dramatically increased. The same conclusion has been drawn by Grasser et *al.* **[210]** using capture/emission time map.

The relatively higher densities observed after NBTI stress in **Fig. V.4** (~10^{12} cm^{-2}) could be explained in part by the contribution of some border traps to the CP-current. It is well known, under the assumption that only interface traps contribute, that the CP-current should actually become independent of ΔV_G as soon as the strong inversion regime is reached. However, I_{CP} continues to increase, even with a much slower rate **[56]**. This increase is commonly attributed to slower oxide traps **[38,133]**. The same observation has been reported by other research groups **[55,211]**. As previously explained, the CP-method also probes a recombination current arising from the

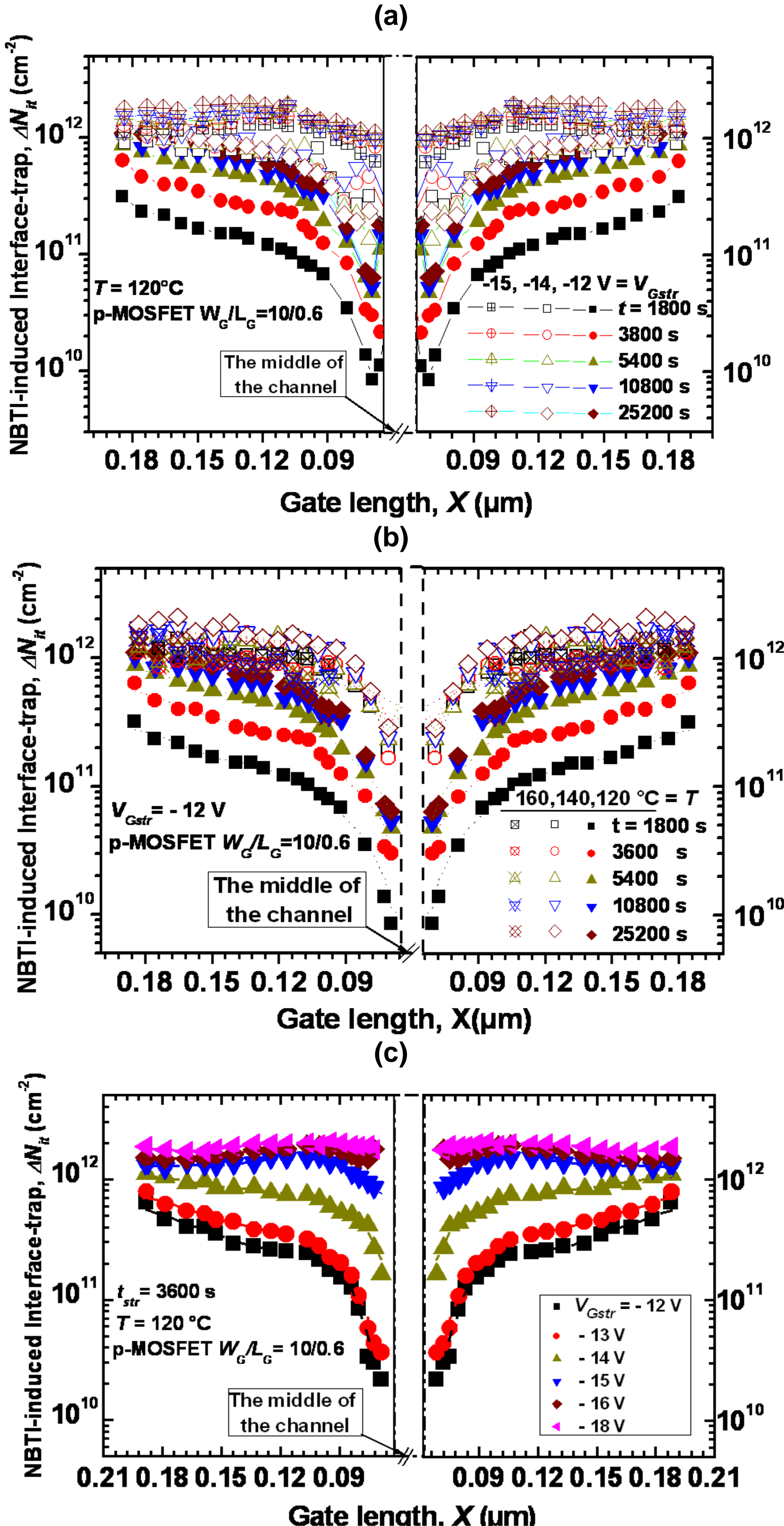


Figure V.4: Lateral distribution of NBTI-induced interface-trap, ΔN_{it} in the channel (a) For different stress times and voltages at 120°C, (b) for different stress times and various temperatures at – 6 MV/cm, and (c) for different stress voltages at stress time of 3600s and temperature of 120°C.

interfacial oxide traps even at high frequency, such as 1 MHz **[55,211]**.

Until now, we have studied the NBTI propagation in short gate length of p-MOS transistors (0.6 µm) using *C-P* technique with varying V_R-S/D. What about the long channel length transistors? To investigate the NBTI propagation in transistors with long gate lengths, we have stressed p-MOS transistors with gate lengths of 1 and 2 µm. The latter are respectively stressed at 120°C and - 12 V (- 6 MV/cm) and - 14 V (- 7 MV/cm). The MSM protocol was the same as described in section **§ V.2.2** except for V_R-S/D, which is varied from 0 to 5 V for transistor with 1-µm gate length and from 0 to 7.5 V for transistor with 2-µm gate length. The results are given by open symbols in **Fig. V.5**, where the NBTI propagation in 1-µm gate length is shown in **Fig. V.5 (a)** and the one corresponding to 2-µm gate length is given in **Fig. V.5 (b)** for different stress times. The solid symbols in **Figs. V.5(a) and (b)** represent the NBTI propagation in p-MOS transistors with gate lengths of 0.6 and 0.8 µm, respectively. All transistors are plotted together to illustrate the propagation kinetic for the same stress conditions. **Figure V.5** clearly shows that the degradation is the same near the edges in both cases **[Figs. V.5 (a) and (b)]**, because these regions are the same in all transistors **[204]**. In fact, the LDD region is the same for all fixed-gate-width transistors, since they were fabricated by the same process in the same line at the same time. Starting from the edges, we observe that the degradation propagates in the same manner in both short and long channels. In shorter channels, it reaches the channel middle more rapidly compared to longer channels. While in the latter, it continues its propagation to the vicinity of the middle.

However, we use different sets of V_R, because we deal with different gate lengths. On one side, to scan traps near the channel center, we have to increase V_R. Therefore, the longer the channel length, the higher has to be the V_R. On the other side, V_R-S/D increase is not only limited by reverse voltage breakdown of the substrate/source and substrate/drain diodes (which is about 16 V), but also by the reverse leakage current of the diodes, which becomes greater than the CP-current. Indeed, when V_R-S/D increases, the CP-current decreases because of length reduction, while the reverse current increases. That is why it is very hard to scan the degradation around the middle of the channel, especially in transistors with long channel **[181]**. Therefore, the lateral screening method, proposed in this work, is effective to probe the lateral profile of interface-trap in devices with small gate lengths. In summary, all curves show important features in the evolution of NBTI-induced traps as a function of time, temperature, and electric field: 1) ΔN_{it} (t_{str}) is more important at the channel edges than at the middle of the channel for low T and E_{OX}, 2) ΔN_{it} (t_{str}) tends to saturate more rapidly at the vicinity of the gate ends than in the middle, 3) At long stress time and/or at high temperature, and/or high electric field, the interface-trap of the middle tends to saturate and becomes equal to that of the edges.

The channel length dependence of NBTI cannot be caused by the lateral electric field, because S/D are biased to zero voltage during the stress period and biased together to the same V_R during measurement period (i.e. V_D - V_S = 0). Similar degradation tendency at S/D and LDD edges, indicating degradation symmetry at the channel ends as well as the damages induced by NBTI stress are more larger than that of the channel middle have previously been found using standard drain current for different V_D and V_S **[179]**. What is the origin of that behavior? What does it imply for the conventional NBTI R-D model? To answer these questions, a further investigation on the lateral evolution of NBTI degradation in the channel is needed. We have focused on the behavior of the well known NBTI

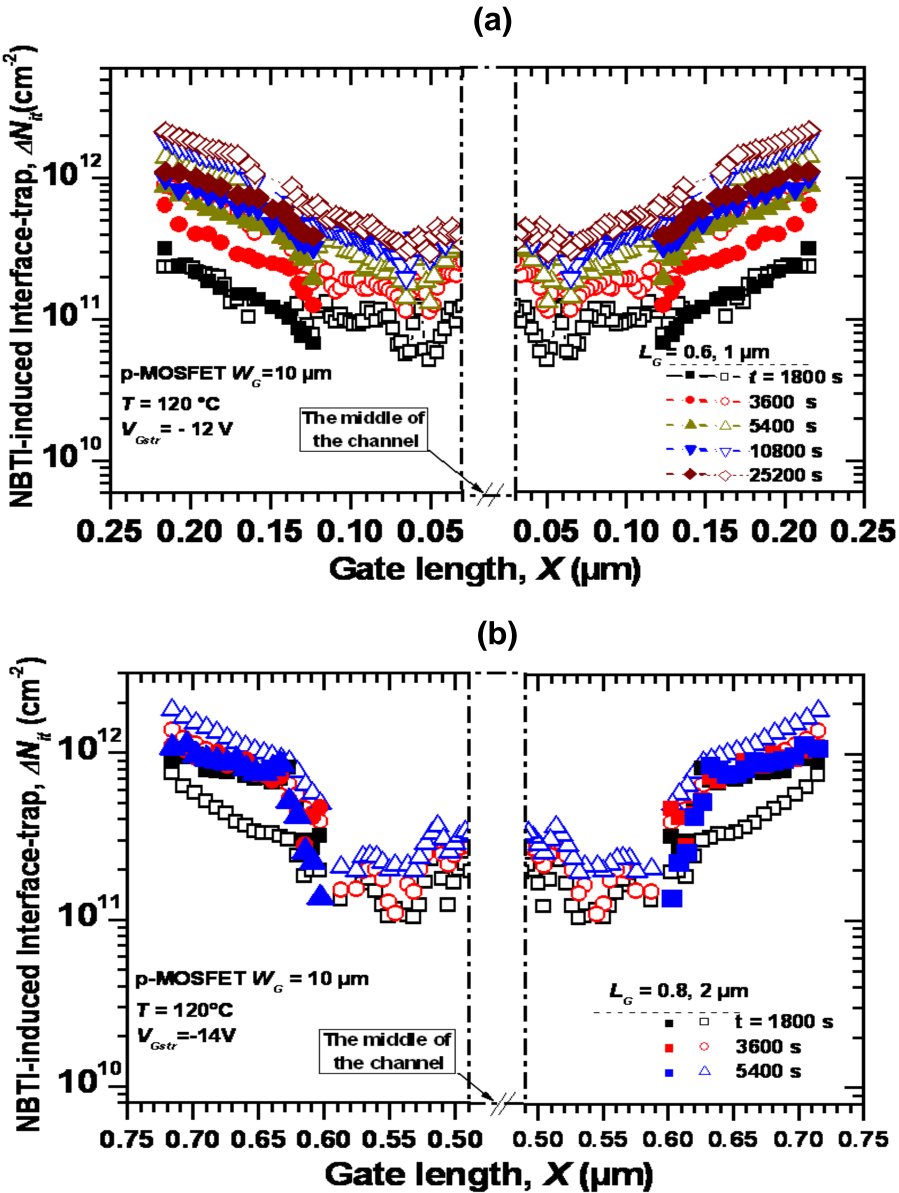


Figure V.5: Lateral distribution of NBTI-induced traps (a) For transistors with channel lengths of 1 and 0.6 µm stressed with – 6 MV/cm at 120°C and different stress times (b) For transistors with channel lengths of 2 and 0.8 µm stressed with – 7.5 MV/cm at 120°C and different stress times.

model parameters such as the power law exponent, n, the activation energy, E_a, and the critical field E_c (or reference field) **[26]**.

V.4- Time, Temperature, and Electric Field Dependence of ΔN_{it}

We start by plotting ΔN_{it} (t_{str}) as a function of the stress time for different regions of the channel in **Fig. V.6**. It is clear that the power law time exponent (n) is not constant with time and tends to saturate after long stress time. On the other hand n varies with the position (x) in the channel. It starts from 0.15 at the S/D edges and increases to a constant value of 0.26 in the middle of the channel at 120 °C and -12 V (-6 MV/cm) (see square symbols in **Fig. V.7**). The value of 0.26 is in agreement with previous results **[50]**. In addition, n decreases with electric field from the S/D edges to the middle of the channel until complete saturation, where n tends to zero, as shown in **Fig. V.7.**

On one side, the exponent n value is related to the amount of traps, i.e. the lower the trap generation, the higher the exponent n and vice versa. This fact is revealed by Ang et *al*. **[50]** using

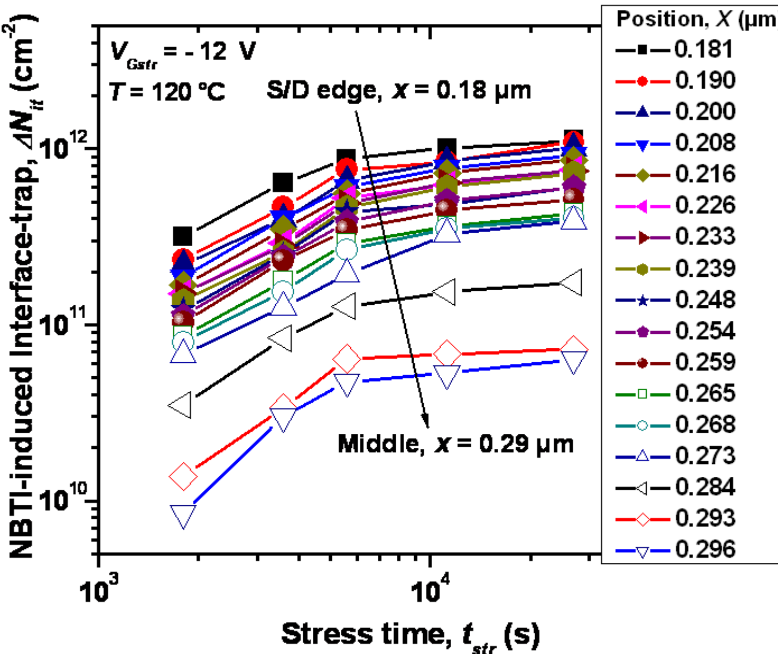


Figure V.6: NBTI-induced ΔN_{it} as a function of stress time for different positions in the channel at 120°C and -6 MV/cm.

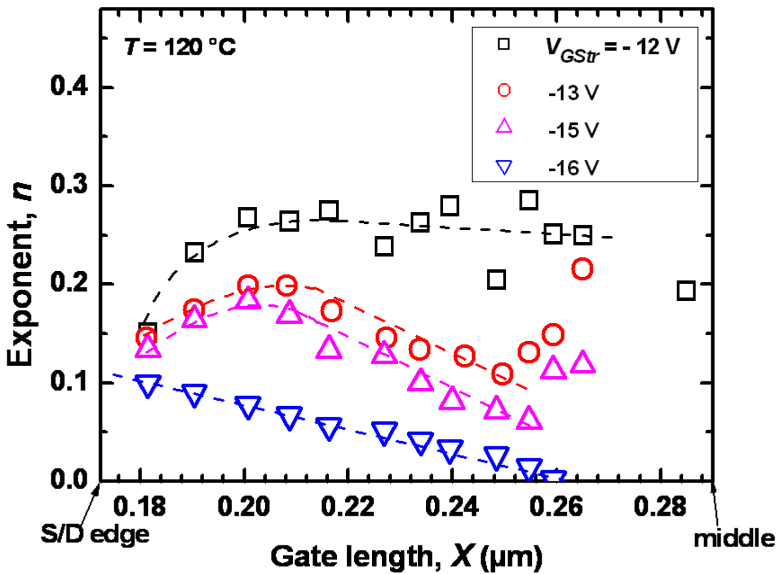


Figure V.7: Exponent n as a function of channel position for different stress voltages at 120 °C.

ultra-fast measurements. They showed that the trap density is inversely proportional to the exponent n. On the other side, n is less sensitive to the electric field at the edges compared to the middle of the channel, because the trap generation located near the edges saturates more rapidly at low field, which then requires long time and high field to reach saturation **[181]**. In addition, the trap precursors at the edge regions are similar for all transistors, since the LDD structures are fabricated by the same for all transistors **[204]**. More likely, the exponent n at the edges decreases slowly with field and is expected to be the same in the whole channel for long stress time, when the NBTI-induced traps will be uniform from the edges to the middle of the channel. This behavior

cannot be revealed in conventional NBTI MSM, where only an average value along the channel is observed. The assumption of diffusion-limited transport as the sole source of time dependence of NBTI degradation is eliminated, since the *n* varies with time and position in the gate channel. From the electrical viewpoint, one can conclude that transistors with shorter gate length saturate faster than those with longer gate length for the same stress conditions **[181]**. Moreover, the saturation of *n*, observed in our experiments, implies an increase in predictive lifetime of the devices contrary to traditional predictive models which are more severe since they are based on power-law fits.

The apparent activation energy ($E_{a,eff}$) as a function of the channel length for different stress times at – 6MV/cm is shown in **Fig. V.8**, where similar dependence on channel length is also observed. At early stages of the degradation, $E_{a,eff}$ shows an increase from edges to the middle of the channel and varies from 0.5 to 0.84 eV. Then, it decreases with stress time up to 10800s and 25200s, where it reaches a constant value of about 0.1 eV. Instead of assuming all experimentally sensed interface defects to be energetically the same over the channel length, one has to distinguish between the contribution of defects from the edges and the middle of the channel **[181]**. For each defect, an apparent energy can be assumed depending on its position in the channel and on its surrounding structure. According to Grasser et *al.* **[62,169]**, the physical activation energy of an individual trap ranges between 0.5 and 1 eV. These values are in accordance with those experimentally obtained at the beginning of the stress. The lower values of activation energy observed at long stress times are probably due to the superposition of activation energies of individual traps. In fact, the longer the stress time, the lower the activation energy. This reinforces the idea that the apparent activation energy is actually a combination of the real individual trap activation energy, the density of state (DOS), the gate geometry, and the experimental conditions **[126,193]**. Unlike the activation energy, the reference electric field (E_{ref}) does not change with stress time and shows a slight variation across the channel (from 0.5 to 1.5 MV/cm). Therefore, it can be assumed to be constant along the channel with a typical value of 1 MV/cm (see **Fig. V.9**).

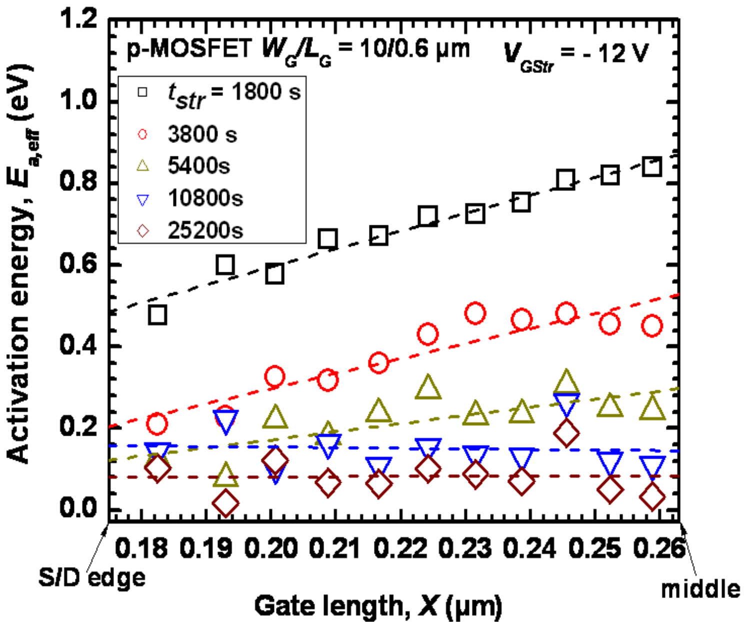


Figure V.8: Activation energy, E_a as a function of channel position for different stress times at – 6 MV/cm.

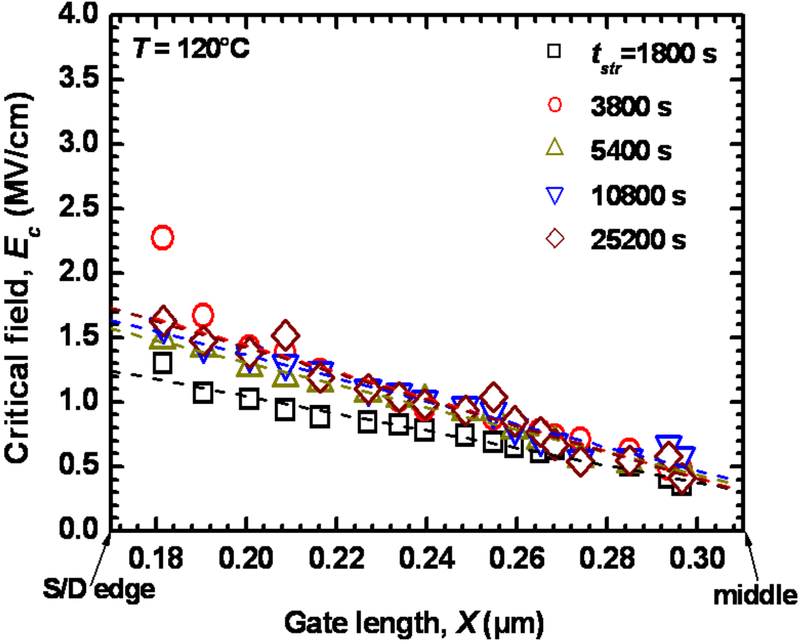


Figure V.9: Reference electric field (E_{ref}) as a function of channel position for different stress times at 120 °C.

V.5- ΔN_{it} Propagation Result Analysis and Discussion

According to previous results, NBTI degradation increases with decreasing gate length. This fact cannot be caused by the lateral electric field, which is always associated with the non-uniform damage in transistors. In addition, it is basically understood that NBTI should not exhibit any gate length dependence. Nevertheless, it is reported elsewhere that NBTI could worsen with gate length reduction, which is still unexplained **[179,180]**. Some reports have assigned it to the proximity of the gate channel to the source and drain (S/D) edges and the dielectric spacers **[188]**. A possible explanation of this inhomogeneous effect during NBTI stress is the non-uniformity of the initial lateral distribution of the interface-trap before NBTI stress, as shown in **Fig. V.1 (b)**. Indeed, Jin et *al.* **[201]** have shown that the enhanced interface-trap generation near the gate edges is mainly responsible for NBTI channel dependence. The latter is affected by technological process steps such as LDD structure, ion implant, etch processes and so on.

We remind here that the channel length dependence of NBTI degradation, studied in this part, has been performed on Boron doped LDD (B-LDD) (see process in **Chapter III,** section **§ III.2**) samples which show strong channel length dependence. The same effect has been found elsewhere for similar devises **[201]**. In the latter, the authors have shown that gate length dependence of NBTI is more important in samples with B-LDD than those with BF_2-LDD. They explained their results by the suppression of the defect generation near the edges due to the incorporation of fluorine, where they showed that the local interface-trap density near the gate edges is much higher in B-LDD devices than that of BF_2 devices. Therefore, in our work, boron from studied devices increases NBTI. It can diffuse into the gate oxide from the B-LDD and source/drain implants. The boron penetration has been observed to increase the oxide traps **[200]**. But its concentration at the edges is higher than at the middle. As a result, it primarily generates defects at the edges and contributes to the intrinsic non-uniform lateral distribution of defects. This can in part explain the higher densities at the channel edge

as well as the strong dependence on L_G (observed in the above figures), since the oxide-trap near the interface (border-trap) could also contribute to CP signal even at 1 MHz **[181]**.

Another possible source of trap generation in our device could be the spacer formation step, which is formed by LPCVD TEOS deposition. The TEOS reaction generates water (H_2O) that can diffuse and contaminate the oxide. The effect of H_2O has previously been reported **[88]**. Molecular H_2O, which is a depassivating reactant, can penetrate into the SiO_2 layer until it finds a favorable site where it reacts to give Si hydroxyl group in the vicinity of the gate-oxide/channel interface. Furthermore, Ushio et *al.* **[212]** have computed the reaction energy of H_2O using first principal molecular calculation. They found lower reaction energy for H_2O than hydrogen (H). H_2O reaction with oxygen (O) induces insertion of OH into vacancy and generates H atom. The latter recombines with the H of P_b passivated Si-H bond, generating interface-trap. In addition, the TEOS annealing densification step under N_2/O_2 forming gas would enhance NBTI degradation in our devices. The nitrogen can diffuse trough TEOS to the gate oxide edge and lead to more sever NBTI effect. Usually nitrogen makes NBTI worse as reported in the literature **[184,213]**.

The process steps provide evidence that enhanced interface-trap near the edges before NBTI stress is responsible for strong channel length dependence of NBTI. A possible role of oxide-trap located at the LDD vicinity cannot be ruled out, since CP-method also measures those types of traps. From the aforementioned analysis, it is clear that the process plays a major role in non-uniformity of lateral distribution of interface- and oxide-trap along the channel length **[181]**. That is why a tradeoff between the process optimization for good NBTI lifetime and optimal device performance should be achieved.

Following the above-cited analysis, boron and hydrogen, diffusing laterally form edges, add more damage in these regions **[22,200,201]**. Since NBTI is sensitive to the initial trap densities, more NBTI degradation occurs if more damage is present in gate edges and LDD overlap. Accordingly, it has been proposed that the pre-stress trap density at the vicinity of the channel ends is higher than the one prevailing in the middle of the channel **[200,214]**. Compared to long channel transistors, the NBTI degradation is significant in transistors with short channel, since the weak points are located near the gate edges **[181]**. Thus, the scaling down of technology leads to a significant increase in the susceptibility to NBTI degradation, not only because of an increasing vertical electric field oxide, but also a reducing of gate length. The same behavior has been found by Zhou et *al.* **[205]** in poly-Si thin-film transistors (TFTs), where NBT-induced degradation is higher and saturates earlier for shorter L devices.

In addition, by screening the lateral distribution of NBTI-induced interface-trap, it is obviously shown that the NBTI degradation propagates from S/D regions toward the middle of the channel until saturation. In other words, it starts from fragile regions and propagates to robust ones. The propagation speed increases with temperature and electric field. The exponent n analysis regarding L, T, E_{OX}, and t_{str} shows that its dispersion, found by different authors **[22,40,53]**, could be explained by the propagation concept. In fact, in the past, researchers have characterized the average NBTI degradation over the whole gate channel length; that is why they found different n values. Thus, the latter not only depends on how the measurement is fast or not, but also on gate length. The longer the gate length, the harder to reach the lower n values.

However, the scanning method, presented here, has a limitation to probe NBTI degradation near the channel center for devices with long gate. However, it can help to deeply analyze the NBTI degradation in transistors with short gate length. This approach could be able to provide more correct evaluation of NBTI, thus enabling to develop accurate models for device life-time prediction. In addition, border traps, having a response time within the pulse period, contribute in CP-current inducing an overestimation of interface traps even at 1 MHz. Therefore, it would be beneficial to carry out analysis to assess their contribution by performing deep scan into the oxide near the interface. We will complete the lateral distribution picture by adding the vertical one.

PART II: VERTICAL PROPAGATION OF THE PERMANENT COMPONENT

In this part, we have screened the NBTI-induced border-trap (N_{bt}) depth in the interfacial oxide region of p-MOS transistors using multi-frequency charge pumping (MFCP) method. We emphasize on the distribution of the permanent component in the oxide near the interface, giving a clear insight on its effect on NBTI features. According to experimental data, the exponent (n) of the power-law time dependence of border-trap generation (ΔN_{bt}) as well as its apparent activation energy ($E_{a,eff}$) decrease with stress temperature (T) and voltage (V_{Gstr}). They are more sensitive to V_{Gstr} than T. Furthermore, the extracted effective dipole moment (a_{eff}) and field-independent activation energy (E_a) have revealed a linear relationship with depth distance (Z), which can consistently explain the variation of n as well as $E_{a,eff}$ with T and V_{Gstr}. In fact, the former parameters decrease because of the cumulative contribution from traps having different thermal activation energies. We suggest that such traps are probably related to $O_{3-x}Si_xSi$-H (x = 1 and x = 2) family defects (or P_b center hydrogen complex) located in the interfacial sub-oxide region.

V.6- Vertical Profiling Experiments

To examine the NBTI-induced traps in the interfacial oxide region, we have performed scanning profile of the permanent components. The profiles are obtained using on the fly (OTF) MFCP **[135,136,209]** (OTF-MFPC) method (Here the term "OTF" refer to the fact that $V_L = V_{Gstr}$ in both stress and measure phases and there is no delay between stress and measure phases). The frequency (f) of the signal, illustrated in **Fig. II.3** of **Chapter II**), is varied from 500 kHz to 5 kHz by changing the high level voltage time (T_H) and the low level voltage time (T_L) ($T_H = T_L$), while rising and falling time slopes are kept constant (α = 0.1 V/ns). This is to guarantee that the lower and higher energy boundaries contributing to CP remain unchanged, even though the amplitude increases. We have used transistors with short gate lengths (< 1 µm) to avoid both geometric and quasi-geometric components at high **[215]** and low **[216]** frequencies, respectively, and a thick gate oxide of 20 nm to reduce the parasitic leakage current and tunneling current.

V.6.1- Vertical profiling before NBTI stress

Before starting NBTI stress, we have first measured CP-current (I_{CP}) as a function of the frequency for all used transistors. **Figure V.10** illustrates the as-measured I_{CP} of transistors with fixed W_G = 10 µm and varied L_G = 1, 0.95, 0.9, 0.85, 0.8 µm at room temperature (27 °C) **[Fig. V.10 (a)]** and 120°C **[Fig. V.10 (b)]**. The curves are obtained using MFCP method with fixed signal amplitude, ΔV_G at 4 V.

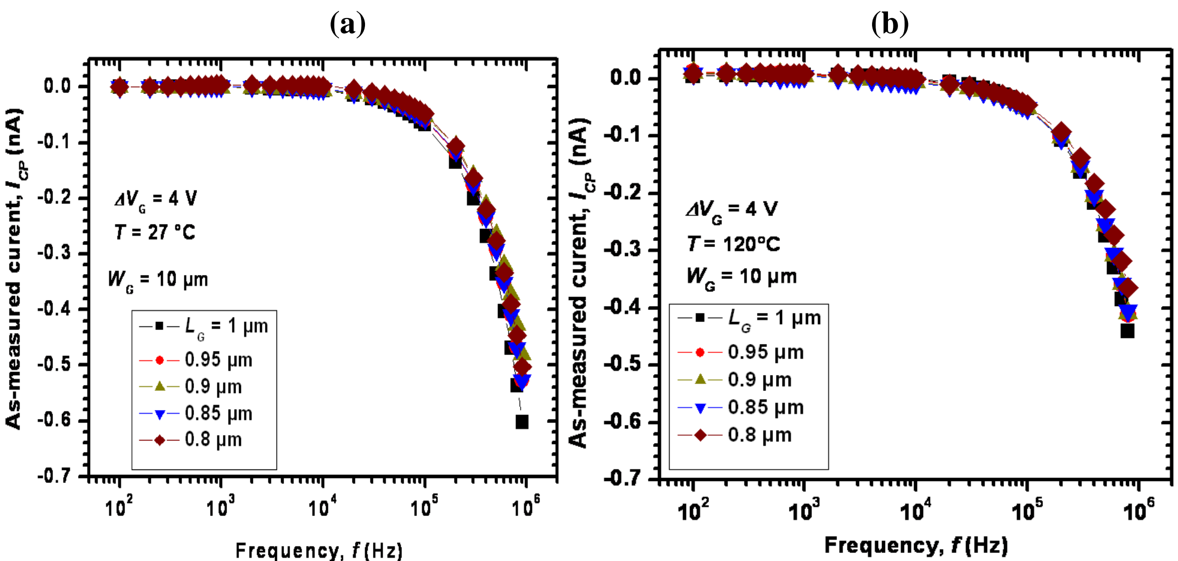


Figure V.10: Charge pumping current, I_{cp} versus frequency for p-channel transistors with fixed gate width and varied gate length at room temperature, 27 °C (a) and 120 °C (b). Measurements are performed using gate pulse amplitude of 4 V.

As expected by theory, I_{CP} decreases with decreasing f as well as with increasing T **[56]**. Indeed, the higher the temperature, the smaller the emission time constants and the narrower the active energy interval, inducing reduction of the maximum CP-current. Moreover, all transistors used in these experiments exhibit the same features regarding I_{CP} versus f, indicating the absence of any artifact due to any difference in devices.

V.6.2- Vertical profiling after NBTI stress

The NBTI permanent component profiling is carried out using MSM protocol, as illustrated on **Fig. V.11 (a)**. During the stress interval, V_{Gstr} is applied, through a *DC* voltage, onto the gate of the device. After each stress time, a gate pulse train with different frequencies is applied, without modifying the experimental setup. The gate trapezoidal signal has an amplitude of $\Delta V_G = V_H - V_{Gstr}$ with $V_L = V_{Gstr}$, duty cycle 50%, source and drain voltage (V_S=V_D=V_R) set at 0 V, while f is varied from 5 kHz to 500 kHz with step of 10 kHz. The measurement time to scan all frequencies is 30 s. This time is kept constant during all MSM cycle for different T and V_{Gstr}. The whole stress time cycle is fixed at 7.5 hours.

The frequency is limited by the Agilent HP 4156C capabilities, while the low frequency is chosen as low as needed for the CP signal to remain distinguishable from leakage current induced by the amplitude of the signal. Obviously, this limits the scanning depth into the oxide layer, but it is not an issue, since NBTI phenomenon occurs at the vicinity of the interface **[29,40,124]**. Different ΔV_G are used; 10, 11, and 12 V, V_L = - 8, - 9, and - 10 V (used for stress), and V_H is fixed at 2 V, respectively, except if otherwise specified. The MSM consists of stressing p-MOS transistors with different V_{Gstr} at room temperature (27 °C) and elevated T (80 and 120 °C). The permanent CP-current component was measured at different frequencies after 30, 90, 180, 300, and 450 min of stress time, as shown on **Fig. V.11 (b)**. The latter gives the as-measured CP-current for different frequencies at V_{Gstr} of - 8 V and T = 120 °C. The first plot illustrates the current taken with ΔV_G = 10 V before stress (i.e. at t = 0). All plots show the same features, they decrease with decreasing f **[56]**. However, the absolute value of

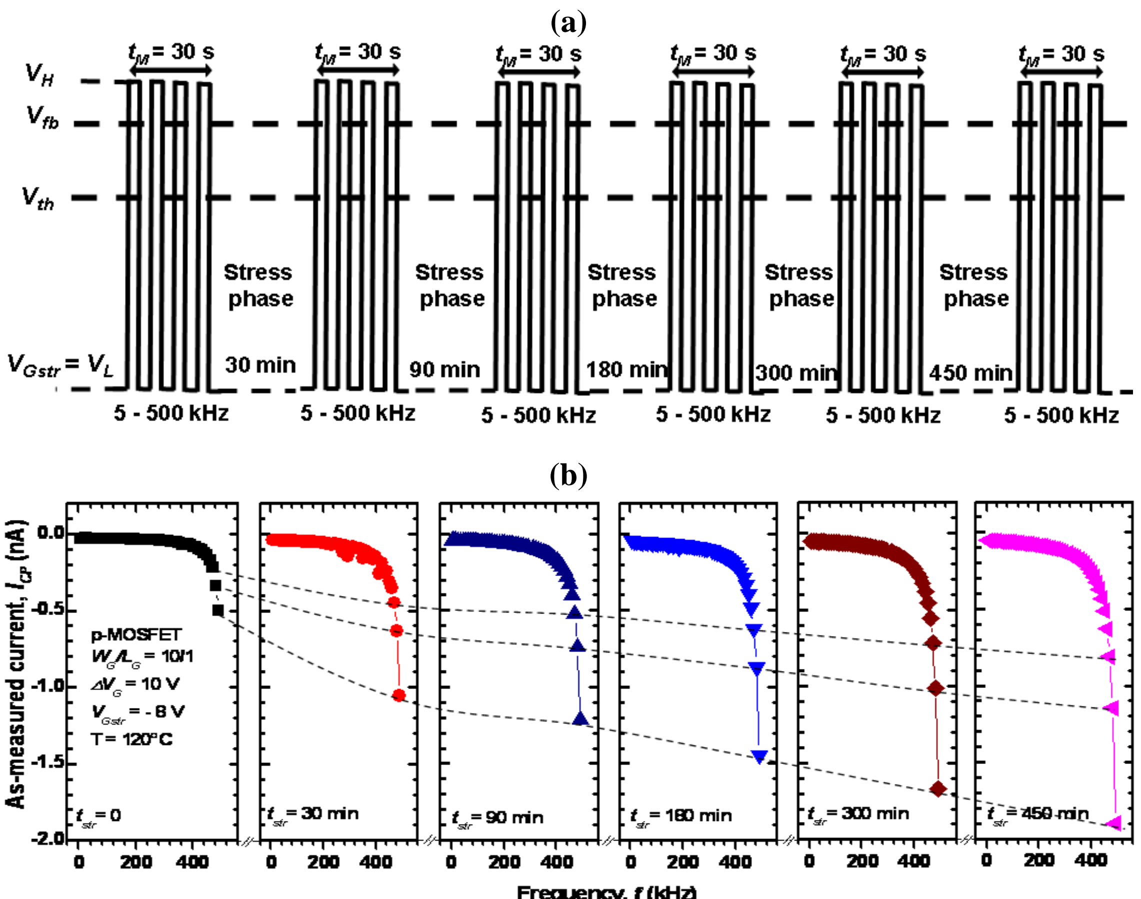


Figure V.11: (a) Meaure/stress/measure (MSM) protocol used to extract the profile of the NBTI permanent component in the interfacial oxide region. (b) Frequency dependence of I_{CP} in p-channel transistor for different stress times at 120 °C and – 8 V. Measurement performed with trapezoidal gate pulse of amplitude 10 V and varied frequency.

I_{CP} increases with stress time for each *f* as illustrated by the dashed lines. In other words, I_{CP} is more important after the stress for the same *f* (i.e. the same region in the Si/SiO_2 interfacial region). This fact indicates that NBTI stress introduces new traps that are lying from Si/SiO_2 interface to the interfacial oxide layer. To deeply investigate such a kind of traps, we have explored their distribution in the next sections.

V.6.3- Extraction method of border-trap density

Using MFCP method, the charge recombined by cycle at the interface and in the sub-oxide interfacial layer can be estimated by:

$$N_{CP}(f) = \frac{Q_{CP}(f)}{qA_G} = \frac{|I_{CP}(f)|}{qA_G f} \quad \text{(V.2)}$$

Typically, CP-current at high *f* (in our case: 500 kHz) is traditionally attribute to recombination current at N_{it} traps of Si/SiO_2 interface **[56]**. As compared to N_{it}, the additional traps N_{CP} at lower frequencies are related to the contribution from bulk traps in the SiO_2 dielectric near the interface **[136]**. These border traps are lying into the sub-oxide interfacial region and their densities can be estimated for each *f* as:

$$N_{bt}(f) = \frac{\left|Q_{CP}(f) - Q_{CP}(f_H)\right|}{qA_G} = \frac{\left|Q_{CP}(f) - Q_{CP}(500kHz)\right|}{qA_G} \quad \text{(V.3)}$$

where q (C) is the electron charge, A_G (cm^2) is the gate area, f_H (Hz) is the higher frequency (traditionally considered for interface-trap), f (Hz) is the frequency, I_{CP} (A) is the CP-current, and Q_{CP} (C) is the charge recombined by cycle. N_{bt} (f) (cm^{-2}) is given as cumulative areal border-trap density (brought to the Si/SO_2 interface area).

On the other hand, f is related to the tunneling distance into the oxide **[139]**, as shown in **Chapter II**. Combination **Eqs. (II.12)** and **(II.13)**, the depth in the oxide as a function of signal parameters can be written as:

$$Z = \frac{\hbar}{2\sqrt{2m_p E_V}} \ln\left[p_s \sigma_p(0) v_{thp} \left(\frac{1}{2f} + (2\frac{V_L - V_{th}}{\Delta V_G} - 1)\frac{\Delta V_G}{\alpha}) \right) \right] \quad \text{(V.4)}$$

where $\sigma_p(0)$ is the capture cross section at the Si/SiO_2 interface, p_s is the hole concentrations at the silicon surface during inversion time, v_{thp} is the hole thermal velocity, E_V is the energy barrier height for holes, m_p is the effective mass for hole, $\hbar$ is the reduced Plank's constant, V_{fb} and V_{th} are the respective flatband and threshold voltages, α is falling time slopes ($\Delta V_G/t_f$). Since some parameters are T-dependent, so Z is calculated for each T. The extraction program T_{acc}, T_{inv}, ΔE^*, and Z is given in **appendix (D.3)**.

From **Eqs. (V.2)-(V.4)**, one can extract the distribution of traps in the interfacial oxide region. To get the cumulative ΔN_{bt} during NBTI stress, we have used the following equation:

$$\Delta N_{bt}(t_{str}) = N_{bt}(t_i) - N_{bt}(t_0) \quad \text{(V.5)}$$

where $N_{bt}(t_0)$ and $N_{bt}(t_i)$ are border-trap densities before and during incremental stress time, respectively.

V.6- Depth Profiling of NBTI-Induced Border-Trap

It is worth recalling that when f is decreased, the applied gate voltage drives the device into inversion regime for a longer time; allowing tunneling processes to take place, not only into the N_{it}, but also into the N_{bt} within a distance appropriate for a given f **[136]**. However, the leakage parasitic current can compromise the analysis of CP data as a function of f, especially in NBTI stress using all OTF CP-based methods **[55,151]** where V_L (for p-MOSFET) is set at high V_{Gstr} resulting in excessive tunneling into oxides **[117,217]**. In fact, in devices with thick a gate oxide, the leakage current is negligible. However, this is not the case in stress phase at elevated temperature and field and hence it should be removed from the measured current **[218]**. Classically, the leakage current correction is applied to the experimental data by either a subtraction of the current at 0 Hz-f CP **[219]** or the subtraction of the current of the lower frequency current from the higher frequency current **[217]**. Veksler et *al.* **[220]** have subtracted 1 kHz-f CP-current from all the experimental data. In our case, we have subtracted CP-current at low frequency (5 kHz) from higher frequencies data.

In **Fig. V.12(a) and (b),** we have respectively presented the NBTI-induced N_{CP} (or N_T) density and the cumulative N_{bt} as a function of the depth into the oxide (Z). They are extracted using **Eqs. (V.3)**

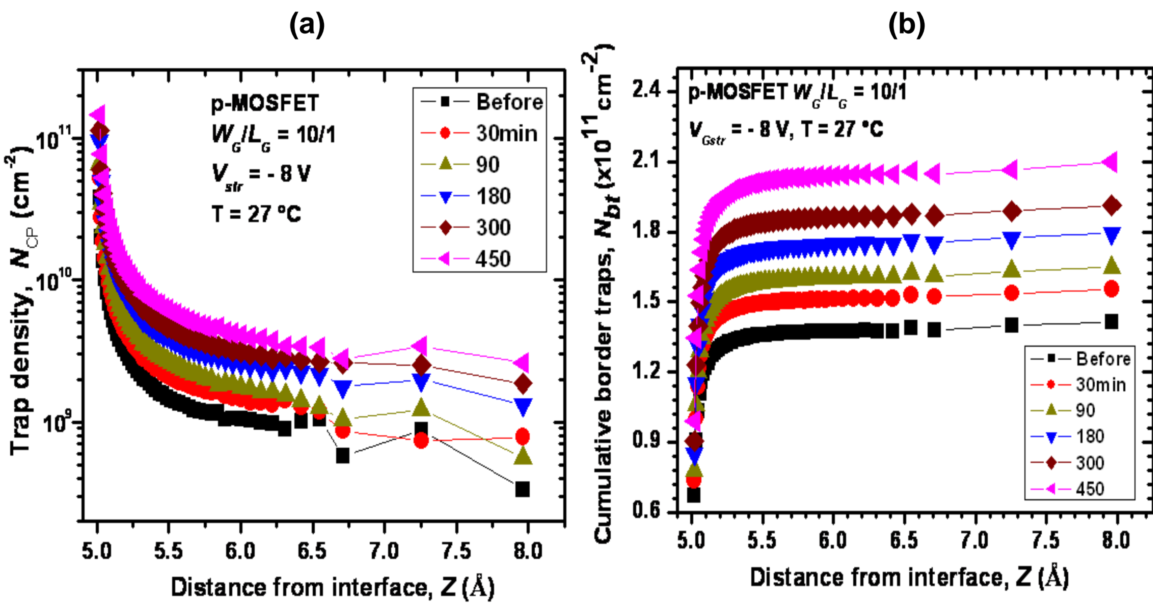


Figure V.12: (a) Depth trap profiling before and after NBTI stress for different stress time at – 8 V and 27 °C. (b) cumulative border trap profiles before and after NBTI stress for different stress time at – 8 V and 27 °C.

and **(V.4)** at 27 °C and – 8 V for different stress time. The trap profile has the same shape as reported in the literature by using calculation and measurement **[221,222]**. The profile before stress is performed at the beginning of stress phase, i.e. at t_{str} = 0, ΔV_G = 10 V and V_{Gstr} = V_L = – 8 V. This measure is taken as the reference for the degraded profiles. Note that the extracted data concerns traps contributing to permanent component of NBTI. It is obviously clear that NBTI stress influences the trap density profile. The longer the stress time, the higher the trap density. To estimate NBTI effect on trap distribution, we have subtracted the profile before stress from the profiles obtained after each stress time as indicated by **Eq. (V.5). Figure V.13** shows the variation of the cumulative ΔN_{bt} profile with NBTI conditions; **Fig. V.13 (a)** for various *T* and **Fig. V.13 (b)** for V_{Gstr}, while stress time is varied from 30 min to 450 min. From the electrical viewpoint, the cumulative ΔN_{bt} effect increases rapidly with *Z* and tends to an almost constant value. That means there are no significant additional traps. However, ΔN_{bt} presents an important augmentation with *T* and V_{Gstr}. Quantitatively, ΔN_{bt} is more affected by V_{Gstr} than *T* and tends to saturate with higher stress voltage at 120°C.

All the illustrated curves in **Figs. V.12 and V.13** start roughly at 5 Å. They are obtained for capture cross sections of electrons and holes at the Si/SiO_2 interface $\sigma_n(0)$ = 5 10^{-15} and $\sigma_p(0)$ = 10^{-16} cm^2 and m_n = m_p = 0.5m_0 (details are given in **[135]**). At f_H = 500 kHz, we have found that CP-signal corresponding to fast traps, comes not only from N_{it} but also from defects located at approximately 5 Å within interfacial oxide layer, even if frequency is increased (for example 1 MHz corresponds to *Z* = 4.6 Å and 10 MHz to Z = 3.5 Å). That means that the electrical CP-interface cannot be a perfect line but rather extends few angstroms into the transition oxide layer. The same observation has been reported by other research groups **[117,211]**. Thus, whatever the frequency, there is always a contribution from traps located in the oxide near the interface to the CP signal. Using f_H only permits to minimize the contribution of border-trap to CP-current. Therefore, what is the consequence of this inference on Reaction-Diffusion (R-D) model? To understand the dynamic of traps located at the interfacial oxide

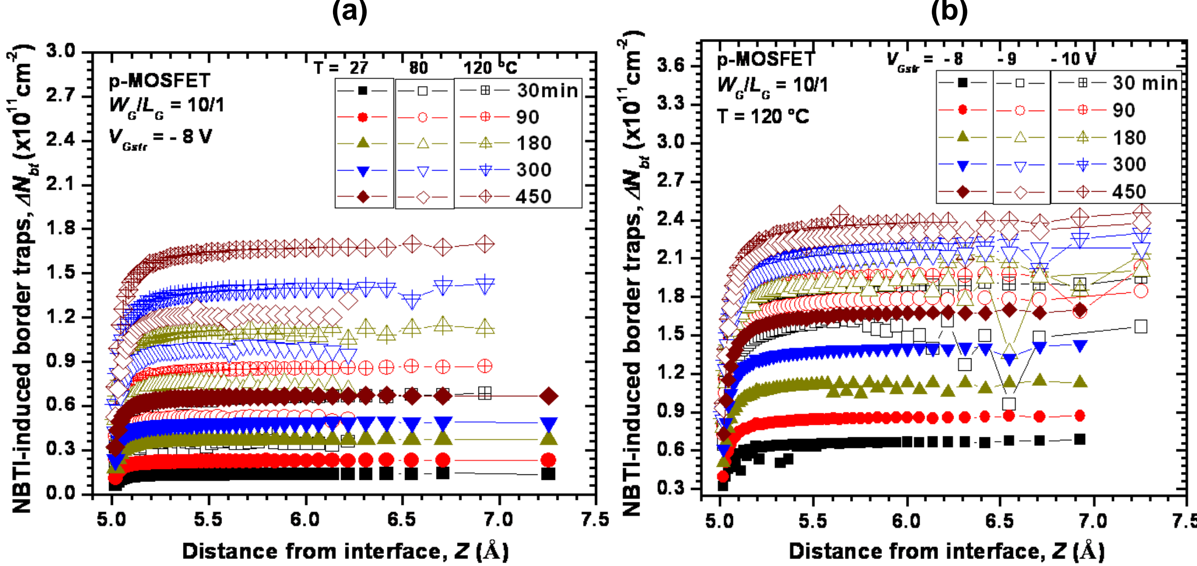


Figure V.13: NBTI-induced cumulative border trap, ΔN_{bt} as a function of depth, Z (a) for different stress temperatures at – 8 V and (b) for different stress voltages and 120 °C.

region and their role in the NBTI degradation, we have deeply investigated *T*, V_{Gstr}, and time dependence of NBTI-induced ΔN_{bt}.

V.7-Time and Temperature Dependence of ΔN_{bt}

V.7.1- Time dependence of NBTI-induced ΔN_{bt}

As NBTI degradation depends primarily on stress time, we initially plot, in **Fig. V.14 (b) and V.14 (c)**, ΔN_{bt} as a function of the stress time for different V_{Gstr}. In log-log scale, all ΔN_{bt} curves (depicted from 5 to 7 Å) follow a power law time dependence with exponent *n* [more data are given in **appendix (E.1)**]. The exponent *n* is plotted in **Fig. V.14 (a)** for different V_{Gstr} and *T*. It is roughly constant with *Z*. However, it decreases with V_{Gstr} and *T*, and is more sensitive to the former than the latter. It varies from 0.58 to 0.34 when *T* is varied from 27 to 120 °C at – 8 V, while it lies between 0.22 and 0.1 when V_{Gstr} is increased to – 9 and – 10 V for the same set of *T* and tends to saturate around 0.1. On the other hand, *n* tends to be less sensitive to V_{Gstr} and *T* when the trap generation reaches saturation, as shown in **Fig. V.13**. This behaviour indicates that ΔN_{bt} increases more at higher V_{Gstr}. Indeed, *n* is related to the amount of traps, i.e. the lower the trap generation, the higher the exponent *n* and vice versa, as reported elsewhere **[50]**. The latter report has also indicated that the variation of *n* with *T*, in the as-measured I_{CP}, could be consistently explained by considering the different thermal activation of two different defects. This supposition could clarify our cumulative border-trap behavior with stress conditions in CP measurement. In addition, the fact that *n* does not change with *Z* under NBTI conditions (used in this work) indicates the presence of the same family of defect precursors with the same apparent thermal activation energy in the scanned interfacial oxide layer (which does not mean the same activation energy for the individual trap). To validate this assumption, we have investigated *T* dependence of border traps and extracted their $E_{a,eff}$.

V.7.2- Temperature dependence of NBTI

The evolution of $E_{a,eff}$ with depth (*Z*) for different V_{Gstr} is plotted in **Fig V.15 (a)**. $E_{a,eff}$(Z) curves are extracted from the slope of ΔN_{bt} as a function of *T* for different stress times and V_{Gstr}, as illustrated in

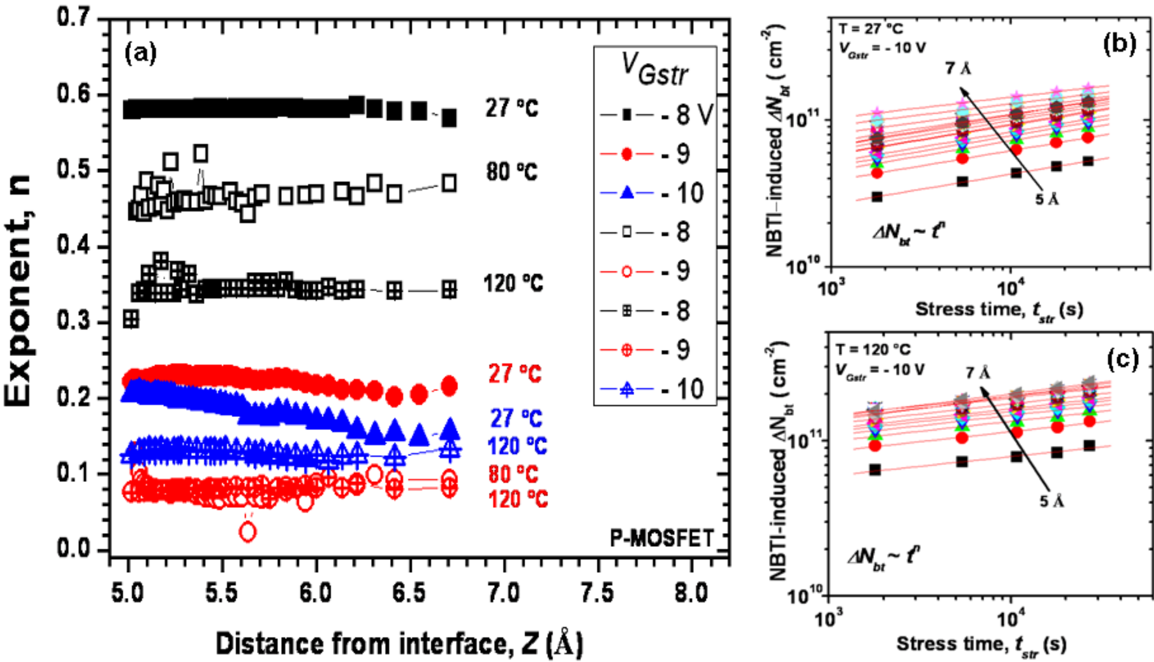


Figure 14: Time dependence of NBTI-induced ΔN_{bt}. (a) Exponent (*n*) as a function of depth (*Z*) for different temperatures and voltages. NBTI-induced ΔN_{bt} as a function of stress time, (b) at 27 °C and – 10 V, (c) at 120 °C and – 10 V.

Figs. V.15 (b) and V.15 (c) [more data are given in **appendix (E.2)**]. ΔN_{bt} dependence on T follows Arrhenius behavior. **Figure V.15 (a)** shows that $E_{a,eff}$ of the processes involved in the generation of ΔN_{bt} decreases with t_{str}, while it is roughly constant with Z (similar behavior as n), except for – 10 V, where a small decrease is observed. Z-$E_{a,eff}$ dependence could explain Z-n dependence shown in **Fig. V.14**. t_{str}-$E_{a,eff}$ dependence arises from the superposition of different traps having different E_a and capture/emission time constant **[50]**. In fact, if the amount of NBTI-induced ΔN_{bt} is only influenced by the creation of a single type of traps (same structure), $E_{a,eff}$ should be the same. Similar deduction has been made by Grasser et *al.* **[192,193]** using time-dependent defect spectroscopy (TDDS) method. They have shown that the physical microscopic E_a of the individual trap is about 0.5 – 1.2 eV in small gate area devices. They explained the small macroscopic $E_{a,eff}$ (0.1 eV) observed in large area devices **[119]** by the individual trap energy superposition. Consequently the measured macroscopic $E_{a,eff}$ in large area devices is an apparent activation energy resulting from a large number of defects **[62]**.

In addition, the field-induced barrier reduction of chemical bonds can also be at the origin of field dependence of activation energy **[17,22]**. In fact, the field dependence of interface-trap activation energy is explained by field-enhanced thermal dissociation of Si-H bond, which is expressed as ~ $exp[-(E_a - a_{eff}.E_{OX})/KT]$, where E_a represents the activation energy for Si–H bond dissociation, $a_{eff}.E_{OX}$ is the thermal barrier lowering due to positioning of Si-H bond in the electric field (E_{OX}), and a_{eff} is the effective dipole moment **[100]**.

To verify whether the above-cited suggestions; i.e. the superposition of trap activation energies, or the field-induced barrier reduction, or both are behind the decrease of $E_{a,eff}$ in our devices, we have investigated $E_{a,eff}$-dependent field in the next section **§ V.7.3**.

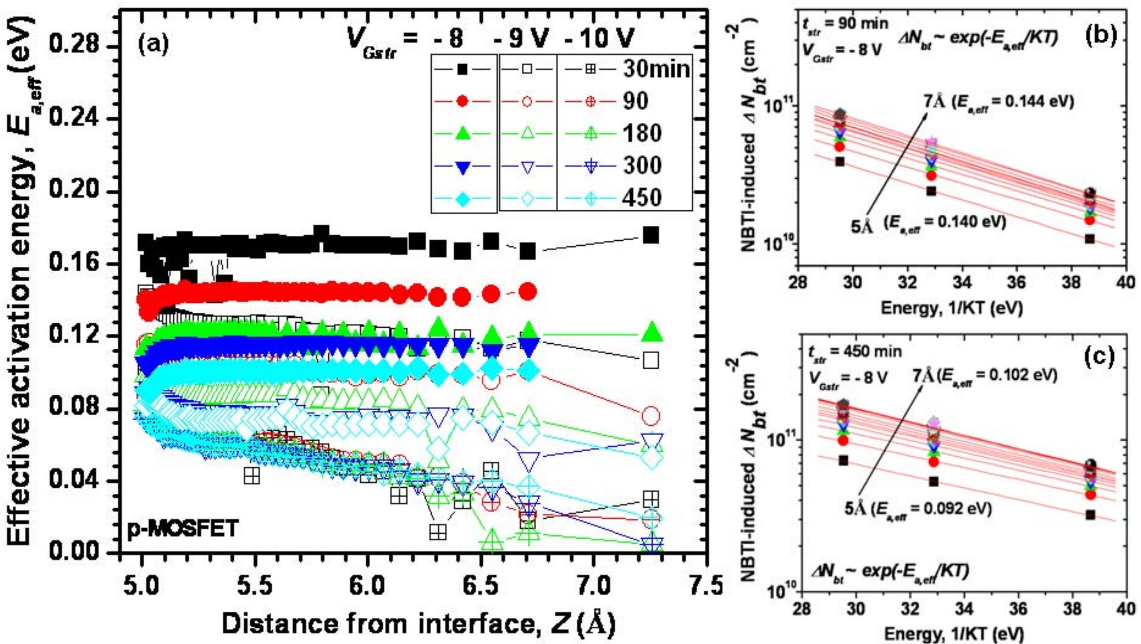


Figure V.15: Temperature dependence of NBTI-induced ΔN_{bt}. (a) Effective activation energy ($E_{a,eff}$) as a function of depth (Z) for different stress times and voltages. NBTI-induced ΔN_{bt} as a function of temperature (b) after 90 min at – 8 V and (c) after 450 min at – 8 V.

V.7.3- a_{eff} and E_a distributions in the interfacial oxide layer

It is widely accepted that the NBTI degradation originates from the electrochemical reaction at the Si/SiO_2 interface, where Si-H bond can break under thermal stress due to strong coupling of intrinsic defect activation energy with the local oxide electric field **[17]**. This dipole-field coupling lowers the activation energy required for thermal bond breakage and accelerates the dielectric degradation process **[100,224]**. As previously shown, our experimental investigations reveal a strong dependence between $E_{a,eff}$ and E_{OX}. To experimentally determine a_{eff} and E_a (for E_{OX} = 0) of traps that are at the origin of ΔN_{bt} behavior, we plot $E_{a,eff}$ versus E_{OX}. **Figure V.16** presents $E_{a,eff}$ (E_{OX}) for stress time of 90 min [**Fig. V.16 (a)**] and 450 min [**Fig. V.16 (b)**]. More data on $E_{a,eff}(E_{OX})$ can be found in **appendix (E.3)**. $E_{a,eff}(E_{OX})$ curves give a_{eff} as the slope and E_a as the intercept at E_{OX} = 0. The extracted parameters versus Z are plotted in **Fig. V.17 (a)** for a_{eff} and **Fig. V.17 (b)** for E_a, respectively. Both parameters present a linear relation with Z (from 5 and 7 Å) and are roughly constant with stress time [see their respective slopes (B and B') versus stress time in **Fig. V.18**]. According to **Eq. (V.4)**, the minimum scanned Z is 5 Å for a frequency of 500 kHz. Therefore, to get E_a and a_{eff} corresponding to Z < 5 Å, we have linearly extrapolated E_a(Z) and a_{eff}(Z) functions to Z-axis. We have found that $E_a(Z_0)$ = E_0 ~ 0.11 eV and $a_{eff}(Z_0)$ = a_0 ~ 1.2 q. Å. These values, calculated and experimentally extracted elsewhere for Si-H bond in R-D model **[17,119]**, are located at a distance Z_0 ~ 3.2 Å. Interestingly, the latter is in the range of the interface roughness (or interface thickness, δ in R-D model), which is about 0.2-0.3 nm **[17,34,86]**.

On the other hand, a_{eff} data rang between 3-10 q.Å, as shown in **Fig. 17 (b)**. Likewise, theoretical calculations of McPherson **[223,224]** have shown that the effective dipole moment of 7 q.Å is consistent with an oxygen vacancy (Si-Si) bond, or a hole-captured Si-O bond, or a Si-H bond, while the strained Si-O bonds are associated with 13 q.Å dipole. They have also found that the normal Si-O

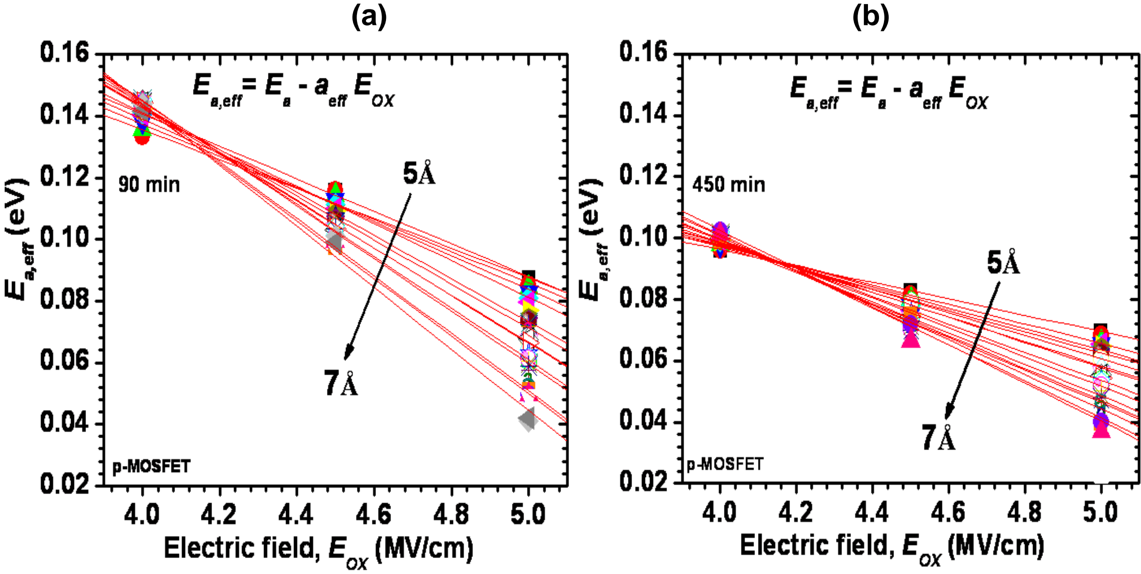


Figure V.16: $E_{a,eff}$ as a function of electric field (E_{OX}), illustrating extraction procedure of E_a and a_{eff}.

bond activation energy reduces from 2 eV at an electric field of 5 MV/cm (when the H^+ ion is far away from the bond) to only 1 eV (when the H^+ ion is within 0.5 Å of the Si-O bond). Contrarily to Si-H bond (located at the interface), which has Si atom back-bonded to three Si atoms, the Si-H located in the interfacial sub-oxide region has Si atom back-bonded to different combinations of Si and O atoms. This point will be detailed in the next section **§ V.8**. Furthermore, E_a ranging between 0.3-0.6 eV **[see Fig. V.17 (a)]** approaches those reported in **[62,192]** for an individual trap in the oxide (between 0.5 and 1 eV). However, the lower activation energies (0.1 – 0.3 eV) result from the superposition of several trap activation energies **[192,193]**. Therefore, there are more defects located at a distance very close to the interface than far away from the interface. According to these data, ΔN_T can be expressed as:

$$\Delta N_T \propto A(E_{OX}) \exp -\left[(E_0 - a_0 E_{OX}) / KT\right] \exp -\left[(B - B' E_{OX})(Z - Z_0) / KT\right] * t^n \qquad \text{(V.6)}$$

where, $A(E_{OX})$ is a pre-factor depending on electric field. From **Eq. (V.6)**, it is clear that traps involved in NBTI degradation using MFCP lie from the interface (represented by the first term) into the near-interfacial oxide region (represented by the second term). In the latter region, different traps with different a_{eff} coexist. That is why n and $E_{a,eff}$ of NBTI-induced ΔN_{bt} decreases with stress conditions, since traps are progressively involved and accumulated during stress, depending on their E_a and a_{eff}.

In our experiments, ΔN_{bt} is the permanent component of NBTI stress, since MFCP method takes 30 s to profile it, which allows to most fast recoverable traps to relax. They could be also considered as quasi permanent component, since it has been shown that defects, which do not anneal in the time scope of a given experiment, are not permanent forever **[58]**. In the scope of the present measurements, NBTI-induced traps at high frequency are not from a perfect interface line, but rather a few angstroms into the transition oxide layer even at higher frequency. The possible candidates of such kind of traps are explained hereafter. In fact, to identify the origin of E_a and a_{eff} variations with Z and subsequent T, V_{Gstr}, and time dependence of ΔN_{bt}, it is important to better understand the local

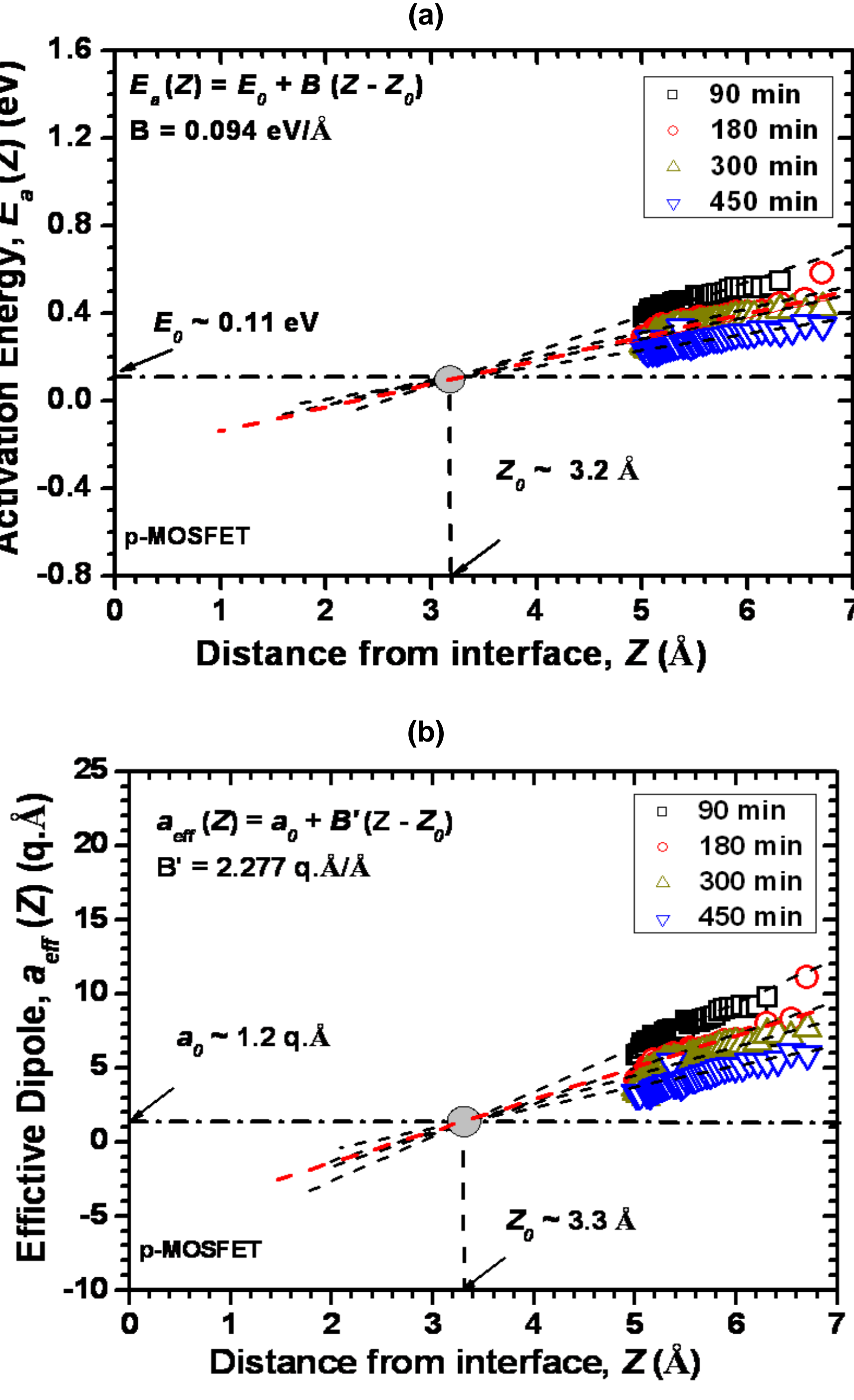


Figure V.17: (a) activation energy as a function of depth and (b) Effective dipole as a function of depth. E_0 = 0.11 eV and a_0 = 1.2q.Å are located at depth of 3.2 Å (roughness thickness) and correspond to Si-H bond at the interface in R-D model.

atomic structure of the interfacial region lying between crystalline Si-substrate and non-crystalline SiO_2 oxide.

V.8- Possible Defect Precursors Related to NBTI-Induced ΔN_{bt}

NBTI degradation is often considered occurring at the Si/SiO_2 interface, which is assumed to be a line. This picture is no long valid, because of the presence of the interfacial layer that lies into the oxide, as shown in **Chapter I,** sections **§ I.4.4 and § I.4.5**. Actually, due to Si/SiO_2 interface and bulk SiO_2 disorders, especially the interfacial region, the Si-H bonds are arbitrary distributed and oriented in

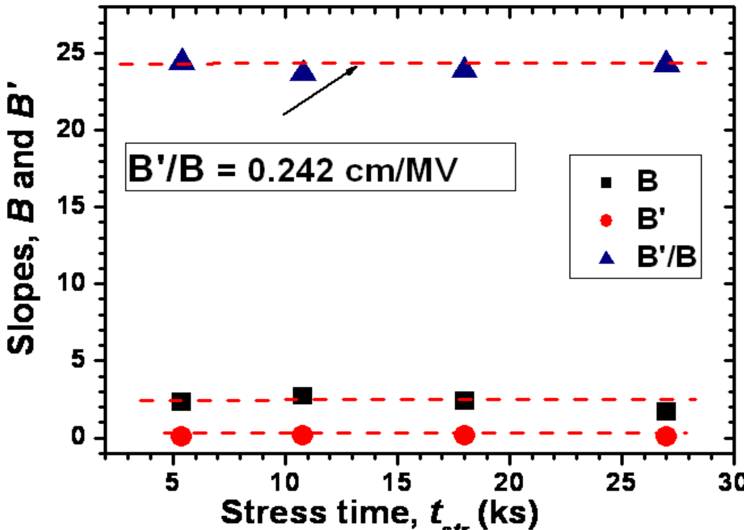


Figure V.18: $E_a(Z)$ and $a_{eff}(Z)$ slopes B and B', respectively versus stress time. B = 0.094 eV/Å, B' = 2.277 q Å/ Å, B'/B = 0.242 cm/MV.

this region, resulting in spread activation energy of different Si-H bonds. Indeed, Si/SiO_2 interface is not atomically abrupt, but somewhat shows a transition region of about 0.5 to 1 nm thick **[89,225]**. In this region, the distribution of local arrangements has an average Si-O composition and a defective region in the Si substrate and is likely to contain Si dangling bonds. Grunthaner *et al.* **[86]** have developed a coherent view of the local atomic structure of the Si/SiO_2 interface, as presented in **Chapter I**, **Fig. I.14**. They found that there is a strained region of about 1.5-3 nm containing oxygen vacancy Si-Si. In addition, there is a transition region of approximately 0.5 nm thick containing SiO_x and Si-H bonds. This region (SiO_x, x < 2) constitutes the chemical transition between the Si-substrate and the oxide in both thick and thin gate oxides **[89]**. The interface roughness is determined by the net stress projection across the interface boundary by the oxide. The interface roughness is related to the electrically active interface state density. The interface region has a substantial population density of Si-H bonds which modifies its electrical activity and chemical reactivity. The Si-H bonds lie from the interface to the strained layer of the oxide.

It is clear that the interface has a thickness in which different types of traps coexist, such as interface traps, border traps (fast and slow), and oxide traps, and hole trapping. Based on electrical electron paramagnetic resonance (EPR) and spin dependent resonance (SDR) signals, Fleetwood *et al.* **[91]** have proposed a classification of traps at and within the interface and interfacial region for radiation issue, respectively, as illustrated in **Chapter I**, **Fig. I.15**. Using this categorization of traps as well as the hydrogen species which have a substantial population in this region, we suggest for the NBTI issue, defect precursors with different Si-H bonds, as schematically represented in **Fig. V.19.** In addition to the saturated Si dangling bonds at the interface (P_b-H), $O_{3-x}Si_x$Si-H family defects coexist with x varying from 0 to 3. Their concentration is more important than that of other defect precursors at the vicinity of the interface. For x = 3 (Si_3Si-H), the Si-H bond is surrounded by three Si atoms, which is a cluster in SiO_x that looks very much like P_b-H. Therefore, when depassivated, it acts like interface P_b, only it switches more slowly, since it is located in the interfacial oxide instead at the interface. For x = 1 or 2 (O_2SiSi-H or OSi_2Si-H), the Si-H is surrounded by two O atoms and one Si atom or by one O

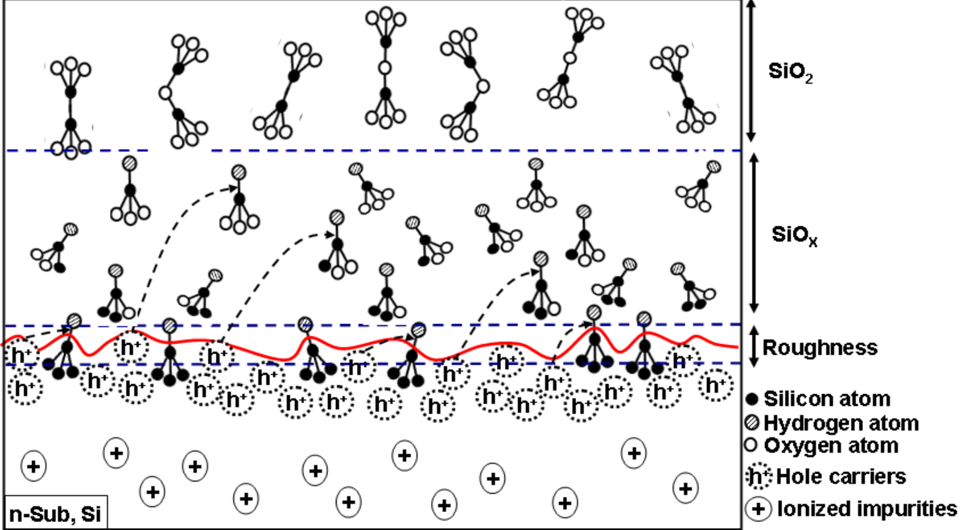


Figure V.19: Schematic representation of defect precursors behind NBTI permanent component. They are mostly located in the interfacial oxide layer.

and two Si, respectively. It is similar to P_{b1}-H center at the (100) Si/SiO_2 **[226]**. For x = 0 (O_3Si-H), the Si-H bond is surrounded by three O atoms. It has gap states and is similar to E'_γ center **[227]**.

The trap precursor distribution in the interfacial region could explain the variation of E_a (0.11-0.6 eV) and a_{eff} (1.2-10 q.Å) as a function of Z (see **Fig. V.17)**. Defect precursors change from the interface Si-H bond surrounded by three Si atoms to Si-H surrounded three O atoms transiting through the other combination of $O_{3-x}Si_x$Si-H family defects. However, the linear extrapolation made from data to the interface (Z_0) (see **Fig. V.17)** is a simple illustrative way to explain why different values of n, E_a, and a_{eff} are often reported in the literature **[12,22,17,27,29,34,40,48,50,62,207,228]** and found here. This interpretation needs more investigation based on both experiments and calculations to link the physical parameters to their respective defects.

In **Fig. V.20**, we plot the volume trap density, n_T (E,Z) (see **Chapter II**), contributing to the permanent component, as a function of Z. n_T profile curves are measured after 30, 90, 180, 300 and 450 min of stress time at 120 °C and different V_{Gstr}. The contribution from traps located in the oxide at a distance Z is extracted using cross section exponential decay with the oxide depth of **Eqs. (II.9)**. At 500 kHz, we have found that CP-signal corresponding to fast interface traps comes from defects located at approximately 5 Å within near interfacial oxide layer. The electrical interface thickness depends on how the frequency is high. Hence, whatever the signal frequency, the CP-current always includes current from border traps. In our case, border traps lie between 5 and 8 Å. The lower the frequency, the thicker the scanned region (for example for f_L = 1 kHz, Z = 9 Å). In addition, NBTI-induced n_T increases and tends to saturate with stress voltage.

Based on the works reported in [**86,89,91]**, we have been able to construct, from the electrical point of view, a picture of NBTI-induced traps. As illustrated in the top of **Fig. V.20**, the border traps are most likely concentrated in the transition layer, where $O_{3-x}Si_x$-H defect family dominates; while NBTI-induced interface traps involve Si_3Si-H and some of $O_{3-x}Si_x$-H defects that respond at 500 kHz.

From the above picture, it is obvious that Si-H dipole, which is commonly used to interpret NBTI degradation, is spatially scattered in the interfacial regions (roughness, transition, and strained) and

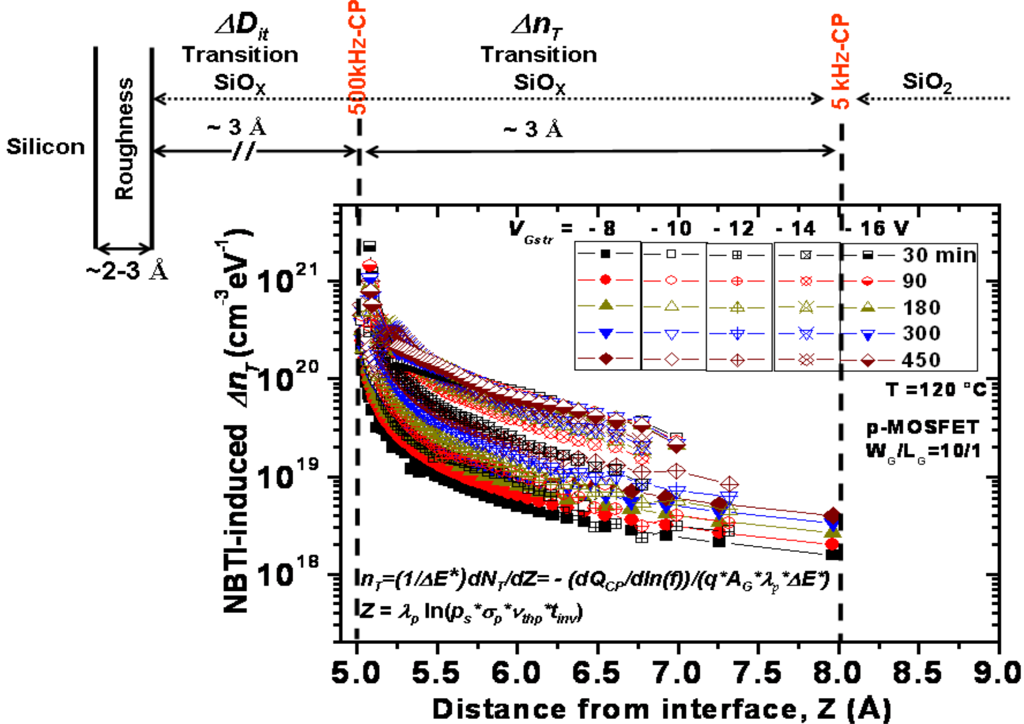


Figure V.20: Profiling of NBTI-induced traps in the interfacial oxide region as a function depth. Onset is qualitative schematic position of the scanned traps. Assuming that traps responding at CP-500 kHz are interface traps and all those below 500 kHz to 5 kHz are considered as border traps.

bonded differently to various O/Si configurations. Consequently, the basic physical and chemical processes that drive the NBTI degradation have different time constants and activation energies. That is why the exponent *n* is dependent on temperature and electric field at least in the time scope of our experiments.

V.9- ΔN_{bt} profile Result Analysis and Discussion

Commonly, traps detected at high CP frequency are associated to the well known P_b centers ($Si_3Si°$) that are located at or very close to the Si/SiO_2 interface and follow SRH recombination dynamics. However, traps screened at low frequency stretch out in the interfacial region with different E_a and a_{eff} and their generation is dependent on stress *T* and V_{Gstr}. Accordingly, we have proposed $O_{3-x}Si_x$-H defect family as possible precursors for such traps This inference is very consistent with the recent quantitative observation of Aichinger *et al.* **[59,60]**. They have pointed out, in their studies of NBTI stress on 5 and 30 nm gate oxide thicknesses, that NBTI can generate traps which contribute to threshold voltage shift, but do not respond to high frequency CP (500 kHz). Based on SDR studies and theoretical calculations using density functional theory **[229]**, they suggested P_b center-hydrogen complex as a microscopic structure for such traps. The measure of the SDR signal of this defect shows a hyperfine (HF) doublet symmetric to P_b line (g = 2.0069), similarly to the HF doublet of E' center-hydrogen complex is symmetrical to E' line (g = 2.005) **[59]**. In addition, both shallow and deep oxide traps have been identified as a possible source for NBTI **[208]**. The former is located in the whole channel, while the latter in the LDD region. However, both **[59,208]** did not specify the atomic structure of defect precursors behind NBTI-induced traps.

Based on the aforementioned data from this work and data collected from **[59,86,89,91]**, we

suggest that $O_{3-x}Si_x$-H complex family is the more probable atomic structure of P_b center-hydrogen complex. Nevertheless, due to the inhomogeneous broadening of trap precursors in space and energy, the NBTI degradation could be underestimated if only one Si-H dipole type is considered. Therefore, any attempt to model NBTI has to account for the bonding within SiO_x sub-oxide, as it plays a critical role in defining the device performance and reliability.

It is important to recall that our results concern primarily the permanent component damage, since the MFCP measurement time is 30 s. This is not really an issue, since during the effective operating (normal) conditions of circuits only the permanent component occurs and affects the circuit performances. However, the recoverable component plays an important role during NBTI stress by using high temperature and voltage to accelerate the degradation. In fact, the fast recoverable component is essential to explain full range of NBTI experiments, including short-time stress data, while for very long time NBTI reliability at working condition is still dominated by the permanent component **[48]**. However, it has been shown elsewhere **[58]** that the permanent component is permanent in the time scope of a given experiment, and not permanent forever, but rather it has recovery time constants beyond the range of experiment time.

Despite its long measurement time, the depth scanning method presented here can help to deeply analyze the NBTI permanent degradation in the interfacial sub-oxide layer. This approach allows profiling the physical parameters of border-trap involved in NBTI degradation; such as the activation energy and the effective dipole moment, hence enabling the development of accurate models to predict device end-of-life.

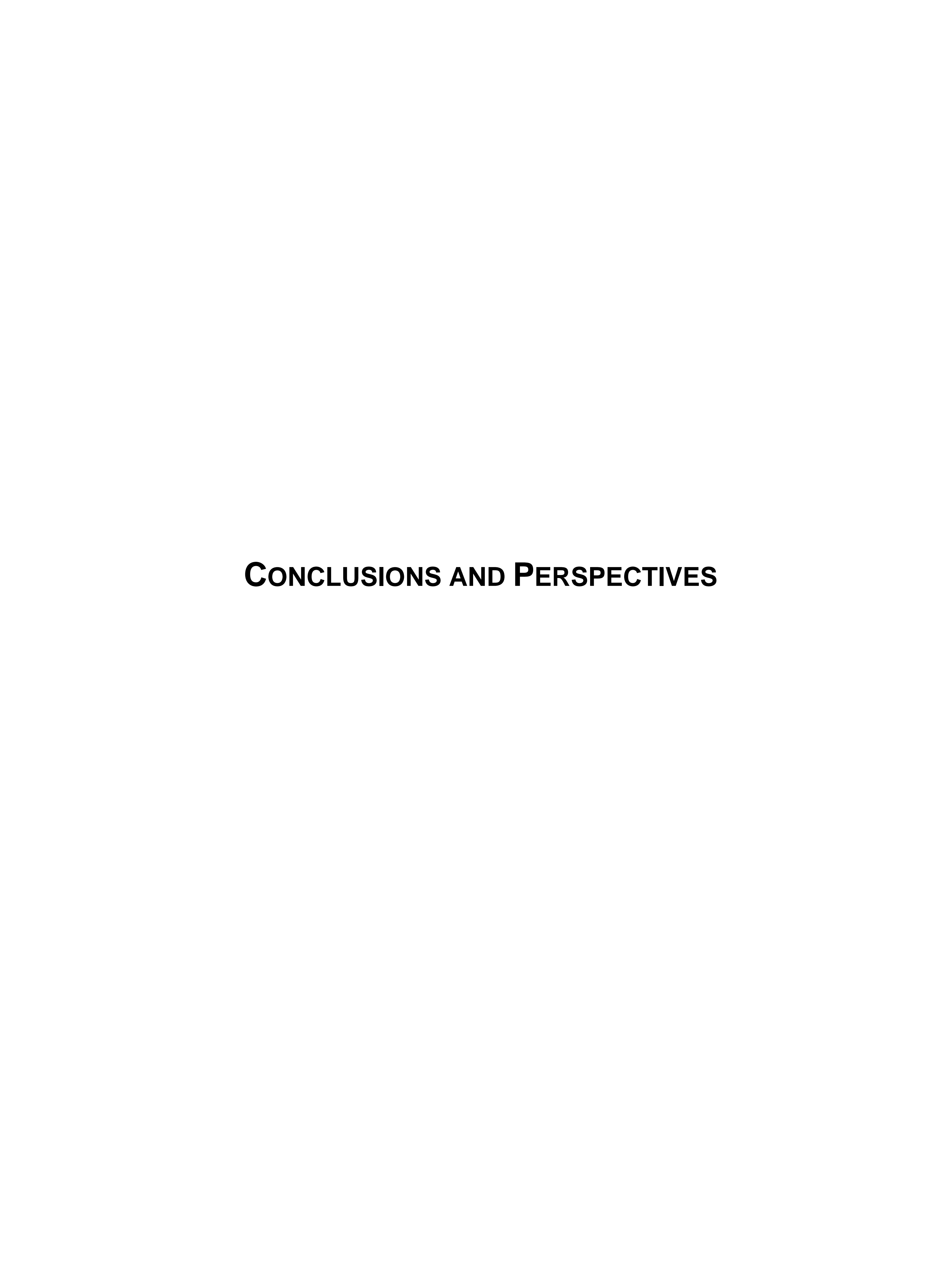
Finally, contrary to the well established reports from different research groups **[135-137,220, 230-233]** regarding the relation between defect depth in the oxide and the CP frequency, Ryan et *al.* **[234]** conclude that the relationship is more complex than that expected. They claim that the effective tunnelling length to an oxide defect can be different than its actual depth. This constitutes an issue for dual layer SiO_2/HfO_2 gate stacks regarding the physical location of stress induced traps, whether they are located in SiO_2 interfacial layer or in HfO_2 bulk. In addition, in very small gate area, each defect presents an individual capture and emission time **[192,193]**, which can be associated with a single frequency. Therefore, considering a straightforward relationship between frequency and depth is, in fact, an easy way to illustrate a so complicated picture of hazardous energy and space distribution of border traps. That is not an issue for large area transistors with single thick layer of SiO_2, where a large number of defects exist and their pathway tunnelling distances can be averaged by a direct relationship between tunnelling distance and frequency.

V.10- Conclusion

On one side, we have revealed that NBTI effect is more severe in short channel transistors than in long channel transistors. Particularly, channel edges and LDD overlapping regions degrade more severely than the middle of the channel. The former regions are subject to higher initial damage from implantation and etch processes as well as hydrogen and boron species diffusion, which probably cause non-uniform distribution of NBTI-induced ΔN_{it}. In addition, the NBTI degradation seems to propagate through the channel until saturation. Therefore, not only T and V_{Gstr}, and stress time play a role in NBTI, but also gate length.

On the other side, using MFCP method, we have been able to profile NBTI-induced border-trap in the interfacial oxide layer. The results have shown a great dependence of n and $E_{a,eff}$ on T and V_{Gstr}. We have found that the decrease of $E_{a,eff}$ and n with T and V_{Gstr} is caused by the cumulative contribution from broad traps having different effective dipole moments and thermal activation energies. The latter have been found linearly distributed from the interface to the sub-oxide layer. We have also shown that ΔN_{bt} could be related to P_b center-hydrogen complex precursors, which could correspond to $O_{3-x}Si_x$-H complex defect family. In addition, data have shown that it is very hard to separate the interface-trap from border-traps, because of the Si/SiO_2 interface, which has always a thickness containing $O_{3-x}Si_x$-H complex. On the other hand, we have found that NBTI degradation tends to saturate with time, T and V_{Gstr}. It seems like the earlier degradation starts very near from the interface and propagates into the interfacial sub-oxide region.

Its capability to sense border-trap, makes MFCP method suitable to scan different quasi permanent NBTI components lying into the interfacial oxide region, since the NBTI degradation processes are located in that region. It will be valuable, in a future work, to deeply extend the investigation on NBTI-induced interface-trap and border-trap to model the degradation propagation along the channel and into the oxide.



CONCLUSIONS AND PERSPECTIVES

CONCLUSIONS AND PERSPECTIVES

In this work, we have focused on one of the major MOS reliability issues, named negative bias temperature instability. It basically deals with the characterization from a methodological approach as well as from a conceptual modelling approach. Instead of focusing on sophisticated high time resolution techniques, we have proposed a novel methodology of NBTI characterization offering a useful alternative insight to the NBTI reliability concerns and the long term power-law exponent *n* discrepancies reported in the literature. The detailed CP-based characterization effort of the permanent component, handled here, has revealed interesting features on the interface and border traps involved in NBTI degradation.

We have proposed a conceptual framework of a new method to separately extract NBTI-induced interface and oxide traps. The OTFOT method allows the determination of interface and border traps using only *C-P* technique at low and high frequencies without combining other techniques. In this thesis, we have mainly exposed, for the first time, the OTFOT methodology for extracting the NBTI effect in MOS transistors. By adjusting high and low frequency measurement times, we can get a comparable relaxation portion in both frequencies. In addition, we have presented the experimental results of OTFOT method by showing the NBTI-induced interface- and oxide-trap densities as well as their contributions to voltage shift extraction. The result shows a good agreement with literature regarding the power-law exponent. However and opposite to existing methods that are more or less complicated, the present method extracts ΔN_{it} and ΔN_{bt} using stress and CP in the same timeframe without changing the experimental setup and without any pre-assumption, except for low and high frequencies conditions. Lastly, ΔV_{th} is obtained from independently extracted ΔV_{it} and ΔV_{bt}.

We have revealed that NBTI effect is more severe in short channel transistors than in long channel transistors. Particularly, channel edges and LDD overlapping regions exhibit more degradation than the middle of the channel. The former regions are subject to more initial damage from implantation and etch processes as well as hydrogen species and boron diffusion which probably cause non-uniform distribution of NBTI-induced ΔN_{it} (t_{str}). In addition, the NBTI degradation seems to propagate through the channel until saturation. Therefore, not only temperature, electric field, and stress time play a role in NBTI, but also gate length.

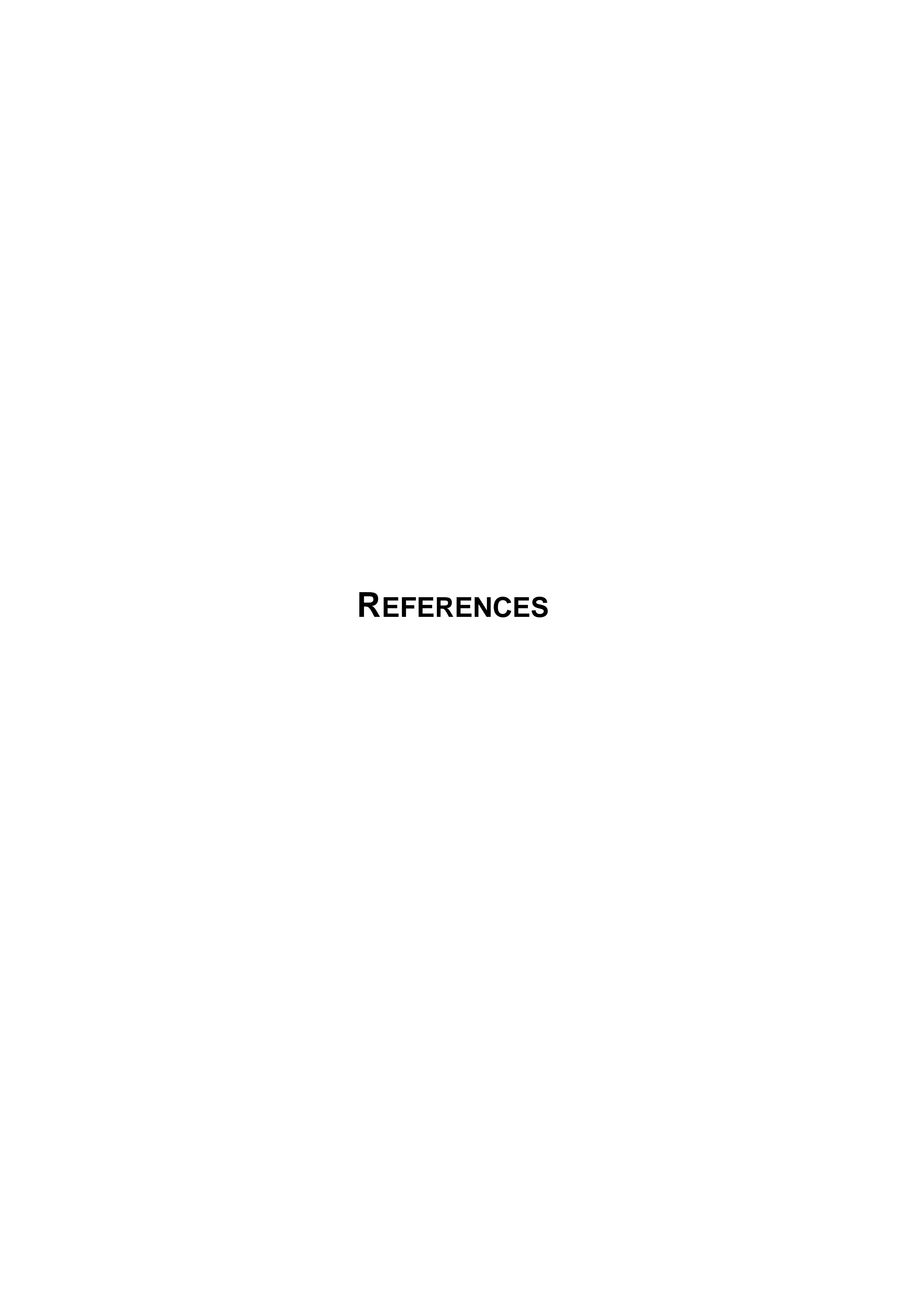
Using multi-frequency method, we have been able to profile NBTI-induced border trap in the interfacial oxide. The results revealed an important dependence as well as a different behavior of stress temperature and electric field. The decrease of the exponent *n* and the apparent activation energy with temperature and electric field results from a cumulative contribution of broad traps having different effective dipole moments and activation energies. The latter have been found linearly distributed from the interface to the sub-oxide layer. We have also shown that border traps could be related to P_b center- hydrogen complex precursors, which might correspond to $O_{3-x}Si_x$-H complex defect family. In addition, data have revealed that it is very hard to separate the interface traps from border traps, because the Si/SiO_2 interface has always a thickness containing $O_{3-x}Si_x$-H defect family. On the other hand, we have found that the degradation tends to saturate with time, temperature and electric field. It seems that the NBTI degradation

starts the interface and propagates into the interfacial sub-oxide region.

In this manuscript, we have focused on the permanent component using relatively slow measurement and large area devices with SiO_2 gate dielectric. It is worth to investigate the following points in the future:

- Due to its inherent bias switch into accumulation, *C-P* technique cannot capture the fast recoverable component. Therefore, to minimize the accumulation duration during charge pumping measurement, one can experiment the duty cycle dependence of OTFOT on SiO_2 and alternative gate isolators using digital scope. By this way, delay measurement could be enhanced and subsequently fast measurement with OTFOT method could be achieved.
- Modelling of the lateral NBTI propagation concept based on its fundamental physical mechanism and parameter.
- Understanding and modelling the physical and chemical forces that drive the breaking bonds of border-trap defect precursors located in the interfacial sub-oxide region during NBTI conditions. Furthermore, calculation of activation energies and effective dipole moments of $O_{3-x}Si_xSi\text{-}H$ complex defect family.
- Investigation of space and energy distributions of defects within the interfacial sub-oxide and oxide regions.

Finally, the profiling approaches, developed here, can help to model NBTI and provide better predictions for long term reliability and longer useful lifetime of devices under use conditions.



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LIST OF OWN PUBLICATIONS RELATED TO THIS WORK

I- Papers-Based Thesis

I.1- Papers published in journals

1- **B. Djezzar**, H. Tahi, A. Benabdelmoumene, and A. Chenouf, "A propagation concept of negative bias temperature instability along the channel length in p-type metal oxide field effect transistor," Solid-State Electronics, Elsevier, vol. 82, pp. 46–53, **2013**.

2- **B. Djezzar**, H. Tahi, A. Benabdelmoumene, A. Chenouf, and Y. Kribes, "A New Method for Negative Bias Temperature Instability Assessment in P-Channel Metal Oxide Semiconductor Transistors," Japanese Journal of Applied Physics, vol. 51, no. 11 pp. 116602-1-116602-7, **2012**.

3- H. Tahi, **B. Djezzar**, A.Benabdelmoumene, "A New Procedure for Eliminationg the Geometric Component from Charge Pumping Application for NBTI and Radiation Issues," Microelectronics Reliability, Elsevier, vol. 53, no.4, pp. 513-519, April. 2013.

4- H. Tahi, **B. Djezzar**, A. Benabdelmoumene, A.Chenouf, M. Goudjil, "Investigation of Interface, Shallow and Deep Oxide Traps under NBTI Stress Using Charge Pumping Technique," Microelectronics Reliability, Elsevier, in press, corrected Proof 2014. http://dx.doi.org/10.1016/j.microrel.2014.01.010.

I.1- Papers published in conference proceedings

5- **B. Djezzar**, H. Tahi, A. Benabdelmoumene, F. Hadjlarbi, A. Chenouf, and Y. Kribes, "On The Fly Oxide Trap (OTFOT) Concept: a New Method for Bias Temperature Instability Characterization," IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits IEEE (IFPA), **2012,** pp. 1-5.

6- **B. Djezzar**, H. Tahi, A. Benabdelmoumene, .A. Chenouf, "A New Eye on NBTI-Induced Traps up to Device Lifetime Using on the Fly Oxide Trap Method," 24th IEEE International Conference on Microelectronics (ICM), **2012**, pp. 1-4.

7- **B. Djezzar**, H. Tahi, A. Benabdelmoumene, A. Chenouf, M. Goudjil, « On the Permanent Components of Negative Bias Temperature Instability, » 25thIEEE International Conference on Microelectronics (ICM'13), Dec. **2013**, pp. 216-219.

8- A. Benabdelmoumene, **B. Djezzar**, H.Tahi, A. Chenouf, L. Trombetta, M. Kechouane, " Investigating the NBTI Effect on P- and N-substrate MOS Capacitors and p-MOSFET Transistors, »" IEEE International Conference on Microelectronics (ICM), **2013,** pp. 236-239.

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10- A. Benabdelmoumene, **B. Djezzar**, L. Trombetta, H. Tahi, A. Chenouf, and M. Kechouane, "Two-Point Capacitance-Voltage (TPCV) Concept: a New Method for NBTI Characterization," IEEE International Integrated Reliability Workshop (IIRW), **2012**, pp.175-178.

II- Papers-Related Thesis

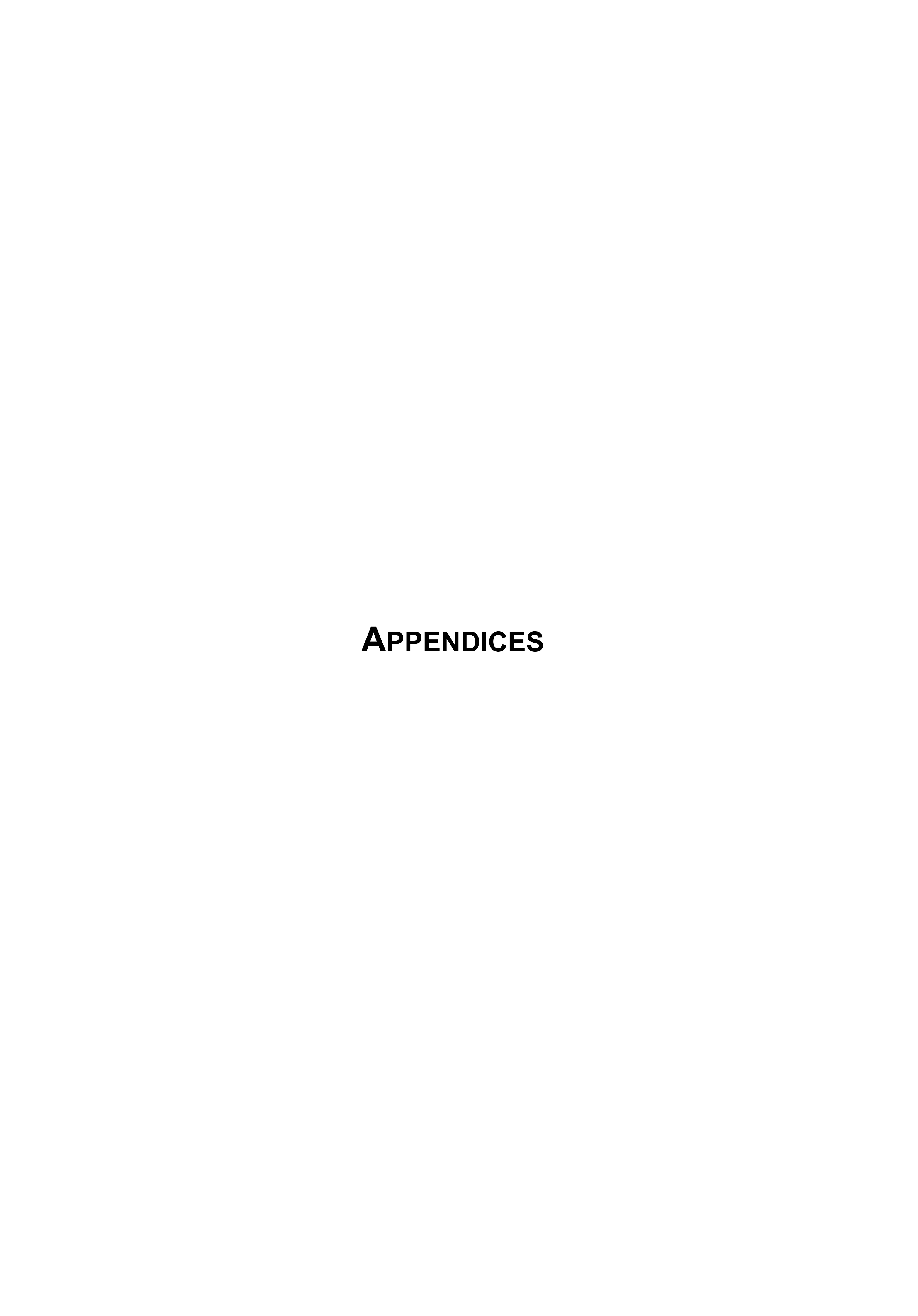
11- **B. Djezzar**, H. Tahi, and A. Mokrani, "Why is oxide-trap charge pumping method appropriate for radiation-induced trap depiction in MOSFET?," IEEE Transactions on Device and Materials Reliability, vol. 9, no. 2, pp. 222–230, **2009**.

12- **B. Djezzar** and H. Tahi, "Using Oxide-Trap Charge-Pumping Method in Radiation Reliability Analysis of Short Lightly Doped Drain Transistor," IEEE Transactions on Device and Materials Reliability, vol. 10, no. 1, pp. 18-28, **2010**.

13- H. Tahi, **B. Djezzar**, A. Benabdelmoumen, B. Nadji, and Y. Kribes, "Geometric Component in Constant-Amplitude Charge-Pumping Characteristics of LOCOS- and LDD-MOSFET Devices," IEEE Transactions Device Materials Reliability, vol. 11, n° 1, pp.113–139, **2011.**

14- H. Tahi, **B. Djezzar**, B. Nadji, "Modeling and Simulation of Charge-Pumping Characteristics for LDD-MOSFET Devices with LOCOS Isolation," IEEE Transactions on Electron Devices, vol. 57, no. 11, pp. 2892-901, **2010**.

15- H. Tahi, **B. Djezzar**, B. Nadji**, "**Radiation Effect Evaluation in Effective Short and Narrow Channel of LDD-Transistor with LOCOS-Isolation Using OTCP Method," IEEE Transactions on Device and Materials Reliability, vol. 10, no. 1, pp. 108-115, **2010**.



APPENDICES

APPENDICES

APPENDIX A

A.1- H-H$_2$ Diffusion with Direct H-H$_2$ Conversion

Chemical reaction of the generalized model requires two hydrogen atoms from dissociation of two Si-H bonds, which dimerize to form H_2 molecule and resultant hydrogen species (i. e. H and H_2) diffuse into the oxide. The reaction equations are as follows:

$$\begin{aligned} Si_3 \equiv Si - H + h^+ &\Leftrightarrow Si_3 \equiv Si^+ + H \\ Si_3 \equiv Si - H + h^+ &\Leftrightarrow Si_3 \equiv Si^+ + H \end{aligned} \tag{A.1}$$

for interface generation and two hydrogen atoms release and

$$H + H \Leftrightarrow H_2 \tag{A.2}$$

for H to H_2 explicit conversion.

From **Eq. (A.1)**, we can express the rate change of the interface trap density as given by **Eq. (I.19)** in **chapter I**. While from **Eq. (A.2)**, we get change rate of hydrogen molecule density N_{H_2}

$$\frac{dN_{H_2}}{dt} = k_H N_H^2 - k_{H_2} N_{H_2} \tag{A.3}$$

Similarly the rate change of N_H writes

$$\frac{dN_H}{dt} = 2k_{H_2} N_{H_2} - 2k_H N_H^2 \tag{A.4}$$

- *<u>Boundary conditions for 1-D diffusion</u>*

The hydrogen diffusion satisfies

$$\frac{dN_H}{dt} = -\frac{dF}{dx} \tag{A.5}$$

where the hydrogen flux is given by $F = -D_H(dN_H / dx)$. Using box integration at the Si/SiO$_2$ interface as described in **Fig. A.1**.

$$\begin{aligned} \frac{d}{dt}\int_0^{\delta/2} N_H dx &= -\int_0^{\delta/2}\left(\frac{dF}{dx}\right).dx \\ &= -F(at\ \delta/2) + F(at\ 0) \\ \frac{\delta}{2}\frac{dN_H}{dt} &= D_H \left.\frac{dN_H}{dx}\right|_{x=\delta/2} + \frac{dN_{it}}{dt} \\ \text{where} \quad -D_H \left.\frac{dN_H}{dx}\right|_{x=0} &= \frac{dN_{it}}{dt} \end{aligned} \tag{A.6}$$

Thus, the boundary equation for 1-D diffusion can write as:

$$\frac{\delta}{2}\frac{dN_H}{dt} - D_H\frac{dN_H}{dx} - \frac{dN_{it}}{dt} = 0. \tag{A.7}$$

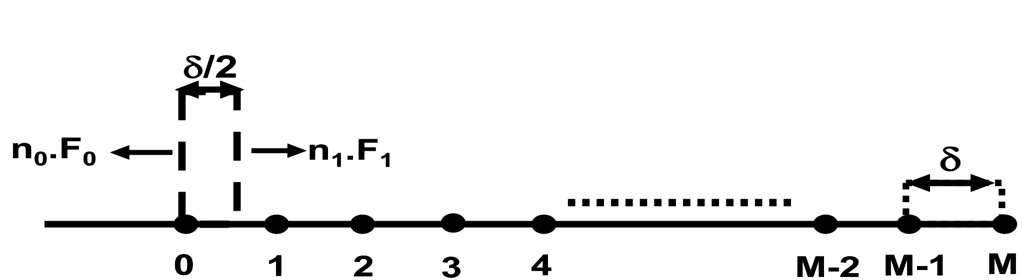


Figure A.1 : Box integration at the Si/SiO2 interface to get boundary equations. The nodes numbered 0-M represent the gate oxide. F_0 and F_1 are the hydrogen fluxes; n_0 and n_1 are the normal vectors at the interface.

A.2- Analytical Solution for NBTI H-H_2 Model

An analytical model is easier to use and provides additional insight. By assuming $N_0 >> N_{it}$ and $\frac{dN_{it}}{dt} = \frac{N_{it}}{t}$, Islam *et al.* **[17]** have deduced $N_H^{(0)}$ from **Eq. (I.19)** as :

$$N_H^{(0)} = \frac{k_f N_0 - N_{it}/t}{k_r N_{it}} \quad \text{(A.8)}$$

Furthermore, numerical simulation have shown that, for continuous stress, $\frac{dN_H^{(0)}}{dt}$ and *H* diffusion are negligible at all stress time, so **Eq. (I.44)** reduces to

$$\frac{N_{it}}{t} = \delta k_H \left(N_H^{(0)}\right)^2 - \delta k_{H_2}\left(N_{H_2}^{(0)}\right) \quad \text{(A.9)}$$

At long stress time, H_2 diffusion dominates the process. For that condition, simulation have shown **[17]** that the numerical solution of **Eqs. (I.41)- (I.45)** fit well the analytic solution for :

$$N_{it} \approx N_{H_2}^{(0)}\sqrt{6D_{H_2}t} \quad \text{(A.10)}$$

Using **Eqs. (A.8)** and **(A.10)** to Eliminate N_H and N_{H_2} from **Eqs. (A.9)** yields

$$\frac{N_{it}}{t} - \frac{\delta k_H \left(k_f N_0 - N_{it}/t\right)^2}{k_r^2 N_{it}^2} + \frac{\delta k_{H_2} N_{it}}{\sqrt{6D_{H_2}t}} = 0 \quad \text{(A.11)}$$

Eq. (A.11) is the analytical expression of *H-H_2* R-D model presented by **Eqs. (I.41)-(I.45)** in **chapter I**. A comparison of the numerical and analytical solutions has shown an excellent matching **[17]**.

At a short stress time, the first and the third terms become negligible and **Eq. (A.11)** reduces to reaction-limited solution:

$$N_{it} = k_f N_0 t \quad \text{(A.12)}$$

At an intermediate stress time, the third term representing H_2 diffusion is negligible and $k_f N_0 >> N_{it}/t$. H-H_2 conversion is dominant:

$$N_{it} = \left(\frac{k_f N_0}{k_r} \right)^{2/3} \left(\delta k_H t \right)^{1/3} \quad \text{A.13}$$

At a long stress time N_{it}/t becomes negligible and the solution reduces to the H_2 limited diffusion:

$$N_{it} = \left(\frac{k_H}{k_{H_2}} \right)^{1/3} \left(\frac{k_f N_0}{k_r} \right)^{2/3} \left(6 D_{H_2} t \right)^{1/6} \quad \text{(A.14)}$$

NBTI voltage dependence comes from two parts. The first is the charge transfer involved in electrochemical reaction, which shows an exponential dependence on electric field ~exp (γE_{OX}). The second is the hole concentration P_s in strong inversion which is linearly dependent on (V_{GS} – V_{th}), where V_{GS} is the gate voltage and V_{th} is the threshold voltage.

$$p_s = \frac{C_{OX}}{q} (V_{GS} - V_{th}) = \frac{C_{OX}}{q} T_{OX} E_c \quad \text{(A.15)}$$

where, $E_C = E_{OX} - E_d$ is the electric field due to the inversion layer carriers, excluding the electric field due to depletion region (E_d) from the total electric field E_{OX}, while it equal to E_{OX} in accumulation.

A.3- NBTI H-H_2 Model Parameters *[48]*

Table A.3.1: Parameters of H-H_2 R-D model for ΔN_{IT} **[48].**

(1) $\frac{dN_{IT(S)}}{dt} = k_{F(S)}\left(N_{0(S)} - N_{IT(S)}\right) - k_{R(S)} N_{IT(S)} N_{H}^{(S)}$; $k_{F(S)} = k_{F0(S)} \left(V_G - V_{T0}\right)^{\frac{3}{2}\Gamma_{IT}} e^{-\frac{E_{AKF}}{kT}}$; $k_{R(S)} = k_{R0(S)} e^{-\frac{E_{AKR}}{kT}}$
(2a) $\frac{\delta}{2}\frac{dN_{H}^{(S)}}{dt} = D_H \frac{dN_{H}^{(S)}}{dx} + \frac{dN_{IT(S)}}{dt} - \delta k_H \left[N_{H}^{(S)}\right]^2 + \delta k_{H2} N_{H2}^{(S)}$; $k_H = k_{H0} e^{-\frac{E_{AKH}}{kT}}$; $k_{H2} = k_{H20} e^{-\frac{E_{AKH2}}{kT}}$; $D_H = D_{H0} e^{-\frac{E_{ADH}}{kT}}$
(2b) $\frac{\delta}{2}\frac{dN_{H2}^{(S)}}{dt} = D_{H2} \frac{dN_{H2}^{(S)}}{dx} + \frac{\delta}{2} k_H \left[N_{H}^{(S)}\right]^2 - \frac{\delta}{2} k_{H2} N_{H2}^{(S)}$; $D_{H2} = D_{H20} e^{-\frac{E_{ADH2}}{kT}}$
(3) $\frac{dN_{IT(P)}}{dt} = k_{F(P)}\left(N_{0(P)} - N_{IT(P)}\right) N_{H}^{(P)} - k_{R(P)} N_{IT(P)} N_{H2}^{(P)}$; $k_{F(P)} = k_{F0(P)} \left(V_G - V_{T0}\right)^{\frac{3}{2}\Gamma_{IT}} e^{-\frac{E_{AKF}}{kT}}$; $k_{R(P)} = k_{R0(P)} e^{-\frac{E_{AKR}}{kT}}$
(4a) $\frac{dN_H}{dt} = D_H \frac{d^2 N_H}{dx^2} - k_H N_H^2 + k_{H2} N_{H2}$ (4b) $\frac{dN_{H2}}{dt} = D_{H2} \frac{d^2 N_{H2}}{dx^2} + \frac{1}{2} k_H N_H^2 - \frac{1}{2} k_{H2} N_{H2}$
Subscript (S) and (P) denote Si/SiO_2 and SiO_2/p-Si interface respectively. Equations (1), (2) and (4) are for conventional H/H_2 RD model; (1), (3) and (4) represents poly H/H_2 RD model; $k_{F(S)}$, $k_{F(P)}$: Si-H bond breaking reaction rate constants; $k_{R(S)}$, $k_{R(P)}$: Si-H bond annealing reaction rate constants; $N_{IT(S)}$, $N_{IT(P)}$: interface trap density; $N_{0(S)}$, $N_{0(P)}$: initial Si-H bond density; $N_H^{(S)}$, $N_H^{(P)}$: atomic H density near the interface; $N_{H2}^{(S)}$, $N_{H2}^{(P)}$: molecular H_2 density near the interface; N_H and N_{H2}: concentration of atomic H and molecular H_2 respectively; D_H and D_{H2} are diffusivities of atomic H and molecular H_2 respectively; k_H and k_{H2}: H to H_2 dimerization and dissociation rates respectively; δ: interfacial thickness (~1.5Å)
Parameters: E_{AKF} = 0.175eV; E_{AKR} = 0.2eV; k_{H0} = 8.56 cm^3/s; E_{AKH} = 0.3eV; k_{H20} = 5.7e5s^{-1}; E_{AKH2} = 0.3eV; E_{ADH} = 0.2eV; E_{ADH2} = 0.58eV; $k_{F0(P)} \approx 3/5 * k_{F0(S)}$. $k_{F0(S)}$ and Γ_{IT} are device dependent parameters
H/H_2 RD model: $k_{R0(S)}$ = 9.9e-7cm^3/s; D_{H0} = 9.56e-8 cm^2/s and D_{H20} = 3.5e-5 cm^2/s.
Poly H/H_2 RD model: $k_{R0(S)}$ = 9.9e-5 cm^3/s; $k_{R0(P)}$ = 8e-4 cm^3/s; D_{H0} = 1.5e-5 cm^2/s and D_{H20} = 9.5e-5 cm^2/s.

Table A.3.2: Parameters of H-H_2 R-D model for ΔN_{OT} and ΔN_{HT} **[48].**

For Stress
$\Delta N_{HT} = B\,(V_G - V_{T0} - \Delta V_T)^{\Gamma_{HT}}\, e^{-\frac{E_{AHT}}{kT}} \left(1 - e^{-\left(\frac{t}{\tau_s}\right)^{\beta_{HTS}}}\right)$ $\Gamma_{HT} = \Gamma_{IT}$, E_{AHT} = 0.03eV, $\tau_s = \tau_{0s}\ e^{-\left(\frac{E_{A\tau s}}{kT}\right)}$ B, τ_{0S}, $E_{A\tau s}$ and β_{HTS} are device dependent parameters.
$\Delta N_{OT} = C\left(1 - e^{-\left(\frac{t}{n}\right)^{\beta_{OT}}}\right)$ $n = \eta\,(V_G - V_{T0} - \Delta V_T)^{\Gamma_{OT}}\, e^{-\frac{E_{AOT}}{kT\beta_{OT}}}$ $\eta = 5\text{x}10^{12}$, β_{OT} = 0.36eV, Γ_{OT} = 9, E_{AOT} = 0.15eV   C is device dependent parameter.
For Recovery
$\Delta N_{HT} + \Delta N_{OT} = B'\, e^{-\left(\frac{t}{\tau_R}\right)^{\beta_{HTR}}}$ Value of B' is adjusted to match the start of recovery with end of stress. τ_R and β_{HTR} are device dependent parameters.

APPENDIX B

Two Stage Model

In this model it is assumed that holes can be captured at first stage via a multiphonon field-assisted tunneling (MPFAT), which was proposed for ionization of deep impurity centers. The underlying theory accounts for the fact that the emission of charge carriers out of bulk traps is accelerated in the presence of an electric field. This effect is eventually related to the shortened tunneling distance through a triangular barrier when considering thermal excitation of the charge carriers. According to theoretical calculations of Ganichev et *al.* **[120]**, it yields a field enhancement factor exp $(E_{OX}/E_{ref})^2$, which is suspected to have a strong impact on hole capture processes in NBTI. The MPFAT process is schematically illustrated in **Fig. B.1** a hole can either be in the valence band or in a trapped state. These two states are represented by the two solid parabolas which give the total energy of the system. The vibration modes can be approximated using a simple oscillator model and at the intersection point a transition can occur. The intersection point determining the barrier ΔE_B is dramatically lowered by the application of an electric field.

Figure B.2 illustrates the energy levels of traps in two-stage model. The energy of the precursor is located below the substrate valence band and subject to a wide distribution due to the amorphousness of SiO_2. Upon hole capture, the defect undergoes a transformation to an *E'* center, which is visible in electron spin resonance (ESR) measurements. Once the silicon bond is broken, the distance between the two silicon atoms increases into a new equilibrium position, which requires a large-range structural relaxation of the surrounding lattice. In this new configuration, the *Si* dangling bond associated with a defect level within or close to the substrate bandgap. The level shifts to a new 'stable' defect configuration, namely the *Si* dangling bond. In the *E'* center configuration, the defect can be repeatedly charged and discharged by electrons tunneling in or out of its dangling bond. The associated switching behavior is in agreement with the experimental observations made in electrical measurements . Only in the neutral state, in which the *Si* dangling bond is doubly occupied by an electron, the *E'* center can be annealed, thereby becoming an oxygen vacancy again.

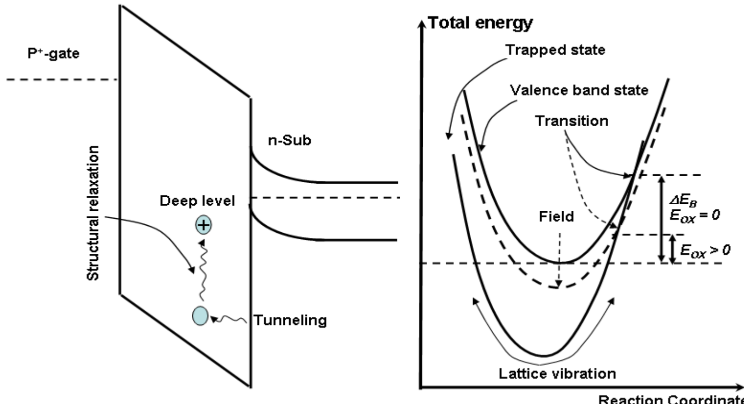


Figure B.1: The multiphonon-field-assisted tunneling (MPFAT) process used to explain the experimental data: elastic tunneling into deep states is only allowed when the excess energy of holes can be released via a multiphonon emission process during structural relaxation. Application of an electric field shifts the total energy of the valence band state (dashed line), increasing the transition probability by exp $(E_{OX}/E_{ref})^2$.

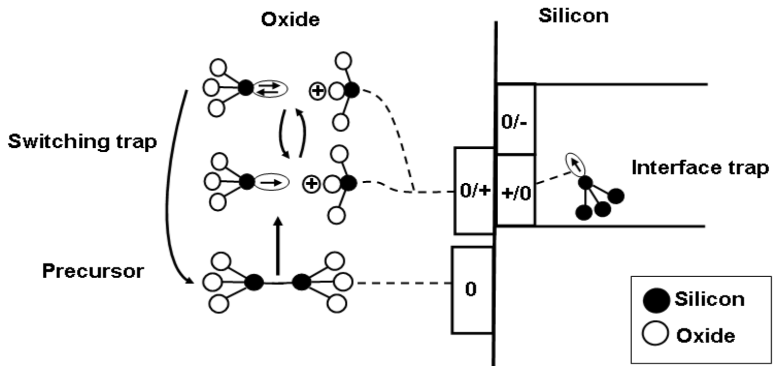


Figure B.2: Electronic traps energy-levels in two stage model: the neutral precursors lie about 1eV below the silicon valence band edge. The *E'* levels are assumed to be inside the silicon bandgap, while for simplicity both the charged and the uncharged level are assumed to be roughly identical. Interface states are assumed to introduce amphotheric defects into the silicon band-gap. All electronic energy-levels are assumed to be homogeneously distributed due to the amorphous nature of the interfacial layer.

The transition rates between state 2 and 4 (see **Fig. I.21** in the text) are modeled by thermal activation over a field-dependent barrier as shown in **Fig. B.1**. The probability of being in state 4 corresponds to a fixed positive charge at the *E'* center and a depassivated interface state. However, only interface states above the Fermi level and up to mid-gap are assumed to be positively charged and their occupancy with an electron is determined using conventional SRH statistics. **Figure. B.3** illustrates the hydrogen transition. The solid line depicts the potentials for a hydrogen reaction in a configuration coordinate diagram. When a bias is applied to the gate, the oxide field lowers the energy minimum of state 4 (E_4). Since the interfacial Si-H bonds are associated with a dipole moment, the shift of the energy minima depends linearly on the oxide field with a proportionality constant of a_{eff}.

- *Model parameters*

- $v_{thp} = \sqrt{\frac{8KT}{\pi m_p}}$, ($m_p$ = 0.8m_0): thermal velocity for holes, $v_{thn} = \sqrt{\frac{8KT}{\pi m_n}}$, ($m_n$ = 0.5 m_0): for electrons.

- σ_p = 3.10^{14} cm^2, capture cross section for holes, σ_n = 3.10^{14} cm^2 for electrons.

- $x_{p,0} = \hbar / 2\sqrt{2m_p\phi_V} = 0.5\ \mathring{A}$, tunnelling distance for large barrier $\phi_V = 4.65eV$.

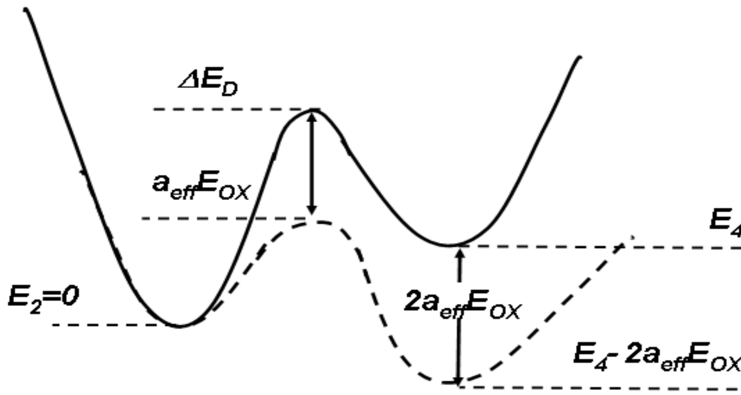


Figure B.3: The transition between state 2 and 4 is modeled by assuming a field-dependent thermal transition over a barrier.

- $x_{n,0} = \hbar / 2\sqrt{2m_n\phi_C} = 0.8\,\mathring{A}$, tunnelling distance for large barrier $\phi_V = 3.2eV$.

- E_{ref} = 2.83 MV/cm: MPFAT reference field. $\nu = \nu_1 = \nu_2 = \nu_3 = 10^{13}\,Hz$: attempt frequency for thermal transition. $\nu_1 = \nu_2 = 10^{13}\,Hz, \nu_3(50\,^\circ C) = 5.11\times10^{15}\,Hz, \nu_3(150\,^\circ C) = 3.54\times10^{10}\,Hz$.

$\Delta E_A \approx \Delta E_B,\ \Delta E_C \approx 0,\ E_T^{'} = E_T,\ \Delta E_B \approx 0.01-1.15eV,\ E_T \approx 0.01-0.3eV$.

- $a_{eff}E_{OX}$: represent the rise or the lowering of the barrier due to electric field, $a_{eff} = 0.75\ q.nm$, E_{OX} = V_G/T_{ox}.

- $E_2 = E_4 \approx 0.01-1.15eV$

$x = \frac{1}{\alpha}\ln(\frac{t}{\tau_0}),\ \alpha = 10^8 cm^{-1},\ \tau_0 = 10^{-11}-10^{-13}s$ (Depend on D_{it}).

k = 1.38066x10^{-23} J/K (N-m/s^2-K=kg-m^2/s^2-K) = 8.6174x10^{-5}eV /K, $\hbar$ =1.05458x10^{-34}J-s = 6.5821x10^{-16} eV-s, 1 eV = 1.60218x10^{-19} J, m_0 = 9.1095 x 10^{-31} kg, e=1.60218x10^{-19}C, K_BT/q= 0.0259 V, kT= 0.0259 eV (Thermal voltage at 300 K),

- Setting $Z = p\nu_{thp}\sigma_p e^{-x/x_{p0}}, Y = n\nu_{thn}\sigma_n e^{-x/x_{n0}}, \beta = 1/KT$

- ***<u>Cases</u>:***

I- K$_{12}$

- $E_{VT} = E_V - E_T \geq 0,\ and\ E_{TC} = E_T - E_C \geq 0, K_{12} = Ze^{-\left(\beta(\Delta E_B + E_{VT}) + \frac{E_{ox}^2}{E_{ref}^2}\right)} + Ye^{-(\beta(\Delta E_B + E_{FC}))}$.

- $E_{VT} = E_V - E_T \geq 0,\ and\ E_{TC} = E_T - E_C \prec 0,\ K_{12} = Ze^{-\left(\beta(\Delta E_B + E_{VT}) + \frac{E_{ox}^2}{E_{ref}^2}\right)} + Ye^{-(\beta(\Delta E_B + E_{TF}))}$.

- $E_{VT} = E_V - E_T \prec 0,\ and\ E_{TC} = E_T - E_C \geq 0,\ K_{12} = Ze^{-\left(\beta\Delta E_B - \frac{E_{ox}^2}{E_{ref}^2}\right)} + Ye^{-(\beta(\Delta E_B + E_{FC}))}$.

- $E_{VT} = E_V - E_T \prec 0,\ and\ E_{TC} = E_T - E_C \prec 0,\ K_{12} = Ze^{-\left(\beta\Delta E_B - \frac{E_{ox}^2}{E_{ref}^2}\right)} + Ye^{-(\beta(\Delta E_B + E_{TF}))}$.

II- K$_{23}$, K$_{32}$

- $E'_{VT} = E_V - E'_T \geq 0,\ and\ E'_{TC} = E'_T - E_C \geq 0,$ $\begin{matrix} K_{23} = Ze^{-(\beta(\Delta E_C - \Delta E_{VF}))} + Ye^{-(\beta(\Delta E_C + E'_{TC}))} \\ K_{32} = Ze^{-(\beta(\Delta E_C - \Delta E'_{VT}))} + Ye^{-(\beta(\Delta E_C + E_{FC}))} \end{matrix}$.

- $E'_{VT} = E_V - E'_T \geq 0,\ and\ E'_{TC} = E'_T - E_C \prec 0,$ $\begin{matrix} K_{23} = Ze^{-(\beta(\Delta E_C - \Delta E_{VF}))} + Ye^{-(\beta\Delta E_C)} \\ K_{32} = Ze^{-(\beta(\Delta E_C - \Delta E'_{VT}))} + Ye^{-(\beta(\Delta E_C - E'_{TF}))} \end{matrix}$.

- $E'_{VT} = E_V - E'_T \prec 0,\ and\ E'_{TC} = E'_T - E_C \geq 0,$ $\begin{matrix} K_{23} = Ze^{-(\beta(\Delta E_C + \Delta E'_{TF}))} + Ye^{-(\beta(\Delta E_C + E'_{TC}))} \\ K_{32} = Ze^{-(\beta\Delta E_C)} + Ye^{-(\beta(\Delta E_C + E_{FC}))} \end{matrix}$

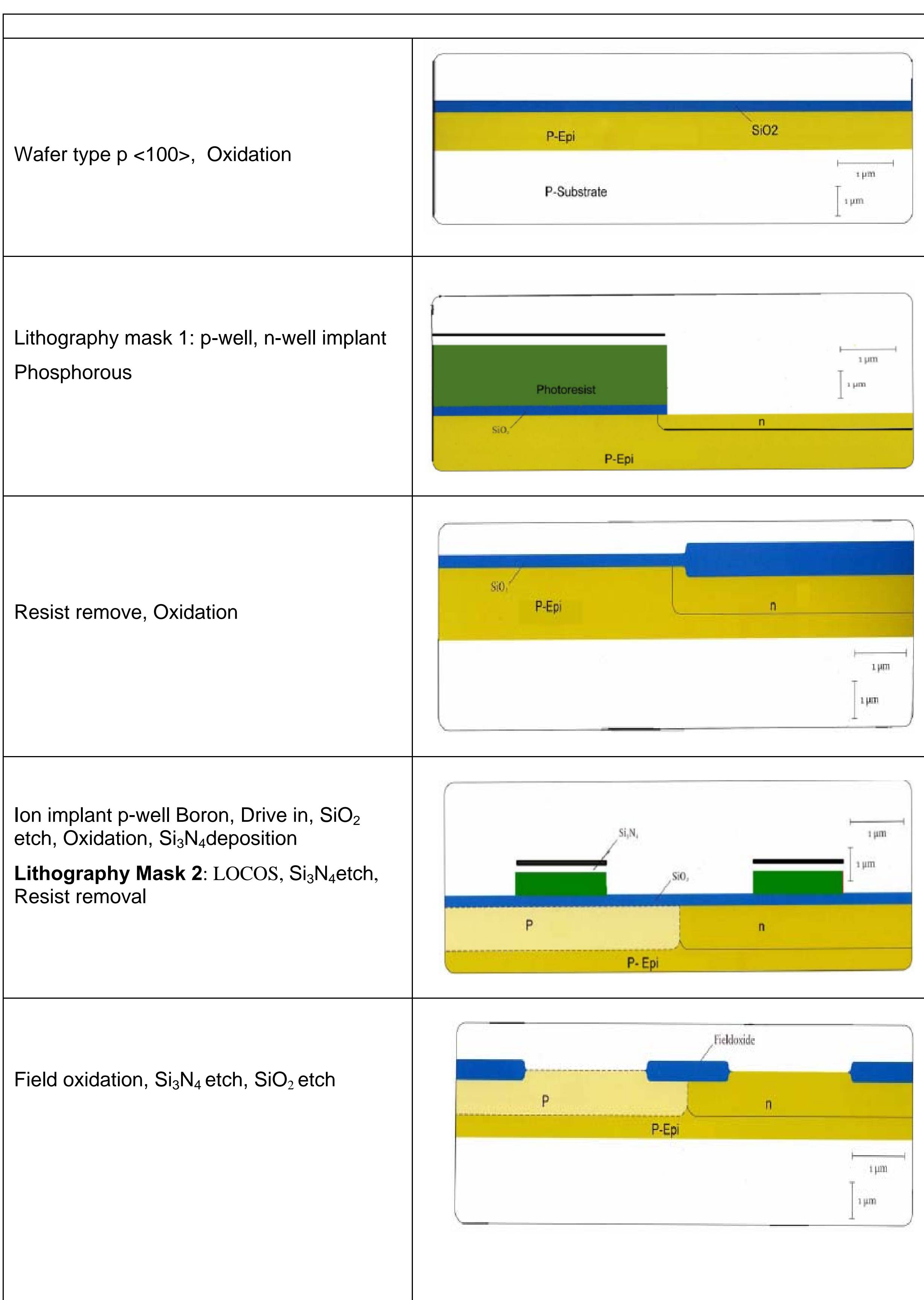
- $E'_{VT} = E_V - E'_T \prec 0,\ and\ E'_{TC} = E'_T - E_C \prec 0,$ $\begin{matrix} K_{23} = Ze^{-(\beta(\Delta E_C + \Delta E'_{TF}))} + Ye^{-(\beta\Delta E_C)} \\ K_{32} = Ze^{-(\beta\Delta E_C)} + Ye^{-(\beta(\Delta E_C + E'_{TF}))} \end{matrix}$

III- K$_{31}$, K$_{24}$, K$_{42}$

$K_{31} = \nu_1 e^{-\beta\Delta E_A}, K_{24} = \nu_2 e^{-\beta(\Delta E_D - E_2 - a_{eff}E_{ox})}, K_{42} = \nu_3 e^{-\beta(\Delta E_D - E_4 + a_{eff}E_{ox})}$.

APPENDIX C

C.1- Process Flow of 1 µm CMOS



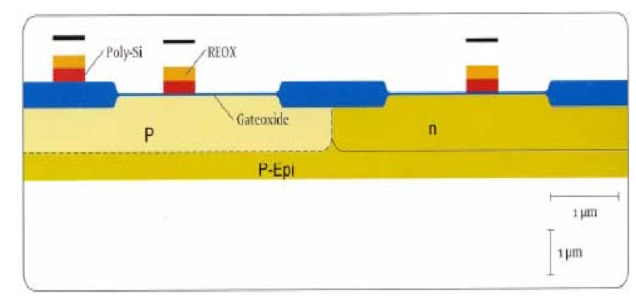
Wafer type p <100>, Oxidation	
Lithography mask 1: p-well, n-well implant Phosphorous	
Resist remove, Oxidation	
Ion implant p-well Boron, Drive in, SiO_2 etch, Oxidation, Si_3N_4deposition **Lithography Mask 2**: LOCOS, Si_3N_4etch, Resist removal	
Field oxidation, Si_3N_4 etch, SiO_2 etch	

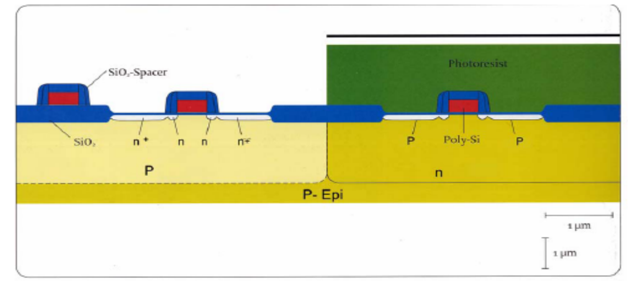
<table>
<tr><td>Oxidation,
Implantation V_T Boron,
Resist removal SiO_2 etch,
Gate oxidation,
Poly-Si deposition,
Poly-SI I doping $PoCl_3$,
Etch oxide.

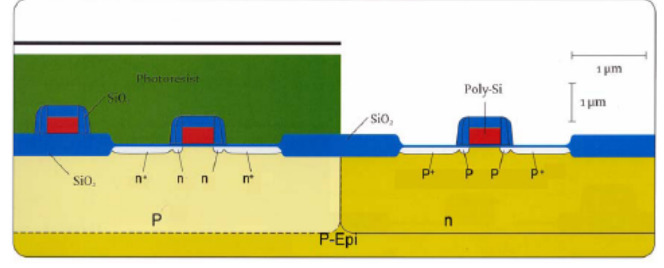
Lithography Mask 4: Poly-Si I, Poly-Si I etch, Resist removal, Reoxidation,

Lithography Mask 5: N^+ LDD, Implant LDD Ph
Resist removal

Lithography Mask 6: P^+ LDD Boron,

Resist removal</td><td>
</td></tr>
<tr><td>SiO_2 deposition: Spacer, SiO_2 etch,
Polymer removal, Oxidation

Lithography mask 7: N^+ Scource/Drain Ion implantation As</td><td>
</td></tr>
<tr><td>Resist removal

Lithography mask 8: P^+ Source/Drain, Ion implantation BF_2, Resist removal / clean</td><td>
</td></tr>
<tr><td>TEOS deposition LPCVD Poly II deposition Doping Poly II

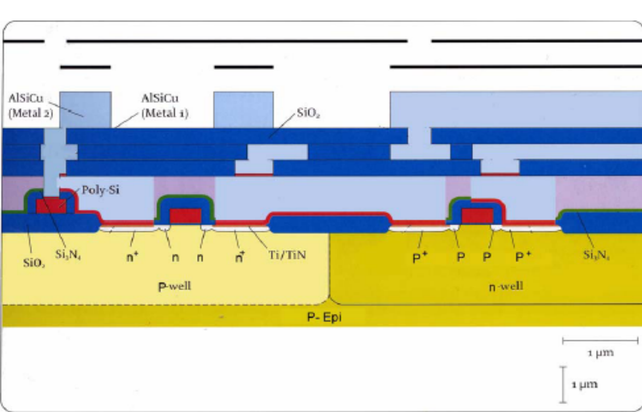
Lithography mask 9: Poly II, RIE Poly II, Resist removal / clean, BPSG deposition, Reflow

Lithography mask 10: Contact, SiO_2 etch, Resist removal, Ti/TiN deposition (sputtering), Sputtering metal 1 (AlCu)

Lithography mask 11: metal 1, Metal 1 etch, Resist removal, TEOS deposition

Lithography mask 12: Via, TEOS etch, Resist removal, TiN deposition

Lithography mask 13: metal 2, Metal 2 etch
Resist removal, SiON deposition

Lithography mask 14: Bondpads, SiON etch
Resist removal</td><td>
</td></tr>
</table>

C.2- Electrical Parameters of 1 µm CMOS

Table C.2.1: p-channel transistor

parameter	draw dim, W/L = 20/1.0			20/20	1.25/20	1.25/1.0	units
	Slow	Nom.	Fast	Nom.	Nom.	Nom.	
VT_0	-1.20	-1.05	-0.90	-1.06	-1.22	-1.21	V
K	0.51	0.42	0.24	0.63	0.73	0.52	$V^{1/2}$
Beta	608	800	1069	37.0	2.14	46.3	$\mu A/V^2$
Beta square	33.0	37.0	41.0	37.0	37.0	37.0	$\mu A/V^2$
W_{eff}	19.72	19.90	20.08	19.90	1.15	1.15	µm
L_{eff}	1.07	0.92	0.77	19.92	19.92	0.92	µm
I_{Dslin}(Bset)	121	163	222	7.47	0.462	10.1	µA
I_{Dslin}(grad)	133		201				µA
I_{Dssat}(Bset)	2.11	2.95	4.22	0.122	0.007	0.165	mA
I_{Dssat}(grad)	2.36		3.77				mA

Table C.2.2: n-channel transistor

parameter	draw dim, W/L = 20/1.0			20/20	1.25/20	1.25/1.0	units
	Slow	Nom.	Fast	Nom.	Nom.	Nom.	
VT_0	0.90	0.73	0.56	0.82	0.90	0.81	V
K_0	0.73	0.58	0.42	0.73	0.82	0.67	$V^{1/2}$
K	0.41	0.30	0.17	0.58	0.68	0.40	$V^{1/2}$
VSBX	1.79	1.31	0.79	1.77	1,87	1.41	V
Beta	1861	2513	3491	96.6	6.49	169	$\mu A/V^2$
Beta square	85.0	95.0	105.0	95.0	95.0	95.0	$\mu A/V^2$
W_{eff}	19.92	20.1	20.28	20.1	1.35	1.35	µm
L_{eff}	0.91	0.75	0.61	19.76	19.76	0.76	µm
I_{Dslin}(Bset)	371	476	610	29.2	2.05	33.5	µA
I_{Dslin}(grad)	402		564				µA
I_{Dssat}(Bset)	5.00	6.55	8.41	0.489	0.033	0.439	mA
I_{Dssat}(grad)	5.40		7.86				mA

Table C.2.3: Dielectric thickness

Itzehoe	-4σ	Typ.	+4σ	units
Gate oxide	18	20	22	nm
Polysilicon/substrate (LOCOS)	540	600	660	nm
MEI/substrate (field)	1080	1200	1320	nm
MEI/polysilicon	513	570	627	nm
MEI/AA	630	700	770	nm
MEII/substrate (field)	1791	1990	2189	nm
MEII/polysilicon (field)	1134	1260	1386	nm
MEII/AA	1332	1480	1628	nm
MEII/MEI (field)	630	700	770	nm

C.3- Effect of High Amplitude on *C-P* Characteristics

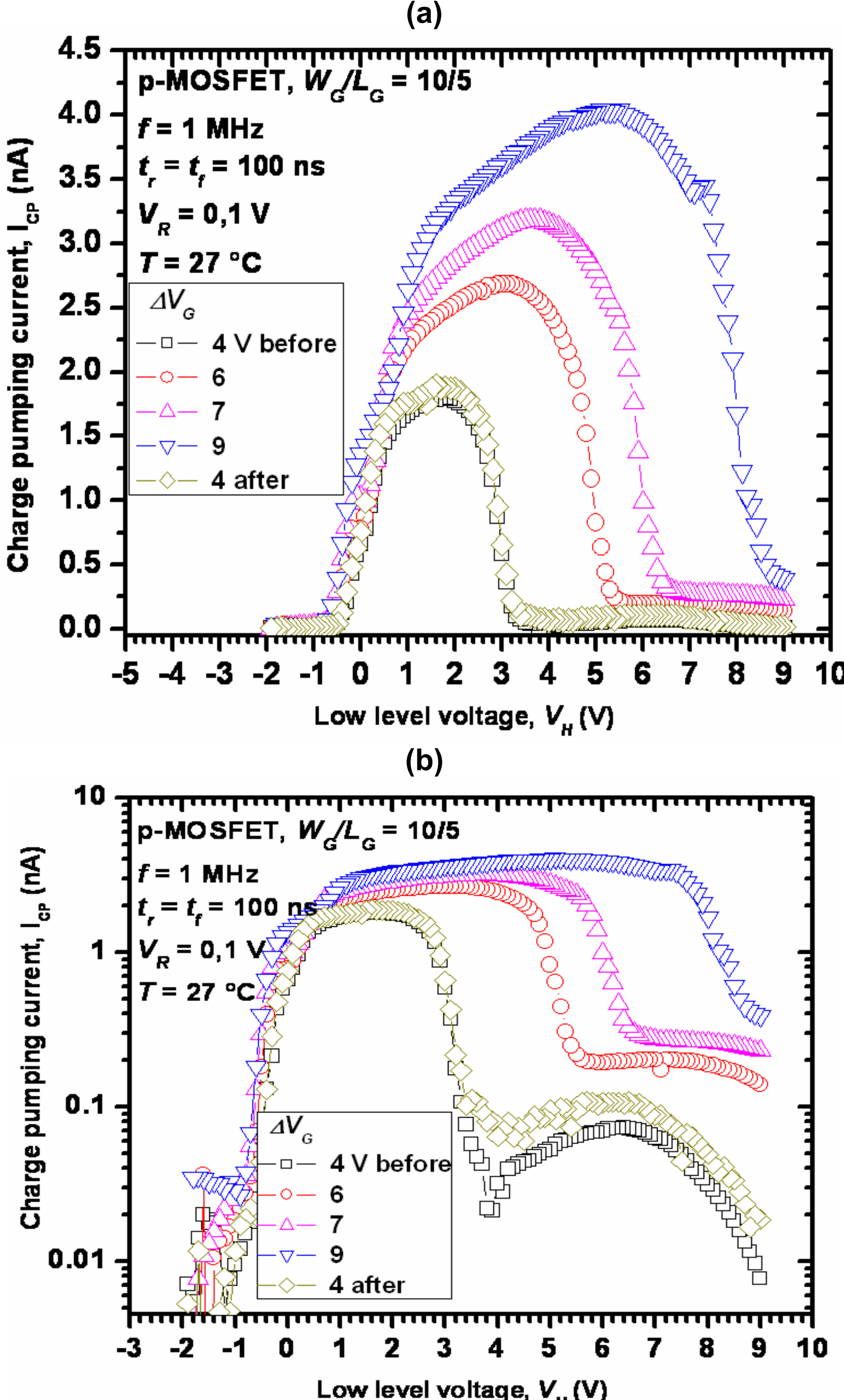


Figure C.1: Charge pumping characteristics for different amplitudes before stress. (a) in linear scale (b) in semi-log scale. It is clear that ΔV_G induces a slight increase of maximum CP-current (I_{CPmax}) due to contribution of traps scanned from additional energy region. High amplitude induces also a slight increase of CP signal at LDD region when comparing CP-current of ΔV_G = 4 V before and after applying 6, 7, and 9 V, while the I_{CPmax} remains unchanged. The latter confirms that the increase of I_{CPmax} with ΔV_G is due to pre-existing traps and not to interface trap creation. However, the former means that high amplitude stresses the LDD region,

APPENDIX D

D.1- Extraction Program of OTFOT Method

```
function varargout = OTFOT_executable(varargin)

% Begin initialization code - DO NOT EDIT
gui_Singleton = 1;
gui_State = struct('gui_Name',       mfilename, ...
                   'gui_Singleton',  gui_Singleton, ...
                   'gui_OpeningFcn', @OTFOT_executable_OpeningFcn, ...
                   'gui_OutputFcn',  @OTFOT_executable_OutputFcn, ...
                   'gui_LayoutFcn',  [] , ...
                   'gui_Callback',   []);
% --- Executes just before OTFOT_executable is made visible.
function OTFOT_executable_OpeningFcn(hObject, eventdata, handles, varargin)

% --- Executes during object creation, after setting all properties.
function w_val_CreateFcn(hObject, eventdata, handles)

% --- Executes during object creation, after setting all properties.
function L_val_CreateFcn(hObject, eventdata, handles)

% --- Executes during object creation, after setting all properties.
function Cox_val_CreateFcn(hObject, eventdata, handles)

% --- Executes during object creation, after setting all properties.
function fh_val_CreateFcn(hObject, eventdata, handles)

% --- Executes during object creation, after setting all properties.
function fb_val_CreateFcn(hObject, eventdata, handles)

% --- Executes during object creation, after setting all properties.
function Nc_val_CreateFcn(hObject, eventdata, handles)

% --- Executes during object creation, after setting all properties.
function Vs_val_CreateFcn(hObject, eventdata, handles)


q=1.6021892e-19; % La charge d'électron en coulombs

w=str2double( get( handles.w_val,'string'));      % Gate length (µm)
l=str2double( get( handles.L_val,'string'));      % Gate width (µm)
Cox=str2double( get( handles.Cox_val,'string')); % Capacitance (F/cm2)
fh=str2double( get( handles.fh_val,'string'));    % High frequency (Hz)
fb=str2double( get( handles.fb_val,'string'));    % Low frequency (Hz)
Nc=str2double( get( handles.Nc_val,'string'));    % colon number
Vs=str2double( get( handles.Vs_val,'string'));    % Stress voltage number

if Vs > 7
    error('myApp:argChk', 'Vs <= à 7')

end

for j=1:Vs

[file path]= uigetfile ('*.*' , 'Open file');
Pathfile_ = [path   file];
fid = fopen(path_file,  'r');
name = file(8:length(fichier)-4);  % file name;
```

```
data = fscanf(fid, '%e',[Nc inf]);      % Data file
data = data';
fclose (fid);
t_Icph = data(:,1);    % measure time for Icph
Icph = data(:,2);      % Icp at high frequency
t_Idch = data(:,3);    % measure time for Idc at high frequency
Idch = data(:,4);      % Idc at high frequency
t_Icpb = data(:,5);    % measure time for Icpb
Icpb = data(:,6);      % Icpb at low frequency
t_Idcb = data(:,7);    % measure time for Idc at low frequency
Idcb = data(:,8);      % Idc at low frequency

n=length(data(:,1));

p0=polyfit([t_Icpb(1),t_Icpb(2)],[Icpb(1),Icpb(2)],1);
Icpb_cal_bis_int = p0(1).* t_Icph(1)+ p0(2);

p01=polyfit([t_Idcb(1),t_Idcb(2)],[Idcb(1),Idcb(2)],1);
Idcb_cal_bis_int = p01(1).* t_Icph(1)+ p01(2);

for i=1:n-1         % Calculation of interpolated data

p1=polyfit([t_Icph(i),t_Icph(i+1)],[Icph(i),Icph(i+1)],1);
Icph_cal_bis(i) = p1(1).* t_Icpb(i)+ p1(2);

p2=polyfit([t_Idch(i),t_Idch(i+1)],[Idch(i),Idch(i+1)],1);
Idch_cal_bis(i) = p2(1).* t_Icpb(i)+ p2(2);

p3=polyfit([t_Icpb(i),t_Icpb(i+1)],[Icpb(i),Icpb(i+1)],1);
Icpb_cal_bis(i) = p3(1).* t_Icph(i+1)+ p3(2);

p4=polyfit([t_Idcb(i),t_Idcb(i+1)],[Idcb(i),Idcb(i+1)],1);
Idcb_cal_bis(i) = p4(1).* t_Icph(i+1)+ p4(2);

end

Icph_cal_int = p1(1).* t_Icpb(n)+ p1(2);
Icph_cal=[Icph_cal_bis,Icph_cal_int];
Icph_cal0=Icph_cal';
Icph_cal = [Icph,Icph_cal0];
Icph_M_cal = reshape (Icph_cal',2*length(Icph_cal),1);

Idch_cal_int = p2(1).* t_Icpb(n)+ p2(2);
Idch_cal=[Idch_cal_bis,Idch_cal_int];
Idch_cal0=Idch_cal';

ind=find(isnan(Idch_cal0)==1);
Idch_cal0(ind)=0;
Idch_cal = [Idch,Idch_cal0];
Idch_M_cal = reshape (Idch_cal',2*length(Idch_cal),1);
Icpb_cal=[Icpb_cal_bis_int,Icpb_cal_bis];
Icpb_cal0=Icpb_cal';
Icpb_cal = [Icpb_cal0,Icpb];
Icpb_M_cal = reshape (Icpb_cal',2*length(Icpb_cal),1);
 Idcb_cal=[Idcb_cal_bis_int,Idcb_cal_bis];
Idcb_cal0=Idcb_cal';

ind=find(isnan(Idcb_cal0)==1);
Idcb_cal0(ind)=0;
Idcb_cal = [Idcb_cal0,Idcb];
```

```
Idcb_M_cal = reshape (Idcb_cal',2*length(Idcb_cal),1);
t_Icp_M_cal = [t_Icph,t_Icpb];
t_Icp_M_cal = reshape(t_Icp_M_cal',2*length(t_Icp_M_cal),1);

%_____________Extaction of Icph_M et Icpb_M________________________________
Icph_M_cal_n = abs(Icph_M_cal - Idch_M_cal);
Icpb_M_cal_n = abs(Icpb_M_cal - Idcb_M_cal);
%________________Extaction of Qit et Qbt________________________________
Qit_h  =  (Icph_M_cal_n)./fh;    %  Recombined  charge  per  cycle  at  high
frequency
Qit_b  =  (Icpb_M_cal_n)./fb;    %  Recombined  charge  per  cycle  at  high
frequency

%________________Extaction of Nit et Nbt________________________________
Ag = (w.*l).*1E-8;
Nit_h = (Icph_M_cal_n)./(q.*Ag.*fh);
Nit_b = (Icpb_M_cal_n)./(q.*Ag.*fb);
Nbt = Nit_b-Nit_h;
DNit_h = Nit_h-Nit_h(1);
DNit_b = Nit_b-Nit_b(1);

DNbt = Nbt-Nbt(1);

 %________________Extaction of Vit et Vbt________________________________
Vit = (q.*Nit_h)./Cox;
Vbt = (q.*Nbt)./Cox;

DVit = (q.*DNit_h)./Cox;
DVbt = (q.*DNbt)./Cox;

 % ________________Data ____________________________________________
All_data0=[t_Icp_M_cal,Icph_M_cal_n,Qit_h,Nit_h,Vit,DNit_h,DVit,Icpb_M_cal,
Qit_b,Nit_b,DNit_b,Nbt,Vbt,DNbt,DVbt];
All_data1=[t_Icpb,Icph_cal0,Idch_cal0,t_Icph,Icpb_cal0,Idcb_cal0];
All_data2=[t_Icp_M_cal,Icph_M_cal,Idch_M_cal,Icpb_M_cal,Idcb_M_cal];

All_data_total_DNit = [t_Icp_M_cal, DNit_h, DVit];
All_data_total_DNbt = [t_Icp_M_cal, DNbt, DVbt];

% ________________Save data ______________________________
 [file  path]= uiputfile ({ '*.xls';'*.dat'} , 'save file');
path_filme = [path   file];

%name(j)=path_file;

Label0={'t_Icp_M_cal(Sec)','Icph_M_cal_n(A)','Qit_h(C)','Nit_h(cm-
2)','Vit(V)','DNit_h(cm-2)','DVit(V)','Icpb_M_cal(A)','Qit_b(C)','Nit_b(cm-
2)','DNit_b(cm-2)','Nbt(cm-2)','Vbt(V)','DNbt(cm-2)','DVbt(V)'};
xlswrite(num2str(path_filme),Label0,titre,'A1');
xlswrite(num2str(path_filme),All_data0,titre,'A3');

Label_data={'t_Icph(Sec)','Icph(A)','t_Idch(Sec)','Idch(A)','t_Icpb(Sec)','
Icpb(A)','t_Idcb(Sec)','Idcb(A)'};
xlswrite(num2str(path_filme),Label_data,
name,['A' num2str(length(Qit_h)+5)]);
xlswrite(num2str(path_filme),data, name,['A' num2str(length(Qit_h)+7)]);

Label1={'t_Icpb(Sec)','Icph_cal0(A)','Idch_cal0(A)','t_Icph(Sec)','Icpb_cal
0(A)','Idcb_cal0(A)'};
```

```
xlswrite(num2str(path_filme),Label1,name,['A'num2str(length(Qit_h)+length(t
_Icpb)+9)]);
xlswrite(num2str(path_filme),All_data1,name,['A'num2str(length(Qit_h)+lengt
h(t_Icpb)+11)]);

Label2={'t_Icp_M_cal(Sec)','Icph_M_cal(A)','Idch_M_cal(A)','Icpb_M_cal(A)',
'Idcb_M_cal(A)'};
xlswrite(num2str(path_filme),Label2,name,['G'num2str(length(Qit_h)+length(t
_Icpb)+9)]);
xlswrite(num2str(path_filme),All_data2,name,['G'num2str(length(Qit_h)+lengt
h(t_Icpb)+11)]);

Label3={'t_Icp_M_cal(Sec)','DNit_h(cm-2)','DVit(V)'};
xlswrite(num2str(path_filme),Label3,'Total_DNit',[char(double('A')+3.*(j-
1)) num2str(1)]);
xlswrite(num2str(path_filme),All_data_total_DNit,'Total_DNit',[char(double(
'A')+3.*(j-1)) num2str(3)]);

Label4={'t_Icp_M_cal(Sec)','DNbt(cm-2)','DVbt(V)'};
xlswrite(num2str(path_filme),Label4,'Total_DNbt',[char(double('A')+3.*(j-
1)) num2str(1)]);
xlswrite(num2str(path_filme),All_data_total_DNbt,'Total_DNbt',[char(double(
'A')+3.*(j-1)) num2str(3)]);

clear Icph_cal_bis Idch_cal_bis Icpb_cal_bis Idcb_cal_bis

tVs = name(13:length(name)-12);

hold on
a=get(gca,'ColorOrder');

h1=subplot('Position',[0.42 0.5 0.5 0.3]);
hc=plot(t_Icp_M_cal,DVit,'o-','color',a(j,:) );
set(hc,'DisplayName', ['Vs='  tVs  ' V']);
xlabel('t (sec)')
ylabel('\DeltaV_i_t (Volt)')

hold on

h2=subplot('Position',[0.42 0.10 0.5 0.3]);
bc=loglog(t_Icp_M_cal,DVbt,'o-','color',a(j,:));
set(bc,'DisplayName', ['Vs=' tVs  ' V']);


xlabel('t (sec)')
ylabel('\DeltaV_i_t (Volt)')

end

legend(h1,'show');
legend(h2,'show');
grid(h1,'on' )
grid(h2,'on' )
```

D.2- Extraction Program of *ΔL*, *L_{eff}*, and *X* for Lateral Scan

```
clear all
close all
clc
```

Semiconductor parameters

```
q=1.628e-19;            % electron charge
kb= 1.380658e-23;       %(J/K), (N-m/K=kg-m2/s2-K)  Boltzmann constant
kb1=8.6174e-5;          %eV /K Boltzmann constant
h= 6.62617e-34;         %(J-s) Plank constant
hb = h/(2*pi);          %(J-s) Plank constant
epsilon0= 8.85418e-14; %[F/cm]
epsilons= 11.9;
m0 = 9.01e-31;          % Kg
Nd= 3.910e16;           % [cm-3]
LG = 2;                 %gate length (µm)
DeltaL = 0.1;           %LDD sub-diffusion
T = 27+273;
Eg0=1.169;              %eV
a=4.9e-4;               %eV/K
b=655;                  %K
Eg=Eg0-(a*T^2/(T+b));   %eV
ni=1e-6/4*(2*kb/(pi*hb*hb))^(3/2)*(m0*m0)^(3/4)*T^(3/2)*exp(-Eg/(2*kb1*T));
VR = [0:-0.05:-7];
PhiF = kb1*T*log(Nd/ni);
```

Calculations

```
DeltaLeff =DeltaL+sqrt((2*epsilon0*epsilons)/(q*Nd))*(sqrt(2*PhiF-VR)*1E4);
Leff= LG-2*DeltaLeff;
Leffhalf = Leff/2;
hold on
figure(1)
plot(abs(VR),DeltaLeff)
figure(2)
plot(abs(VR),Leff)
```

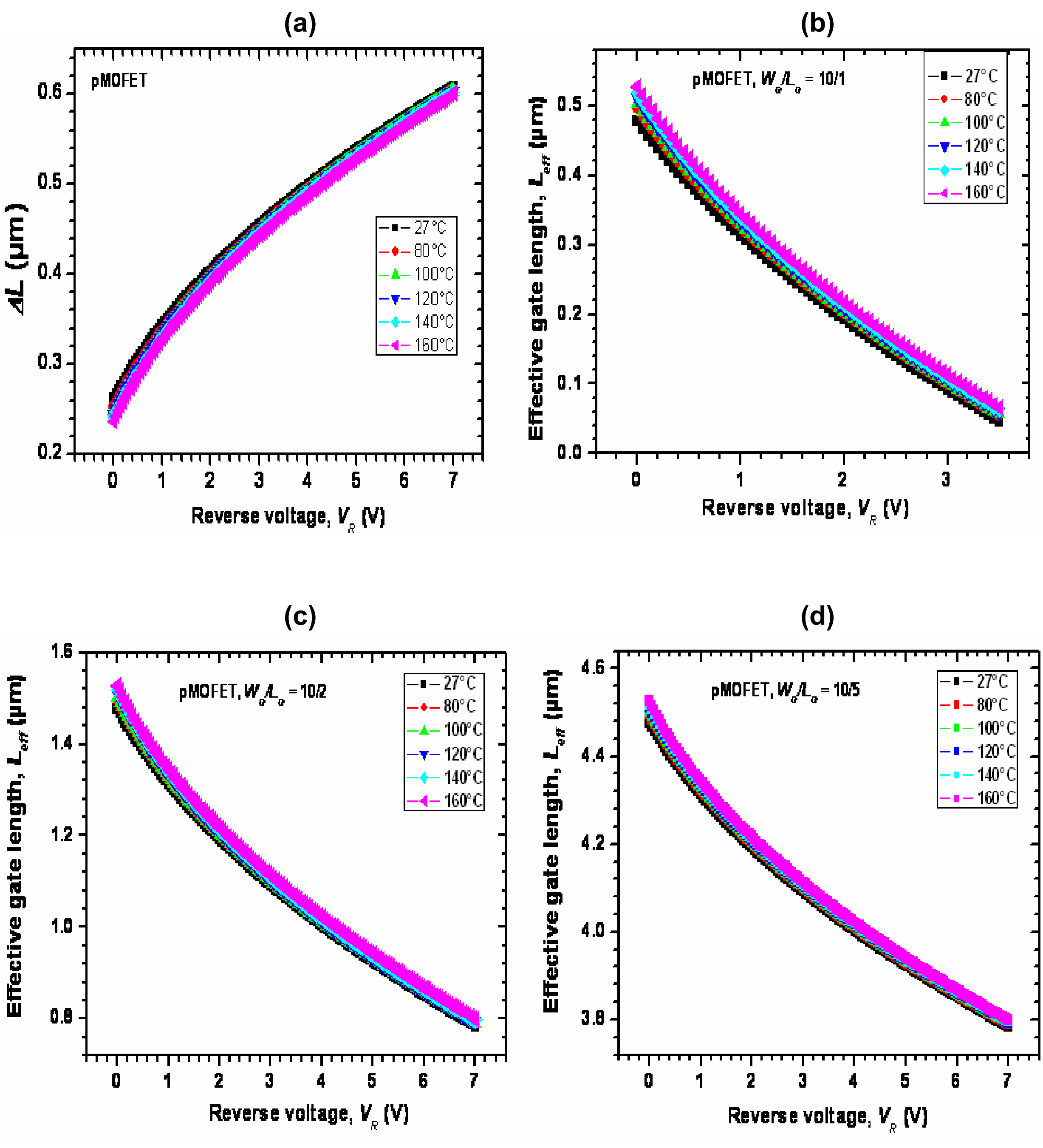


Figure D.1: (a) Sub-diffusion of LDD region (*DL*) beneath the gate versus the source and drain reverse voltage (V_R) for different temperatures. Effective gate length (L_{eff}) versus V_R for p-MOFET with L_G = 1, 2 and 5 μm are represented in (b), (c), and (d), respectively.

D.3- Extraction Program of T_{acc}, T_{inv}, ΔE^*, and Z for Vertical Scan

```
clear all
close all
clc
                                         Semiconductor parameters
q=1.628e-19;             % electron charge
kb= 1.380658e-23;        %(J/K), (N-m/K=kg-m2/s2-K)   Boltzmann constant
kb1=8.6174e-5;           %eV /K Boltzmann constant
m0 = 9.01e-31;           % Kg
mn = 0.5*m0;             % Kg
mp = 0.5*m0;             % Kg
h= 6.62617e-34;          %(J-s) Plank constant
hb = h/(2*pi);
epsilon0= 8.85418e-14;   %(F/cm)
epsilonsio2 = 3.9 ;      % Dielectric constant of SiO2
epsilons= 11.9;
phic = 3.2 ;             % eV
phiv = 4.6 ;             % eV
phis = 0.4;              % eV
sigman0 = 5e-15;         % (cm2) electron capture cross section in SiO2
sigmap0 = 1e-16;         % (cm2) hole capture cross section in SiO2
Nd = ns = 3.9e16;        %(cm-3) electron concentration
ps = 1e18;               %(cm-3) hole concentration
T = 100+273;             % K
Eg0=1.169;               % eV
a=4.9e-4;                % eV/K
b=655;                   %K
Eg=Eg0-(a*T^2/(T+b));    % eV
ni=1e-6/4*(2*kb/(pi*hb*hb))^(3/2)*(m0*m0)^(3/4)*T^(3/2)*exp(-Eg/(2*kb1*T));
vthn = 100*sqrt(8*kb*T/(pi*mn));
vthp = 100*sqrt(8*kb*T/(pi*mp));
cn0=ns*sigman0*vthn;
cp0=ps*sigmap0*vthp;
lambdan=hb/(2*sqrt(2*mn*phic*1.60218e-19));
lambdap=hb/(2*sqrt(2*mp*phiv*1.60218e-19));
```

Charge pumping signal parameters

```
tr=1e-7;
tf=1e-7;
VH=2;
VL= -11;
deltaVG=VH-VL;
Vth=-1.2;
Vfb=0.1;
temh = abs((Vfb-Vth)/deltaVG)*tr;
teme = abs((Vfb-Vth)/deltaVG)*tf;
```

Calculations

```
f = [5000:10000:500000];
tacc = (1./(2*f)-tf+(tr+tf)*abs((VH-Vfb)/deltaVG));
tinv = (1./(2*f)-tf+(tr+tf)*abs((VL-Vth)/deltaVG));
DeltaE= (2.*kb1.*T).*log((sqrt(ns.*ps)./ni).*(sqrt(tinv.*tacc)./sqrt(temh.*teme)));
Znm=lambdan*log(-cn0/(log(0.5))*(1./(2*f)-tf+(tr+tf)*abs((VH-Vfb)/deltaVG)));
Zpm=lambdap*log(-cp0/(log(0.5))*(1./(2*f)-tf+(tr+tf)*abs((VL-Vth)/deltaVG)));

hold on
figure(1)
plot(f,tacc)
figure(2)
plot(f,tinv)
figure(3)
plot(f,DeltaE)
figure(4)
plot(f,Zpm)
figure(5)
plot(f,Znm)
```

Figure D.2: (a) and (c) Calculation of T_{acc}, T_{inv}, and T_H (=T_L) for different temperature and stress voltages. (b) and (d) Depth into the oxide Versus frequency for different temperature and stress voltages.

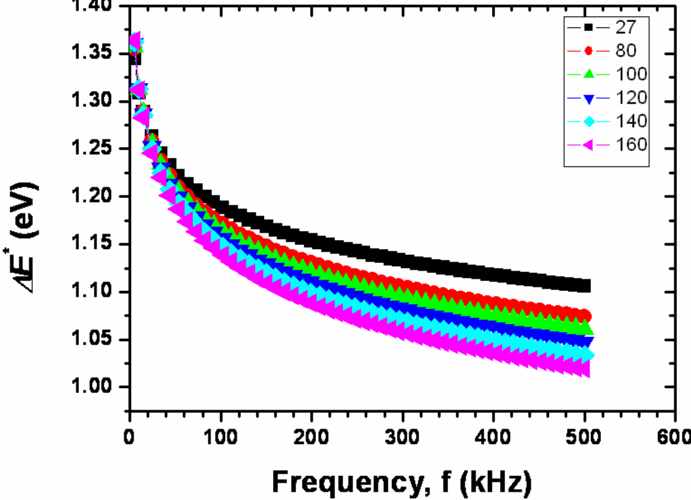


Figure D.3: Energy scanned by C-P into the oxide as function of frequency at different temperatures.

APPENDIX E

E.1- Time Dependence of ΔN_{bt} Data

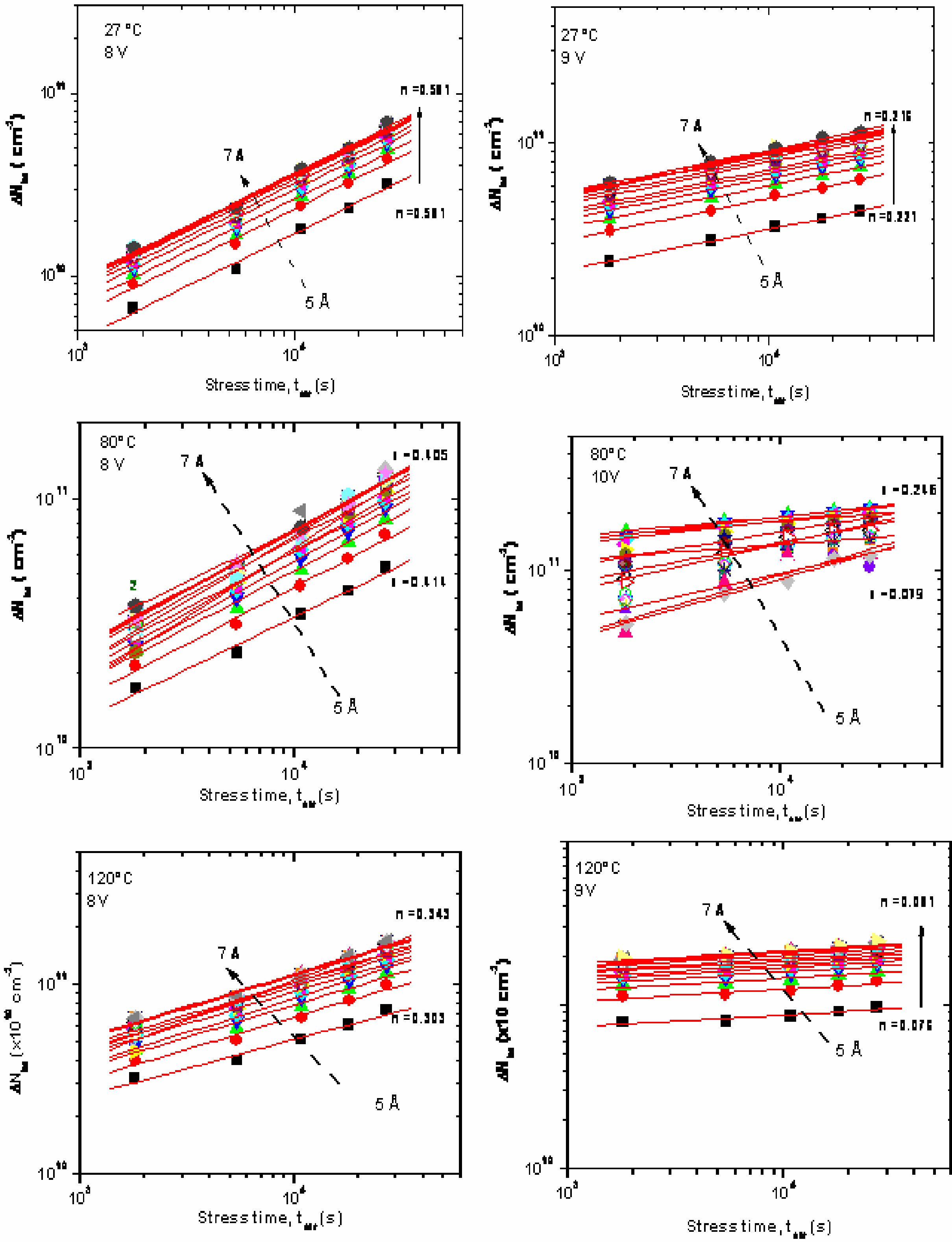


Figure E.1: NBTI-Induced ΔN_{bt} as a function of stress time for different stress voltages and temperatures.

E.2- Temperature Dependence of ΔN_{bt} Data

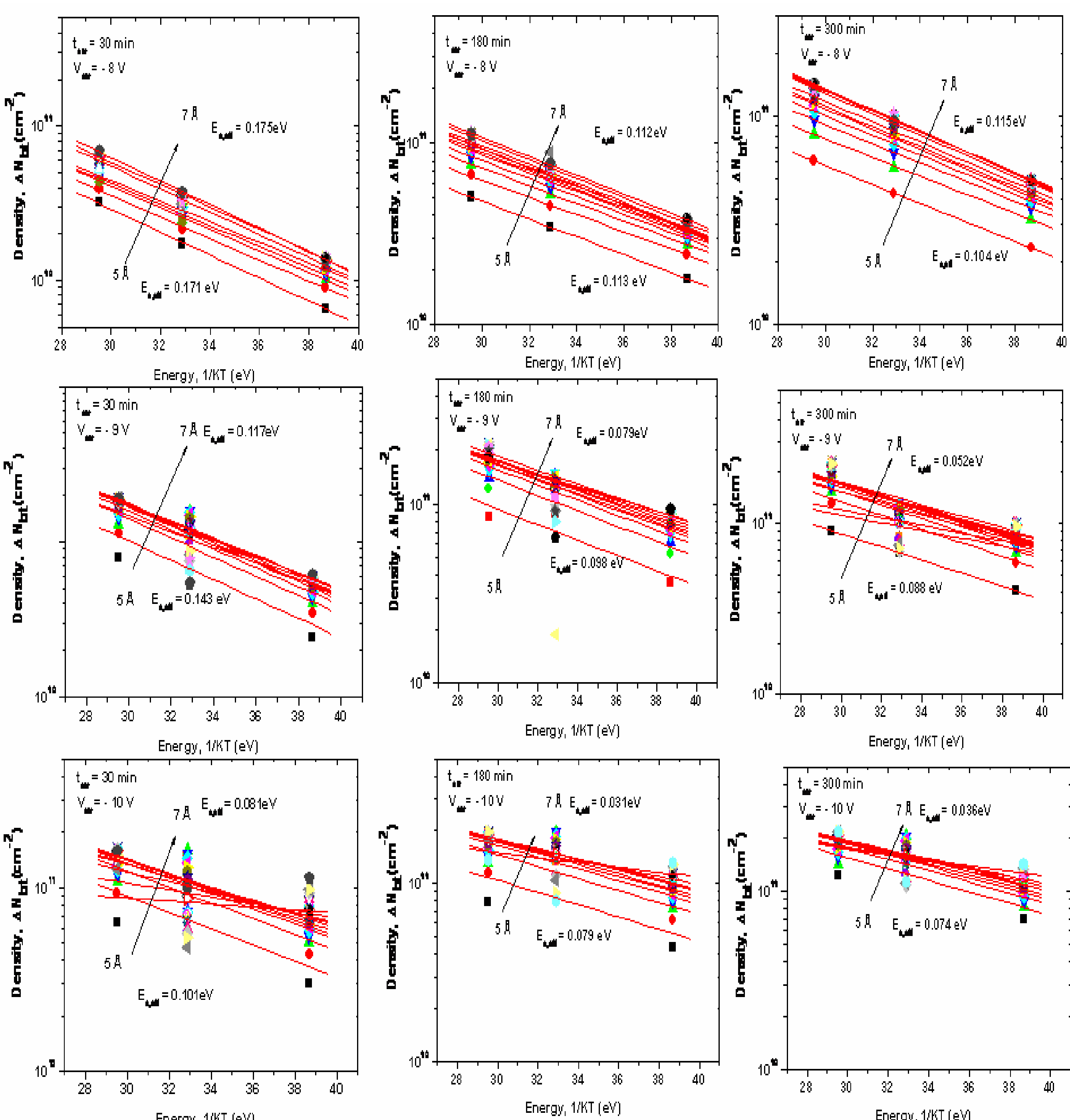


Figure E.2: NBTI-Induced ΔN_{bt} as a function of temperature for different stress voltages and times.

E.3- Field Dependence of Effective activation Energy Data

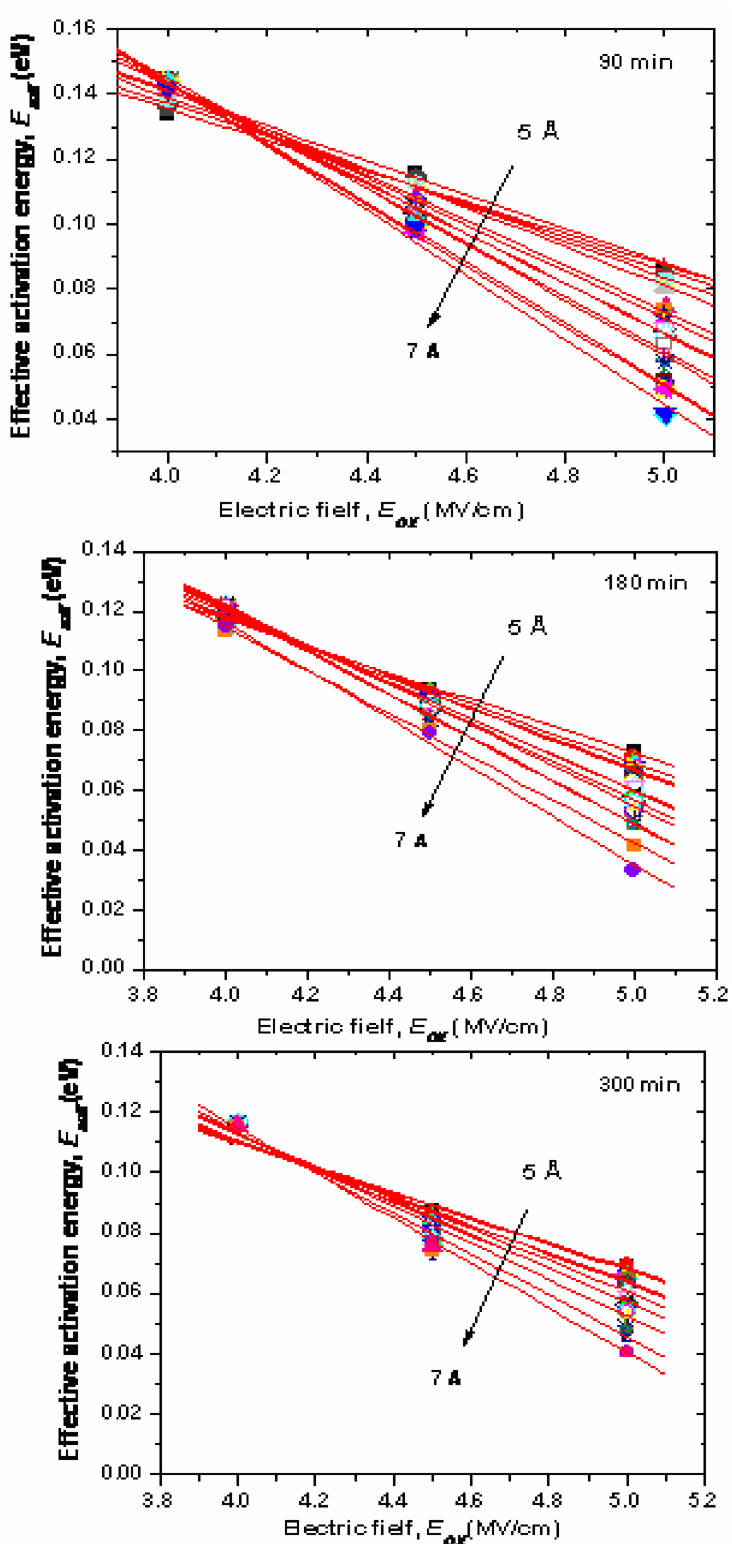


Figure E.3: Effective activation energy as a function of electric field for different stress times.