Digital Distance Relay Reliability Enhancement Using Real-Time Filter

ABDERRAHMANE OUADI*, HAMID BENTARZI* and JEAN CLAUDE MAUN**

*Signals and Systems Laboratory (SiSyLAB)
IGEE, Boumerdes University
E-mail: sisylab@yahoo.com
ALGERIA
** Beams, ULB, Brusselles
BELGIUM

Abstract: - In the conventional three – zone stepped directional distance scheme, distance relay is used to provide the primary as well as remote backup protection. However, the mal-operation of this relay under stressed conditions such as power swing and switching action transient instability may affect the reliability of the whole protective scheme. The voltage and current phasors needed by the distance relay for determining the impedance may be measured with integrated Phasor Measurement Unit. However, this measurement accuracy may be affected by several power disturbances such as fast and slow dc offsets decaying due to sudden current changes, inter-harmonics, etc. To avoid these effects for improving the quality of measurements and hence the distance relay reliability, this work proposes a new real-time filtering method for removing the unwanted DC offset and hence improving SDFT algorithm. To validate the present method, the performance of developed distance relay is tested using the data generated by Simulink/MATLAB simulator. The obtained simulation results are satisfactory.

Key-Words: - Power system, distance relay Unit, real-time digital filter, SDFT algorithm.

1 Introduction

Power system protection is the process of making the production, transmission, and distribution of electrical energy as safe as possible from the effects of failures and events that place the power system at risk. When the faults occur in such power system, protection systems are required to isolate faulted part of the power system, and leave the healthy parts of the system connected in order to insure the continuity of the power supply. The operational security of the power system depends upon the successful performance of the thousands of relays that protect equipments and hence protect the whole system from cascading failures. Thus, the failure of a relay to operate as intended may jeopardize the stability of the entire system and equipment in it. The mal-operation of this relay is generally due to unnecessary tripping that reduces the security of such system and hence its reliability. In order to avoid the unnecessary tripping, many techniques have been developed using filter.

Accurate and fast measurement of the voltage and current phasors of the fundamental components is very important in three-phase distance relay that may be investigated by an integrated Phasor Measurement U<nit (PMU). In relaying system, discrete Fourier transform (DFT) is the most widely used filtering algorithm [1-3] for computing the fundamental phasors and their components. However, some transient disturbance currents of a transmission line may contain a DC offset which decays exponentially with time (time constant of the line inductance to resistance ratio L/R), or a large number of unwanted sub-synchronous frequency or decaying DC components due to the thyristor-controlled switched capacitor (TCSC) compensated lines [4]. This latter always needs few cycles for decaying DC component or 10– 20 cycles for sub-synchronous frequency component to obtain the accurate fundamental phasors by Discrete Fourier Transform (DFT) algorithm. From the evaluation performed using the ideal network [5], the DC offset may have an effective impact on the Fourier algorithm and if no correction is applied, the relative error of the real amplitude from the Fourier algorithm may reach 20%, which purely caused by this decaying offset. For a high performance control and protection applications such a large relative error is not allowed. The performance of the techniques employed directly determine the functions of this equipment and affect their behaviors under various service conditions. Hence, the real-time accurate phasor measurement of the fundamental component and/or symmetrical components is essential and crucial to the safe and economic running of modern electric power systems [6, 7].

For an ac input signal that is associated with a DC offset component, a constant DC and exponentially decaying signal, Gu and Yu [8] propose a modified Fourier filter algorithm using a data window of one cycle plus two samples to compute and perform compensation to remove the unwanted DC offset. The idea behind this algorithm is that the decaying component can be completely removed from the original signal once its parameters are determined. The weakness of the proposed algorithm is that more calculation is needed for eliminating the DC offset. The data window is relevant when implementing this algorithm for the real-time application. A digital mimic filter has been proposed [9], to suppress the effect of an exponentially decaying component over a wide range of time constant (0.5 to 5 cycles and larger) and then apply the DFT algorithm to compute the phasors. A good performance is obtained with this mimic filter when its time constant is identical to the time constant of the exponentially decaying DC component. Another way where the Taylor series expansion is used to approximate the decaying direct component, then the fundamental phasors are estimated by means of curve fitting technique, using least error squares [10]. To enhance the computation speed, the recursive least squares computation curve fitting algorithm is introduced [11]. In addition, a DFT algorithm and least error square technique are combined to estimate the phasor without DC offset signal. Another method was proposed to identify the magnitude and the time constant of the decaying DC offset component [12]. In this method, the residual terms caused by some harmonics are ignored in the estimation procedure. The assumption that these residuals are negligible should not be taken for granted, and needs to be investigated further [5]. The performance of Kalman filters is evaluated in [9]. It was concluded that the third-order Kalman filter is sensitive to variations of the DC offset time constant. A kalman filter should only be superior in removing the DC-offset if its time constant is the same as one modeled in the state transition matrix [9].

This work proposes a method that can correctly extract the phasors of the fundamental components as well as symmetrical components from voltage or current waveforms and then estimate their instantaneous amplitude, phase angle, and frequency with good accuracy and in real-time, even when disturbances occur in large scale and complex power systems. The proposed algorithm is a real-time processing system since a sample by sample basis instead a frame or cycle basis (data window) to obtain the accurate fundamental phasors. This is to fulfill the high speed measurement and detection feature required by the PMU and other applications such control and protective system [13,14]. The approach consists first of removing unwanted dc components of the input measured signal using a fast digital filter algorithm, which is suitable for such a real-time application, and then provide the filtered signal to the Smart DFT[15] algorithm to accurately generate the filtered phasor measurement components.

2 DC Offset

The ideal network shown in Fig.1 may be used to reveal how the source of the decaying DC offset that is induced in the current. In the network, the L/R is variable according to the power system operation conditions and the fault is variable as well. Assume the switch k is closed at t=0, and applying the Kirchhof voltage law leads to the following differential equation:

$$V_m \sin(\omega t + \varphi) = Ri + L\frac{di}{dt} \tag{1}$$

By solving Eq.(1), the current $i(t)$ will be as follows:

$$i(t) = -\frac{V_m e^{-\frac{R}{L}t}}{\sqrt{R^2 + (L\omega)^2}} \sin\left[\varphi - tan^{-1}\left(\frac{L\omega}{R}\right)\right] + \frac{V_m}{\sqrt{R^2 + (L\omega)^2}} \sin\left[\omega t + \varphi - tan^{-1}\left(\frac{L\omega}{R}\right)\right] \tag{2}$$

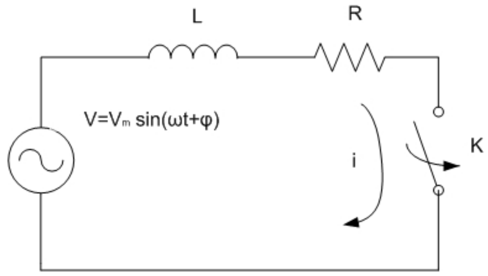

Fig.1 Ideal network

As seen in Eq.(2), the first term is a transient decaying offset component that is function of the parameters R, L ω, φ and V_m. The effect of this term has been evaluated in reference [16] and concluded that the DC offset may have a severe effect on the Fourier algorithm. The relative error of the amplitude from the Fourier algorithm may reach 20% due to this decaying DC offset.

3 Digital Filter

Many filters have been proposed to eliminate the DC offset in the waveforms. A high pass filter with small cut-on frequency as compared to the Nyquist frequency is a required specification for the optimum design of the filter. As the sampling rate is high as compared to a required cut-on frequency, finite impulse response (FIR) standard design leads to very long filter length and computations [17, 18]. In order to reduce the

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memory length and computation effort, to suit the high speed real-time system, an infinite impulse response (IIR) recursive filter that achieve extremely low cut-on frequencies is presented in this paper.

The proposed DC removing filter is composed mainly of a differentiator cascaded with an integrator to shore up the spectral components attenuated by the differentiator. A differentiator that has an infinite attenuation at 0Hz perfectly blocks DC offset. The difference equation describing the filter in time domain is:

$$y_k = x_k - x_{k-1} - p y_{k-1} \qquad (1)$$

Where y_k : the actual output of the filter,
y_{k-1} : the previous output of the filter,
x_k : the actual input of the filter,
x_{k-1} : the previous input of the filter.

The first two terms represent an ideal differentiator (first order difference operator) while the last term describes a leaky integrator. A non-ideal integrator leaks some energy away rather than integrating DC. The leaky term is used, since it resembles to an analogy capacitor used as an integrator and presenting leakage current due to imperfect dielectric.

The filter represented by Eq.(1) is recursive since the previous output is used as input of the system along with a previous and new input sample. This is an infinite impulse response (IIR) filter as the previous output is feedback to the input. To analyze the filter stability and its response, a Z -transform of Eq.(1) may used :

$$H(z) = \frac{Y(Z)}{X(Z)} = \frac{1 - Z^{-1}}{1 - pZ^{-1}} \qquad (2)$$

where p is real pole which, for stability, must lie inside the unit circle $0 < p < 1$.

The differential block is represented by the numerator in Eq.(2) while the denominator represents a single pole transfer function describing the leaky integrator. The filter's pole/zero locations are illustrated in Fig.3 (a), where a zero resides at z = 1 providing infinite attenuation at DC (zero Hz) and a pole at z = p making the magnitude notch at DC very sharp.

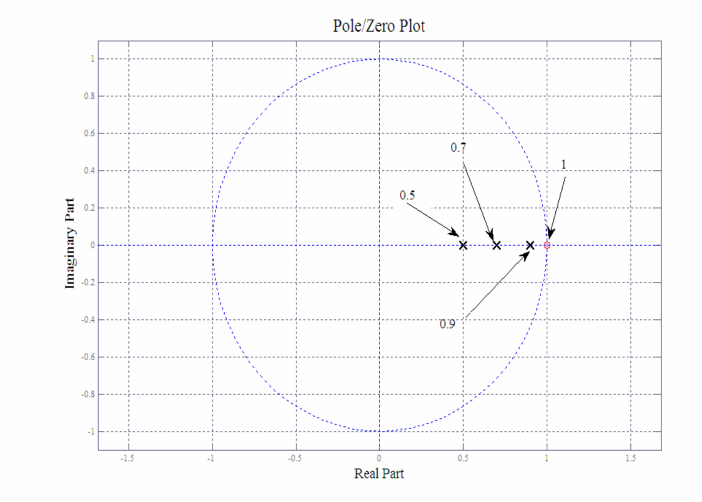
The pole p presents a trade off between the filter bandwidth and the time domain transient response as shown in Fig.4-c.

The magnitude and the phase response can be obtained by substituting $z = e^{j\Omega}$ into (2) and taking the modulus and phase of the transfer function, which are:

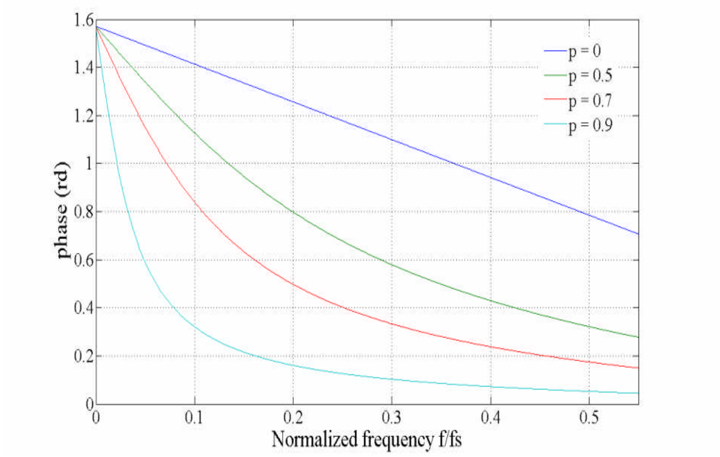
$$H(\Omega) = \frac{2\sin((\pi\Omega/2)}{\sqrt{1 + p^2 - 2p\cos(\pi\Omega)}} \qquad (3)$$

$$\theta(\Omega) = tan^{-1}\left[\frac{(1-p)\sin(\pi\Omega)}{(1+p)(1-cos(\pi\Omega))}\right] \qquad (4)$$

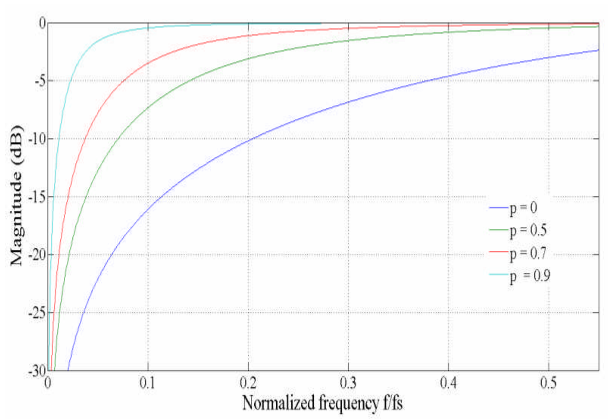
Where $\Omega = \pi f / f_N = 2\pi f / f_s$ is the normalized digital frequency that changes from 0 to 1.



(a)



(b)



(c)

Fig.2 (a) zero and poles plot for different values of p, (b) Magnitude and (c) phase response for different filter pole p values.

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Figures 2-b and 2-c show respectively the magnitude and the phase responses for different values of p. In Fig.2-c the phase response is non-linear in general except when p=0. The phase nonlinearity increases at low frequencies near the cut-on frequency and when the poles tend to unity.
The filter coefficient p can be determined to match an optimal filter design specification mainly, the cut-on frequency and the system dynamic response trade-off.

To investigate the overall shape of the signal output of the filter with respect to its input signal, the group delay property that is also known as the differential phase response is investigated. The group delay (number of samples) in terms of the normalized frequency is given by:

$$Tg = -\frac{d\varphi}{d\omega} = \frac{\sin 2\varphi}{2\sin \Pi\Omega} \qquad (5)$$

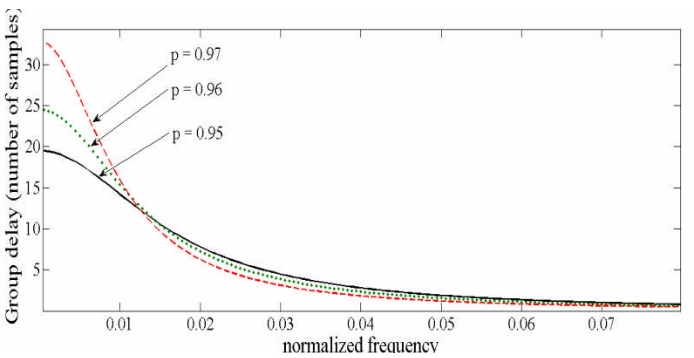

Fig.3 Group delay versus normalized frequency

As the group delay becomes smaller, the distortion of the output signal decreases. Figure 3 shows that the group delay (in number of samples delay) is larger at low frequencies (near cut-on frequency) and for increased values of pole p. For p=0.97 the corresponding normalized cut-on frequency $F_C(f/F_S)$ is 0.78% after which the group delay response falls off rapidly. Its effect could still be noticeable up $10F_C$.

4 Digital Filter implementation

The filter consists of two processing blocks: the integral-differentiator first order IIR filter block for removing dc offset and an all-pass filter for the group delay equalization or phase shift compensation.
This latter block can be cascaded with the first block filter, to alter the phase response while leaving the magnitude response unaffected (see Fig.4). Several techniques may be used for an optimal design of a group delay or phase equalization filter over the pass band interval of the main filter, for application where the time domain signal is important. In fact, this method is relatively complicated and need more computing power.

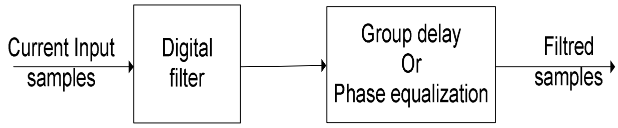

Fig.4 IIR filter block for removing dc offset and an all-pass filter.

The difference equation Eq.(2) defines a sequence of operations that are to be performed in order to implement the IIR filter system. Figure 10 shows that there is more than one way to implement a system and those structures are alike [8]. Since their time domain difference equations relating the various nodes in the feedback path are similar as long as the constant gain are ignored. Some of them may be convenient configuration for fixed-point implementation, by adding a quantization to the feedback path, since the scaling factors are used to avoid the overflow of binary fixed point.
To show the time-domain IIR filter performance, that means the speed and accuracy, a simulated signal using the formula of the ideal fault network. The input signal is considered with the following relation:

$$x(t) = -e^{-\frac{t}{\tau}} + \sin(\omega_o t) \qquad (6)$$

The characteristics of this signal are:

- The fundamental frequency is 50 Hz, thus $\omega_o = 2\pi f_o = 100\pi$,
- The time constant τ considered range from 100 ms to 300 ms,
- The sampling rate considered is 36 samples per cycle.

Figure 5-a shows the time-domain input/output performance of the general DC-removal filter (with α = 0.95). When filter input is fed by a sinusoid suddenly contaminated with a low frequency DC signal (solid line), that is the fundamental components decaying exponentially having a long time constant of about five cycles. Its output (dashed line) falls abruptly with short time (time response of the IIR filter), thus, blocking or eliminating the exponentially decaying offset and leaves only the desired ac signal. The amplitude overshoot appears for short duration (a half cycle) with a small steady state error.
Figure 5-b shows the input and output signals by considering again the signal relation (12) but with longer time constant that is greater than 250 ms. The time of the output response confirms the ability of this filter to remove the decaying DC offset even for longer time constants.

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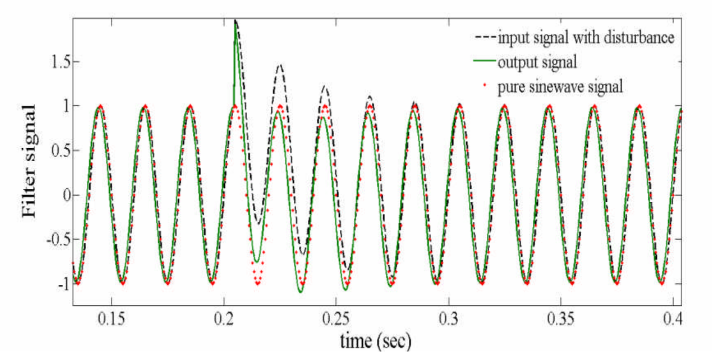
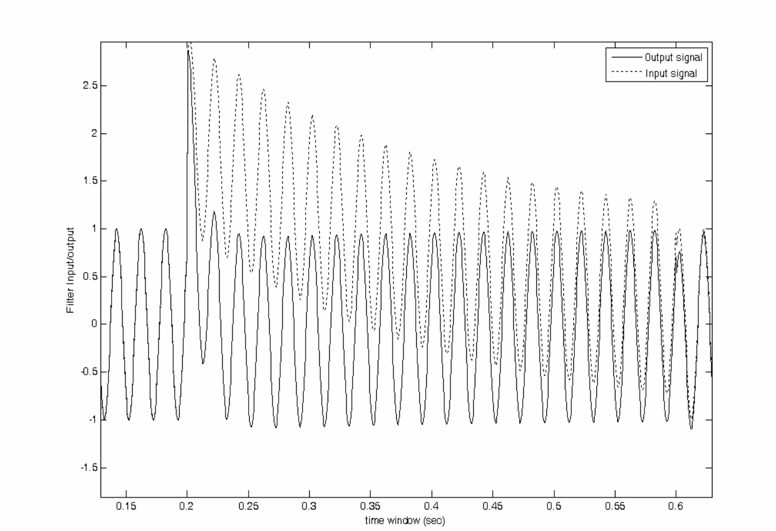
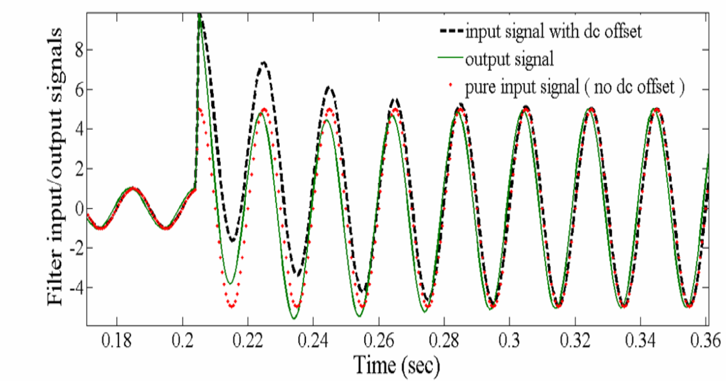


(a)





(c)

Fig.5 sudden change current with dc offset exponentially decaying signal for ideal network (a) for 5 cycle time constant, (b) 20 cycle time constant and (c) realistic configuration.

Figure 6 shows the case when a transient ac signal is applied to the filter, the output is slightly phase shifted, which may be easily compensated by the technique described before. Hence, the input signal is completely passed to the output of the filter without distortion.

The ideal network as presented considers only the exponentially decaying component to reveal the error induced after switching action. In real power system case [10], the transient signal may contain an exponentially decaying DC offset, high frequency components and larger amplitude as shown in Fig.5-c. It also shows the output time response of the IIR filter, where the steady state output signal amplitude removes the decaying offset for a time less than one cycle after the transient signal occurs. The phase shift introduced is minimum and may be corrected after extracting the phasors.

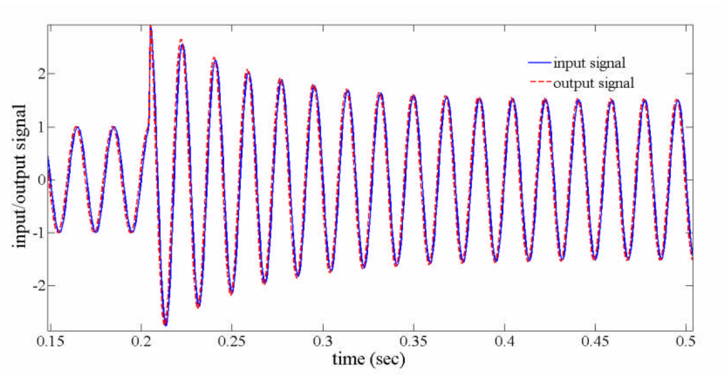


Fig.6 Filter response to transient ac input signal

5 Conclusion

The PMU part of distance relay is tested by applying to it different current signals generated by computer simulation. The obtained simulation results show that the used method is capable of completely eliminating the DC offset and hence greatly improving the reliability of the full-cycle DFT algorithm. Moreover, the performance of the proposed algorithm has been tested under transient and dynamic power system conditions, which are important for the protective relaying applications. These tests have been investigated for signals as function of time by varying magnitudes and/or frequencies. It can be noticed that the digital filter that is appropriate to digital relay tests results are satisfactory.

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