A Rapid Analysis of Very Short Channel MOSFET Performances by Using a Dynamic Simple Model

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***Abstract*—A simplified MOSFET model is presented in this paper. The performances of the model, UNICELL (Unique Cell Model), are compared to those provided by BSIM3V3 taken as reference, even for very short channel length MOSFET (45 nm). It is shown that using only two UNICELL cells (BICELL) gives a good deal for CAD static and dynamic usage, because of the few number of parameters to be used in comparison to BSIM3. BICELL can also be used for determining internal performance analysis.**

***Index Terms*—MOSFET Modeling, BSIM3V3, VERILOG-A**

I. Introduction

MAIN objective of this paper is to present a model of MOSFET much simpler than BSIM3 models, but leading to obtain rapidly and nearly the same simulation results for very short channel MOSFET (45 nm) and giving the possibility of getting internal physical performances of the device.

It's why we developed a single cell model called UNICELL, which can be used in CAD, the model being quasi-static. Section II describes the UNICELL modelling obtained by integrating basic physical equations, and how to make it non-quasi-static by distributing internal capacitances in cells. In section III, are presented DC and TR simulation results with UNICELL implemented into the VERILOG-A module of SILVACO SMARTSPICE. They are compared to Berkeley BSIM3V3 results, taken as reference. They show that comparisons are good even for 45 nm channel length, in DC and in transient analysis.

The important thing to note is that a BICELL model, i.e. a model composed of two UNICELL cells (called also UNICELL2), needs a number of parameters much less (~ten times) than BSIM3V3's.

II. The UNICELL Model

UNICELL model is obtained by integrating channel charges to get only a one cell model.

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A. UNICELL Drain current

Van de Wiele [1] developed an expression of drain current for all operating modes of long channel MOSFET, incorporating the local channel charge. The list of constants and variables used in UNICELL model is given in table 1.

TABLE I. CONSTANTS AND VARIABLES OF UNICELL MODEL

L	Channel length
L_c	Effective Channel length
W	Channel width
I_d	Drain Current
L_i	Length of cell i
V_d	Drain voltage
V_s	Source voltage
V_g	Gate voltage
V_b	Bulk voltage
u_t	Thermodynamic potential
V_t	Local threshold voltage
$\Psi_d(L)$	Surface potential on drain
$\Psi_S(0)$	Surface potential on source
Cox	Oxide capacitance per area
q	Elementary charge
n_i	Intrinsic carrier concentration
N_a	Bulk concentration
ε_0	Vacuum permittivity
ε_s	Silicon permittivity
μ_n	Electron mobility
K	Boltzmann constant
T	Absolute temperature (K)
γ	Threshold Factor
x_d	Thickness of the area of charge space controlled by gate on the drain side
x_s	Thickness of the area of charge space controlled by gate on the source side
x_0	Depth coefficient of area of charge space

Drain current is determined by (1):

$$I_d = \mu_{eff} * \frac{W}{L} * Cox * \int_{\psi_s(0)}^{\psi_s(L)} (V_g - V_t) \frac{\partial V}{\partial \psi} \partial \psi_s \qquad (1)$$

After integration,

$$I_d = \mu_{eff} * \frac{W}{L} * Cox * \left\{ \begin{array}{l} (V_g - V_{fb} + u_t) * (\psi_s(L) - \psi_s(0)) - \frac{1}{2} * (\psi_s^2(L) - \psi_s^2(0)) \\ -\frac{2}{3} * \gamma * \left(A^{\frac{3}{2}} - B^{\frac{3}{2}} \right) + \gamma * u_t * (\sqrt{A} - \sqrt{B}) \end{array} \right\} \quad (2)$$

where

$$A = \psi_s(L) - u_t, \quad B = \psi_s(0) - u_t,$$

$$u_t = KT/q, \quad \gamma = \frac{\sqrt{2 * \varepsilon_0 * \varepsilon_s * q * N_a}}{Cox}$$

1) Effective mobility

The mobility is modulated by transverse and longitudinal electric fields whose effects are taken into account by the way of two empiric parameters Θ_d and Θ_g in next expression (3).

$$\mu_{eff} = \frac{\mu_0}{1 + \Theta d * (\psi_d - \psi_s) + \Theta g * \left(\left(V_g - V_{fb} - \frac{(\psi_d + \psi_s)}{2} \right) + \frac{2 \cdot \gamma}{3} * \frac{\left(\sqrt{(\psi_d - u_t)} - \sqrt{(\psi_s - u_t)} \right)}{(\psi_d - \psi_s)} \right)} \quad (3)$$

2) Channel length modulation

The effect of length modulation is modelled by the simple following expression (4):

$$L_c = L(1 - \lambda * (V_d - V_s)) \quad (4)$$

where λ is an adjustable empiric parameter.

B. Internal and overlap capacitances

Because of the integration, UNICELL is quasi-static. For making a non quasi-static model, it is necessary to use at least two UNICELL cells for distributing charges along the channel. That is possible by introducing 4 internal capacitances by cell, ones modelling the oxide part of the cell Cox_{s_i} (source side) and Cox_{d_i} (drain side), the 2 others the deserted zone part C_{sb_i} and C_{db_i}.

That can be done in the following way:

$$Cox_{s_i} = Cox_{d_i} = 0.5 * \varepsilon_o * \varepsilon_{ox} * W * L_i / t_{ox}$$

$$C_{sb_i} = C_{db_i} = 0.5 * \varepsilon_o * \varepsilon_s * W * L_i / x_{s_i}$$

where t_{ox} is the oxide thickness, x_{s_i} and x_{d_i} respectively the thickness of deserted zone controlled by gate at the drain and source sides of each cell.

$$x_{d_i} = x_d = x_0 * \sqrt{\psi_s(L) - u_t}, \quad x_{s_i} = x_s = x_0 * \sqrt{\psi_s(0) - u_t}$$

with $x_0 = \sqrt{\frac{2 * \varepsilon_0 * \varepsilon_s}{q * N_a}}$

In addition, as usual, it is necessary to add overlap capacitances Covlsb, Covldb and Covlgb considered as parameters.

C. UNICELL model parameters for N channel

Table 2 shows the UNICELL parameters used. for a Nchannel MOSFET.

The number of parameters used by UNICELL is about ten times less than BISIM3V3 model. Three adjustable empiric parameters aid to model mobility and channel length modulation, the others are SPICE physical parameters.

TABLE II. UNICELL PARAMETERS

Param.	*default value*	*unity*	*name*
l	*1.0e-6*	*m*	*Channel length*
w	*1.0e-6*	*m*	*Channel width*
tox	*1.0e-7*	*m*	*Oxyde thickness*
ld	*0.0*	*m*	*Channel length reduction*
xj	*1.0e-7*	*m*	*Junction thickness*
mu0	*0.06*	*$m^2/V{\cdot}s$*	*Surface mobility at weak field*
na	*1.0e22*	*m^{-3}*	*Substrate density*
nd	*1.0e26*	*m^{-3}*	*Source and drain density*
thetag	*0.0*		*Mobility transverse factor*
th etad	*0.0*		*Mobility longitudinal factor*
lambda	*0.01*		*Channel length modulation fact.*
ni0	*1.0e16*	*m^{-3}*	*Free carrier density at 300K*
phi	*0.7*	*V*	*Built in voltage*
vfb	*-0.8*	*V*	*Flat band voltage*
ut0	*0.025*	*V*	*Thermodynamic voltage at 300 K*
covlsb	*0.01*	*pF*	*Overlap so urce-bulk capacitance*
covldb	*0.01*	*pF*	*Overlap drain-bulk capacitance*
covlgb	*0.01*	*pF*	*Overlap gate-bulk capacita*

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III. UNICELL SIMULATIONS WITH VERILOG-A IN SMARTSPICE

For testing UNICELL models, SPICE environment [2, 3, 4] has been used, here SMARTSPICE [5, 6], giving the possibility to compare their performances to SPICE models.

A. DC simulations

The implementation of UNICELL can be set up in SILVACO SMARTSPICE simulator through two ways: by using the SMARTSPICE INTERPRETER module and/or by using the VERILOG-A module [7]. Both were tested, but we present here the VERILOG-A solution much simpler.

Figure 1 shows UNICELL simulations results compared to those obtained by BSIM3V3 for a 0.18 micron channel length.

a) $\mathrm{Log}(I_{ds}(V_{gs}))$ characteristics for V_{ds} = 0.05V and V_{bs}=0.0V
b) $I_{ds}(V_{ds})$ characteristics for V_{gs} = 0.8V, 1.15V, 1.5V and V_{bs} =0.0V.

These curves present a good behaviour not far from the weak inversion (V_{th0} = 0.7V)

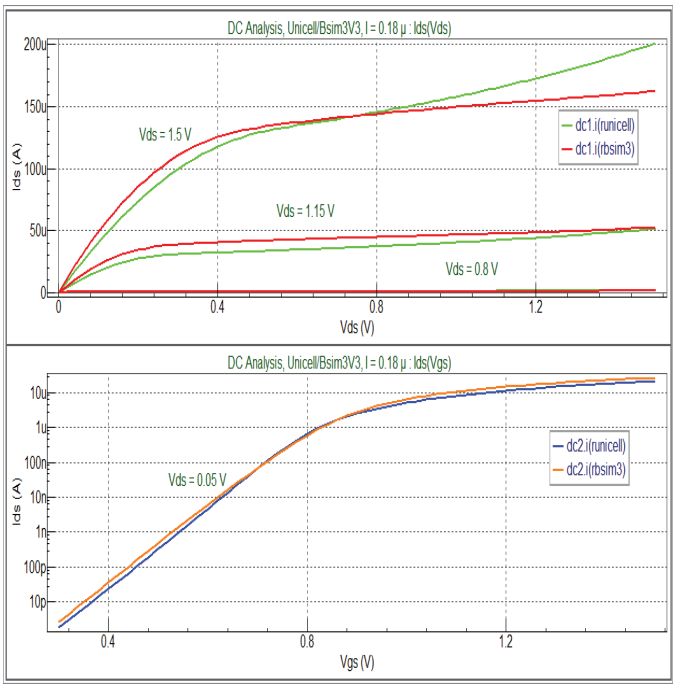

Fig. 1. log Ids(Vgs, Vbs) and Ids(Vds, Vgs) characteristics comparisons with UNICELL 3 and BSIM3V3, L=0.18 micron

DC simulations ($I_{ds}(V_{ds})$ characteristics for V_{gs} = 0.6V, 0.85V, 1.0V and V_{bs} =0.0V) has been performed with SILVACO SMARTSPICE running on WINDOWS XP Pro for comparing CPU times consumed by 1, 2 and 3 UNICELL cells and by resident and BSIM3V3 translated into SMARTSPICE VERILOG-A (table 3).

TABLE III. COMPARISONS OF CPU TIMES WITH BSIM3V3 MODELS AND UNICELL MODELS

model type	**BSIM3V3***	**BSIM3V3.a**	
load time	0	2.408s	
total time analysis	0.016s	2.454s	
time for only analysis	0.016s	0.046s	
model type	**UNICELL (UNICELL1)**	**BICELL (UNICELL2)**	**TRICELL (UNICELL3)**
load time	0.578s	1.186s	1.814s
total time analysis	0.608s	1.233s	1.878s
time for only analysis	0.030s	0.047s	0.061s

*MOS81 resident in SMARTSPICE.

BSIM3V3.a and UNICELLn are translated into VERILOG-A [8] and interpreted by SMARTSPICE.

As it is well known, interpreted (i.e. models written in an other language than the simulator one's) are slower than resident models such as MOS81 (SMARTSPICE BSIM3V3). They have to be loaded and translated, this takes time for loading (load time) and for treating itself (analysis time). Taking the resident BSIM3V3 only analysis time as reference, comparisons give respectively 2, 3 and 4 times for UNICELL1, UNICELL2 and UNICELL3.

UNICELL can then be used in DC regime:

- UNICELL1 for CAD with a CPU time twice than BSIM3V3's, but with ten times less parameters, easier to characterize.
- UNICELLn ($n \geq 2$) for the internal performance analysis with a CPU time increasing with the number of cells. In next section, it will be shown that $n \geq 2$ are necessary for TRAN NQS usage.

Figure 2 shows DC simulations for 45 nm.

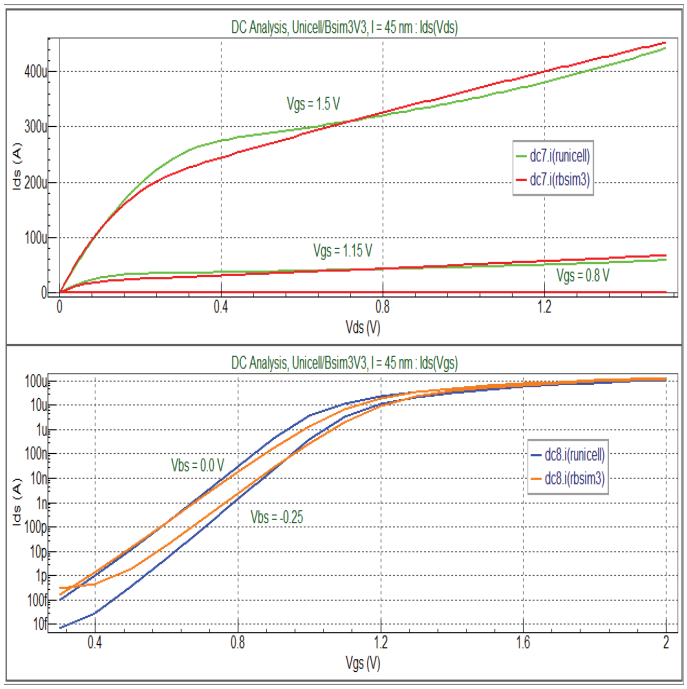

Fig.2. Ids(Vds, Vgs) and Ids(Vgs, Vds) characteristics comparisons with UNICELL 3 and BSIM3V3, L= 45 nm

B. TRAN simulations

UNICELL is quasi-static; charges are not distributed along the channel, but integrated. It is necessary to use at least two UNICELL cells (UNICELL2 or BICELL) to make it non-quasi-static.

1) Charge inertia

On a MOSFET with V_{ds}=1.4 V, a voltage ramp is applied on gate from 0 to 1.15 V during 1ns, followed by a 1.15V constant value till 2ns. Comparisons are done on drain $Ird_{unicelln}$ and source $Irs_{unicelln}$ currents by using UNICELLn (n=1, 2, 3 UNICELL cells) (Figure 3). The UNICELL2 and UNICELL3 curves show that charge inertia is taken into account, because after 1ns drain and source currents return to the same steady state value with nearly the same constant time: UNICELLn, with $n \geq 2$ is NQS. It is not the case with UNICELL1 which is only QS.

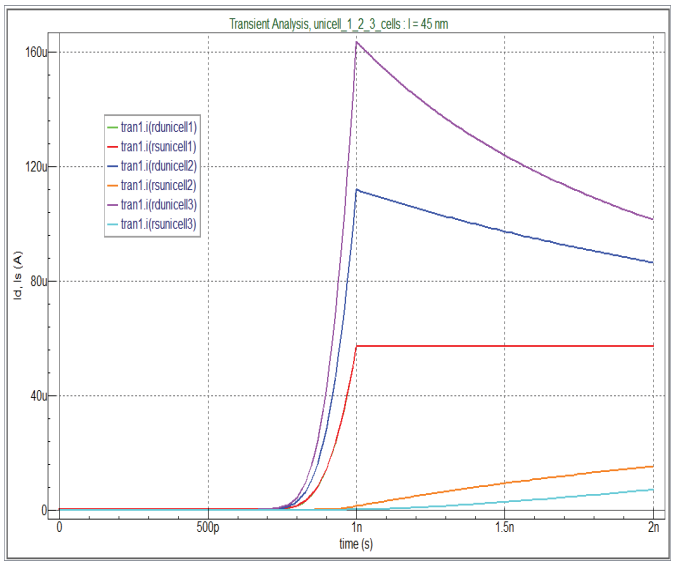

Fig. 3. Dynamic drain current Id, Source current Is obtained with UNICELL1, UNICELL2 and UNICELL3

2) Charge injection in a MOSFET used as a switch

A zero signal is applied on the input of a MOSFET switch V_{db}=0V and a pulse is applied on the gate; V_{gb} (amplitude 2V, rise times 0.1ns, pulse width 2ns), a capacitor is set between the output s and b [10]. For V_{gb} high (2V) the transistor operates in strong inversion and when V_{gb} comes back to 0, the output voltage comes back to a value less than the input value (here a negative value), this effect is caused by the gate charge injection. Figure 4 compares the simulated output voltage using UNICELL2, BSIM3V3.

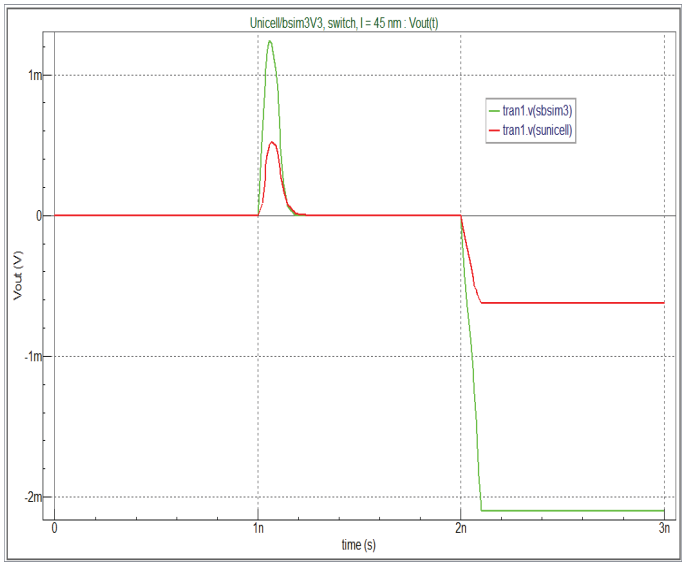

Fig: 4. Output response Vout of a MOSFET switch to a 0 drain pulse with UNICELL and BSIM3V3

IV. Conclusion

We introduced a new simple MOSFET model (UNICELL) whose properties are:

- Integrated charge in one unique cell (UNICELL).
- Charge sheet model.
- Charge conservation.
- Continuity of the drain-source current from weak to strong inversion.

Compared to BSIM3V3 model, taken as reference, this models have the following characteristics and advantages:

- Implemented in a SPICE environment (SILVACO SMARTSPICE through the VERILOG-A module).
- Number of parameters 10 times less than BSIM3V3, with similar CAD performances, even for 45 nm channel length.
- In addition analysis of MOSFET physical internal performances.Non-Quasi-Static UNICELL, if used with at least 2 cells.

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