On the Circuit-Level Reliability Degradation Due to AC NBTI Stress

Amel Chenouf, Boualem Djezzar, Abdelmadjid Benabdelmoumene, and Hakim Tahi

***Abstract*—In this paper, an experimental analysis of the impact of dynamic negative bias temperature instability (NBTI) stress on the CMOS inverter dc response and temporal performance is presented. We analyzed the circuit behavior subjected to ac NBTI in the prospect to correlate the induced degradation with that seen at PMOS device level. The results revealed that, while ac NBTI-induced shift of the inverter features shows both voltage and temperature dependence, it does not always exhibit stress time dependence. Indeed, the time exponent n is found to depend on both voltage and temperature. The analysis of such behavior when correlated with the PMOS threshold shift points toward the coexistence of more than one physical mechanism behind the degradation, where one mechanism could dominate the other under certain stress conditions. Depending on these conditions, circuit lifetime could be more or less affected.**

***Index Terms*—AC NBTI, NBTI characterization, CMOS inverter reliability, performance analysis, stress time dependence, interface states, hole trapping.**

I. Introduction

NEGATIVE bias temperature instability (NBTI) [1]–[3] continues to present one of the major reliability issues for CMOS circuits especially in deep submicron technologies. This is mainly due to the shrinking of the gate oxide thickness with very large scale integration (VLSI) and the introduction of more nitrogen into the oxide [4]. Actually, from a technology node to another, the constant voltage scaling makes transistors to undergo an incessant increase of the longitudinal oxide electric field. Moreover, the tremendous number of transistors resulting from this large scale integration has resulted in a more self-heating of circuits during the normal operating conditions. As a result of the high undergone electric field and/or elevated temperature, CMOS circuits are experiencing a temporal instability of device parameters namely NBTI.

It is well known that NBTI is ascribed to Si/SiO_2 interface states and positive charges in the oxide resulting from the breaking down of Si-H bonds at the SiO_2/Si interface and hole trapping [5], [6]. NBTI is characterized by a positive shift in the absolute value of the PMOS threshold voltage $|V_{\rm thp}|$, a decrease of the transistor transconductance g_m and the drain current $I_{\rm DS}$. CMOS integrated circuit performances are therefore affected and their lifetime reduced [7]–[10].

At the device level, many research works have been performed to study the fundamentals behind the NBTI effect on PMOS transistor, and/or to develop new measurement techniques to capture and separate the degradation components [11]–[14]. This has made modeling theories for the NBTI degradation to be still under debate [15]–[17]. Nevertheless, the focus of the low-level details does not provide insight into the circuit degradation due to NBTI on a larger scale. In fact, it has been shown that the degradation of circuit performance is mainly dependent on the circuit configuration and its application rather than the absolute value of the degradation at the device level [10], [18], [19]. Moreover, the switching (dynamic) nature of digital circuits operation makes them less affected by NBTI as the drift of the device parameters during the stress phase is partially annealed during the recovery phase. Accordingly, predicting digital circuit lifetime based on static NBTI would overestimate the degradation of circuit performance [19], [20]. Actually, it was found that there was a four-decade enhancement in lifetime for ring oscillator as compared to devices stressed in DC NBTI [19]. Therefore, admitting by knowing the voltage threshold degradation of a single PMOS transistor, one can be able to predict circuit degradation is not very true [21]. As such, an extra effort has to be made to bridge the gap between circuit and device reliability analysis. A very few works have dealt with the experimental analysis of dynamic NBTI at circuit level and correlate it with that of device level [22]–[27]. In fact, Fernandez *et al.* [22], [24] found the shift in the inverter logic threshold to be governed by that of PMOS threshold voltage and to be frequency independent. They also found that the $V_{\rm th}$ shift due to AC NBTI is following the same trend shown under DC NBTI with power law time exponent of 0.17–0.20 [22], [24]. It was also found that the data obtained by a ring oscillator frequency shift over 700 days of work is consistent with models based on accelerated testing of PMOS transistor and that the degradation shows a power law with different time exponents of 0.174, 0.211 and 0.186 [23]. In the same prospect, we show with experimental evidence how NBTI degradation at circuit-level is dependent on the circuit configuration and its operation mode. We particularly show how the degradation time dependence varies with voltage and temperature rather than showing a constant value due to the switching nature of the circuit. These findings are the outcome of an experimental analysis of dynamic NBTI stress impact on the CMOS inverter DC logic threshold and temporal performance. We show that even the induced degradation on the circuit performance presents voltage, temperature, and stress

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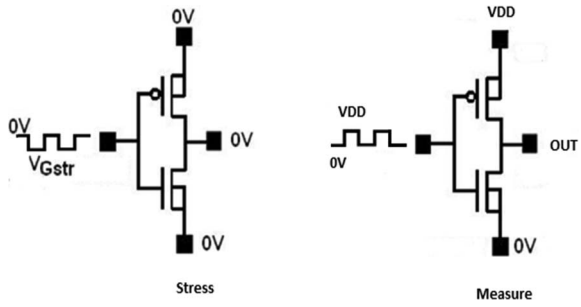

Fig. 1. Stress and measure configurations used to characterize the CMOS inverter temporal performance under ac NBTI stress.

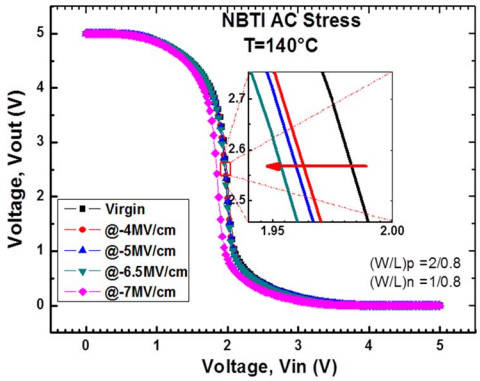

Fig. 2. CMOS inverter dc response subjected to ac NBTI stress.

time dependencies, the time exponent n is both voltage and temperature dependent.

Moreover, when correlated with device-level degradation, the analysis of the shift of CMOS inverter responses due to AC NBTI revealed a signature of the co-existence of more than one physical mechanism behind NBTI degradation where the dominance of one mechanism over another depends on stress time, voltage, and temperature conditions.

The rest of the paper is organized as follows. In Section II, the circuit under test, the experimental AC NBTI setup details, and the Measure/Stress/Measure (MSM) protocol are described. The obtained results are analyzed and discussed in Sections III and IV, while Section V concludes the paper.

II. Experimental Setup

The Circuits Under Test (CUTs) consist in CMOS inverters with aspect ratios of 1 μm/0.8 μm and 2 μm/0.8 μm for NMOS and PMOS transistors, respectively. These inverters are of 20 nm SiO_2 gate oxide grown with dry O_2 using a conventional CMOS process at ISIT (Institute for Silicon Technology) of Fraunhofer, Germany.

The experimental setup is based on MSM technique where the MSM sequences have been performed using fully automated benches. The bench included an Agilent HP 4156C Semiconductor Parameter Analyzer for both DC polarization and stress of CUTs, an Agilent 16440A SMU/Pulse Generator Selector to ensure automatic switch of the output between stress and measurement, and a Tektronix Digital Oscilloscope TDS 3054 to track the inverter temporal response. Besides, a PID-controlled hotplate was used, inside Karl SUSS PA300 micro-manipulator probe station, to set the temperature of the chip during the experiments. The test circuit chip (non-packaged) within and the probe station were enclosed in a grounded Faraday cage to avoid both RF and light effects.

Two stress frameworks have been used: one of 3600 s to characterize the inverter DC response and another of 3 hours and half (12 600 s) to characterize its temporal response. The test protocol adopted in the first framework is described as follows: a measure of the DC response of the inverter was done and saved. Then, for a period of 3600 s, an AC pulse signal of 10 kHz and 0.5 duty cycle with a V_{Gstr} ranging between -8 and -14 V was applied to the input of the inverter while the rest of the circuit pads were grounded (see left-side of Fig. 1). Once the stress was completed, the DC response of the inverter was redone and saved. In the second stress framework, during the measurement, a square pulse with the same frequency and duty cycle of AC NBTI stress, but with a positive voltage, was applied to the inverter input (see right-side of Fig. 1) before and after the stress. The measurement of the inverter temporal response was conducted after each 1800 s of the stress time which lasted for a total period of 3 hours and half. The switch between stress and measure configurations was automated via a LabVIEW program. The obtained results are given hereafter.

III. Results

A. Impact of AC NBTI on the Inverter DC Response

Fig. 2 illustrates the inverter voltage transfer curve (VTC) subjected to AC NBTI at 140 °C under a series of negative voltages ranging from -8 V to -14 V (-4 to -7 MV/cm). The curve denoted by virgin presents the response of the inverter before applying any stress.

As expected, AC NBTI stress induces a shift of the inverter VTC to the left side as does the DC NBTI stress. The analysis of AC NBTI against DC NBTI impact on the DC response of the inverter revealed that the former induces a shift of the inverter logic threshold (ΔV_{inv}) 3 times lower than that induced by DC NBTI. This ratio is found to be less than expected by theory for an AC NBTI with a 0.5 duty cycle and reported elsewhere [25]. Besides, noise immunity shift due to AC NBTI is found to be 7 times lower than that due to DC NBTI. As such, DC NBTI is presenting the worst case degradation and could not be suitable for use to properly predict digital circuit's lifetime. The detailed comparison between DC and AC NBTI impacts on the inverter's robustness can be found in [27]. Hence, we review here the shift of one of the main inverter DC features that is ΔV_{inv} and its trend under AC NBTI stress in the prospect to correlate it with PMOS threshold voltage V_{th} shift (ΔV_{thp}).

Fig. 3 shows the AC NBTI-induced shift of ΔV_{inv}, plotted in a semi-log scale, as a function of the oxide field in (a) and the temperature in (b).

It outcomes that ΔV_{inv} increases with increasing electric field and worsens at elevated temperature. Besides, two trends of oxide field and temperature dependencies can be observed. In Fig. 3(a), under AC NBTI stress with oxide field up to 6.5 MV/cm, the electric field acceleration parameter (γ) of ΔV_{inv} is almost constant and equals 0.15 cm/MV. Then, it

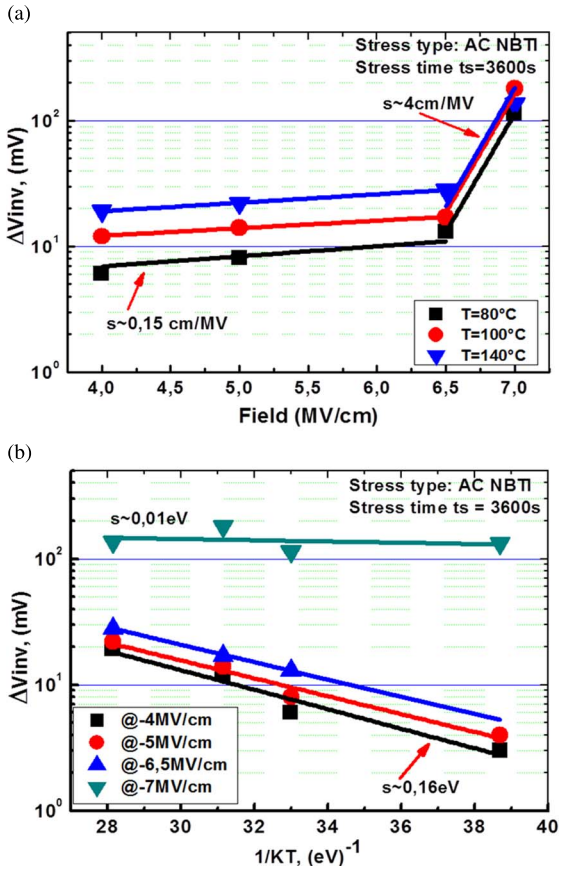

Fig. 3. Inverter logic threshold shift due to ac NBTI with respect to the applied field in (a) and to the temperature in (b).

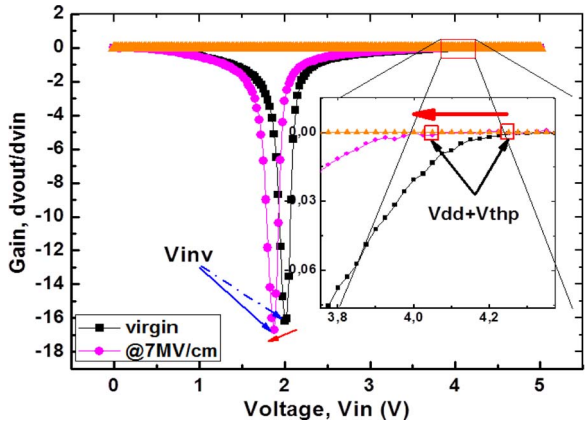

Fig. 4. Method of extracting PMOS threshold $V_{\rm thp}$ from the inverter gain.

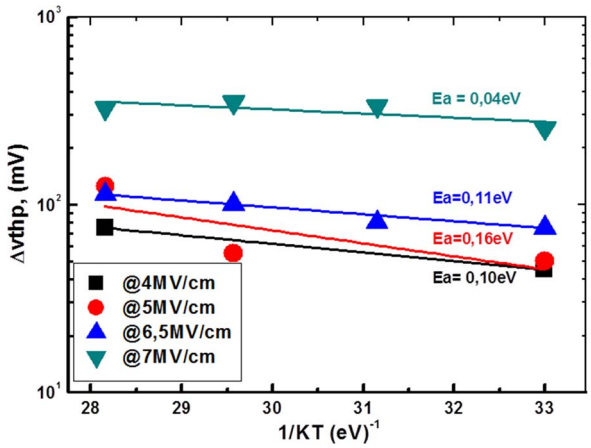

Fig. 5. Shift of the extracted PMOS threshold voltage under ac NBTI with respect to the energy under different electric fields.

rises to 4 cm/MV when the electric field goes higher. The opposite trend can be observed for the activation energy value [see Fig. 3(b)]. This latter equals 0.16 eV under AC NBTI with low oxide field, then it drops to 0.01 eV under higher oxide field. Consequently, $\Delta V_{\rm inv}$ shows two tendencies: degradation with low field acceleration (0.15 cm/MV) and high activation energy (0.16 eV) then degradation with high field acceleration (4 cm/MV) and low activation energy (0.01 eV).

These two different temperature dependencies of $\Delta V_{\rm inv}$ seem to point toward the co-existence of the two physical mechanisms behind the NBTI degradation of the PMOS threshold shift $(\Delta V_{\rm thp})$ to know: interface traps creation (with 0.16 eV) and holes trapping (0.01 eV) [1], [15].

To give more insight about this assumption, we examine, in the following, $\Delta V_{\rm inv}$ against $\Delta V_{\rm thp}$.

Recall that the inverter logic threshold $(V_{\rm inv})$ is the point on the inverter VTC at which Vin = Vout. It is resolved by equating the inverter NMOS and PMOS transistors drain currents in their saturation mode. It is expressed as a function of the ratio of the NMOS and PMOS gains and their threshold voltages as

$$v_{\rm inv} = \frac{r\,(V_{\rm DD} - |V_{\rm thp}|) + V_{thn}}{r+1} \tag{1}$$

$$\text{Where}: \; r = \sqrt{\frac{\beta_p}{\beta_n}} = \sqrt{\frac{\mu_p w_p}{\mu_n w_n}}. \tag{2}$$

$V_{\rm DD}$ is the supply voltage, $V_{\rm thp}$, and $V_{\rm thn}$ are, PMOS and NMOS threshold voltage, respectively.

β_p, and β_n present PMOS and NMOS transconductances, while μ_p and μ_n correspond to their motilities.

By assuming r constant, the differentiation of (1) with respect to $V_{\rm thp}$ results in

$$\Delta v_{\rm inv} = \frac{r}{r+1}\Delta v_{\rm thp}. \tag{3}$$

This latter equation expresses the shift of the inverter logic threshold as a function of that of the inverter's PMOS threshold voltage. Then, one can expect if governed by the same physical mechanisms, $\Delta V_{\rm inv}$ and $\Delta V_{\rm thp}$ under NBTI ought to show similar temperature dependencies.

For this aim, we have extracted the PMOS threshold voltage from the inverter VTC before and after stress by differentiating this latter and resolving where the slope drops down to zero as shown in Fig. 4. The corresponding shift with respect to the energy is depicted in Fig. 5.

It is clear that $\Delta V_{\rm thp}$ is larger than $\Delta V_{\rm inv}$ with slightly different activation energies. In fact, $\Delta V_{\rm thp}$ shows an activation energy (E_a) of 0.11 eV against 0.16 eV of $\Delta V_{\rm inv}$ under AC NBTI with $E_{\rm ox} \leq 6$ MV/cm. Then, it shows an E_a of 0.04 eV against 0.01 eV of $\Delta V_{\rm inv}$ with Eox $>$ 6.5 MV/cm.

This slight difference can be attributed to the influence of the shift of NMOS threshold ($V_{\rm thn}$) and that of the transistor's transconductances on the measured $\Delta V_{\rm inv}$.

Based on the similar temperature dependencies shown by ($\Delta V_{\rm inv}$) and ($\Delta V_{\rm thp}$). (Figs. 3(b) and 5), we can conclude that the inverter threshold shift is governed by the same physical mechanisms behind the PMOS threshold shift.

The range of the activation energy (E_a) found here for $\Delta V_{\rm thp}$ (0.11 eV–0.04 eV) is consistent with values of (0.063 eV) and (0.115 eV) reported by Huard *et al.* [1] and Ang *et al.* [15], respectively.

Based on the discrepancy between the E_a of the $\Delta V_{\rm thp}$ and that associated with interface states, both Huard and Ang made evidence of the co-existence of two mechanisms of the degradation. The first one is related to hole trapping with a low E_a (0.02 eV) [1] and (0.06 eV) [15] and the second one is related to the interface states generation with a higher E_a (0.16 eV) [1], and (0.144 eV) [15]. Based on the same thinking, we can say that the discrepancy of activation energies shown by both $\Delta V_{\rm inv}$ and $\Delta V_{\rm thp}$ (*see* Figs. 3(b) and 5 under $E_{\rm ox} \leq$ MV/cm ($\sim$0.16 eV) and under a higher oxide field; $E_{\rm ox} >$ 6.5 MV/cm ($\sim$0.01 eV), would advise on the signature of more than mechanism behind the degradation which is dominated by interface states under low oxide field and by hole trapping when the oxide field goes higher.

On the other side, the first $E_{\rm a}$ found here for $\Delta V_{\rm thp}$ under $E_{\rm ox} \leq$ 6.5 MV/cm that is 0.11–0.16 eV coincides with the $E_{\rm a}$ measured by Huard *et al.* [1], [5] for $\Delta V_{\rm thp}$, at the end of the recovery phase of dynamic NBTI, and by Ang *et al.* [15], after a dynamic NBTI of 30 cycles of Stress. They found this energy to be consistent with that of interface traps extracted using charge pumping method. So, they concluded the permanent component of dynamic NBTI to be attributed to interface traps. However, if the permanent component NBTI would be only due to interface traps, then how would we explain the large $\Delta V_{\rm thp}$ with low activation energy undergone when the oxide field goes higher than 6.5 MV/cm in our experiment? There might be another component which slowly recovers as does interface states but has low temperature dependence. Based on the resemblance between this latter and that reported for hole trapping [1], [15], we can say that this part may be related to hole traps with large recovery times.

Accordingly, we can say the characterization of the inverter DC response subjected to dynamic NBTI stress has advised us on the existence of more than one physical mechanism behind the NBTI degradation.

B. AC NBTI Impact on the Inverter Temporal Performance

To more comprehend the NBTI effect at circuit-level, and give more insight on the mechanisms behind the degradation, we examine, in this section, the CMOS inverter temporal performance subjected to AC NBTI stress. Therefore, besides voltage and temperature dependencies of the NBTI-induced degradation, its stress time dependence is also reviewed. For this aim, one inverter was used for each (voltage, temperature) pair. Each inverter was stressed for 3 hours and half by a 10 kHz, 0.5 duty-cycle AC NBTI pulse.

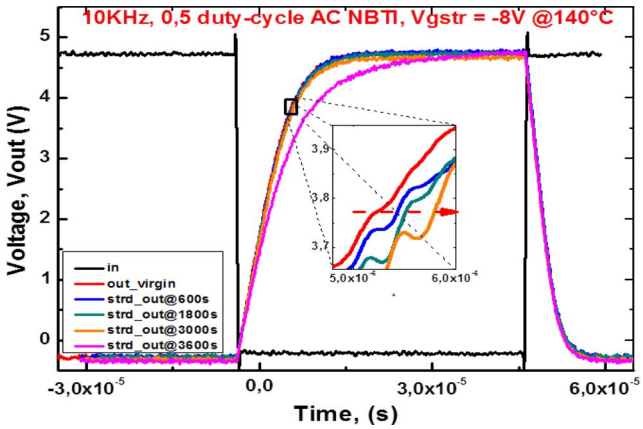

Fig. 6. CMOS inverter temporal response subjected to ac NBTI stress.

Fig. 6 shows an example of the temporal response of the CMOS inverter subjected to AC NBTI stress. The out_virgin curve denotes the inverter's temporal response before applying any stress, while the other curves correspond to its response after 600, 1800, 3000, and 3600 s of the stress time.

It can be observed that the low-to-high switching feature of the inverter response experiences an increasing shift to the right-side. This shift becomes more apparent when the stress time increases.

Subsequently, two temporal features of the inverter might be influenced by this shift: the rise time (Tr) and the low-to-high delay ($D_{\rm LH}$). The former corresponds to the time that takes the output to rise from 10% to 90% of its steady state value, while the latter corresponds to the time that takes the output to reach 50% of its steady state value after the input has crossed it. In this section, we focus on the analysis of the rise time shift under AC NBTI.

To obtain a first-order estimation of the switching time, a simple RC model can be used. During the rise time interval, the inverter's NMOS transistor is cutoff, while its PMOS transistor is conducting from the power supply. In such model, the nonlinear resistance of PMOS is approximated by its best-case value where the transistor is assumed to be saturated. Then, the inverter rise time can be expressed by:

$$T_r = \frac{c_{\rm Load} \times 2V_{\rm DD}}{\beta_p \left(V_{\rm DD} - |V_{\rm thp}|\right)^2} = \frac{K}{\left(V_{\rm DD} - |V_{\rm thp}|\right)^2} \tag{4}$$

where $V_{\rm DD}$ is the supply voltage, $C_{\rm load}$ is the inverter load capacitance, and βp is the PMOS gain factor given by

$$\beta_p = c_{\rm ox}\left(\frac{w}{l}\right)_p. \tag{5}$$

By differentiating the rise time in (4) with respect to $V_{\rm thp}$, the relative rise time shift can be expressed in terms of $\Delta V_{\rm thp}$ as

$$\frac{\Delta T_r}{T_r} = 2\frac{\Delta V_{\rm thp}}{\left(V_{\rm DD} - |V_{\rm thpo}|\right)}. \tag{6}$$

Based on (6), one can expect the relative shift of the inverter's rise time to follow a similar time dependence as that of $\Delta V_{\rm thp}$ under NBTI stress. Hence, if the shift of $\Delta V_{\rm thp}$ would follow a

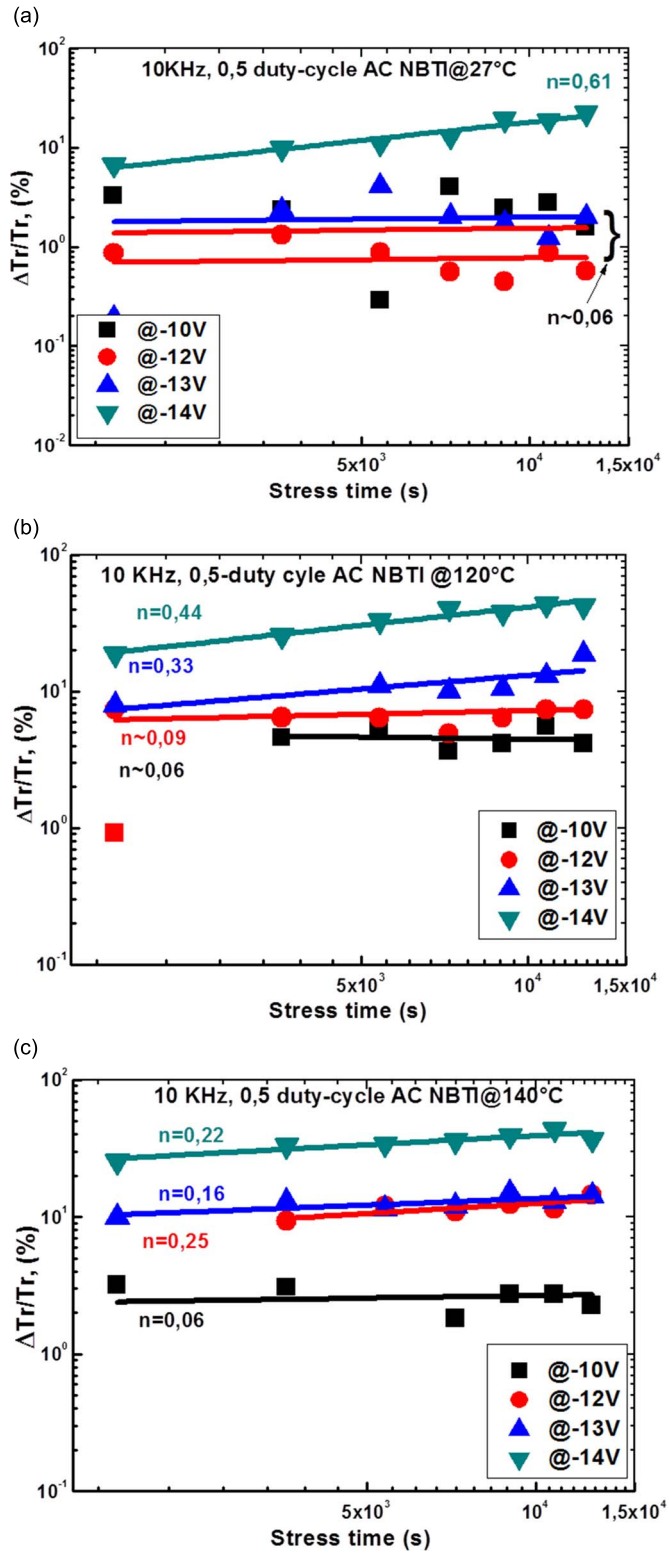

Fig. 7. CMOS inverter rise time shift with respect to stress time under a series of electric fields at different temperatures.

power law with stress time, then the shift of the relative rise time would too. To verify such statement, we have plotted, in log-log scale, the rise time shift with respect to the stress time at different temperatures and under different voltages as shown in Fig. 7.

Two different behaviors can be observed. The first one is shown at room temperature and under low AC NBTI stress voltage. The second is observed under higher voltage and at elevated temperature.

In the first case [see Fig. 7(a)], under an AC NBTI stress at room temperature, the rise time shift is trivial and remains quasi constant with time stress under different stress voltages except under -14 V. The same trend can be observed at elevated temperature when the stress voltage is set to -10 V (-5 MV/cm) (see the fitted data in black line (b) and (c) of Fig. 7).

The second behavior is observed when the AC NBTI pulse voltage is set to a higher value than 10 V and the temperature is elevated above 100 °C. In such case, the amount of the rise time shift becomes more important and starts to increase with stress time increasing. Indeed, under an AC NBTI of -12 V (-6 MV/cm) the degradation does not show a time exponent (n) higher than 0.1 until the temperature is elevated to 140 °C [Fig. 7(c)]. However, for an AC NBTI stress voltage of -13 V (-6.5 MV/cm), a temperature of 120 °C was large enough to induce a degradation with a similar time exponent [Fig. 7(b)]. So, contrary to other works conducted at circuit level which found that the degradation showing a power law with time exponent n of 0, 16 [31], the time exponent found in our experiment framework does not show a constant value. Based on these observations, one can speculate on the voltage and temperature dependence of the time exponent n. We further examine, in the following, the observed trends.

The relatively low degradation with slightly stress time dependence ($n = 0.06$) shown by the inverter rise time at room temperature and under low AC NBTI stress voltage (-10 V) seems to mimic the trend of hole trapping in preexisting traps, while that shown at higher voltages and at elevated temperature seems to include two parts which could be attributed to both hole trapping and the generation of interface state (traps). This can be justified as follows.

At room temperature and under AC NBTI stress with negative voltages lower than 14 V, the insignificant shift which remains quasi constant with stress means no creation of traps has happened. Therefore, the observed shift could be attributed to hole trapping in preexisting deep level traps. This thought is consolidated by the fact that our circuits are made with dry thermally grown SiO_2 and an experimental evidence of hole trapping in such oxides at room temperature has been reported in [28]. It was also found that NBTI degradation of PNO based PMOS transistors below 290 K is dominated by hole trapping process and that it is unnecessarily related to nitrogen but the incorporation of nitrogen in the gate dielectric increases the probability of hole trapping in the NBTI process [6].

When the temperature is elevated, the degradation becomes more important and the time exponent starts to increase above 0.1. The increase of the time exponent is induced by the combination of voltage and temperature. On one hand, if the stress voltage of the AC NBTI is low (Vgstr $<$ 13 V) a higher temperature ($T > 120$ °C) is needed to induce an $n > 0.1$. On the other hand, when the stress voltage is increased (Vgstr $\geq$ 13 V) less temperature is required to observe an $n > 0.1$. This trend of the time exponent n of the inverter rise time shift with voltage and temperature looks like the trend seen for its logic threshold and

shown in Fig. 3: that is high temperature acceleration coupled with low field acceleration for $E_{\rm ox} < 6.5$ MV/cm, and high field acceleration coupled with low temperature acceleration for $E_{\rm ox} \geq 6.5$ MV/cm. Hence, we can assume that the degradation of inverter rise time would be dominated by the interface states creation in the first case and by hole trapping generation in the second case.

Fig. 8 can give more insight on the possible origins of the degradation. Indeed, in the case of an AC NBTI stress under low voltage, the activation energy of the rise time is around 0.06 eV while it equals 0.25, 0.17, and 0.09 eV under -12, -13, and -14 V, respectively. This trend consolidates the idea that the NBTI degradation can be due to trapping in pre-existing traps (with $E_a \sim 0.06$ eV), or to new generated traps (interface traps with higher activation energy (0.17–0.25 eV) or to both interface states and oxide traps under certain conditions with dominance of these latter as the E_a decreases to 0.11 eV then to 0.04 eV with stress time increasing. Therefore, the signature of the NBTI-induced inverter rise time shift when correlated with the PMOS threshold shift also reveals the co-existence of more than one physical mechanism behind the degradation. Moreover, higher the electric field and temperature and longer the stress time are, more likely is to observe a power law dependence with time stress of the circuit performance degradation.

On the other side, when the AC NBTI stress voltage is set to -14 V, the shift of the rise time at room temperature becomes significant and shows an increase with stress time increasing with an important time exponent $(n = 0.6)$. The shift continues to increase at higher temperature but with a decreasing time exponent. In fact, at the beginning of the stress, the shift becomes more important when the temperature is elevated from room temperature to 120 to 140 °C, meaning more traps are generated. Then, it tends to increase slowly with both temperature and stress time increasing. This could be due, on one hand, to the temperature accelerated recovery [29] during the half period of the AC stress when temperature is elevated from 120 to 140 °C, and on the other hand, to decrease of available defect precursors to break when stress time goes longer. Such trend of time exponent decrease with higher temperature was interpreted by Pobegen *et al.* by the time-temperature concept merging from the logarithmic nature of NBTI recovery [30].

IV. Discussion

As point out, the NBTI degradation under AC NBTI stress is much less important than that under DC NBTI stress. Indeed, the configuration of the circuit and its operation mode (switching) largely influences the way the circuit is degraded. The results of the characterization of the inverter DC response and temporal performance presented here have confirmed many aspects and revealed others.

The confirmed aspects are:

The Circuit-level NBTI degradation is voltage, temperature and stress time dependent.

The circuit-level degradation follows device-level degradation in terms of voltage and temperature dependence.

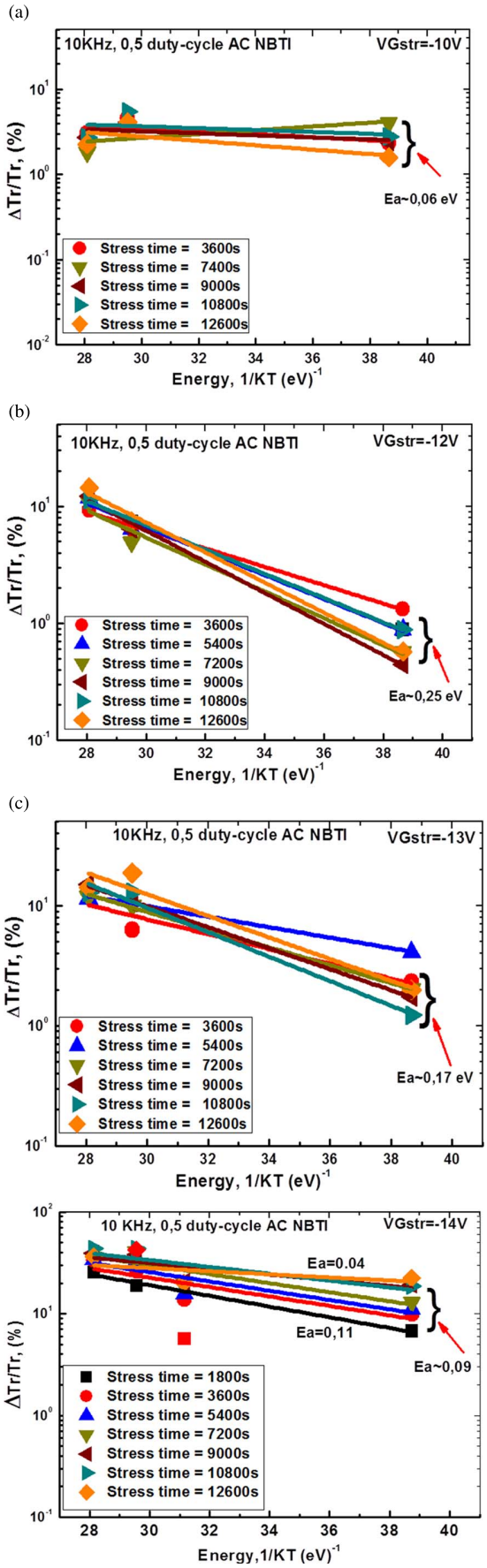

Fig. 8. CMOS inverter rise time shift with respect to the energy under different ac NBTI stress voltages.

The revealed aspects are:

Experimental evidence of the signature of more than one physical mechanism behind the degradation where the dominance of one mechanism over the other depends on voltage, temperature, and stress time conditions.

The time exponent found here is not a fixed value but rather depends on both voltage and temperature Contrary to what is reported elsewhere [31] about the fixed value of the time exponent to 0.16 for digital circuit NBTI degradation. Time exponent observed increases with stress voltage increasing at low temperature or with temperature increasing under low stress voltage. This finding of voltage and temperature dependence of the inverter switching time is consistent with other works conducted at circuit-level [23] where it authors found that time exponent depends on the circuit workload. In fact, they found system 1's frequency degradation to show a time exponent higher than that shown by system 2 within the same chip due to the fact that system 1 is operated at a voltage which is about 80 mV higher than that of system 2. Besides, the average temperature of sytem1 is about 13 degrees higher than system 2 due to the difference in the cooling.

On the other hand, the time exponent decreases at higher temperature under high voltages leading to saturation with stress time.

In the light of these findings, the degradation of digital circuits would be minimized if one could maintain time exponent under a certain threshold value. This is can be possible by keeping the stress voltage and temperature within certain limit. For the inverter, we have seen that if the oxide field would not reach 6.5 MV/cm and the temperature would not exceed 120 °C, the power law time exponent n would not exceed 0.1. Hence, in the latter case, it would require about 5 times longer, to reach the same degradation, than the case where the time constant is assumed to be 0.16 as in [31] for the power law exponent of digital circuits degradation due to NBTI. Thereby, the circuit' lifetime would be enhanced in the first case by lowing VDD.

On the other side, if lowering the supply voltage is not possible, then managing temperature profile would the only way to reduce the induced degradation. Either by cooling down the circuit to reduce the induced degradation during its on state (stress phase) or elevating its temperature during its off state (recovery phase) to accelerate its recovery and thereby compensate the induced degradation during stress phase. Thereby, the circuit lifetime would be enhanced.

V. Conclusion

An attempt to correlate circuit-level NBTI degradation with that of device-level using an AC NBTI characterization of the CMOS inverter DC response and temporal performance has been presented. The analysis of the inverter DC and temporal response has revealed that AC NBTI-induced degradation shows both voltage and temperature dependences with more than one acceleration factor for each. However, it does not unconditionally present stress time dependence. Actually, the time exponent is found to be governed by both voltage and temperature. Moreover, the induced degradation tends to saturate with both temperature and stress time.

Furthermore, circuit-level NBTI characterization has revealed a signature of the co-existence of more than one physical mechanism behind the degradation where the dominance of one mechanism over another depends on voltage, temperature and the stress time.

Finally, we think that if the circuit is kept operating under certain conditions, the NBTI-induced degradation of its temporal performance could be minimized and its lifetime enhanced.

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