# Evaluation of Hot Carrier Impact on Lateral-DMOS with LOCOS feature

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**Abstract:** Hot carrier stress is evaluated on a laterally diffused MOSFET (LDMOS) by TCAD simulation. Thedevice under test is obtained from process simulation under a 1µm CMOS flow available at CDTA. The n-typetransistor uses the LOCOS (local oxidation of silicon) and single RESURF (reduced surface field) features.Using the trap degradation model, degradation over time and different biases, the shift of threshold voltage $V_{TH}$,ON-state resistance $R_{ON}$, saturation current $I_{Dsat}$, and device lifetime are extracted. The shifts were foundto be manageable, they have a single process mechanism and are due to hot electrons in our case. But, flickernoise assessment under the same stress shows noticeable instabilities.

**Keywords:**LDMOS, Hot Carrier Stress, LOCOS, Flicker noise

## 1. INTRODUCTION

LDMOS transistors are an essential component of modernhigh voltage (HV) and RF circuits. It is a standard becauseit presents a lot of flexibility from operatingconditions likevoltages, currents, andtemperatures [1]. LDMOS transistorsare also compatible with many process technologies,allowingmore integration [2], [3]. LDMOSdevices are present inextremely downscaledtechnologies like 22nm, as well as incircuits that use large feature sizes like 1µm [4], [5].

The characterization of hot carrier injection (HCI) by TCADsimulation depends heavily on the sizing of the transistor, thusan adequate selection of physical models is obligatory. Manyrecent papers use degradation models that take into accountsingle-particle (SP) and multiple-particle (MP) processes todescribe the bond breakage andthe interface trap formation,which is often found in scaled-down devices [6]. Some otherworks solve the full-Boltzmann equation (full-band Monte-Carlo), but it is computationalheavy [7]. In our case, thedevice under test is an n-type LDMOS obtained from the1µm CMOS technology [8], [9]. It has been proventhat HCIfor such devices is primarily induced by hot electrons [10].Therefore, we modeled the HCI using the trap degradationmodelavailable in SentaurusSdevice [11].

As the amount of power carried by an RF analog signalis significant, it is necessary toevaluatethe degradation. Inpractice, the RF signal is held at the cutoff frequency fora prolonged stress time, then trace the outputcharacteristic[12]. But in simulation, and due to the complexity of thephysical models required, we encountered few convergenceissues. Thus, we proceeded to quasi-staticstress, that is aDC stress followed by RFevaluation.

Flicker noise, also called *1/f* noise, found approximatelyin 100KHz to 1MHz, also relates to the $Si/SiO_2$ interface.One of the core assumptions about its mechanism is thatrandom trapping/detrapping of charges induce carrier densityfluctuations, which in turn translates into flicker noise powermodulation [13], [14]. Flicker noise is calculated using theimpedance field method [15], where diffusion, trapping, andgeneration-recombination noises are declared at once. Fromthe extracted power spectral densities (PSD) andnoise correlationcoefficients ($C_i$), we have been able to evaluate the impactof HCI on flicker noise generation after various stress times.

This paper is organized as follows. In sectionII, we describethe device's technological parameters relevant to this research,physical models, and inputparameters. SectionIII includes DC and AC results after stress. We conclude the paper insectionIV.

## 2. SIMULATION SETUP

The 2D structure is obtained using Sprocess tool [16],where a CMOSprocess flow is used. The process usesa 1µm technology node that is available atCDTA [8], [9]. TheLOCOS separation technique is used as a field oxide above thedrift region, as shown in Fig. 1. The source and the body areshorted tosuppress bipolar effects, that rise from theparasiticBJTs.

During the process simulation, at the LOCOS growth step, we used agas mixture of $H_2O$, $O_2$, $H_2$, $N_2O$, and $N_2$ of partial pressuresof 0.5, 0.5, 0.2,1, and 1 respectively. The LOCOS thicknessis 787 nm, the gate oxide thickness is 15nm. The $N_2O$ datasetis saved for later use during the degradation simulation.

To evaluate the device using Sdevice tool, we used forglobal physics Fermi statistics to accurately model highlydoped regions. Also, we chose the thermodynamic transportmodel to solve for the lattice temperature, and a device widthof 1µm is set using the area factorfunction (not actual 3D).For Silicon, we modeled the mobility using the inversion andaccumulation layer mobility model, coupled with the Hänschmodel for high-field saturation [17]. For recombination,we used Shockley–Read–Hall with doping and temperaturedependence, Auger, and avalanchegeneration as well as theSlotboom model for the bandgap narrowing [18].

It has been reported, via simulations and experiments, thathot electrons are the main cause of HCI degradations innLDMOS devices that use the LOCOS feature [7]. While aMonteCarlo simulation, that solves the full Boltzmannequations,is the most accurate, the well-calibrated trap degradationmodel is less computationally expensive. Thus, it is used tomodel the degradation at the $Si/SiO_2$ interface.

The $Si/SiO_2$ interface is passivated usinghydrogen. Afterstressing the device,depassivation occurs, leaving Si danglingbonds, which are responsible for trapformation. After earlydepassivation, theremaining Si-H bonds $N_{hb}$follow thepower-lawdefined as:

$$N_{hb} = \frac{N_{hb}^0}{1 + (\nu t)^{\alpha}} \quad (1)$$

where $N_{hb}^0$ is the initial concentration of Si-H bonds, $\nu$is thereaction constant andis stress-dependent and varies between0 and 1.According to ab-initio density functionalsimulation[19], the detached hydrogen couldhave a negative charge.The accumulation ofsuch charges will change the electricpotential, dictating the afterward breaking.This phenomenonis formulated in equation 2,describing the activation energy:

$$\varepsilon_A = \varepsilon_A^0 + (1+\beta)kT\ln\left(\frac{N - N_{hb}}{N - N_{hb}^0}\right) \quad (2)$$

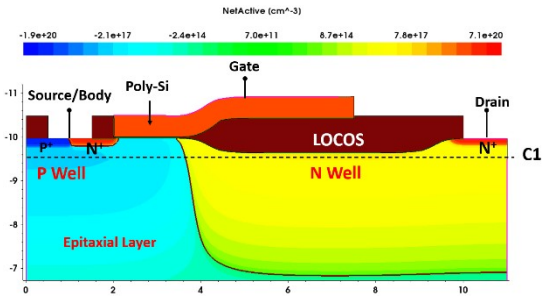


Fig. 1 Final structure net-doping profile.

where N is the total Si- Bonds, $N - N_{hb}$ is the concentrationof the released hydrogen. Thelast term represents the Si-H density-dependent change with a pre-factor (1+β). Inour simulation, we took intoconsiderationvarious reactionenhancementfactors such ashot carrier current andtunneling.Wesummarized the parameters ofthe traps inTable 1.

Table 1Input Trap Parameters

| Parameter | Properties |
|---|---|
| Initial trap concentration | 5e8 $cm^{-2}$ |
| Central energy of the trap distribution. | @ MidGap |
| Trap Type | Acceptor |
| Total silicon-bond concentration (maximum) | 5e12 $cm^{-2}$ |
| Critical trap concentration | 1e12$cm^{-2}$ |
| Passivation coefficient | 0 |
| Equilibrium activation energy of hydrogen on Si-H bonds | 0.2 |
| De-passivation coefficient | 1e-8 |
| Parameters of the electric field–dependent terms of the Si-H bond energy and the activation energy | (0 1.0 2e-3 0.33) |
| Parameters of the tunneling and hot carrier–dependent terms of the de-passivation constant | (1.0 1.0 6e6 0.33) |
| Fowler–Nordheimtunneling enhancementparameters for theDegradation model depassivation constant | (1e6 1.0) |
| Parameters of hydrogendiffusion in oxide | (2e-7 1e-15 0.05 1 1e13 15.0) |
| Gate Current | At the gate: Lucky and Fowler–Nordheim |

## 3. DEGRADATION RESULTS

### A. DC ANALYSIS

The first result to check is the evolution of the total generatedinterface traps over time. The gate and drain various biasvalues all fall under the device safe operating area (no drainon-state breakdown occurs). However, according to Fig. 2, theSOA could be more precisely defined. Meaning, we need toreduce the total number of interface traps ($N_{it}$), it must beas low as possible. We get such a case under medium gate and drain stress. In fact, under $V_{GS}$= 3V and $V_{DS}$= 10V, the$N_{it}$ curve is at the bottom. Although it is in the same orderof magnitude as in other conditions, the effect onlifetime issignificant.

Such a generation of interface traps could be acceleratedby ramping the device temperature it is the method usedexperimentally to avoid long stress times [20].The temperatureimpact on the device is manifested as a higher leakage current,higher threshold voltage, lower saturation current and as result,a lower transconductance, as shown in Fig. 3. Such distortion inthe characteristic of the stressed device will ultimately translateinto inferior RF performance than of a fresh transistor.Although the lattice temperature will rise, we kept the startingtemperature at 300K, as the DC stress is already exaggeratedthan a real-life condition.

The bond breakage from collisions with hotelectrons iscalled a single process (SP)mechanism. If the carriers werecold and yet bond breakage still happens, then it is calleda multiple process (MP) mechanism. We can firmly attributeour device degradations to energetic electrons because we arenoticing, on a logarithmic scale, a one-directional linear shiftin $V_{TH}$, $R_{ON}$, and $I_{Dsat}$ on Fig. 4,5, and 6respectively.If aMPmechanismwere tooccur, cold carriers will involve holesand not electrons. Trapped holes will create anegativemirror charge. By then, the shift willbe slow in small stresstimes, or change directionality [21].

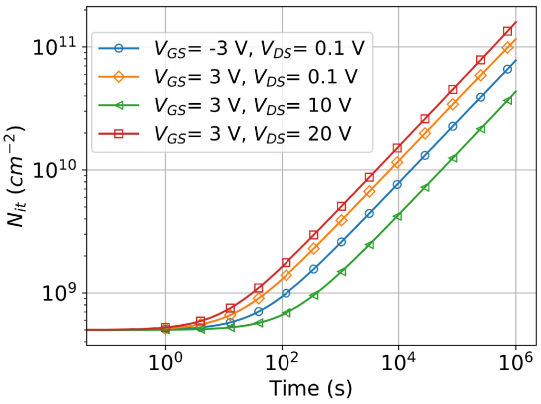


Fig. 2 Evolution of $N_{it}$ over time at $Si/SiO_2$ interface

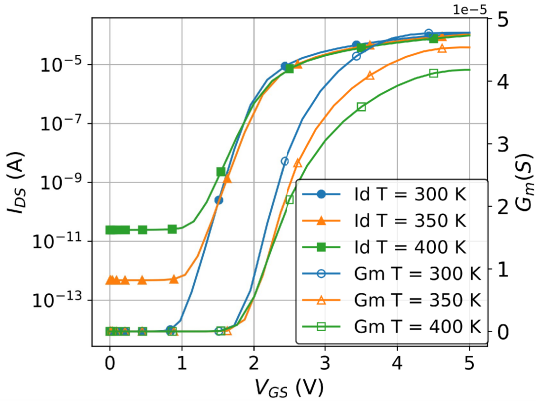


Fig. 3 Accelerated DC stress by device temperature ramping

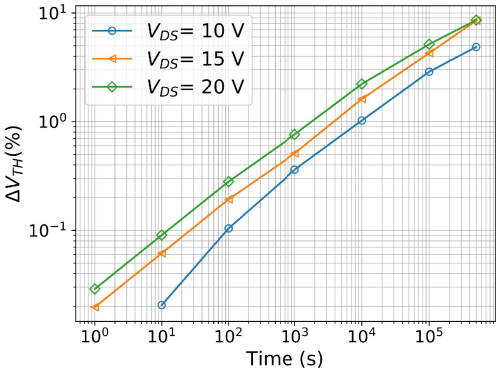


Fig. 4 Threshold voltage degradation over time under various drain stress biases

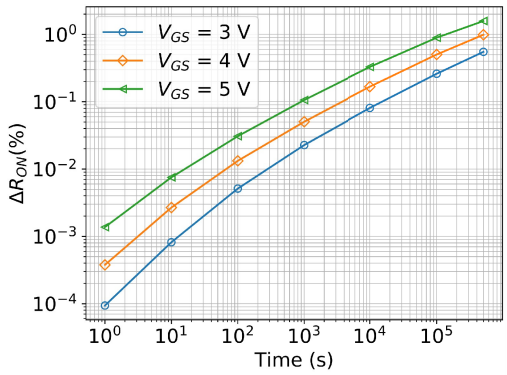


Fig. 5 ON-Resistance degradation over time under various gate stress biases

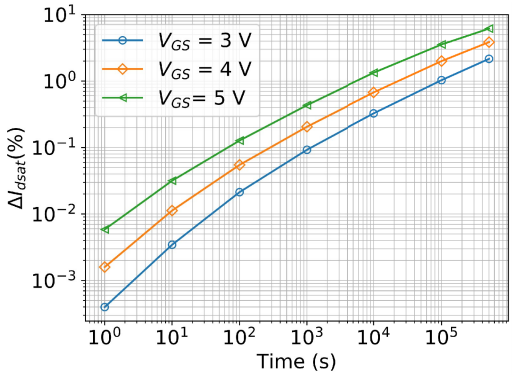


Fig. 6 Saturation current degradation over time under various gate stress biases

It is worth mentioningthat the $N_{it}$ value under low bias is still higher than$N_{it}$ undermedium bias as shown in Fig. 2, Theimpact of drain-inducedbarrier lowering (DIBL)on the amount of carrier scatteringand fluctuation in mobility is another potentialmechanismto explain this behavior. DIBL isoften tied to the size andlayout of the device.This paper does not present any scatteringformalism.

Technologically speaking, the uneven gate oxide and thegradually increasing LOCOS thicknesses are the cause of hotelectrons. However, it has been reported that the total amountof damage is similar to more advanced field oxides (FOX) suchas shallow trench isolation, even if the underlying mechanismis different [10].

The maximum electron temperature in Fig. 7, which clearly shows the bird's beak reaches the highest values, further supporting our assertion about thedamage location. Under high stress, up to 4300K is reached,and underSOA $V_{DS}$ values, e-Temperature is between 2500Kto 4000K.

Furthermore, we extracted the normal-field right under theLOCOS region, as shown in Fig. 8. Again, in low $V_{DS}$ bias,thedamage is situated under the right side ofthe channel, whilethe wider and higher valuepeaks are under the bird's beak. Afinalscreenshot of the electron temperaturedistribution under$V_{DS}$ = 30V and $V_{GS}$ = 8Vis also provided in Fig. 9. An estimation of the device lifetime is presented in Fig. 10. If weallow a 10% decrease from the peak lifetime, the drain voltagehas to be between 6.5 and 10V and the gate voltage should be3V. This way, we will achieve full inversion, prevent channelmodulation, thus reducing HCI. Any other bias conditionsmean improved performance and a shorter lifetime.

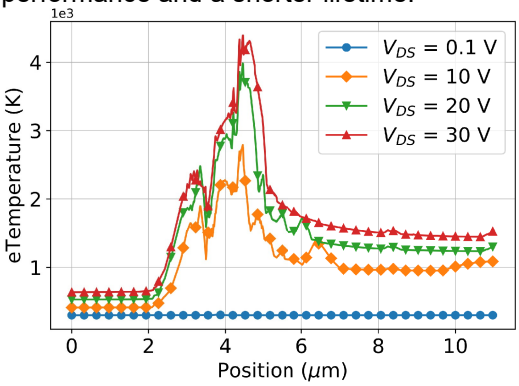


Fig. 7 Maximum electron temperature over the device with $V_{GS}$=8V

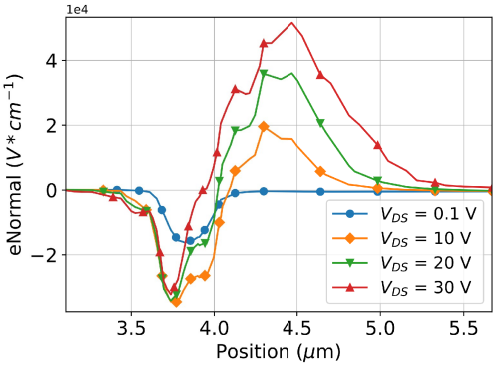


Fig. 8 e-Normal cut at C1 with $V_{GS}$= 8 V

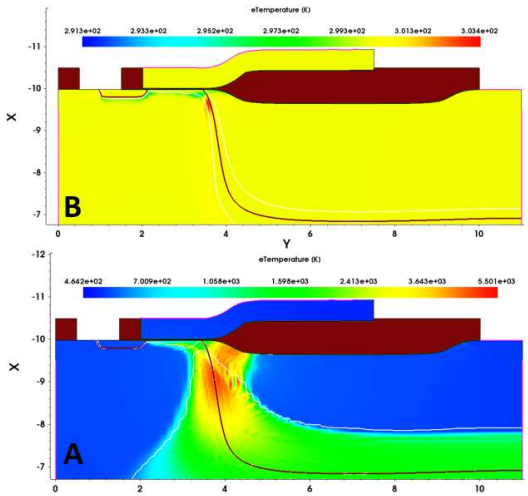


Fig. 9 Electron Temperature Distribution under $V_{GS}$= 8V, (A) under $V_{DS}$= 0.1V, (B) under $V_{DS}$= 30V.

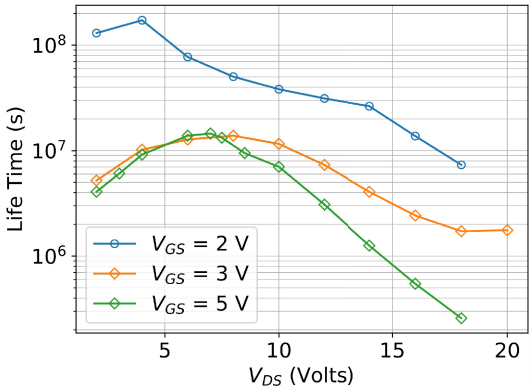


Fig. 10 Device lifetime as a function of drain bias under different gate voltages

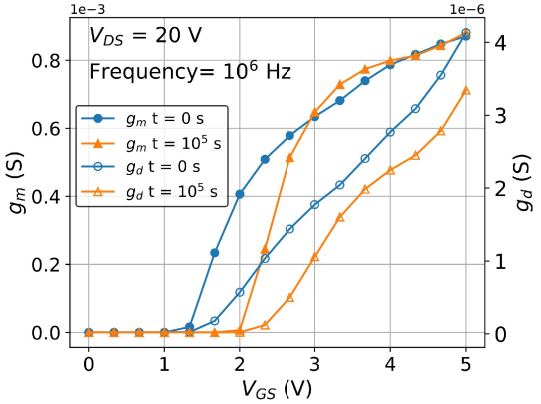


Fig. 11 Dynamic $g_m$and $g_d$evaluated for a fresh and stressed device under 1 Mhz

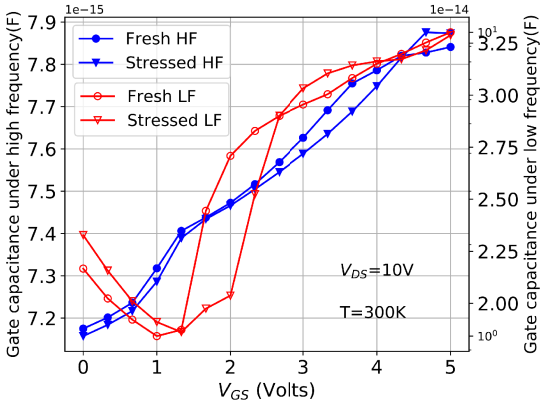


Fig. 12 Gate-togate capacitance evaluation after stress under LF and HF signals.

## B. AC ANALYSIS

In this section, due to the amount of powerRF signaldelivers, we chose thehydrodynamic transport model formore accuracy. For noise evaluation, we studiedthe impactof HCI with bulk flicker noise, with trapping, and diffusionnoise models activated for both carrier types [11], [15], [22].Fowler–Nordheim tunneling model is notincluded inthissection as it causes convergenceproblems.

The shifts in $V_{TH}$ and $R_{ON}$ entail shifts in transconductance($g_m$) and output conductance ($g_d$), respectively. We examinedthese parameters under 1Mhz, within the electrical SOA fora fresh device, and after $10^5$seconds. The results plotted inFig. 11 show a significant reduction in both parameters afterprolonged stress. Both of these parameters reflect already RFdegradation as they are decencies of the maximum oscillationand cut-off frequencies. Also,we examined the change inthe gate capacitance ($C_{gg}$) under both low (100MHz), andhigh frequencies (100Ghz) (frequencies where flicker noiseis absent), both before and after DC stress. The results areplotted in Fig. 12. Under HF, no change is observed, But, inLF,ΔVTH impact is directly observed. Nonetheless, noshift in the total capacitance value, especially after 4V. Thisresult justifies our focus on the next analysisof flicker noise.

All major DC and RF parameters are recapitulated in Table2. The most noticeable shift is thesubthreshold swing ($SS_{sat}$)at $V_D$=10V, which increased by 26% after $10^4$seconds.

Wealso noticed an increase in peak $f_{MAX}$ measured after a 10dBpower loss from the initial value. Along with thefluctuationsnoticed in the gate voltage atpeak $f_{MAX}$ ($V_{gfMaxPeakdB}$), andthe maximum oscillation frequency ($f_{MaxPeakfq}$),it is clear thattraps cause instability issues inthe AC regime. These results willbe used to build a SPICE model, to check how thoseshiftsimpact performance at the circuit level.

Table 2 Additional Noticeable DC and AC Shifts After Various Stress Times

| Parameter | After t=0s | After t=$10^3$s | After t=$10^4$s |
|---|---|---|---|
| $V_{tgmSat}$ (V) | 2.4 | 2.5 | 2.57 |
| $V_{tigmSat}$ (V) | 0.836 | 0.96 | 1.2 |
| $SS_{Sat}$ (mV/dec) | 127 | 128 | 171 |
| $g_{mSat}$ (S) | 8.59E-4 | 8.5E-4 | 8.47E-4 |
| $f_{tPeak}$ (Ghz) | 4.43 | 4.43 | 4.44 |
| $f_{MaxPeakdB}$ (Ghz) | 25.09 | 25.25 | 25.22 |
| $V_{gfMaxPeakdB}$ (V) | 4 | 4.33 | 3.33 |
| $f_{MaxPeakfq}$ (Ghz) | 23.36 | 23.61 | 23.5 |
| $V_{gfMaxPeakfq}$ (V) | 4 | 4.33 | 4.33 |

For the flicker noise AC sweep, after thesame DC stress, weramped down the voltages to 0V. Then, we biased the drainat10V and simulated the device from 0.1Hz to $10^{13}$Hz foreach gate bias point. Fig. 13illustrates the PSD of the gateand drain noise spectral densities ($S_{VG}$ and $S_{VD}$) for$V_{GS}$=3Vknowing that $P_{av}$ is calculated usingthe equation below [23]:

$$P_{av} = \int_{f1}^{f2} S_{v_n} df \qquad (3)$$

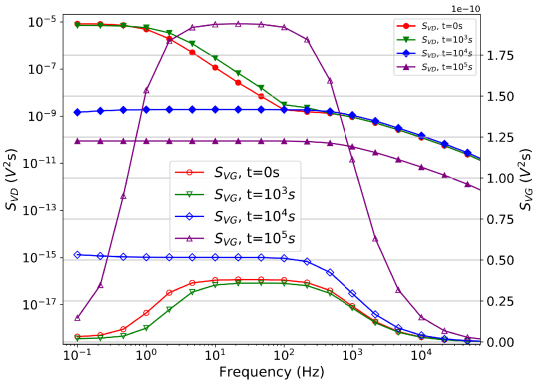


Fig. 13 Gate and drain voltage noise spectral density as a function of frequency after different stress times and $V_{GS}$ = 3 V during the RF sweep.

Practically, there is a direct correlation between the numberof interface traps and $S_{VG}$, corresponding to the theory whichstates that the origin of *1/f* noise is $N_{it}$. The channel surfacefluctuations, caused by the random trapping and de-trappingof the charges near the $Si/SiO_2$ interface,modulates thecarrier density. Although thistheory is backed by experimentalmeasurements, the value of $S_{VG}$ after $10^5$seconds remains tobe checked, as it could bebased on inconsistencies that relatethe value of the mobility after the band-gapnarrowing occurs,which in turn, influencesthe impedance field method (IFM)used in this simulation.

Finally, the noise correlationcoefficient ($C_i$) between thegate and drain noise current sources as a function offrequencyis calculated and plotted in Fig. 14.$C_i$ is defined as [23]:

$$C_{i_n v_n} = \frac{S_{i_n \overline{v_n}}}{\sqrt{S_{i_n} S_{v_n}}} \qquad (4)$$

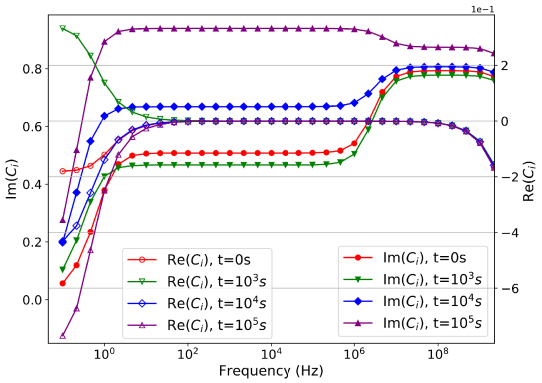


Fig. 14 Correlation coefficient between the gate and drain noise current sources as a function of frequency after different stress times and $V_{GS}$ =3 V during the RF sweep.

In LF, the real part of $C_i$ is practically null, as this is athermal channel noise, which produces “drain-channel” and“induced-gate” noise. Since LDMOS transistors generally havea long channel length, operate at highvoltages and temperatures,$C_i$ is more pronounced. The “gate-to-gate” and“drift-gate”capacitances are stronglyimpacted by the $N_{it}$ build-up.

According to Fig. 13 and 14, *1/f* noise isnoticeably sensitiveto HCS [24]. This evaluation helped us to choose thebest-operatingconditions, not only electrically,but also the bestfrequency band. Since thefinal application of this transistorwill be for broadband RF amplifiers and/or microwaveoscillatorsthis characterization is required.Besides, it could serveas verification ofinterface states results obtained from chargepumping measurements as done in [25].

Practical solutions to avoid flicker noisedepend heavily onthe final circuit application and requirements. If the circuitallows a discrete LDMOS, then a different process flow is theeasiest solution. Otherwise, a designer can change the circuitto depend on a pLDMOS rather than an nLDMOS, as it willexhibit one-tenth the amount of flicker noise [13]. It is alsoimportant to note that avoiding flicker noise by operating inweak inversion regimes is not advised as we pointed out thatlow bias not optimal for the device lifetime.

## 4. CONCLUSION

In this paper, an adequate evaluation of the SOA of an nLDMOS is carried out. The DC hot carrier stress allowed us to extract the best electric bias conditions and subsequently obtaining the longest lifetime.

The gate and drain voltages mustremain under medium values.

Also, we report that flicker noise is more sensitive and undergoes a more noticeable shift. Thus, we proposed practicalsolutions to reduce such degradation such as using a different process flow or opting for a p-type LDMOS.

Electrothermal simulations are not sufficient for the final determination of the SOA, because many degradation phenomenasuch as bias temperature instability and electromigration willalter. Furthermore, the characteristics, which are a subject forfuture studies.

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