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Title:

Design of a Digital PI Controller for a Power Factor Correction Boost Converter

Presented by:

- **BENSIDI AISSA Elyes**
- **MOUDOUD Adel**

Supervisor:

Dr. Razika Boushaki

Registration Number:……/2019

Abstract

The Power Factor Correction (PFC) is an important stage for the boost converter. Its controller is among the most complex with its two-loop structure and multiplier/divider. This project studies the design method of both analog and digital control for a PFC boost converter using Continuous Conduction Mode (CCM). The effectiveness of the solution is verified by simulation.

Dedication

To those who cared and still care, who loved and still love, who supported and still support. To our parents who were a constant source of inspiration.

Acknowledgements

We would like to express our sincere appreciation to our supervisor Dr. Boushaki R. for her guidance, encouragement and continuous support.

Table of Contents

List of Tables

List of Figures

List of Abbreviations and Acronyms

PFC	Power Factor Correction
CCM	Continuous Conduction Mode
PF	Power Factor
SMPS	Switch Mode Power Supplies
THD	Total Harmonic Distortion
DSP	Digital Signal Processor
AC-DC	Alternating Current – Direct Current
LPF	Low Pass Filter
DC	Direct Current
EMI	Electromagnetic Interference
LF	Low Frequency
DCM	Discontinuous Conduction Mode

Introduction

There are inherent mechanisms in diode rectification systems which cause these systems to produce severe distortion of the input current and, consequently, a poor power factor (PF). These problems arise because the rectifier diodes are backward biased for a large amount of the line voltage period. This leads to the fact that the current is only drawn when the instantaneous input voltage surpasses that of the output capacitor. Thus, the current will be a “pulse” which is centered around the peak value of the input voltage, this current pulse will act to charge the capacitors. Moreover, the output voltage is directly proportional to the input peak voltage and as such disturbances in the input voltage will be reflected in the output voltage.

Problems with diode rectification may be alleviated by using an active Power Factor Correction (PFC) circuit after the diode rectification bridge - typically a boost converter is used. There is also a possibility to introduce the PFC directly into the rectification bridge.

This circuit is controlled so that the inductor current follows a sinusoidal reference to produce an input current which is in phase with the input voltage; thus, emulating the subsequent circuitry as a resistor to the power source. Another great benefit of this set-up is that the output voltage of the rectifier is being controlled independently of line voltage. Previously, PFC-circuits have been incorporated in Switch Mode Power Supplies (SMPS) - e.g. computer power supplies - and these are operated at public grid frequency of 50/60 Hz. These systems have been implemented with varying sophistication depending on cost and application. Cheap consumer electronics may have better displacement power factor but with a relatively high distortion of input current; however, some sensitive electronics may be more sophisticated to reduce harmonics to a very low level (THD < 5%).

Chapter 1 Generalities on PFC boost converter

1.1 Introduction

The increasing popularity of switched-mode power supplies to fulfill effectiveness and performance goals has been met with the growth of industry legislation and recommended practices for power quality assurance (e.g., IEC 61000-3-2). The generation of harmonic content induced by non-linear loads is an undesirable side effect to the conversion of electrical energy, it can cause serious problems, such as damage to cabling and other equipment within networks as well as overheating and fire risk, high voltages and circulating currents, equipment malfunctions and component failures, etc. To overcome these problems, we will discuss the design process of a digital controller for an active Power Factor Correction (PFC) boost converter.

1.2 Design Specifications and Goals

There are some design specifications that has to be taken into account to be able to design the controller in a suitable way. These specifications involve what output power levels are desired, output voltage and input voltage range, etc.

Design criteria for this system involve working towards a Total Harmonic Distortion (THD) of less than 5%, a Power Factor (PF) of more than0.93 andan overall efficiency of above 90%.

Table 1.1 Power stage specifications

Input AC Voltage	$85 - 265\ V_{ac}$
Input AC Frequency	$50 - 60\ Hz$
PFC Output Voltage	$390\ V$
PFC Output Power	$1.8\ kW$
PFC Switching Frequency	$100\ kHz$
Output Filtering Capacitor	$1.68\ mF$
Boost Inductance	$170\ \mu H$

1.3 Purpose and steps

The purpose of this project is to design and study both the performance of analog and digital control for a PFC boost converter. Plus, the digital implementation of the controller using a DSP (Digital Signal Processor).

Chapter 1 is the General introduction to this project; it provides a summary of the background of this work. Detailed design specifications are listed and project outline is also given.

Chapter 2 surveys some power quality theories, PFC types, PFC topologies briefly and the PFC boost converter topology with more details, in addition to small-signal model of the boost-type PFC AC-DC (Alternating Current - Direct Current) Converter.

Chapter 3 covers the control strategies and the procedures applied to design the current loop, and the voltage loop, for both, the analog and the digital controllers.

Chapter 4 describes and discusses the design results for both the analog and digital controllers PFC converter, simulations performed using MATLAB Simulink. At the end of this chapter, details results, analysis and discussions are presented.

Finally closes the Project by the conclusions. Several suggestions for future research are also included in this chapter.

Chapter 2 Power Stage Background

Most of the studies on the power factor correction for the nonlinear loads is mainly associated to reducing the harmonic content present in the input line current. There are several methods are present in order to get power factor nearly equal to unity or unity in the input side. The distortion in the shape of the input current can be again improved by the use of LPF (Low Pass Filter) in the input and output sides. There are several PFC techniques we can use to achieve unity power factor. Depending on whether controlled-switches using an external control signal are used or not, these techniques are divided as "Active PFC" and "Passive PFC". As a sign of the great importance of regulating the line current harmonic content of any equipment connected to the grid, The Committee of European for the Electro technical Standardization – CENELEC mandated the IEC 555-2 standard followed by the IEC 1000-3-2 standard and European EN 61000-3-2 standard [1], [2].

2.1 Power Quality

Power quality is an important concept in the design and analysis of AC-DC converters, and is the primary motivation behind this Project. In this section, an overview of total harmonic distortion (THD) and power factor (PF) is presented. In addition, the relationship between THD and power factor, as well as the negative effects of low power factor on power systems are shown.

2.1.1 Total Harmonic Distortion

THD is defined as the ratio of the non-fundamental rms components to the fundamental rms component. The total harmonic distortion for current is given by equation (2.1).

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} I_{n,rms}^2}}{I_{1,rms}} \qquad \text{Equation 2.1}$$

Requirements and regulations for the line voltage THD are strict, and a voltage THD of only 10% can cause problematic interactions with sensitive loads [3]. Since the power

system supply voltage is generally well regulated and has minimum distortion, it isreasonable to assume that the input voltage is perfectly sinusoidal to simplify analytical techniques. Input current THD however, can easily exceed 100% depending on the load and converter in use.

2.1.2 Power Factor

The ratio of real power P to the magnitude of apparent power S is defined as power factor. Real power contributes to actual work through the transfer of energy. A heater, for instance, generates heat purely through real power. Apparent power is a scalar quantity and is the product of the rms current, I_{rms} and rms voltage,V_{rms} as given in equation (2.2). If a load is purely resistive and consumes all transferred energy, its apparent power would be equal to its real power. However, if apparent power is not equal to real power, there exist energy storage devices, such as capacitors and inductors, storing and releasing energy during the energy conversion process. In such cases, a byproduct is incomplete net energy transfer to the load.

$$S = I_{rms}V_{rms} \qquad \text{Equation 2.2}$$

Power factor provides a dimensionless measure of useable energy efficiency, with values constrained between zero and one, this relation is shown in equation (2.3). When the sinusoidal source voltage is perfectly in-phase with the sinusoidal source current, as in Figure 2.1 [4], the power factor is unity.

$$PF = \frac{P}{S} \qquad \text{Equation 2.3}$$

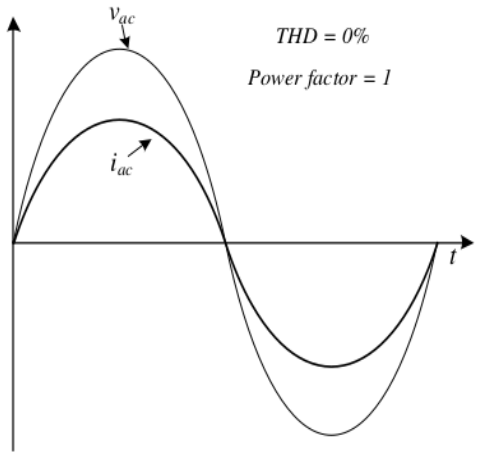

Figure 2.1 Ideal input current and voltage with unity power factor and no current distortion

With unity power factor, the current drawn from the source is minimized and the load appears purely resistive from the input source, thereby enabling maximum power transfer capability. Practically, unless the load is purely resistive, unity power factor is impossible, but power factors exceeding 0.99 are achievable. If a normally non-sinusoidal load, such as a computer power supply, is controlled to draw a sinusoidal load current, this control method is called power factor correction (PFC).

There is a direct relationship between total harmonic distortion and power factor: a term called the displacement factor that relates the fundamental current phase φ_1, to the fundamental voltage phase θ_1, is defined by equation (2.4). In addition to the displacement factor, a term called the distortion factor, which relates the fundamental rms current to the total rms current, is defined by equation (2.5).

$$displacement\ factor = \cos(\varphi_1 - \theta_1) \qquad \text{Equation 2.4}$$

$$distortion\ factor = \frac{I_{1,rms}}{I_{rms}} \qquad \text{Equation 2.5}$$

The definition of power factor is the product of the displacement and the distortion factors, as given by equation (2.6), and with no DC current component, as given by equation (2.7).

$$PF = (displacement\ factor)(distortion\ factor) \qquad \text{Equation 2.6}$$

$$PF = \left(\frac{1}{\sqrt{1+(THD)^2}}\right)\cos(\varphi_1 - \theta_1) \qquad \text{Equation 2.7}$$

2.2 PFC Circuits Types

There are several methods to reduce the harmonic contents of the line current in single-phase systems. The classification of single-phase PFC topologies is shown in Figure 2.2 [2].

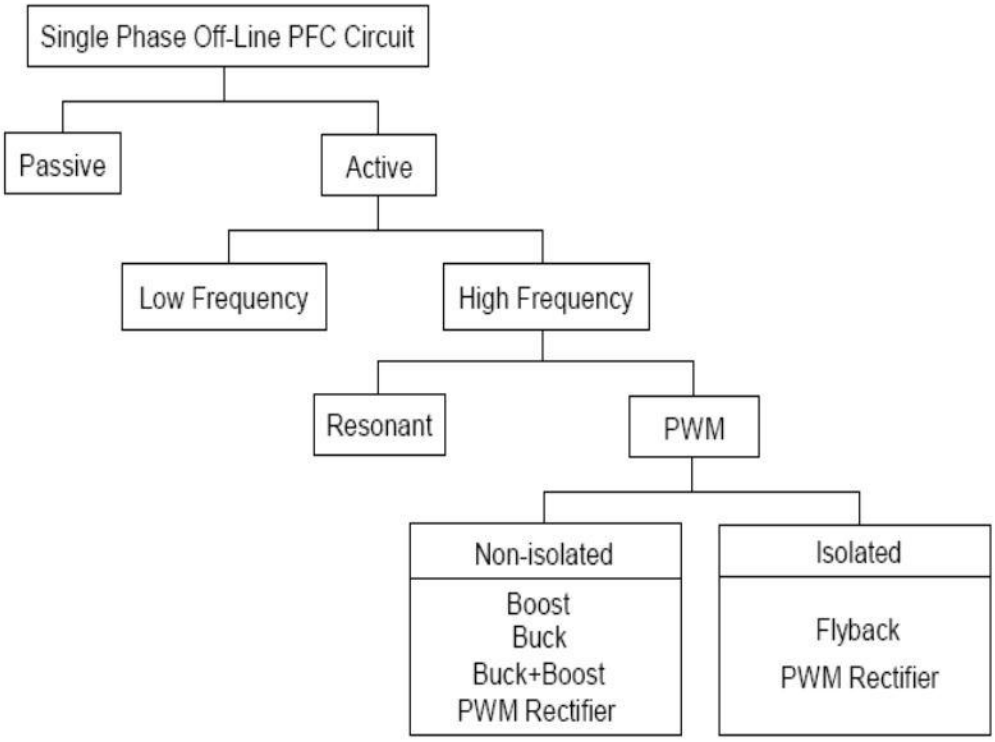

Figure 2.2 Classification of PFC single-phase topologies

2.2.1 Passive PFC

In this circuit type, only the passive elements are being used along with diode bridge rectifier in order to improve the power factor and shape of the input line current. Using this PFC circuit type, input power factor of the system can be increased from the value of 0.7 to 0.8 nearly. The size of the PFC circuit and its cost will increase according to the increase in the input supply-voltage. The main objective of the PFC is filtering the input current harmonics in line current. These current harmonics can be filtered using LPF by only allowing the fundamental component to pass and blocking all the other harmonics to improve the power factor. Using the passive PFC, current harmonics can only be decreased to a certain limit and the power factor cannot reach a value near unity. The output voltage cannot be controlled in this PFC type [2].

Figure 2.3 below presents a passive PFC circuit.

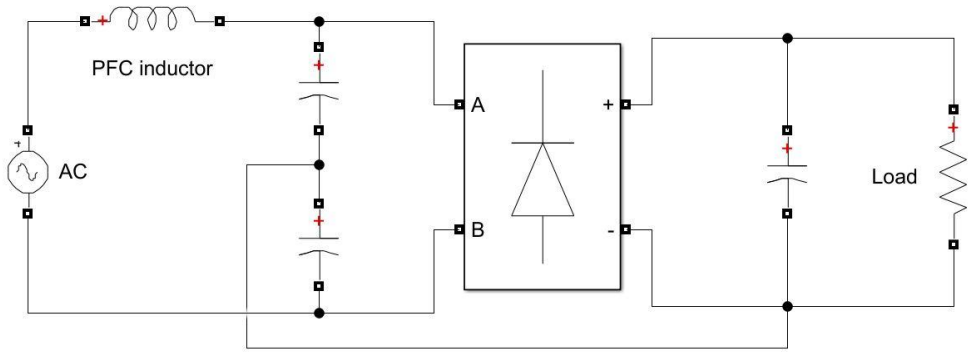

Figure 2.3 Passive PFC circuit

Advantages

- Simple in structure.
- More reliable and rugged.
- Equipment's used in passive PFC will not generate high frequency EMI [5].
- The cost required to process this method is very low.
- High frequency switching losses are not present in this method and it is insensitive to noise and surges.

Disadvantages

- Bigger filter size.
- Dynamic response of the system is very low.
- Output voltage control is difficult and it is not possible.
- As inductors and capacitors are present in the circuit, there will be a chance of interaction between the elements in the circuit.
- With the use of filters in this method, harmonics can be decreased but the fundamental component of the line current will shift its phase from the original one [6].
- The load connected to the system decides the shape of the input line current.

2.2.2 Active PFC

An active PFC circuit is designed to control the power drawn by the load from the power supply and to rise the power factor to near unity. Active PFC designed for power factor improvement operates by making the current drawn by the load follow the source voltage. The components used in this circuits type are strictly chosen to correct the shape of the input current waveform, to eliminate the phase between the input current and voltage, and to get an almost-constant output voltage. According to the frequency of switching, the active PFC solution can be divided into two classes [6].

2.2.2.1 Active Low Frequency PFC

Active low-frequency (LF) PFC circuits operate at a switching frequency of twice the line frequency, 100 or 120 Hz, and in synchronism with it. This method uses an active switch, a LF inductor, and a control circuit to perform PFC [7].

2.2.2.2 Active High Frequency PFC

In this class of circuits, switching frequency is greater than the line-frequency, 20kHz to 200 kHz [6]. The power factor value obtained in this circuit is more than 0.9. And further, the value of power factor can be increased to a higher value to reach unity, this can be achieved by adding some filtering elements to the circuit [8]. With the active

PFC circuit, the size of the circuit is smaller comparing to a passive one. Harmonics in this case are decreased to the lower values.

Advantages

- Power factor ≥ 0.95
- Small system size and power factor value can reach approximately unity.
- Decreases the harmonics to lower values.
- Wide range of input voltages.
- Greater flexibility and control

Disadvantages

- Design of this system is more complex than the passive PFC.
- Higher overall cost [9].

2.3 Single-Phase Power Factor Correction Topologies

While not technically being a "topology" there is still a way of improving the power factor of the diode bridge rectifier using passive components on the input, namely inductors and capacitors. The addition of an inductor on the ac-side helps to increase the power factor by making the current waveform better; however, the resulting power factor is not perfect [10]. By only providing passive power factor correction, the output voltage remains uncontrolled and dependent on the input voltage. To make the output voltage controllable, there are some different topologies that can be used depending on the need of either increasing or lowering the output voltage.

The buck-converter topology in Figure 2.4 works in a way that it decreases the output voltage compared to the input voltage. Due to the criteria of having an input voltage greater than the output voltage to work properly, this makes the buck-topology a bad choice for a pre-regulator because of the inability to work in the skirts of the half input sine wave having V_{in} less than V_{out}. On the other hand, having a buck converter connected after for example a boost pre-regulator makes it a great choice for lowering the "constant" DC voltage or providing a current limiting feature [11].

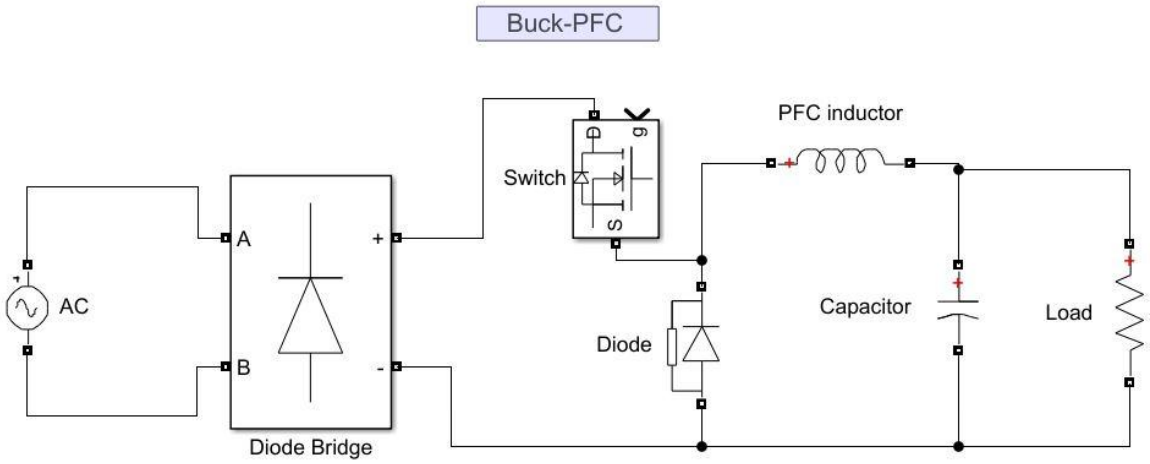

Figure 2.4 Buck PFC converter circuit

Compared to the buck converter, the boost converter in Figure 2.5 boosts the output voltage compared to the input voltage. The Boost-PFC topology is the most used and preferred topology in PFC circuits and one of the reasons to this is the ability to control the input current. Criteria's for making a boost converter work in a convenient way is that the output voltage is higher than the input voltage. If the circuit is constructed in such a way that the output voltage exceeds the maximum peak of the input voltage it will be able to work in the full range from zero to max peak value. Due to the ability to work at high power levels and the possibility to use current mode control to program the input current half sine wave, it makes the boost topology a popular choice. If the converter works in Continuous Conduction Mode (CCM), the inductor and input current will always be continuous, helping to reduce input current harmonics. If there is a need to have lower voltage levels it is often popular to have a buck converter connected in series with the boost to make this transformation instead of having a buck right from the start. The only drawback of the boost topology is that it does not have a switch in series between the input and output, therefore it is unable to limit the input current. This means overload and/or startup currents cannot be controlled. Also, if the input voltage surpasses that of the output voltage the converter is unable to control the current as the diode will be forward biased and the current will flow continuously [12].

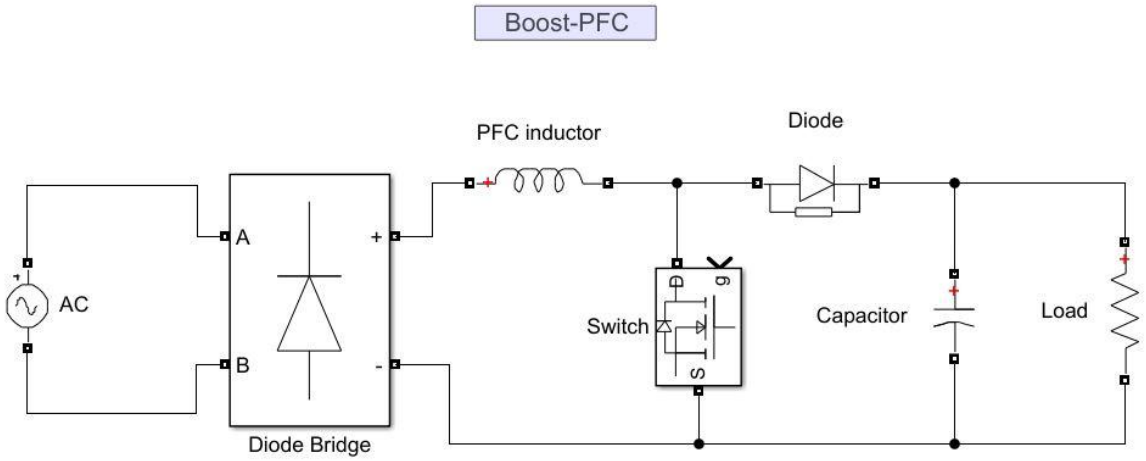

Figure 2.5 Boost PFC converter circuit

When it comes to the feature of being able to create either a higher or a lower output voltage compared to the input voltage, there are some different converters that can be used. This can come in handy when there is a special need for the circuit to be able to do both conversions without using two different converters connected in series. Two common converters are the buck/boost converter and the flyback converter. The mentioned features make these topologies viable choices compared to only a buck or boost. The basic concept of the two is the same but they are constructed in two different ways that will be described further down. Examples of simple schematics that are most common for the converters are shown in figures 2.6 and 2.7 below.

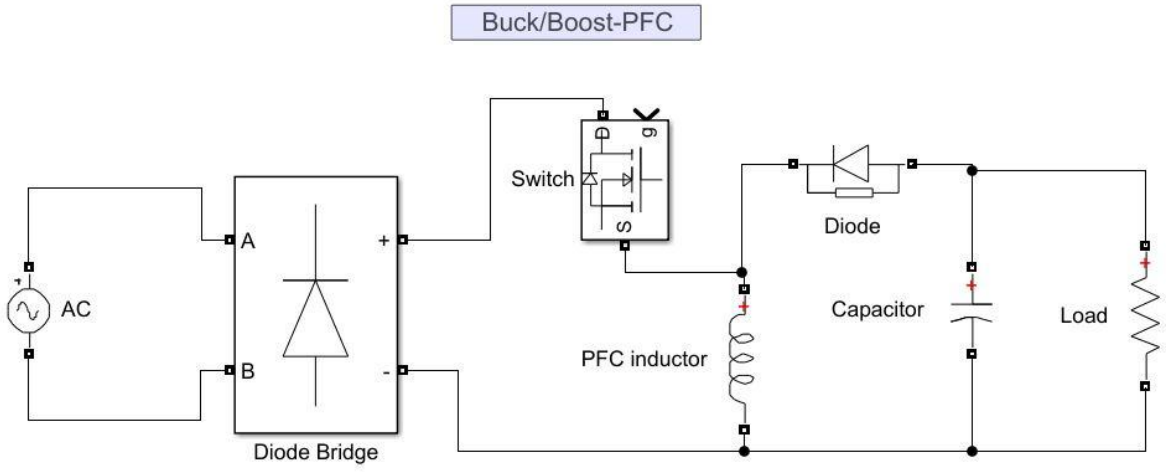

Figure 2.6 Buck/Boost PFC converter circuit

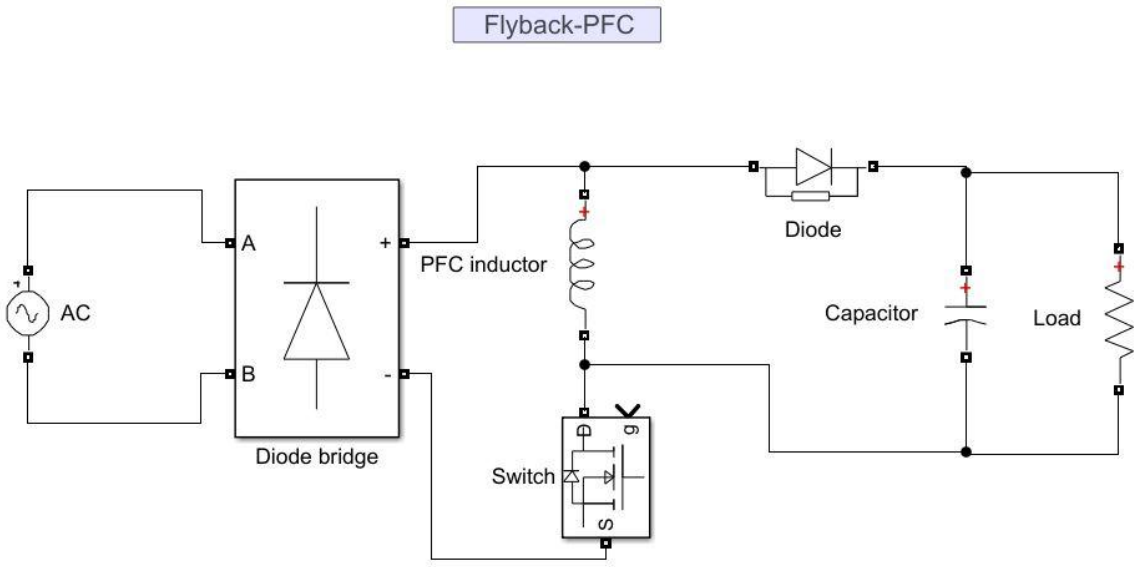

Figure 2.7 Flyback PFC converter circuit

Several different approaches are possible when constructing buck/boost and flyback converters. In the buck/boost case, there are versions where two switches are used instead of the conventional single-switch topology, there are also some topologies involving magnetic isolation, i.e. there is a galvanic isolation between the input and output sides. Also, flyback converters have the advantage of having low cost and galvanic isolation of the voltage. It is also able to both regulate the output voltage both up and down as mentioned making it a competitive choice when choosing converter topologies for power factor correction. While working under optimal conditions, flyback converters have high efficiency, and that is when power levels$< 500\,W$. For applications using higher power levels, it is required to use parallel devices. To achieve this, there is also a need to use the right control algorithms, the optimal controller to drive this circuit is the DSP [13].

The buck, buck/boost and flyback topologies have discontinuous input current due to the fact that there are switches in series with the power line. However, the boost-topology can have an input current in both CCM and DCM. The ability to operate in CCM makes the boost-topology the most viable option of the mentioned topologies for high performance power factor correction circuits.

2.4 The Boost Power Factor Correction Topology

As discussed in the previous section, the boost PFC-topology has the ability to control the input current in continuous conduction mode.

2.4.1 Theory of the Boost PFC Topology

The boost converter functions as a variable AC transformer, but for DC voltages. With a boost converter though, it is only possible to output a higher voltage. An electrical diagram of an ideal boost converter is shown in Figure 2.8.

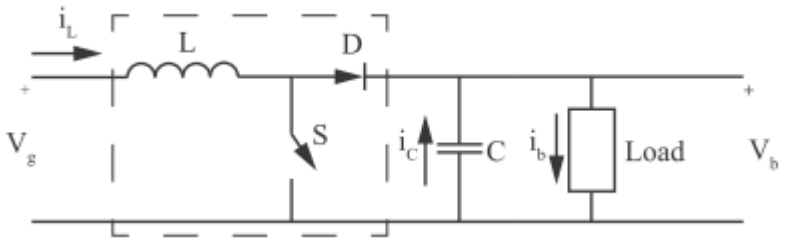

Figure 2.8 Electrical diagram of an ideal boost converter

Where:

- V_g is the rectified grid voltage.
- V_b is the output from the boost converter (the outputDC voltage).
- $S$is a switch.
- i_L is the inductor current.
- i_C is the capacitor current.
- i_b is the load current.

The switch is assumed to switch instantaneously. This yields to two electrical diagrams, one with the switch on and the other one with the switch off. The two diagrams are shown in figure 2.9. The inductor, switch, diode and capacitor are not considered ideal and thereby each have a resistance, as seen in figure 2.9.

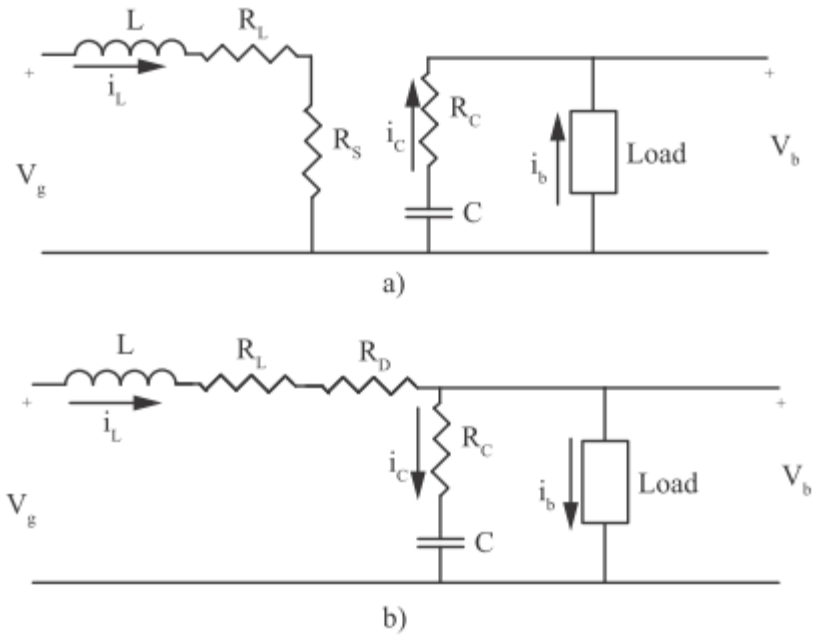

Figure 2.9 Electrical diagrams of a boost converter. a) the electrical diagram with the switch on, and b) with the switch off

In figure 2.9 a), the switch is on,thereby the on circuit is modeled by these governing equations:

$$V_g = L\frac{di_L}{dt} + R_L i_L + R_s i_L \qquad \text{Equation 2.8}$$

$$V_b = v_C + R_C i_C \qquad \text{Equation 2.9}$$

$$i_C = -i_b \qquad \text{Equation 2.10}$$

$$v_C = \frac{1}{C}\int i_C dt \qquad \text{Equation 2.11}$$

The off circuit is shown in figure 2.9 b). The governing equations for the off circuit are thereby, equations 2.12, 2.13, 2.14 and 2.15.

$$V_g = L\frac{di_L}{dt} + (R_L + R_D)i_L + V_b \qquad \text{Equation 2.12}$$

$$i_L = i_C + i_b \qquad \text{Equation 2.13}$$

$$V_b = v_C + i_C R_C \qquad \text{Equation 2.14}$$

$$v_C = \frac{1}{C}\int i_C dt \qquad \text{Equation 2.15}$$

2.4.2 Small-signal Model of the Boost Type PFC AC/DC Converter

To understand the relation between current compensator and power factor, a small-signal model for the frequency range (twice line frequency ~ 1kHz) is necessary. While a quasi-static small signal model is not valid for frequency range around line frequency, [14] derived a small-signal model for this frequency range. For low frequency range, the relation between current compensator and input voltage might be explained by this model.

2.5 Circuit Analysis for Discontinuous Conduction Mode

The only difference in the principle of discontinuous mode as compared to the continuous mode is that the inductor is completely discharged at the end of the commutation cycle. In this node of operation before the switch in the circuit is opened the inductor current value reaches zero. This kind of case happens when the energy to be transferred is very small and the process of transfer requires a time period less than the commutating time period. We can see the waveforms in Figure 2.10 [15].

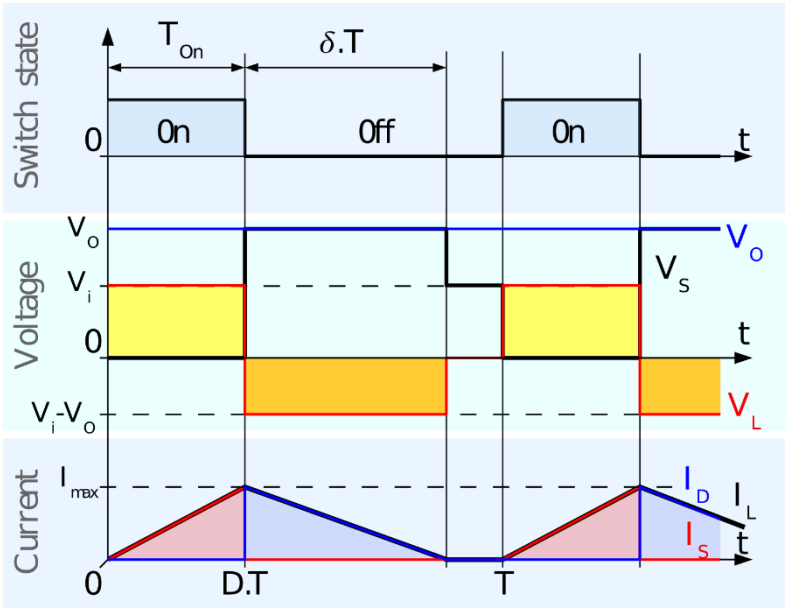

Figure 2.10 Waveforms of current and voltage of a boost converter operating in discontinuous conduction mode

2.6 Circuit Analysis for Continuous Conduction Mode

During continuous mode of operation of a boost converter, the inductor current $I_L$never becomes zero during a commutation cycle. We can see the waveforms in Figure 2.11 [16].

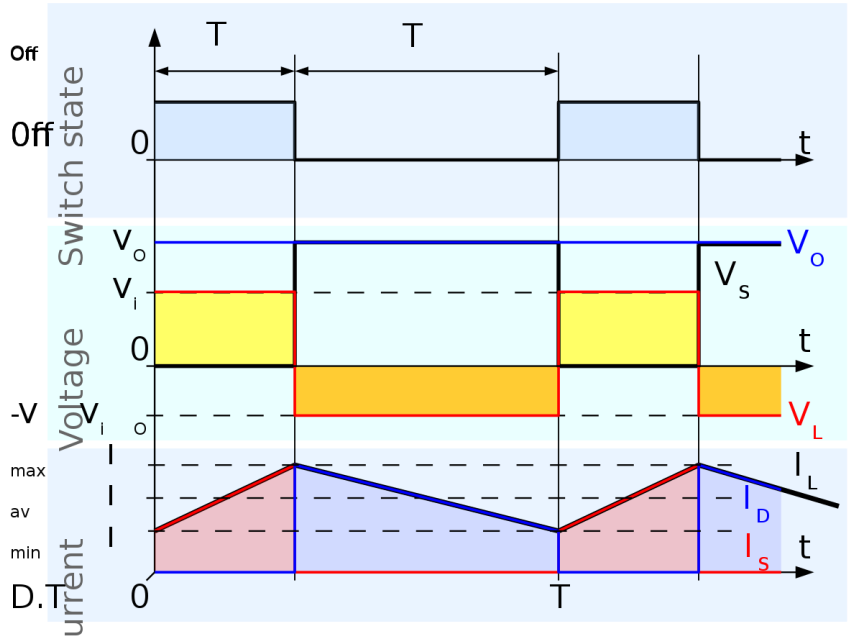

Figure 2.11 Current and voltage waveforms of a boost converter operating in continuous conduction mode

The switch (MOSFET) is closed to start the On-state. This makes the input voltageV_L appear across the inductor, and that causes change in inductor current I_L during a finite time period Δt which is given by the formula:

$$\frac{\Delta I_L}{\Delta t} = \frac{V_i}{L} \qquad \text{Equation 2.16}$$

When the On-state reaches its end, the total increase in I_L is given by:

$$\Delta I_{L_{on}} = \frac{1}{L}\int_0^{DT} V_i dt = \frac{DT}{L} V_i \qquad \text{Equation 2.17}$$

Where $D$is known as the duty cycle, i.e. the ratio of time period for which the switch is on and the total commutating time period T. Therefore, D has a value between 0 (indicates that S is never on) and 1 (indicates that S is always on).

When the switch is made open, the converter operates in Off-state. During that time period, the load serves as a path for the inductor current. If voltage drop in the diode is neglected or assumed to be zero, and the capacitor is taken to be large enough for maintaining a constant voltage, the equation of I_L is given by:

$$V_i - V_o = L\frac{dI_L}{dt} \qquad \text{Equation 2.18}$$

During the time period for which the converter remains in Off-state, the change in I_L is given by:

$$\Delta I_{L_{off}} = \int_0^{(1-D)T} \frac{V_i - V_o}{L} dt = \frac{(V_i - V_o)(1-D)T}{L} \qquad \text{Equation 2.19}$$

We find out too that:

$$D = (1 - \frac{V_i}{V_o}) \qquad \text{Equation 2.20}$$

From the above expression, it is observable that the output voltage is always greater than the input voltage (as D is a number between 0 and 1), and that it increases as D increases. Theoretically, it should approach infinity as D approaches 1. For this reason, boost converter is also known as step-up converter [13].

2.7 Control Techniques

Control techniques for DC-DC converters are well-established and mature. Although numerous control approaches have been published in the literature, two main control strategies can be identified: voltage-mode control and current-mode control [8-9].

2.7.1 Voltage Mode Control

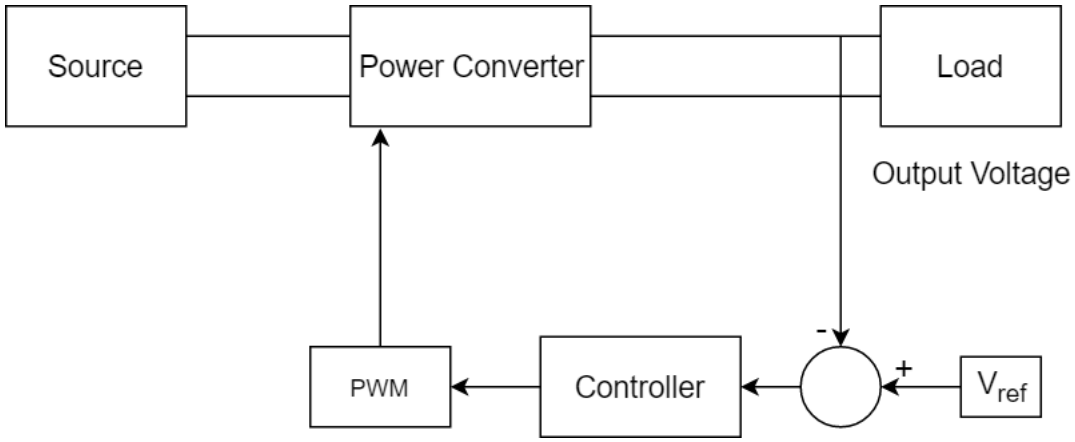

Figure 2.12 Concept of voltage-mode control

Voltage-mode control in its most simple form incorporates a single control-loop to regulate the output voltage of the converter. Figure 2.13 illustrates a schematic diagram where the voltage-mode control is implemented for a boost or step-up converter. The output-voltage of the converter V_o, is fed back and compared against a target constant voltage-reference V_{ref}. The error between the signals V_{err}, is passed through an analog compensation network$H(S)$, which in its simplest form can be a lead, lag or a lead-lag compensator. The compensator network generates a control signal V_m, forming the input to the PWM modulator, which in its simplest form consists of a saw tooth waveform generator and a comparator. The compensation network usually comprises one or more operational amplifiers plus passive components. Whilst being simple and easy to implement, this architecture is not particularly effective at compensating for rapid load and line-variations as these will take some time to be reflected in the output voltage, resulting in a slow response, large voltage deviations and/or the requirement for a large output filter capacitor [17].

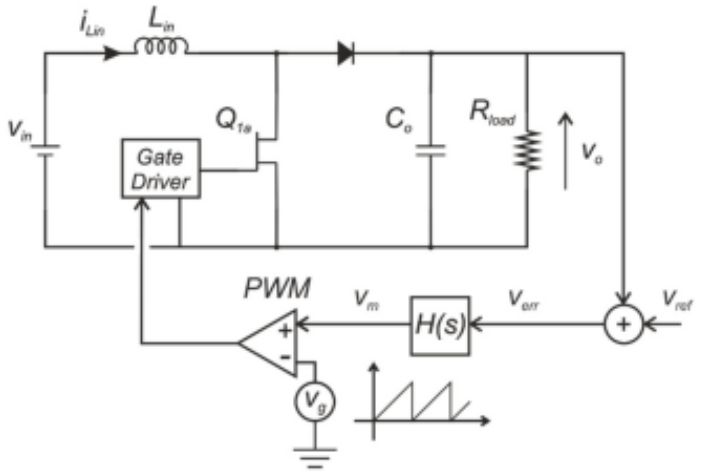

Figure 2.13 Boost converter with analog voltage-mode control

A variant of this architecture is sometimes used to improve immunity to line-variations [18]. In this variant, the input-voltage is employed as a feed-forward signal to adjust the slope of the modulator ramp. In consequence, any change in the input voltage is compensated for almost immediately, improving the overall dynamic response of the system.

2.7.2 Current Mode Control

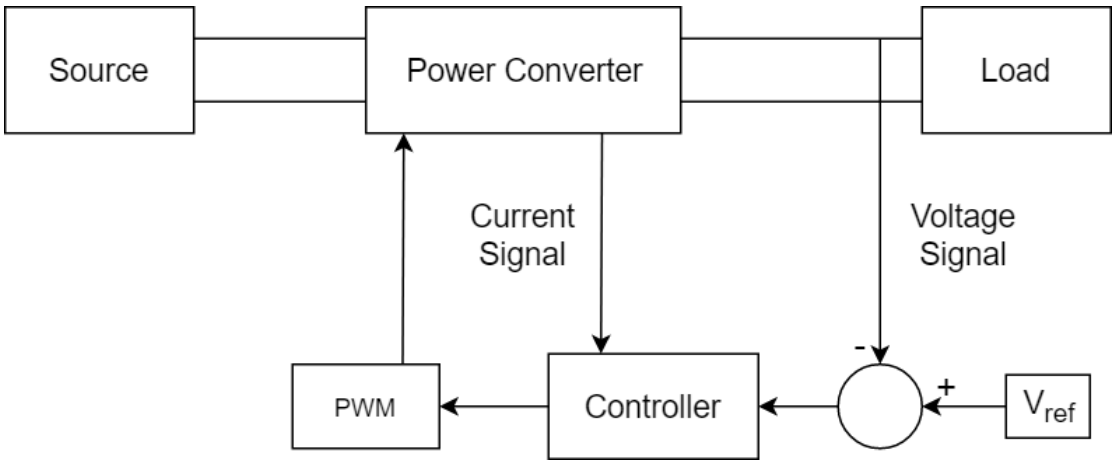

Figure 2.14 Concept of current-mode control

There exist many types of current-mode control which may be divided in two categories: fixed-frequency and variable-frequency, fixed frequency being the most common. Figure 2.15 (a) illustrates the architecture of the peak-current mode control for a boost converter which is a form of fixed-frequency control. There are two control loops,

an outer voltage-loop and an inner current-loop. The inner control loop regulates the peak current or maximum current circulating through the input inductor, whilst the outer control loop provides a reference current for the inner control loop.

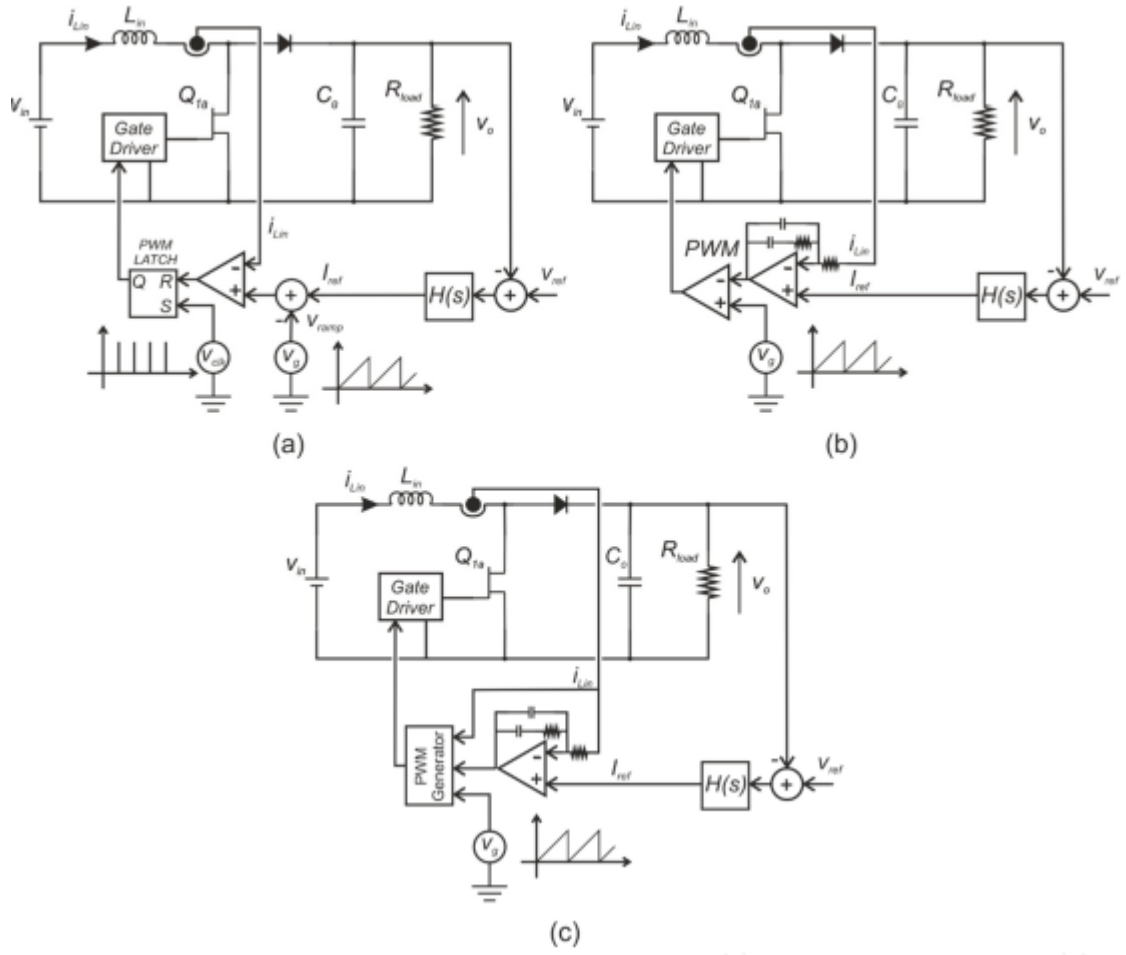

Figure 2.15 Boost converter with analog current-mode control. (a) Peak-current mode control. (b) Average-current mode control. (c) I² averaged-current mode control

In contrast to voltage-mode control, the duty-ratio of the converter transistor is generated by comparing the sensed inductor current against a threshold value. This is commonly accomplished by employing an analog comparator. When the inductor current reaches the threshold, the comparator resets the state of an SR-latch, which consequently turns the transistor off. A fixed-frequency clock-pulse is fed into the set terminal of the SR-latch which turns the transistor on at the start of each cycle. The constant activation/deactivation of the SR-latch produces a fixed-frequency driving signal. The outer-loop operates in a similar way to voltage-mode control. The sensed output voltage is

fed-back and compared with a target reference. The error signal generated is then passed through a compensation network which will produce the reference current signal.

Employing this technique can be problematic in that instability is caused by the propagation of sub-harmonic oscillations when the converter operates at duty-ratios above 0.5. To address this issue, a compensating ramp is added to the reference current before it is compared against the inductor current. The slope of the compensating ramp is selected to ensure stability of the system over a determined range of operation [3].

The advantages of the current-mode control can be summarized as: immediate response to input voltage variations effectively providing input-voltage feed-forward, reduction of the order of the system transfer functions since the operation of the input inductor is similar to that of a voltage-controlled current source, inherent over-current protection, and inherent load-sharing when several converters are employed in parallel. The main disadvantage of this type of control is its susceptibility to switching noise generated by the transistor switching transients which might generate current overshoots larger than peak-current and that can result in erratic operation and instability [8, 9, 10].

A number of variations on this control method have been proposed, for example using fixed on-time or fixed off-time in the current control loop as a free-running hysteresis technique [17]. Also, an integrator is sometimes included in the current control loop to force the average inductor current to follow the current reference signal. This technique is known as average-current mode control [12], see Figure 2.15 (b), and is often employed in applications where the converter input current must be shaped or accurately controlled, for example in power factor correction circuits [19].

More recently (2014), a new control method termed I^2 average-current mode control has been proposed in [14] to improve the transient response of average current mode control and to improve also light-load efficiency through using fixed on-time, variable switching frequency. Figure 2.15 (c) shows a diagram of a boost converter with this control scheme where an outer voltage loop is employed for voltage regulation. This technique combines both the fast-direct feedback of the peak-current mode control to ensure fast transient response with the slow integral feedback of the average-current mode control to achieve an accurate control of the inductor current. Moreover, by the use of fixed on-time

modulation in conjunction with this technique, the propagation of sub-harmonic oscillations is avoided thereby eliminating the requirement for a compensating ramp.

Control systems in continuous-time setting in the past were usually implemented using analogue devices such resistors, capacitors, inductors and operational amplifiers together with some necessary mechanical components. These devices are neither economical nor durable. The advances in computer technologies made the implementation of control systems in discrete-time setting (i.e., digital controllers) much more efficiently and economically possible. Most of control systems nowadays are implemented using either computers such as PCs or Digital Signal Processors (DSPs), which are specially designed to carry out heavy computations related to control-algorithms realization. The advantages of digital controllers using PCs or DSPs are obvious — it is fast, reliable, reusable and can be modified thru simple recoding whenever needed [20].

Chapter 3 Analog and Digital Design of PID Controller

3.1 Introduction

This chapter is about the controllers' part, using continuous conduction mode, and average current control mode.

3.2 Analog PI Controller Design

The controller synthesis is carried out in two major steps. First, a current inner loop is designed to cope with the PFC issue. In the second step, an outer loop is built-up to achieve voltage regulation. The analog controller for PFC is often achieved by a current-mode PFC control chip such as the Unitrode UC3854 [21]. In other words, the PFC converter has a two-loop control structure. The fast-current loop keeps the input current shape as of the input voltage, which renders the unity PF. The voltage loop keeps the output voltage at 380~400V. The voltage loop is very slow to avoid introducing 2nd harmonic ripple into the current reference [22], [23].

The figure 3.1 represents a general description of the PFC boost converter circuit, and the corresponding inductor current, and output voltage waveforms.

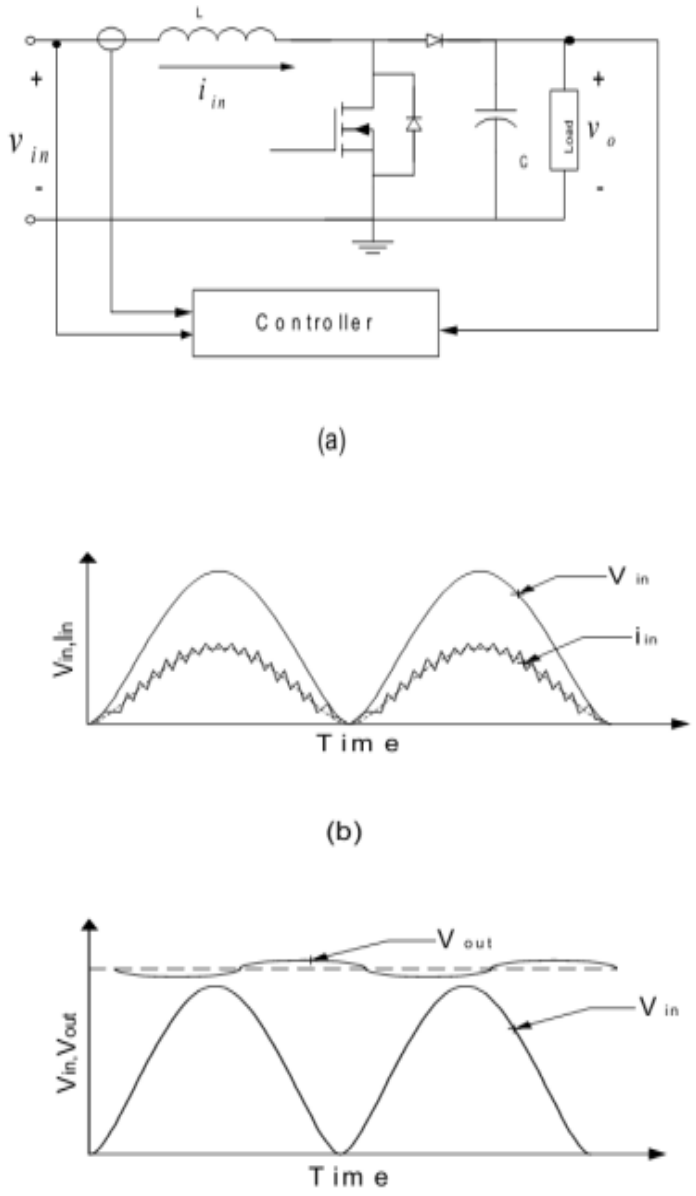

Figure 3.1 (a) Boost PFC with controller, (b) Waveforms of input voltage and inductor current, (c) Waveforms of input voltage and output voltage

3.2.1 Current Loop Control

The main feature of the average current control is the presence of the current error amplifier (compensator) that provides the control of the average inductor current. The inner current loop block diagram can be built with the combination of the current sensing circuit, current error amplifier, PWM generator and power stage of the PFC boost converter as shown in the Figure 3.2.

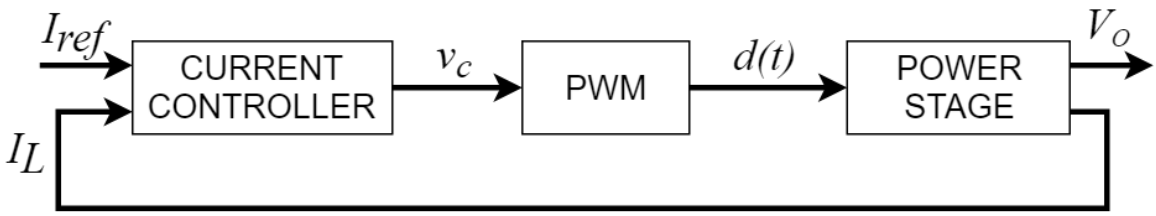

Figure 3.2 Current control loop

The function of the current compensator is to force the current to track the current reference that is given by the multiplier which has the same shape as the input voltage. So, the current loop bandwidth must be higher than the reference bandwidth. For faithfully tracking a semi-sinusoidal waveform of 100 or 120Hz, the bandwidth of the current loop is usually set to 2-10KHz [22].

The current is desired to have the same characteristic as the input rectified voltage V_g i.e. numerical sine wave. By multiplying the output of the voltage loop controller with V_g (scaled input rectified voltage), a reference for the current controller is found. V_g is normalized to be a maximum of 1, i.e. For a line voltage of 220V the K_g is 1/220. The reference signal i_{ref} is thereby ensured to be a numerical sine wave with the same frequency as V_g and a satisfactory controller will have a power factor PF close to 1.

Using the three terminal average models, a small-signal equivalent circuit of the current loop is shown in Figure 3.3.

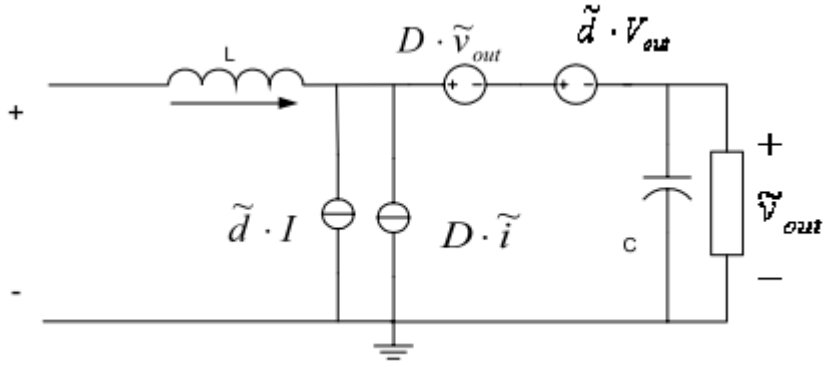

Figure 3.3 Small signal model of the current loop

The power stage small-signal duty-to-current transfer function is derived as follows [22]:

$$G_{id}(s) = \frac{\tilde{\imath}}{\tilde{d}} = \frac{2V_{out}}{R_L(1-D)^2} \cdot \frac{1+\frac{sR_LC}{2}}{1+\frac{sL}{R_L(1-D)^2}+\frac{s^2LC}{(1-D)^2}}$$ Equation 3.1

Where: $D$is the duty cycle.

R_L is the load resistance.

C id the output capacitance.

L is the inductance.

V_{out} is the output voltage.

For $\omega = js$, when ω is large enough,the high frequency approximation can be derived as follows:

$$G_{id}(s) = \frac{\tilde{\imath}}{\tilde{d}} \approx \frac{V_{out}}{Ls}$$ Equation 3.2

$$G_{id}(s) = \frac{390}{(170 \times 10^{-6})\mathrm{s}}$$

Where: $L = 170\ \mu F$

$V_{out} = 390\ V_{dc}$

Figure 3.4 shows the Bode plots for duty-to-current transfer function of small signal model, and for the high frequency approximation. For the high frequency approximation, the phase margin $PM = 90°$ and the gain margin $GM = inf$, for the small signal model when $V_{in} = 220\ V$, the $PM = 90°$ and the gain margin $GM = inf$.

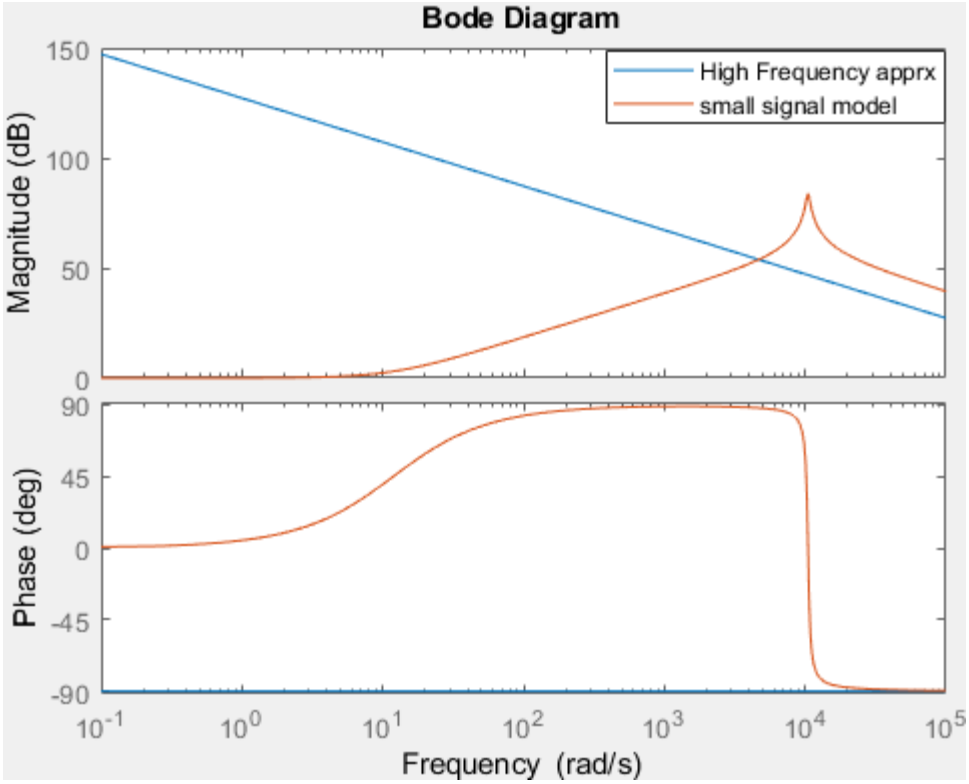

Figure 3.4 Small-signal duty-to-current transfer functions Bode plot

The controller used for the control loops compensation is a well-known PI controller is described by:

$$C_i(s) = K_p + \frac{K_i}{s} = K_i\left(\frac{1+\frac{s}{\omega_z}}{s}\right) \qquad \text{Equation 3.3}$$

Where: ω_z is the controller zero.

K_p is the proportional term.

K_i is the integral term.

The disadvantage of the PI controller in the AC systems is the permanent tracking error, which can be eliminated by the fast-current loop. The performance of the control loop is defined by the cross-over frequency ω_c and the phase margin ϕ_{pm}. Because the cross-over frequency directly impacts the total harmonic distortion (THD) of the PFC, it must be as high as possible. On the other hand, the cross-over frequency must not be higher than 10-20% of the control-loop sampling frequency. The phase margin impacts the

overshoot during the step change at the input of the PI controller. A good compromise is the phase margin between 45-60°.

The parameters of the PI controller are calculated using the known transfer function of the open loop and the rules for a stable control loop. The position/frequency of the controller zero ω_z is calculated as:

$$\omega_z = \frac{\omega_c}{tan(\phi_m)} \qquad \text{Equation 3.4}$$

When ω_z is known, the integral gain $K_i$of the PI controller is obtained as:

$$K_i = \frac{L}{V_{out}} \frac{\omega_c^2}{\sqrt{1+\frac{\omega_c^2}{\omega_z^2}}} \qquad \text{Equation 3.5}$$

Finally, the proportional gain of the controller is calculated as:

$$K_p = \frac{K_i}{\omega_z} \qquad \text{Equation 3.6}$$

The PI controller parameters were found to be:

$$K_p = 0.0237$$

$$K_i = 860.4$$

$$C_i(s) = 0.0237 + \frac{860.4}{s}$$

The open loop current-to-duty transfer function is then:

$$G_{i_{open}}(s) = C_i(s).G_{id}(s) = (K_p + \frac{K_i}{s})\frac{V_{out}}{(Ls)} \qquad \text{Equation 3.7}$$

$$= \left(0.0237 + \frac{860.4}{s}\right)\frac{390}{(170 \times 10^{-6})s} = \frac{9.243s + 335556}{(170 \times 10^{-6}).s^2}$$

Figure 3.5 shows Bode plots of $G_{i_{open}}(s)$ with 10kHz crossover frequency and 60° phase margin.

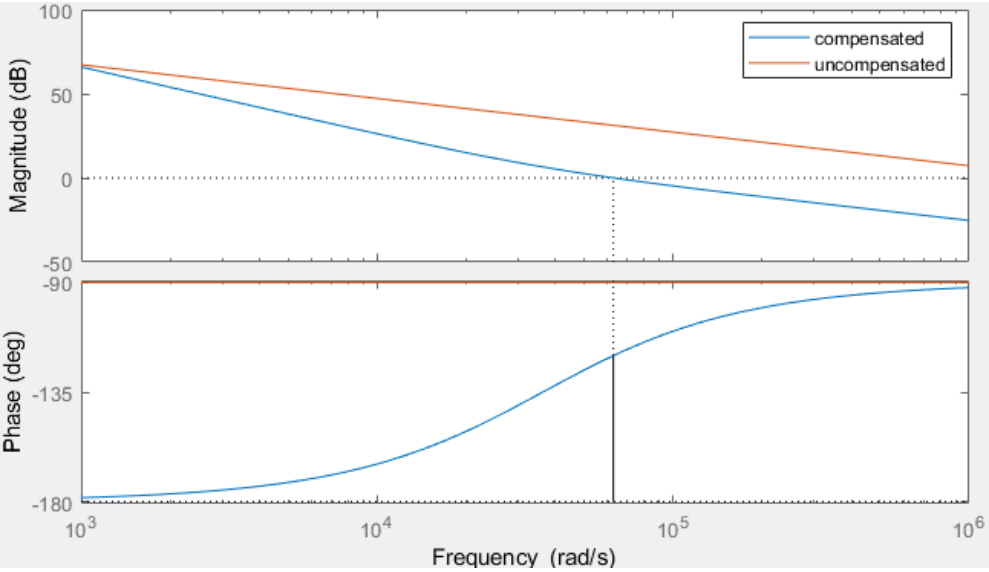

Figure 3.5 Bode plot of the compensated and uncompensated systems

As can be seen, the compensated system has a $PM = 60°$ at a crossover frequency of 10kHz, which obviously meet the design specification listed before.

The current-to-duty closed loop transfer function is shown in the following equation:

$$G_{i_{closed}}(s) = \frac{9.243\,s + 335556}{0.00017s^2 + 9.243s + 335556}$$

The system has two complex poles, and one zero:

$$P1 = 10^4.(-2.7185 + 3.5140i)$$

$$P2 = 10^4.(-2.7185 - 3.5140i)$$

$$Z1 = -3.6304e + 04$$

As can be seen, both of the poles have negative real part, which is another indicator about the stability of the system.

The next step is to verify its step response using MATLAB, to plot and check for the stability of the system. The step response is represented in the figure below:

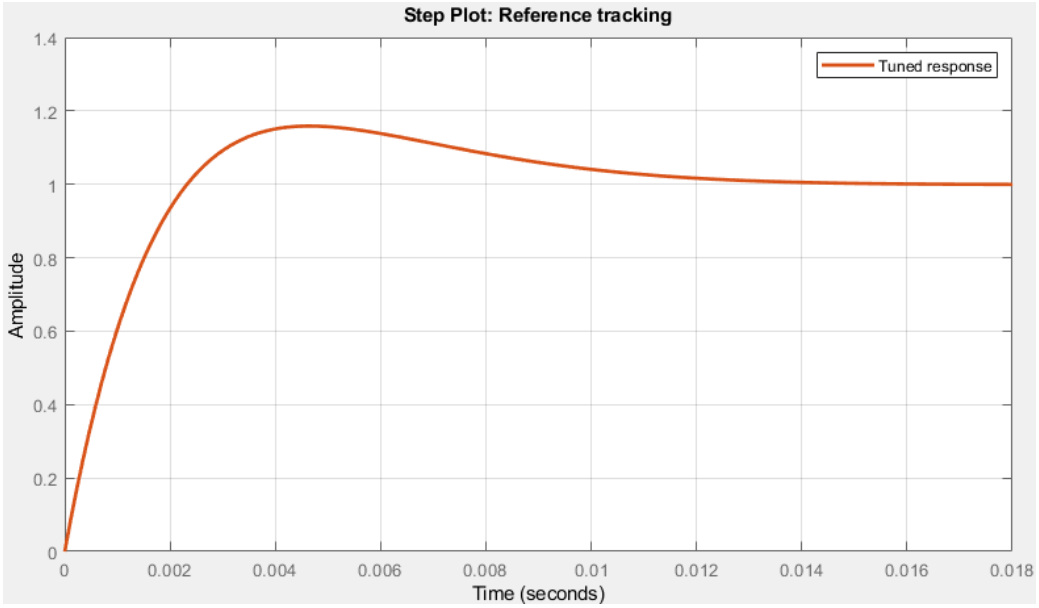

Figure 3.6 Step response of the current closed loop

The step response of the current closed loop presents a stable response, with a very short transient state and an overshoot of 16.3%.

3.2.2 Voltage Loop Control

The outer voltage loop determines the required amplitude of the current reference due to the requirement for the power balance operation. On the other hand, it is necessary that the outer voltage loop should have limited bandwidth, less than half of the line frequency, for minimum distortion in the line current. This limited bandwidth brings slower transient response. The outer voltage loop should be designed for optimal transient response with minimal input current distortion due to the 2nd harmonic component in the output capacitor voltage. The block diagram of the outer voltage loop can be constructed with closed current loop as shown in Figure 3.7.

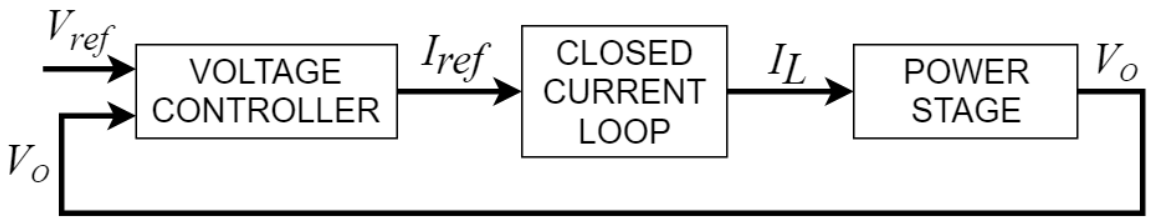

Figure 3.7 Voltage control loop

Assuming the inner current loop is well designed, it provides a good current regulation according to the predefined current reference. It can be assumed that the closed current loop has no effect in the outer voltage loop, simply behaves as a unity gain block in the block diagram of the voltage loop shown in Figure 3.7. So, the only thing is the design of the voltage error amplifier. This voltage compensator should be designed according to the low frequency behavior of the power stage of the PFC. Because the outer voltage loop has smaller crossover frequency around 20 Hz, a small signal model of the power stage accurate at frequencies below 100 Hz should be used. The small signal model of the PFC converter consists of a controlled power source modeled as a current source shunted by a resistor [24].

Then open-loop transfer function can be written as:

$$G_{v_{open}}(s) = C_v(s)G_v(s) = (K_p + \frac{K_i}{s})\frac{1}{2s}\frac{V_{in}}{(CV_{out})} \qquad \text{Equation 3.8}$$

The performance of the control loop is again defined by the control loop bandwidth ω_c and phase margin ϕ_{pm}. One of the requirements for the voltage-control loop is to attenuate the voltage ripple at $2\omega_s$. Therefore, the bandwidth of the control loop must be very small, usually set from 0.1 to 0.2 of $2\omega_s$. The phase margin is set close to 90°, because the voltage overshoot of the DC-bus voltage is not desired [25].

When the settings $f_c = 20\,Hz$ and $\phi_{pm} = 60°$ are defined, the PI controller constants are calculated as:

$$\omega_z = \frac{\omega_c}{tan\left(\phi_m - \frac{\pi}{2} + arctan(w_c C\frac{R}{2})\right)} \qquad \text{Equation 3.9}$$

$$K_i = \frac{4V_{out}}{RV_{in}} . \frac{w_c\sqrt{1+(w_c C\frac{R}{2})^2}}{\sqrt{1+\frac{\omega_c^2}{\omega_z^2}}} \qquad \text{Equation 3.10}$$

Finally, the proportional gain of the controller is calculated as:

$$K_p = \frac{K_i}{\omega_z} \qquad \text{Equation 3.11}$$

The PI controller parameters were found to be:

$$K_p = 0.0642$$

$$K_i = 4.7069$$

$$C_v(s) = 0.0642 + \frac{4.7069}{s}$$

The open loop transfer function then is:

$$G_{v_{open}}(s) = C_v(s)G_v(s) = \left(0.0642 + \frac{4.7069}{s}\right)\frac{220}{2(168 \times 10^{-6})390s} = \frac{7.062s + 517.8}{0.06552s^2}$$

The Bode plot for the voltage open loop transfer function is shown below:

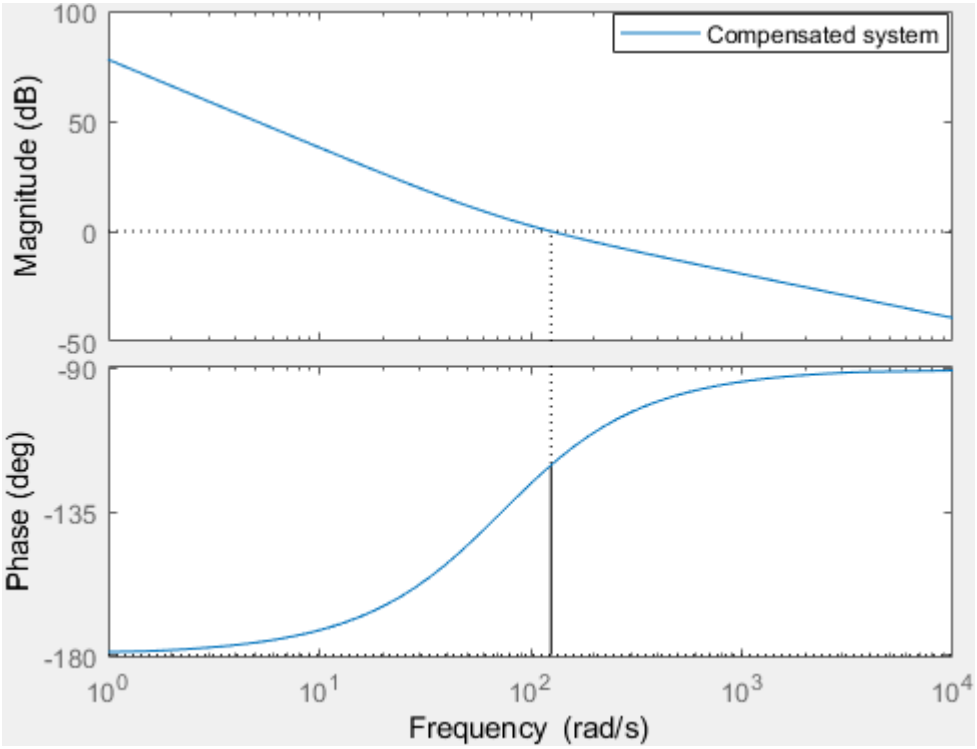

Figure 3.8 The Bode plot for the voltage open loop transfer function

From the Bode plot, it is clear that the phase margin is 60 and the crossover frequency is 20Hz, which meets the design requirements.

The step response of the voltage closed loop is shown below:

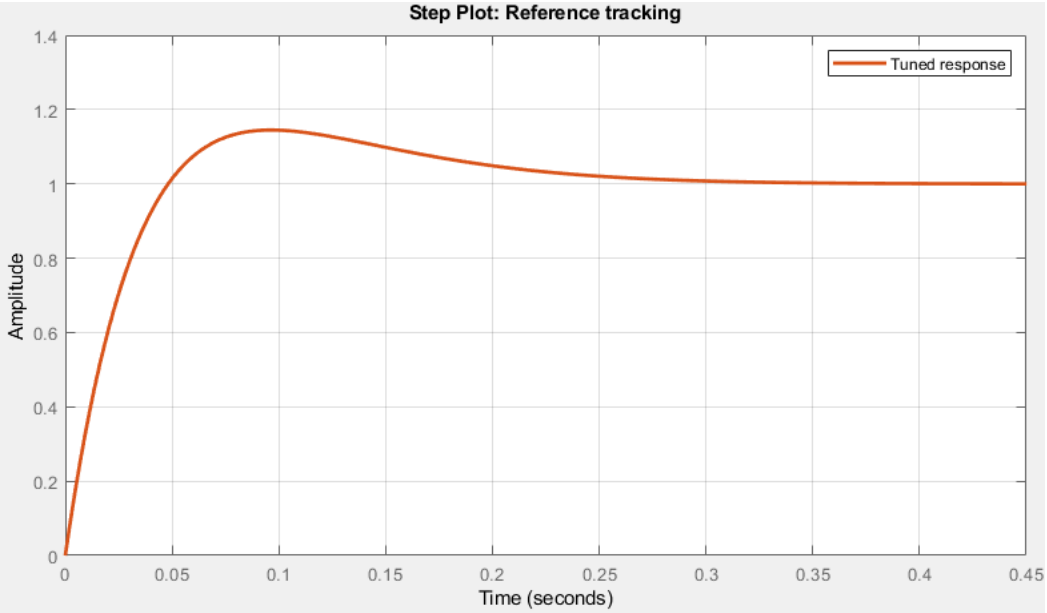

Figure 3.9 Step response of the voltage closed loop

The step response shows very small settling and rising times with overshoot peak amplitude of 14.7%, which is a satisfactory overshoot percentage.

3.3 Digital PI Controller Design

To implement digital control on a continuous system, we need an ADC, sample-and-hold circuits and a digital-to-analog converter (DAC) for digital and analog signal interface. Because the ADC and digital PWM quantize signals, the speed and resolution of ADC and PWM are critical in this application [26].

Different from analog control, in which the compensator is realized by operational amplifiers, the control law in digital control system is realized by binary calculations. As a result, delay is inevitable and depends on the speed of the digital controller. The presence of a signal of frequency higher than half of the sampling frequency can affect the controller by the aliasing effect. This can be relieved by low pass filter or by selecting a higher sampling frequency.

The sample-and-hold of continuous signals and the non-zero computation time cause delay in a digital control system. Delay in a system usually causes phase lag that leads to reduction of the phase margin.

3.3.1 Current Loop

The design target is similar to that of the analog compensator. For robustness, the phase margin is set to 60°.

Since the control bandwidths are sufficiently low, as compared to the sampling frequency, it is possible to use a simple discretization method, without an excessive frequency response distortion. In bilinear transformation, the formula below is used:

$$s = \frac{2}{T}\frac{z-1}{z+1} \qquad \text{Equation 3.12}$$

Where: T is the sampling time.

The current to duty loop transfer function obtained before, was converted to digitize the system using the Tustin method, the discrete plant is:

$$G_i(z) = \frac{11.47z+11.47}{z-1} \qquad \text{Equation 3.13}$$

To compensate the digital delay, the one-zero approach is used, in which the zero is moved toward the origin. The current compensator is of the form:

$$G_i(z) = K_p + K_i\frac{T_s}{z-1} = K_p\frac{z-a}{z-1} \qquad \text{Equation 3.14}$$

Where:K_p and $a$are the gain and the zero that defines the compensator.

The open loop transfer function, taking into consideration the delay, is:

$$T_{i_{open}}(z) = C_i(z)G_i(z)z^{-\frac{T_{delay}}{T_s}} \qquad \text{Equation 3.15}$$

$$= K_p\frac{z-a}{z-1}\frac{11.47\,z\ +\ 11.47}{z-1}z^{-1}$$

Where T_{delay} is taken as one switching cycle, and $T_s = 10^{-5}$ sec

The design targets, crossover frequency$\omega_c = 2\pi\ 10{,}000\ rad/sec$ and phase margin are used to determine two unknown variables, as follows:

$$\begin{cases} \left|T_{i_{open}}\left(e^{j\omega_c T_s}\right)\right| = 1 \\ Phase(T_{i_{open}}\left(e^{j\omega_c T_s}\right)) = -180 + 60 \end{cases}$$

The variables were found, and the controller is then:

$$G_i(z) = 0.02848 + 32.21\frac{T_s}{z-1} = 0.02931 + \frac{0.0003221}{z-1}$$

The Bode plot of the open loop current to duty transfer function $T_{i_{open}}(z)$ is shown below:

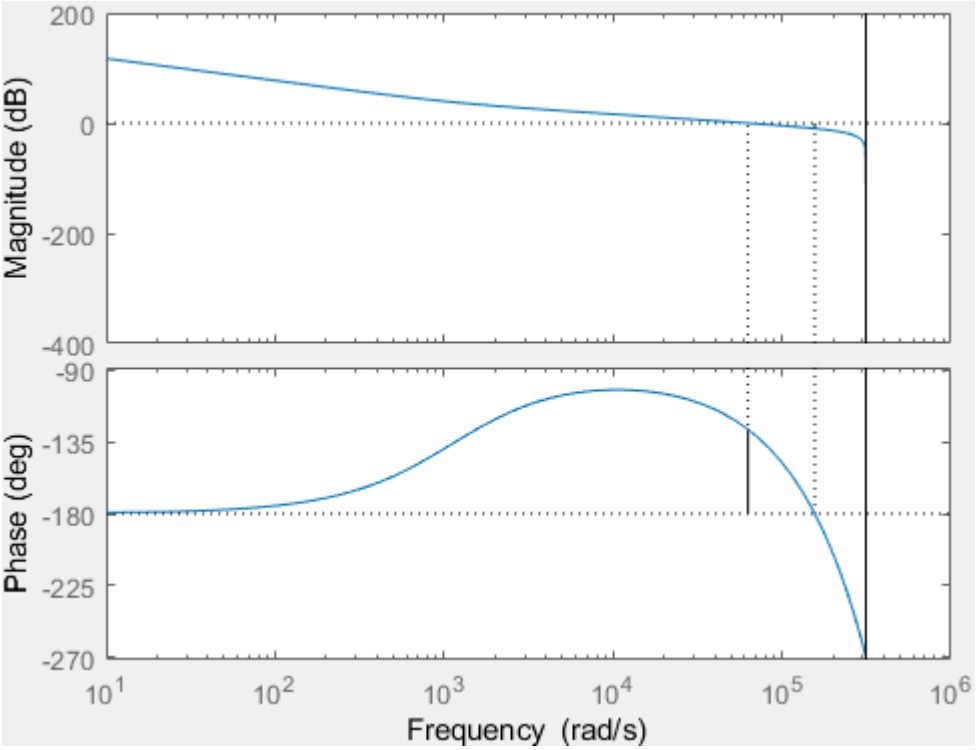

Figure 3.10 The Bode plot of the open loop current to duty transfer function

The phase margin is found to be 60˚ and the crossover frequency is 10kHz are satisfying the design constraints.

The step response of the compensated current closed loop is shown in the next page.

Figure 3.11 The step response of the compensated current closed loop

The current loop as can be seen reaches the steady state in a very short period of time, with an overshoot of 3%.

3.3.2 Voltage Loop

Assuming the inner current loop is well designed, it provides a good current regulation according to the predefined current reference. It can be assumed that the closed current loop has no effect on the outer voltage loop, it simply behaves as a unity gain block in the block diagram of the voltage loop.

The desired control specifications for the voltage loop are the same as for the analog controller; that is a small bandwidth of 20Hz and a phase margin of 60˚.

The voltage-to-control transfer function obtained before is discretized using the Tustin method, the discrete plant is:

$$G_v(z) = \frac{0.008394z + 0.008394}{z - 1}$$

The PI controller transfer function is of the form:

$$C_v(z) = K_p + K_i \frac{T_s}{z-1} = K_p \frac{z-a}{z-1}$$ Equation 3.16

The overall open loop transfer function is no more than:

$$T_{v_{open}}(\mathrm{z}) = C_v(\mathrm{z})G_v(\mathrm{z}) \qquad \text{Equation 3.17}$$

$$= \left(K_p + K_i \frac{T_s}{\mathrm{z}-1}\right) \frac{0.008394\mathrm{z} + 0.008394}{\mathrm{z}-1}$$

The design targets, crossover frequency $\omega_c = 2\pi\ 20\ rad/s$ and phase margin are used to determine two unknown variables, as follows:

$$\begin{cases} \left|T_{v_{open}}\left(e^{j\omega_c T_s}\right)\right| = 1 \\ Phase\left(T_{v_{open}}\left(e^{j\omega_c T_s}\right)\right) = -180 + 60 \end{cases}$$

The variables were found, and the controller is:

$$G_i(\mathrm{z}) = \ 0.02848 + 32.21\frac{T_s}{\mathrm{z}-1} = 0.02931 + \frac{0.0003221}{\mathrm{z}-1}$$

So:

$$T_{v_{open}}(\mathrm{z}) = \frac{0.000246\ \mathrm{z}^2 + \ 2.704\mathrm{e}-06\ \mathrm{z}\ -\ 0.0002433}{z\mathrm{\hat{}}2\ -\ 2\ z\ +\ 1}$$

The Bode plot of the open loop voltage to control transfer function $T_{v_{open}}(\mathrm{z})$ is shown below:

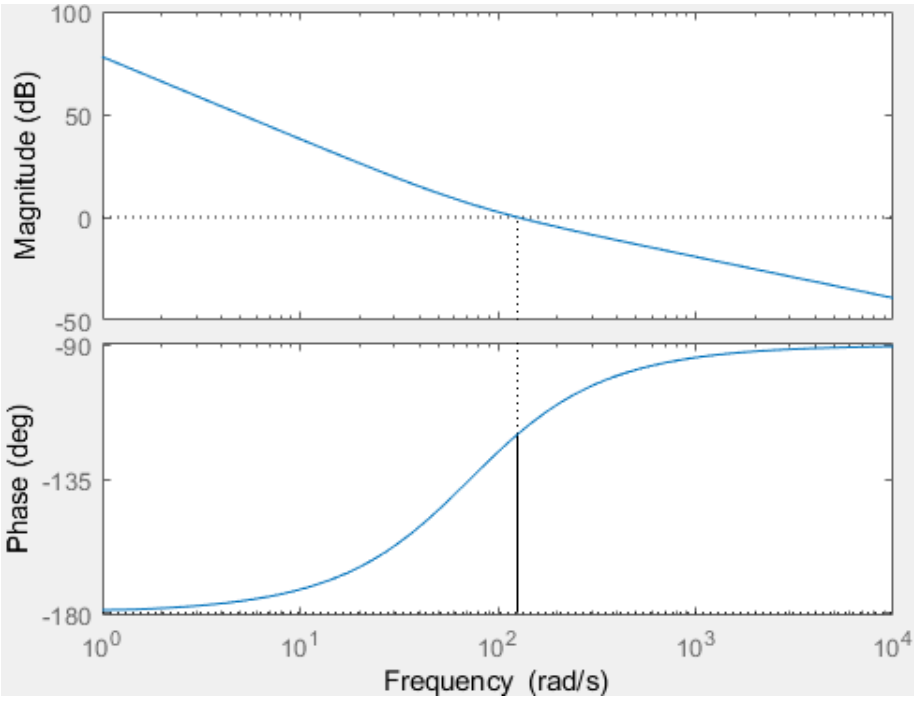

Figure 3.12 The Bode plot of the open loop voltage

The step response of the closed loop system is:

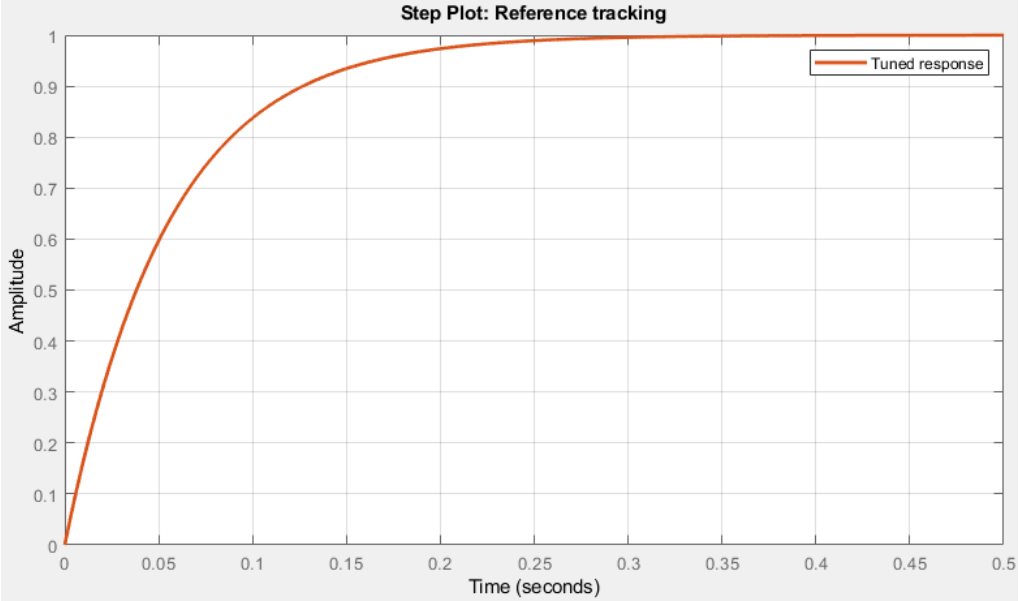

Figure 3.13 The step response of the closed loop system

The step response shows a waveform with no overshoot in the transient state, and a settling time of 0.3 seconds.

3.4 Conclusion

The obtained controllers are fed into the circuit and simulated; the results are gathered on the last chapter.

Chapter 4 Simulation and Results

In order to analyze the behavior of the PFC system, this chapter is divided into three mains parts, the first one shows the circuit behavior without any power factor correction, the second represents the results for the analog design, while the last one is for the digital design. The models presented are all done using MATLAB Simulink.

The power stage simulation parameters are listed in the table below.

Table 4.1 The power stage simulation parameters

Input Voltage	$V_i = 220V_{ac}$
PFC Output Voltage	$V_o = 390V$
PFC Output Power	$P_o = 1.8kW$
PFC Switching Frequency	$f_s = 100kHz$
Output Filtering Capacitor	$C = 1.68mF$
Boost Inductor	$L = 170\mu H$
Load Resistor	$R = 100\Omega$

4.1 Model and Simulation Results for a Boost Converter Without PFC

4.1.1 Circuit Model

The circuit used consists of a diode bridge, two capacitors C1 and C2, a conducting diode and a load R. Shown beneath the circuit diagram and the obtained results in Figures 4.1, 4.2 and 4.3.

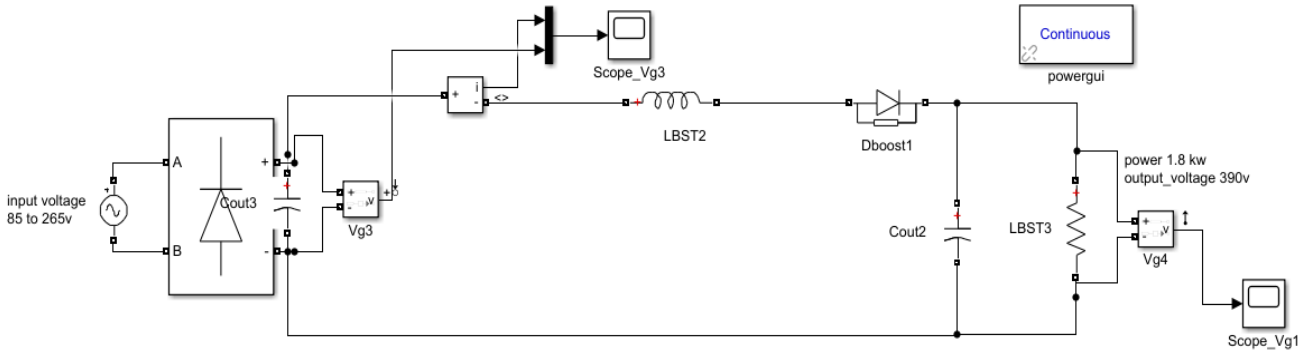

Figure 4.1 Circuit diagram of the boost converter without PFC

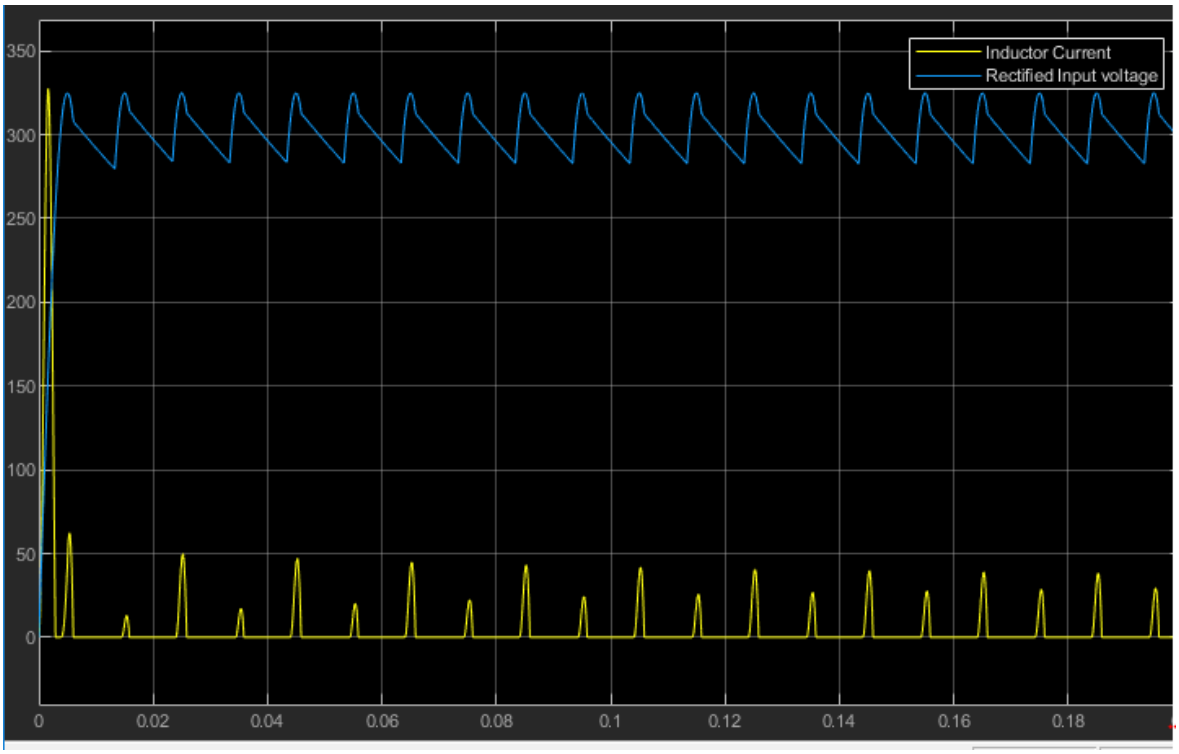

Figure 4.2 Inductor current and Input rectified voltage waveforms

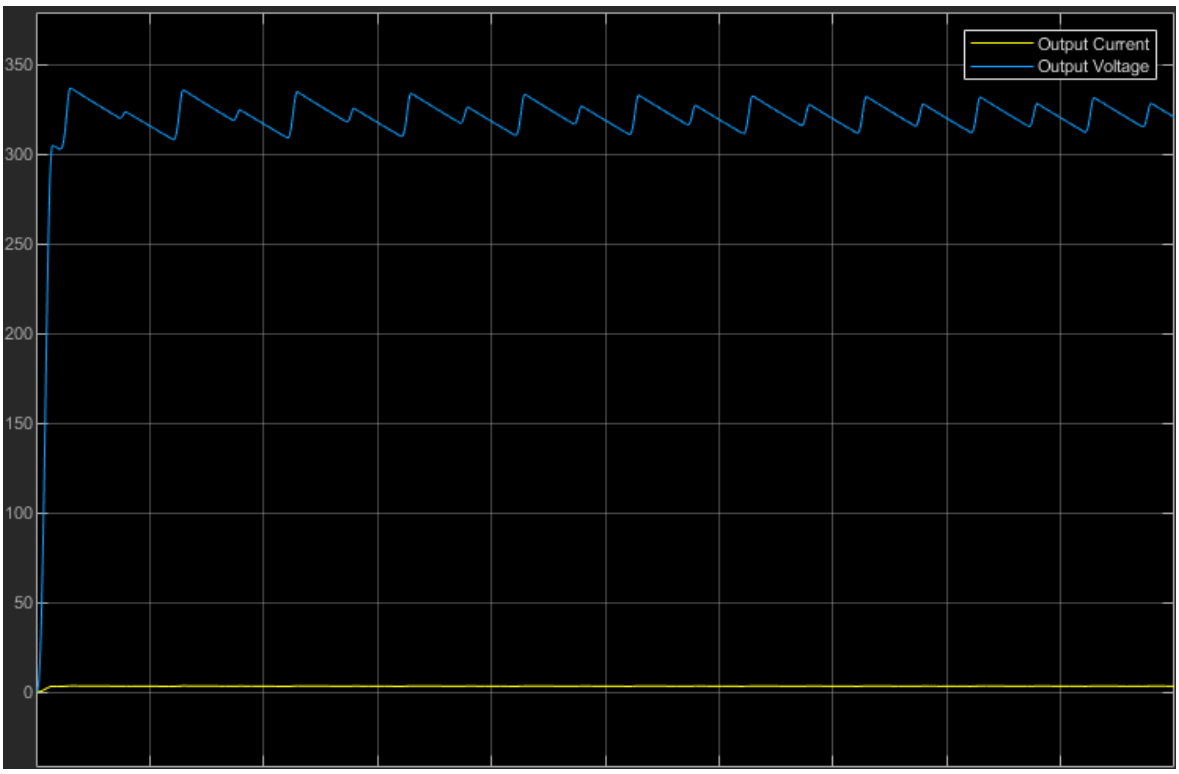

Figure 4.3 Output voltage and current waveforms

4.1.2 Discussion

The bridge rectifier with a capacitor is the simplest form of AC to DC conversion. The capacitor filters the rectified voltage and it provides certain energy storage in case of line failure, but the resulting current is pulsating, as shown in Figure 4.2, causing a high THD of about 109.83% which has an impact over the power factor (PF=0.67). Moreover, the output voltage is not matching the rated value, and the ripple content of the output voltage is significantly high where it is found to be 25V peak to peak, shown inFigure 4.3,which means that power dissipation is very high due to the phase between inductor current and input voltage.

To overcome these problems, we use the single-phase boost PFC as shown in the following part.

4.2 Model and Simulation Results for a Boost Converter with PFC

The PFC boost converter was simulated in Simulink with a dynamic model to represent the dynamics of the boost PFC converter, specifically, to simulate the current shaping properties of this topology. The model was developed with the following assumptions and objectives.

Assumptions:

- The input voltage is a perfect sine wave which is held constant, meaning no sudden changes in amplitude or frequency. Only the fundamental of the voltage is included, so no harmonics exist at the voltage.
- The system is assumed to be operating in steady state; thus, startup is not considered.

Objectives:

- The input inductor current shall follow the shape of the scaled rectified input voltage while having appropriate amplitude to keep the output voltage at the correct level.
- Feed forward of the input voltage is not considered as this is more of a phenomenon during transients.

- The output DC voltage shall be controlled to match the reference.

4.2.1 Analog Controller Simulation Results

The circuit used is composed of the circuit diagram associated with the control blocks are presented in the figure 4.4, a bridge rectifier, a capacitor at the output of the bridge, an inductor, a MOSFET, a conducting diode, an output capacitor and a resistive

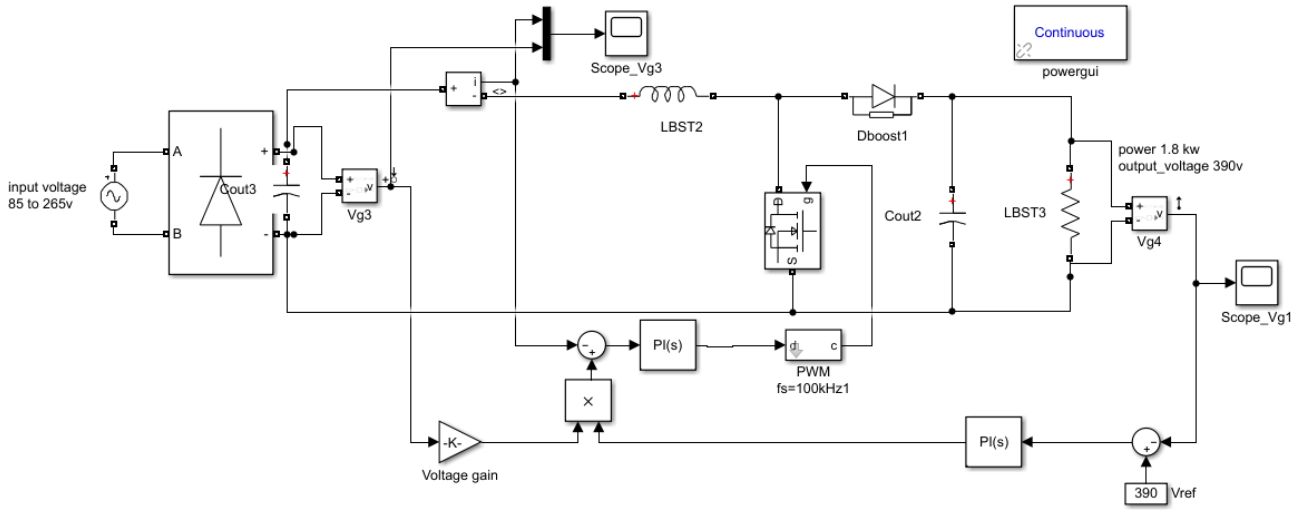

Figure 4.4 The PFC boost converter model in Simulink

load R.

The PWM block is an amplifier that compares the duty cycle of the sawtooth signal, it then goes high when d is higher than the sawtooth waveform signal, and low when the opposite, see below the internal architecture of the PWM module:

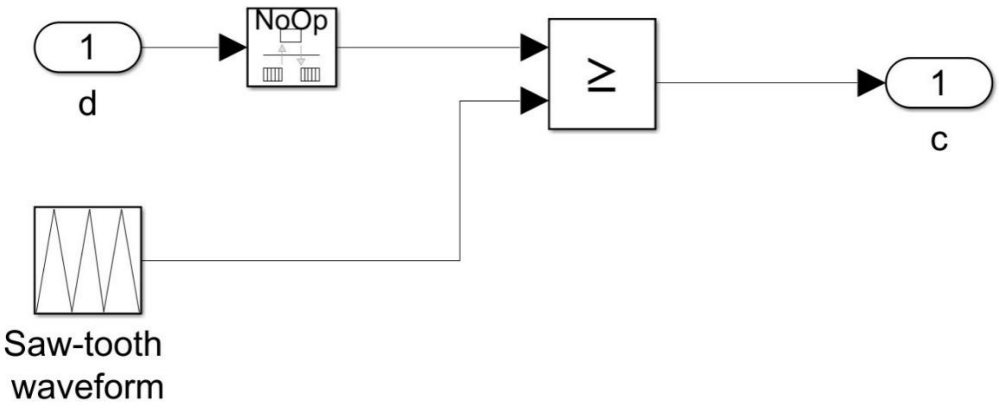

Figure 4.5 Internal architecture of the PWM block

The inner control loop and outer control loop are designed to assure the current tracking to input voltage, and a DC output voltage. The current loop PID receives the error signal that is the product of the normalized (divided by peak input voltage) rectified input voltage from a side which is no more than a sine wave with an amplitude of unity, and the reference current generated by the output of voltage PID. The voltage control loop has the error signal produced by the output voltage and its reference V_{ref} to be tracked. The previously found PID coefficients for both inner loop and outer loop are used, the results beneath were found.

Figure 4.6 represents the duty cycle signal, which is the output of the inner PID the duty cycle goes in between 0 and 1, here it goes high making the PWM block goes high causing the MOSFET to conduct, then goes narrower causing the PWM to generate a 0 which switch off the MOSFET.

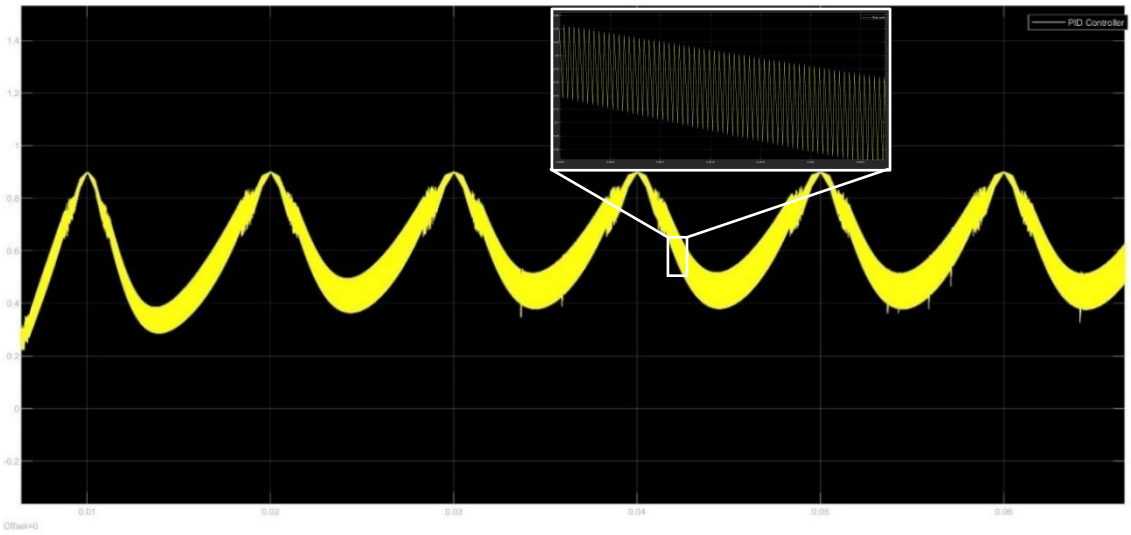

Figure 4.6 The duty cycle (output of the inner PID controller)

The generated PWM signal is shown in Figure 4.7.

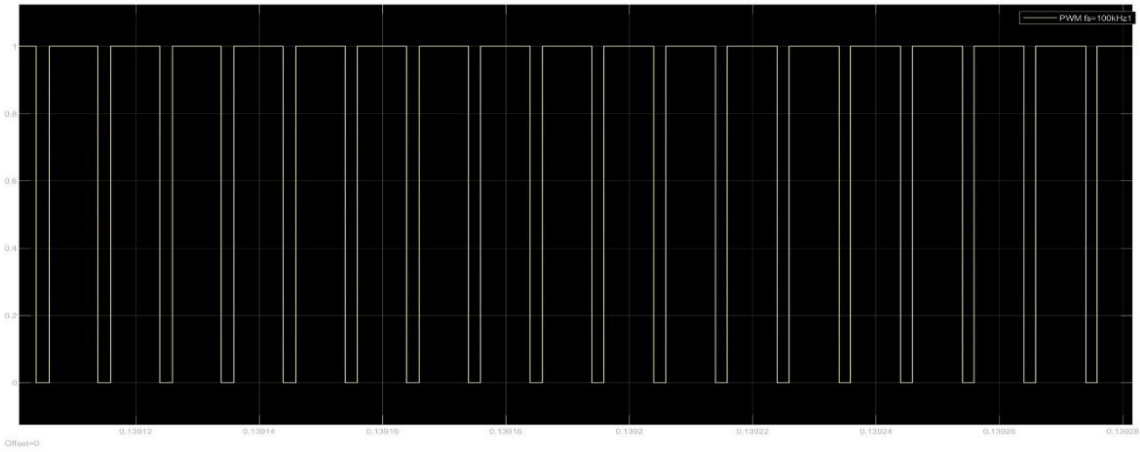

Figure 4.7 PWM waveform

The simulation results the rectified voltage and the input current for 220V input-voltage with a load R are shown in Figure 4.8.

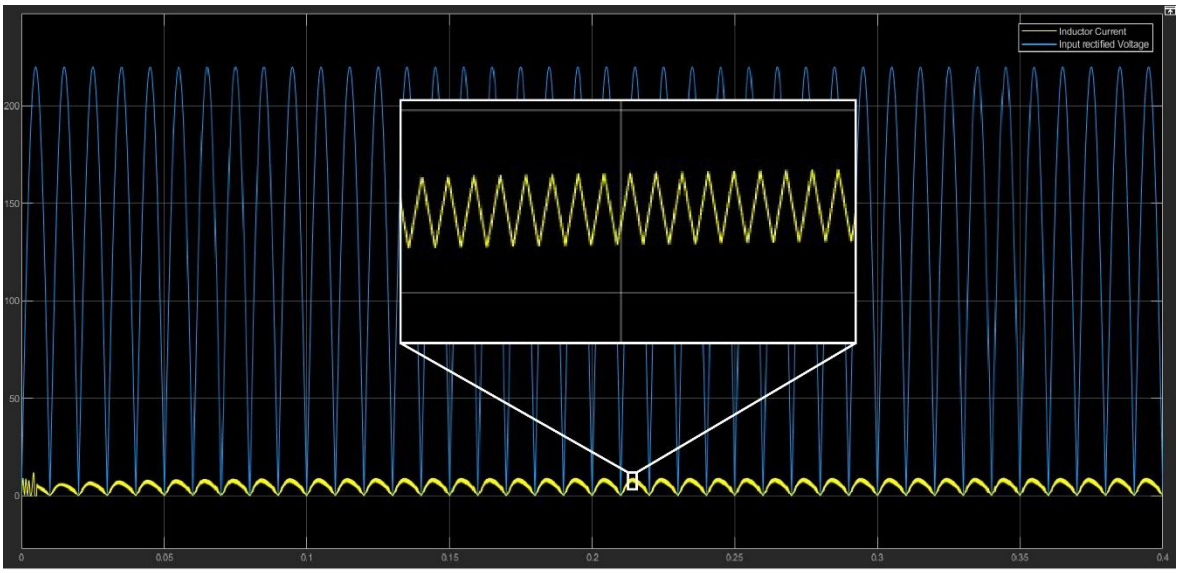

Figure 4.8 Inductor current and rectified voltage waveforms

The output voltage reference is defined as 390 Vdc. The output voltage simulation waveform is shown in Figure 4.9.

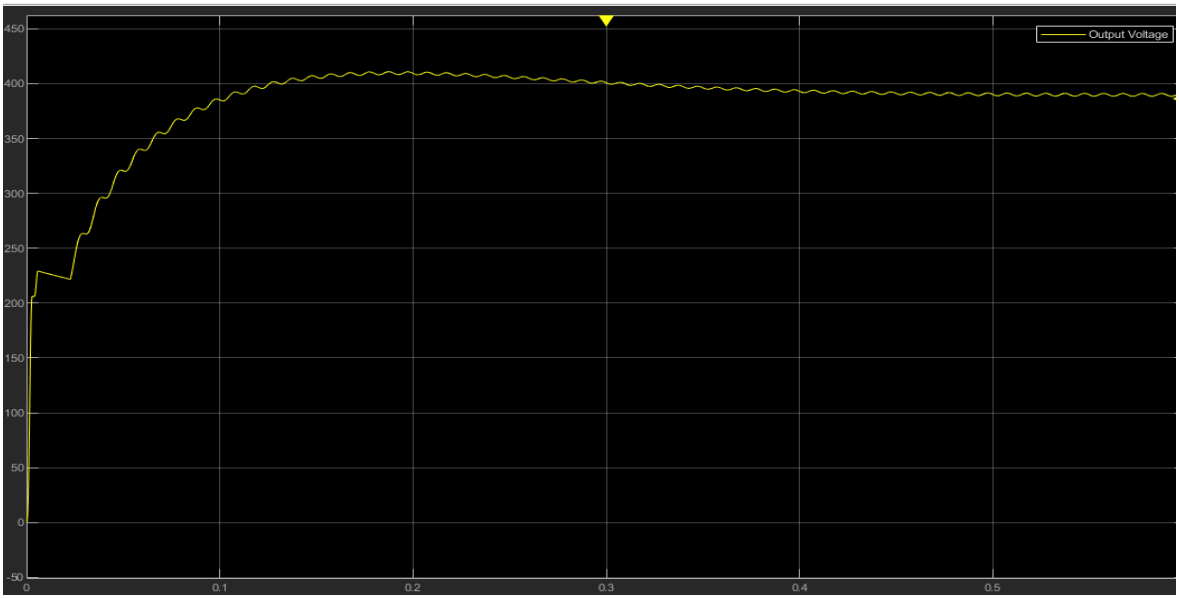

Figure 4.9 Output voltage waveform

4.2.1.1 Discussion

In the above digital simulation results, it is shown that a sinusoidal input current waveform is achieved for 220V since the current waveform is tracking the reference voltage.

The inductor current matches the reference curve quietly good and there is very little zero-crossing distortion present. The distortions in the input current at the zero crossings are due to the lower inductor voltage at these regions. The lower inductor voltage cannot provide enough inductor current to track reference waveform.

The ripple at the inductor current is approximately 1.2A which is less than the acceptable theoretical value (20%) which is:

$$I_{ripple} = 0.2\, I_{peak} = 1.6A.$$

The overshoot at the output voltage is about 8%. The output voltage waveform is almost a DC waveform, with some ripple during the steady state of about 1.5V peak approximately which is an acceptable result for this topology.

A power factor of 0.9879 is achieved with the designed controller, and a total harmonic distortion of 9.7%.

4.2.2 Digital Controller Simulation Results

The digital design has some additional blocks compared to the analog design, ADC (analog-to-digital converter), discrete PID controller, rate transition block which is used to handle transfer of data between ports operating at different rates, and a digital PWM block. The Simulink model is shown below in Figure 4.10.

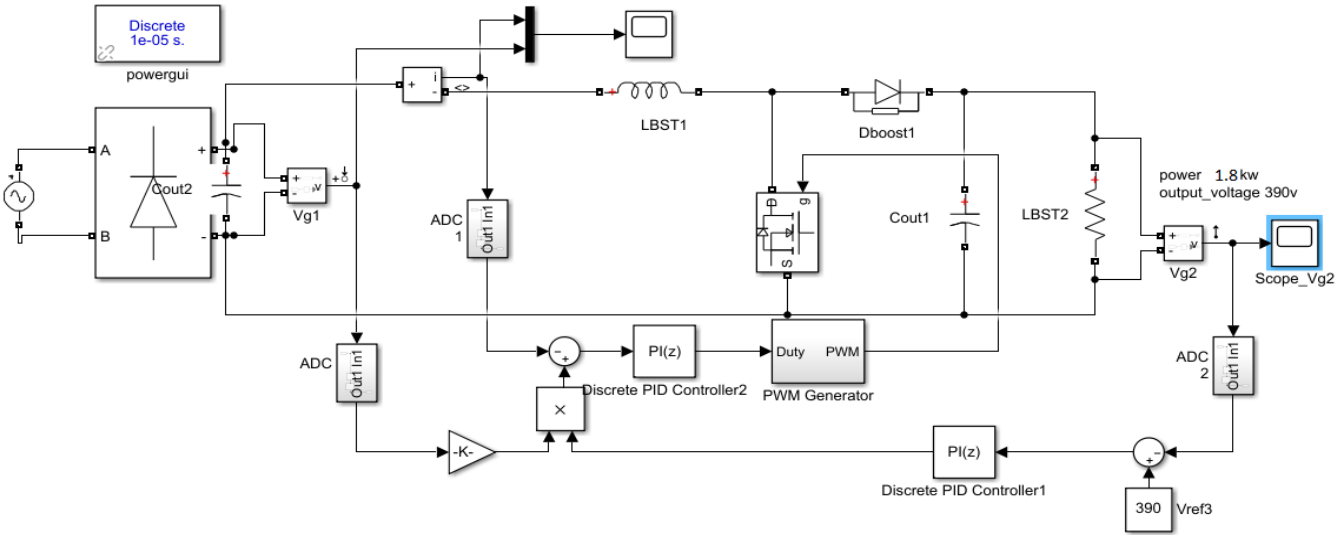

Figure 4.10 Digital controller for a PFC boost converter model in Simulink

The waveform below represents the inductor current waveform for the 220V input voltage.

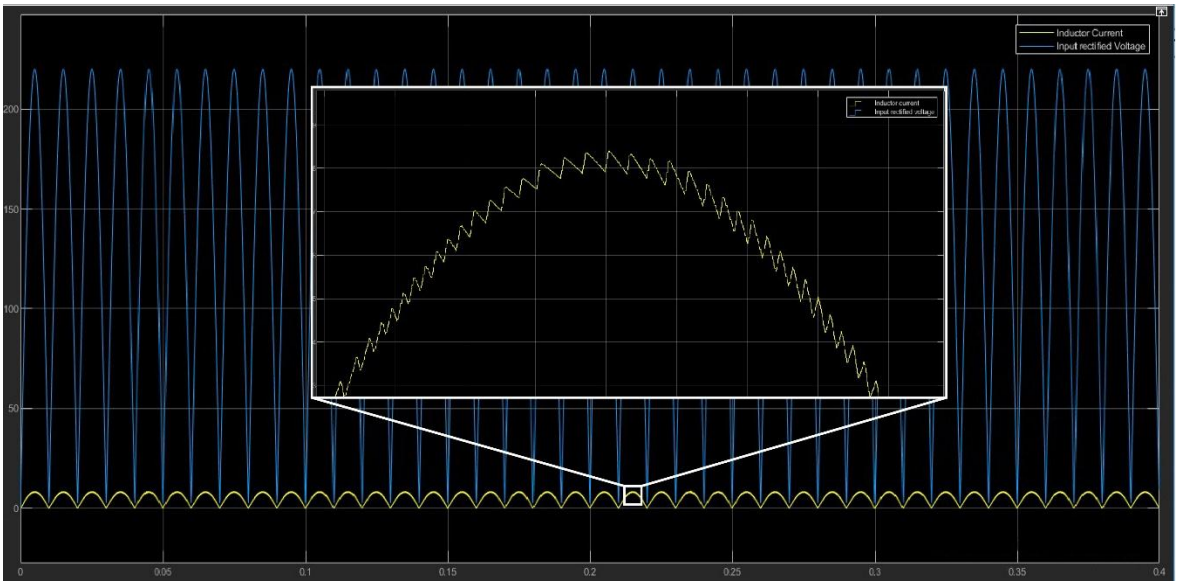

Figure 4.11 The inductor current waveform for 220V input voltage

The waveform below represents the output voltage waveform for the 220V input voltage.

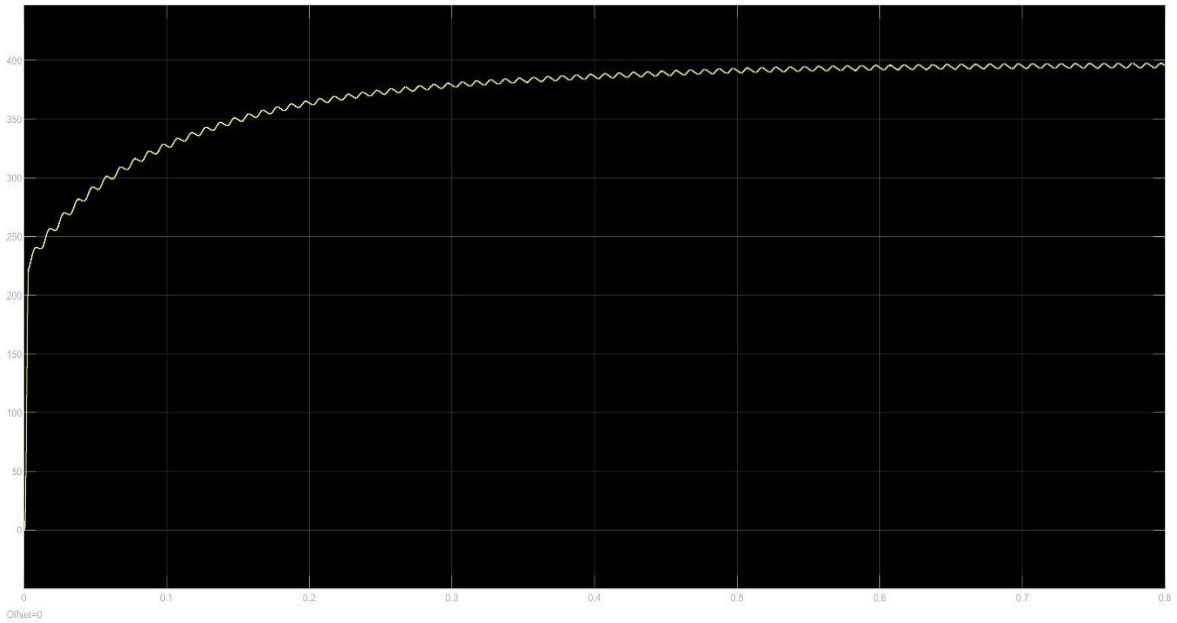

Figure 4.12 The output voltage waveform for 220V input voltage

4.2.2.1 Discussion

In the above simulation results, it is shown that a sinusoidal input current waveform is achieved for 220V since the current waveform is tracking the reference voltage. These two align very well and there seems to be no noticeable phase-shift between the waveforms.

- The inductor current matches the reference curve very well and there is no zero-crossing distortion present.
- The ripple at the inductor current is approximately 0.2A which is in the desired region(less than 20%), where due to the fast switching operation, the current increases and decreases without reaching zero which represents a continuous mode operation.
- The overshoot at the transient state of the output voltage is eliminated, which is desirable in boost converters' topologies. The output voltage waveform is almost a DC waveform, with some ripple during the steady state of about 1.2V peak approximately which is an acceptable result for this topology.

» The power factor of PF=0.9989 is achieved with the designed controller, and the THD is only 2.5%.

4.3 Conclusion

A comparison between current loop and voltage loop for the analog and the digital controllers:

- **Current loop**

Table 4.2 Current loop control parameters

	Analog control for PFC	Digital control for PFC
Overshoot	exists	No overshoot
Settling time(sec)	0.01	0.01
Peak inductor current ripple	1.2A	0.2A

As can be seen, on the current loop, the digital controller is superior when it comes to peak inductor current ripple, where it decreases from 1.8A to 0.2A.

- **Voltage loop**

Table 4.3 Voltage loop control parameters

	Analog control for PFC	Digital control for PFC
Overshoot	exists	No overshoot
Settling time (sec)	0.5	0.5
Peak output voltage ripple	1.5V	1.2V

The output voltage ripple is enhanced from 1.5V peak on the analog controller to 1.2V peak on the digital one. Also, the overshoot is eliminated on the digital controller.

Table 4.4 Comparison between the parameters of a boost converter without PFC, with analogically-controlled PFC and with digitally-controlled PFC

	Boost converter without PFC	Analog control for PFC	Digital control for PFC
PF	67 %	98.79 %	99.89 %
THD_i	116.6 %	9.7 %	2.50 %
$Efficiency$	43.9%	93.2 %	95.6%

After viewing the results of the simulations and Table 4.4, it is clear that the digital controller is superior in terms of performance parameters. The power factor correction boost converter is a very powerful tool to decrease power losses, and both analog and digital controllers give the desired results.

When analog control is applied, implementing optimal control requires much complex inflexible designs. Digital control implements optimal control without extra components.

Conclusion

Our project has been carried out to get an optimal control of the power factor correction using analog and digital PID control techniques.

According to the obtained results, it was shown by comparison of input current shapes, output voltage waveforms and the computed power factor and total harmonic distortion values of a boost converter with and without power factor correction stage, that having a power factor correction in a power conversion system is vital for power consumption efficiency.

The comparison of the input current and output voltage waveforms of both our designed analog and digital PID controllers show us that the digital controller out-performed the analog one in terms of overshoot, settling time and rising time. Therefore, digital control of power factor correction shows more accuracy in regulating the shape of the input current thus reducing its total harmonic distortion to a minimal value (less than 10%) and increasing the power factor to an optimal value (above 99%). The obtained results which are a more precise copy of our objectives approve the quality of our design.

Future research

Can be made in three directions:

- Other control methods will be used for a better performance, the design will be developed using genetic heuristic optimization techniques (PSO and DE).
- Implementation of the digital controller on a DSP.
- Extending this research to Uninterrupted Power Supply (UPS) systems.

References

[1] M. S. Kurma, "Topological issues in single phase power factor correction," M.Tech.project, National Institute of Technology, Rourkela, 2007.

[2] H.Z.Azazi, E. E. EL-Kholy, S.A.Mahmoud and S.S.Shokralla, "Review of Passive and Active Circuits for Power Factor Correction in Single Phase, Low Power AC-DC Converters," In Proc. the 14th International Middle East Power Systems Conference'10, 2010, pp. 217-224.

[3] S. P. B. A. Hsu, L. Rensink, and R. D. Middlebrook, "Modelling and analysis of switching dc-to-dc converters in constant-frequency current-programmed mode," In Power Electronics Specialists Conference. PESC '79. IEEE 10th Annual, 1979, pp. 284-301.

[4] C. C. Clark, "Digital Control Techniques for Power Quality Improvements in Power Factor Correction Applications", M. App. Sci. thesis,British Columbia University, British Columbia, 2012.

[5] M. K. W.Wu andC. K. Tse, "A review of EMI problems in switch mode power supply design," *J. Electric. Electron. Eng. Australia*, vol. 16, no. 3/4, pp. 193-204, 1996.

[6] R. Dash, "Power Factor correction using parallel boost converter", M. Tech. thesis, National Institute of Technology, Rourkela, 2007.

[7] F. F. Mazda, *Power Electronics Handbook*. Amsterdam: Elsevier, 1997.

[8] M. H. Rashid, *Power Electronics: Circuits, Devices, and Applications*.Upper Saddle River, New Jersey: Prentice Hall, 2013.

[9] Fair Child Semiconductor, Appl.Note 42047 Power Factor Correction (PFC) Basics,pp. 1-10

[10] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications, and Design*. New York: Wiley, 1995.

[11] Y. Rozanov, S. Ryvkin, E. Chaplygin, and P. Voronin, *Power Electronics Basics: Operating Principles, Design, Formulas, and Applications*. Boca Raton, FL: CRC Press, 2015.

[12] Unitrode, Application Note U-140, pp. 356-369.

[13] S. B. Santra, "Design and Implementation of UPFC based Boost Converter for Efficiency

Optimization of Brushless DC Motor Drive System", M. Tech. thesis,Jadavpur University, Kolkata, 2012.

[14] Y. Yingyi, F. C. Lee, P. Mattavelli, and L. Pei-Hsin, "I^2 Average Current Mode Control for Switching Converters," Power Electronics, IEEE Transactions on, vol. 29, pp. 2027-2036, 2014.

[15] C. Buttay. "File:Boost chronogram discontinuous.png." Internet: https://en.wikipedia.org/wiki/File:Boost_chronogram_discontinuous.png, Mar. 12, 2006 [Apr. 28, 2019].

[16] C. Buttay. "File:Boost chronogram.svg." Internet: https://en.wikipedia.org/wiki/File:Boost_chronogram.svg, Mar. 12, 2006 [Apr. 28, 2019].

[17] S. S. Ang and A. Oliva, *Power-switching Converters*. Boca Raton, FL: CRC Press, 2005.

[18] Unitrode, Design Note DN-62, pp. 1-7.

[19] STMicroelectronics, Application Note AN-628, pp. 5-11.

[20] B. M. Chen, Topic: "Digital Control Systems (Part 2)." EE3304, Department of Electrical and Computer Engineering, The National University of Singapore, Singapore, 2015.

[21] Unitrode, Application Note U-134, pp. 271-272.

[22] F. C. Lee, Topic: "Power Converter Modeling and Control." ECE5254, Virginia Polytechnic Institute, USA, 2003.

[23] C. Zhou and M. M. Jovanovic, "Design Trade-offs in Continuous Current-mode Controlled Boost Power-Factor Correction Circuits," In Proc. International High Frequency Power Conversion (HFPC) Conf. '07, 1992, pp. 209-220.

[24] M. M. Karapartal, "Design, Analysis and Implementation of an Interleaved PFC Boost DC-DC Converter for an LCD TV Power Supply", M. Sci. thesis, Dokuz Eylül University, İzmir, 2011.

[25] FreescaleSemiconductor, Appl.Note AN5257Average Current Mode Interleaved PFC Control,pp. 9-10.

[26] M. K. Kazimierczuk, *Pulse-Width Modulated DC-DCPower Converters*. Hoboken, NJ: Wiley, 2008.

Appendices