People's Democratic Republic of Algeria
Ministry of Higher Education and Scientific Research

University M'Hamed BOUGARA – Boumerdes

Institute of Electrical and Electronic Engineering

Department of Power and Control

Final Year Project Report Presented in Partial Fulfilment of
the Requirements for the Degree of

MASTER

In **Electrical and Electronic Engineering**

Option: **Power Engineering**

Title:

FPGA Based Control of Three Level NPC Inverter

Presented by:

- **KHENFER Zoubir**

Supervisor:

Dr. B. METIDJI

Registration Number:……/2016

Dedication

I have a great pleasure to dedicate this modest work
To my Beloved Mother, my Father
To my Dear Sisters, Brothers, Uncles, Aunts and Cousins

To Adel, To Juba

To all my Friends

To all my Teachers from primary school to my last year of university

And to all with whom I spent wonderful moments

Zoubir KHENFER

ACKNOWLEDGEMENT

I want absolutely to express my thanks and deep gratitude to my supervisor ***Dr. METIDJI Brahim****, for his consistent support, orientation, advices and encouragement during the accomplishment of this project.*

I would like to thank all the people who contributed in any way to the work described in this thesis.

Abstract

Power electronics is the technology associated with efficient conversion, control and conditioning of electric power from its available input in to the desired electrical output form. The actual work falls into this scope presenting an FPGA based control and implementation of three levels voltage NPC inverter.

The Multi-Carrier Sinusoidal Pulse Width Modulation (MC-SPWM) is the control method adopted in order to digitize power so that a sequence of voltage pulses can be generated by the on and off of the power switches. writing a VHDL code of the adopted modulation technique ,checking the code on MODELSIM software then loading the code to the FPGA kit through QUARTUS environment are the carried steps in order to end up with the right switching signals.

The design and implementation of the appropriate gate drive circuitry is a the next step in order to assure a suitable driving circuit that is required to supply the necessary charge to the power valves gates .

Using this control method and the gate driving circuitry along with the specified topology of the three levels NPC inverter leads to the desired results of this works. Results that are presented and discussed.

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Introduction

In recent years, there has been increased interest in renewable energy sources, development of this field along with other fields recognize power electronics systems as a core enabling technology. As other engineering fields power electronics is relatively old and vast field. However the area of multilevel power conversion can still be considered young. In 1980, early interest in multilevel power conversion technology was triggered by the work of Nabae, I.Takahashi, and H.Akagi who introduced the neutral-point-clamped (NPC) inverter topology and at that time wide doors where opened for new topologies and new configuration to be dissected, analyzed and manufactured leading to an explosion in the field of multilevel inverters to serve different fields of power engineering.

As mentioned, the three-level NPC converter was the first widely popular multilevel topology. A significant amount of research effort was invested in the development of this family of converters,. This is in part because the converters of this type are currently in the phase of rapid market introduction; this was the motivation for this work to be carried out not only at the theoretical level but also taking the chance to implement this kind of inverters in a laboratory, the actual work is presented in four chapters that are ordered as follows:

The first chapter one through a survey of basic multilevel inverters topologies, their basic principles, it gives a general description of the basic functionality of each of the treated inverters along with the main advantages and drawbacks of each of them giving a comparative study between the different topologies treated .

The second chapter deals with the control methods of the aforementioned inverters taking two examples of them the first being the high frequency switching techniques represented in the sinusoidal pulse width modulation and a representative of low switching frequency techniques which is the selective harmonic elimination.

The third and the fourth chapters are dedicated to the practical side of our thesis starting by the third chapter which is mainly concerned with the utilization of the FPGA board to generate switching signals the programing side is presented and its outcomes examined experimentally .

While the fourth chapter gives a general description for the steps taken in order to implement the three level voltage source NPC inverter. These steps where carried out in the laboratory, their outcomes are detailed and discussed in this last chapter.

1.1 Introduction:

Interest in multilevel inverters has been increasing in the last decades when such kinds of topologies were selected as the power inverters choice in much high voltage and high power applications, due to advantages of high quality wave forms, low switching losses; their structure allows them to process high voltages while generating low harmonics with low electromagnetic capability concerns. The basic idea behind the multilevel inverters is to synthesize a sinusoidal voltage waveform from several voltage levels, typically obtained from capacitor voltage sources, as the number of level increases, the synthesized output waveform adds more steps leading to a staircase wave which approaches the sinusoidal waveform. Basically the synthesized output is achieved by dividing the dc link potential into multiple sections, so that each phase leg can switch between multiple voltage levels. Shown in figure 1-1.a tow level inverter figure (a) for example generates tow levels with respect to the midpoint terminal M .the three level figure (c) can produce three, figure (d), while the generalized n-level inverter figure (e) is able to switch among n voltage levels figure (f) [1]

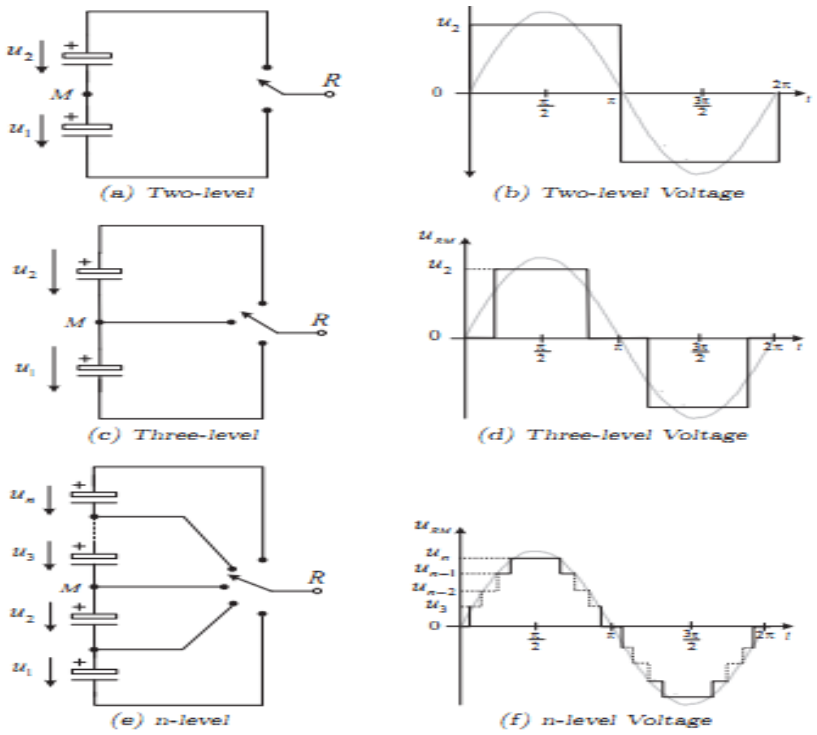


Figure 1-1: simplified circuit and generated output voltage of (a)(b) tow two levels (c) and (d) three levels and (e) (f) n level inverter.

1.2 Basic multilevel inverters topologies

1.2.1 Neutral point clamped inverters:

The neutral point converter proposed by Nabae, Takahashi, and Akagi in 1981 was essentially a three-level diode-clamped inverter .generally In a three phase m - level NPC inverter , each leg is composed of 2(m − 1) series connected switches and (m – 1) dc link capacitors charged with a voltage equal to $\frac{Udc}{(m-1)}$. Under balanced conditions, the maximum blocking voltage applied to the switches is the voltage across one capacitor, thanks to the clamping diodes . One leg of a three - level and five-level diode clamped multilevel structures are shown in Figure 1 .2 The other two legs have the same switch -diode configuration and share the same dc - link source . The input voltage U_{dc} is equally divided by the dc link capacitors C_1 and C_2 . The common terminal of both capacitor s (M point) represents the mid-point terminal with respect to the input voltage. This topology uses the capacitor voltages U_{C1} and U_{C2} to produce three different levels on its output terminal referred to the mid- point M $\frac{Udc}{2}$:, 0 and -$\frac{Udc}{2}$

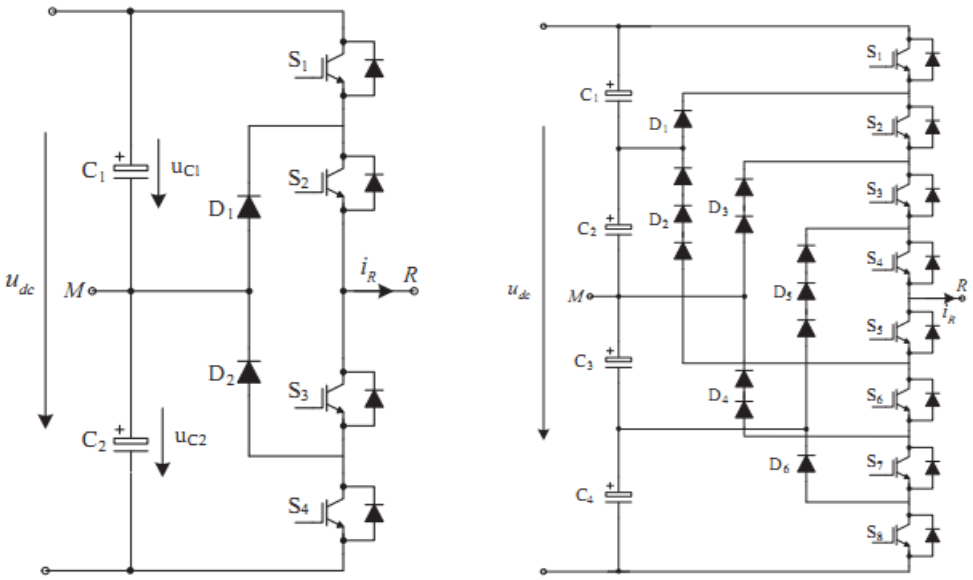


Figure 1-2: Neutral point clamped a) three level and b) five level topology

Output level	**Switching states**			
	S_1	S_2	S_3	S_4
$\frac{Udc}{2}$	1	1	0	0
0	0	1	1	0
$-\frac{Udc}{2}$	0	0	1	1

Table 1-1: Three level NPC inverter output voltage levels and switching states

-A positive $\frac{Udc}{2}$ performed by turning on the switches S_1 and S_2 . For an output voltage equal to 0 the switches S_2 and S_3 are turned on, while the switches S_3 and S_4 are used to generate an output voltage equal to $-\frac{Udc}{2}$. From Table 1 .1 , which summarizes the NPC switching states , it can be seen that switch S_1 conducts only during $U_{RM} = \frac{Ud\,c}{2}$.while switch S_2 is used to change between $\frac{Udc}{2}$and 0 . The same logic is employed on the negative and null output voltages ($-\frac{ud}{2}$and 0) with the switches S_3 and S_4 .When both S_1 and S_2 turn on, for example , the clamping diode D_2 balances the voltage sharing between S_3 and S_4 , with S_3 blocking the voltage across C_1 and S_4 the voltage across C_2 . Therefore, the blocking voltage is half of the dc voltage source U_{dc}. However , unbalance in the dc - link capacitors voltage may produce excessively large voltage in the respective switching devices , and in consequence a failure may occur .Therefore , a well performed control of the two voltages must be carried carefully . Generally this type of configuration has some features as follows:

- For the clamping diodes a high voltage rating is required .although each active switching device is only required to block a voltage level of $\frac{Udc}{(m-1)}$the clamping diodes need to have differant voltage rating for reverse voltage blocking for example some of the interconnection diodes have to block voltage up to $\frac{(m-2)\,Udc}{m-1}$
- From table 1-1 we notice that in such configuration there is unequal distribution of conduction between different switches as some would conduct only at some values of the output while others may conduct approximately over the entire cycle such conduction inequality necessitates different current rating for switching devices

- This topology presents an issue with capacitor voltage unbalance where In most applications, the power inverter is required to transfer real power from DC to AC so when operating at unity power factor, discharging time for each capacitor is different, resulting in unbalanced capacitor voltages between the different levels. However, when operating at zero power factor, the capacitor voltages can be balanced by equal charge and discharge in one half cycle. This indicates that the inverter can theoretically transfer pure reactive power without the voltage unbalance problem[2]

- **Advantages :**

-All of the phases share a common dc bus, which minimizes the capacitance requirements of the inverter.

- For fundamental frequency switching, efficiency is proven to be high.[3]

- **Disadvantage** :

As the number of levels goes high, the number of clamping diodes also goes high. This introduces a problem in terms of both cost and packaging process, as well as exhibiting parasitic inductances; this fact plays a role in limiting the number of levels in NPC multilevel inverters to only seven or nine levels in practice

-Real power flow is difficult for a single inverter because the intermediate dc levels will tend to overcharge or discharge without precise monitoring and control.

1.2.2 T-Type topology of NPC inverters

The figure below illustrates the basic topology of a T type three phase neutral point clamped.The general idea behind this configuration can be stated as follows :The conventional two level voltage source inverter topology is extended with an active, bidirectional switch to the dc-link midpoint . In this configuration conduction takes place in the form of T shape to give the three level output voltage which also give this topology its name For The T-type NPC inverter to be implemented a per phase single bidirectional switch is needed .Bi-directional switches are typically realized with a common-emitter series connection of two IGBT / Free Wheeling Diode (FWD) modules. As a consequence, two series connected semiconductor components, a diode and an IGBT, conduct the current through the bi-directional switch.

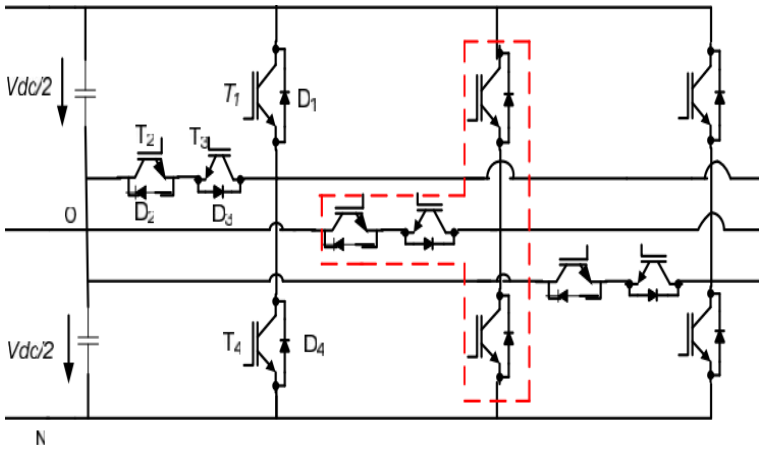


Figure 1-3 Circuit diagram of Three level T-Type inverter.

. The high side and the low-side switches (T1 /D1 and T4 /D 4) are typically implemented with 1200-V IGBTs/diodes as the full dc-link voltage has to be blocked. Differently, the bidirectional switch to the dc-link midpoint has to block only half of the dc-link voltage. It can be implemented with devices having a lower voltage rating, in the case at hand two 600-V IGBTs including antiparallel diodes are used Due to the reduced blocking voltage, the middle switch shows very low switching losses and acceptable conduction losses, although there are two devices connected in series. An Additional benefits related to using single 1200-V devices to block the full dc-link voltage are reduced conduction losses, if bipolar devices are considered .Whenever the output is connected to (P) or (N), the forward voltage drop of only one device occurs, contrary to the NPC topology where always two devices are connected in series . The conduction losses are considerably reduced making the T type NPC an interesting choice even for low switching frequencies. For one leg the output voltage and the switching pattern is as table 1-2 below (Operation of the other legs also same as this, they have the phase displacement of 120 degrees each.)[4]

V_{out}	T_1	T_2	T_3	T_4
$V_{dc}/2$	1	0	0	0
0	0	1	1	0
$-V_{dc}/2$	0	0	0	1

Table 1-2 Switching states of three level T type NPC

1.2.3 Flying - Capacitor Converters:

Meynard and Foch introduced a flying-capacitor-based inverter in 1992. The design structure of this inverter is based upon the same principal of that of the diode clamped configuration except that in here, capacitors are used as the clamping elements instead of diodes ,the figure below illustrates the fundamental building blocks of a single-phase half-bridge flying capacitor based three -level inverter

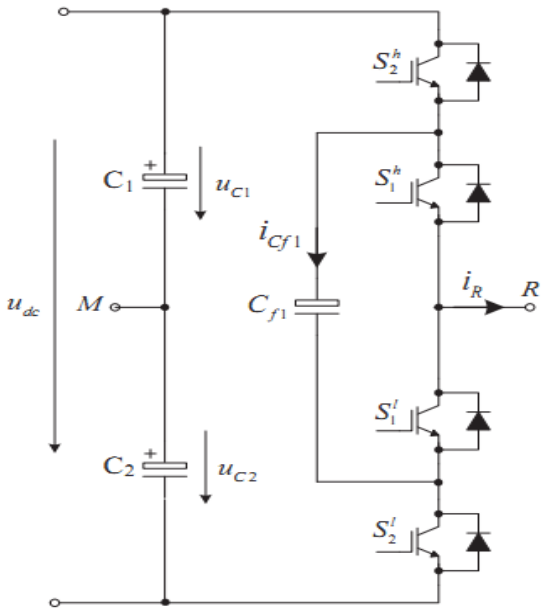


Figure 1-4 Three Level flying capacitor.

For a full-bridge, each phase leg has an identical structure. Assuming that each of the capacitors has the same voltage ratings as that of each of main switches, the voltage level between the clamping points can be identified through the number of capacitors connected in series. Each phase form an independent block in terms of capacitors used, in other words different phases don't share capacitors. However, the main DC bus capacitors are shared by different phases. For an m-level FC converter, a total of $\frac{(m-I).(m-2)}{2}$ auxiliary capacitors per phase leg are required in addition to (m-1) main DC bus capacitors, assuming that all capacitors have the same voltage rating. However, an m-level NPC inverter only requires (m-1) capacitors [5]. The features of this type of the inverters are summarized in the following table :

Output levels	Switching states
	S^h_1 S^h_2 S^l_2 S^l_1
$U_{dc}/2$	1 1 0 0
0	1 0 1 0
0	0 1 0 1
$-U_{dc}/2$	0 1 0 1

Table 1-3 three level FC inverter output voltage levels, respective switching.

The voltage synthesis in a FC inverter has more flexibility than that in a NPC inverter. Taking a three-level FC as an example, Table 1.3 lists the possible switching states In order to obtain three voltage level.[6]

Advantages:

-Phase redundancies are available for balancing the voltage levels of the capacitors. Real and reactive power flow can be controlled.

-The large number of capacitors enables the inverter to ride through short duration outages and deep voltage sags.

Disadvantages:

-Control is complicated to track the voltage levels for all of the capacitors. Also, recharging all of the capacitors to the same voltage level and startup are complex. [3]

-Switching utilization and efficiency are poor for real power transmission.

-In terms of cost and packaging issues flying capacitor topology can be even worse than that of the NPC inverters due to the large number of capacitors this problem gets worse as the number of levels increases.

1.2.4 Cascaded H-Bridges:

A single-phase structure of an m-level cascaded inverter is illustrated in Figure 1-5. Each separate dc source (SDCS) is connected to a single-phase full-bridge, or H-bridge, inverter. Each inverter level can generate three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$ by connecting the dc source to the ac output by different combinations of the four switches, S_1, S_2, S_3, and S_4. To obtain $+V_{dc}$, switches S1 and S4 are turned on, whereas $-V_{dc}$ can be obtained by turning on switches S_2 and S_3. By turning on S_1 and S_2 or S_3 and S_4, the output voltage is 0. The ac outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels m in a cascade inverter is defined by m = 2s+1, where s is the number of separate dc sources.

An example phase voltage waveform for an 11-level cascaded H-bridge inverter with 5 SDCSs and 5 full bridges is shown in Figure 1.5. The phase voltage van = va1 + va2 + va3 + va4 + va5.[7]

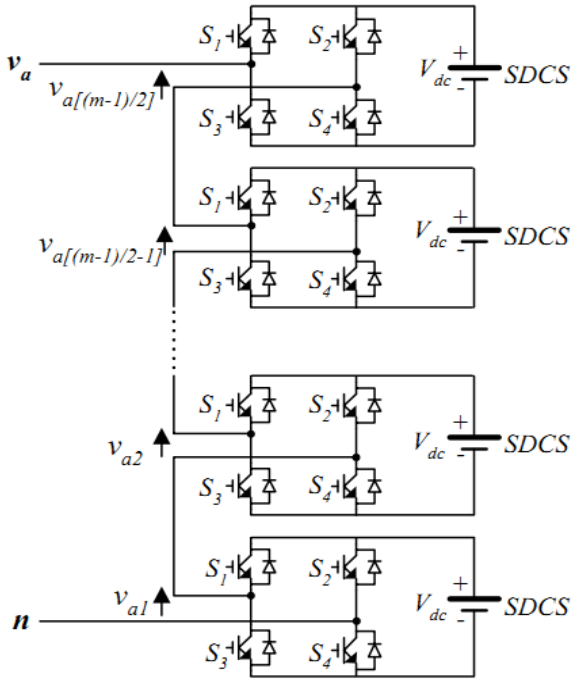


Figure 1-5: Single-phase structure of a multilevel cascaded H-bridges.

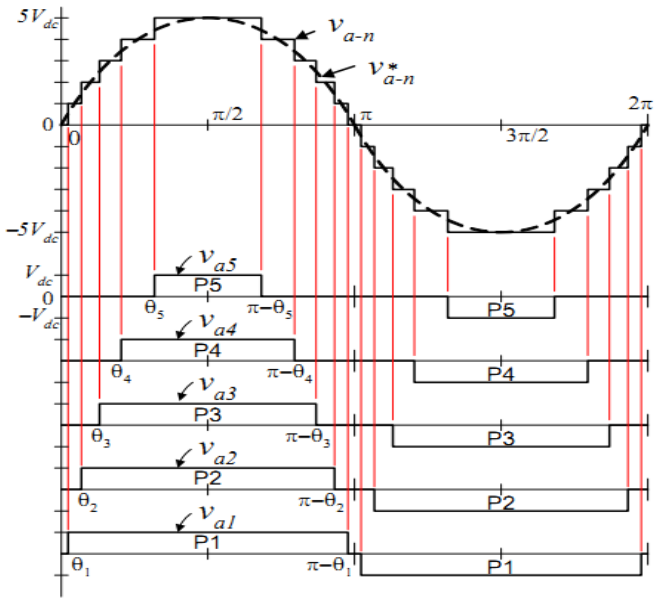


Figure 1-6: Output phase voltage waveform of an 11-level cascade

The few number of components used to achieve the same number of levels is the major advantage of this topology compared to other component-requiring configuration such as

NPC and Flying Capacitor . Clamping element are not needed in this type of inverters. In addition, it provides the flexibility of expansion to a higher number of levels. The whole structure can be considered as a combination of complete independent cells consisted from single phase H bridge inverter. Thus, the ability of adding extra level is always possible. However, besides all the advantages mentioned, the necessity of multiple isolated dc sources tends to limit the utilization of such topology. One alternative is to employ a transformer with multiple isolated secondaries or even several transformers. Nevertheless, adapting such solution will lead even to a more complex circuit.[2]

1.2.5 Generalized Multilevel Current Source Inverter:

The vast majority of multilevel inverters that can be come across would be mainly multilevel voltage sources ,the multilevel voltage inverters are the most widely used .However there do exist multilevel Current Source Inverters (CS I). The general principal behind the multilevel current sources is to inject levels of current to a load thanks to power electronic components. The GMCSI is a three-phase topology that consist of a number of "current -source six-valve modules", the figure below illustrates this valve modules in a dashed line (see Figure 1-7)

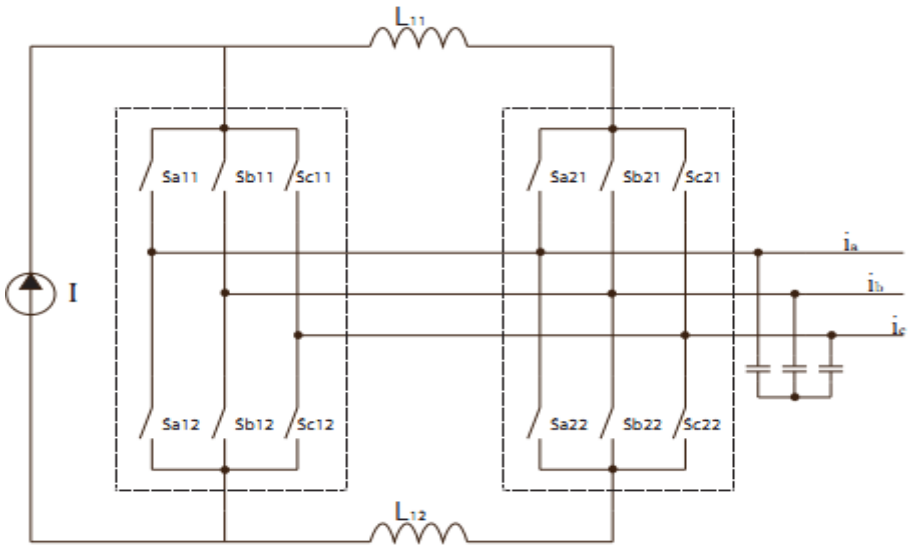


Figure 1-7: A three-phase five-level Generalized Current Source Inverter.

This configuration contains also (m-3) positions with inductors to smooth the DC-side current and to divide its source into deferent current ratings. Only one current source is needed. Compared to other topologies in high power application the GCSI doesn't require the use of transformer which can be considered as an advantage compared to other VSI configurations. As well as that it doesn't require great amount of components as compared to those voltage based -topologies .in contrast, one of the drawbacks of such topology is the current unbalance that may take place at the level of the smoothing inductors .However redundant switch can be used to solve this unbalance problem.

I_a	I_b	I_c	Switches on
0	I	-I	Sb_{12}, Sb_{22}, Sc_{11}, Sc_{21}
$\frac{I}{2}$	-I	$\frac{I}{2}$	Sa_{11}, Sb_{12}, Sb_{22}, Sc_{21}
I	-I	0	Sa_{11}, Sa_{21}, Sb_{12}, Sb_{22}
I	$\frac{-I}{2}$	$\frac{-I}{2}$	Sa_{11}, Sa_{21}, Sc_{12}, Sc_{22}

Table 1-4: Examples for some GMCSI switching

The number of switching states for a GMCSI can also be calculated by the number of modules n (n = (m -1)/2) with the equation Nc = 3^{2n} where Nc is the number of switching states. For instance the five-level GMCSI, Nc = 3^{2*2} = 81 , meaning 81 switching states on five levels for three phases. Some of these states is shown in Table 1.3. The voltage across the inductor is the reason why there is a current unbalance in an inductor,. Depending on if the voltage positive or negative the current through the inductors will ramp up or down from its supposed value. By the proper change of the states the current in the inductor can be maintained at balanced levels. And because the topology is a current-based one the current in an inductor is dependent upon the inductor position within the configuration**,**. For every valve module that is passed the current amplitude drops$\frac{I}{n}$ since the amount of current that goes through every closed switch (in every module) is $\frac{I}{n}$.Moreover at a at any moment ,only one switch on the upper half and a single one on the lower half are turned on. This also means that the current rating of a valve should be at least $\frac{I}{n}=\frac{2I}{m-1}$

Since different amounts of current flow through the inductors depending on their position it is necessary to add inductors in parallel closer to the source if components with the same current rating are to be used. The number of the required modules for m current level is identified using$\frac{m-1}{2}$ when a module is consisted of 6 switches. For the position of inductors we have total number of (m-3) positions. With the different inductors having the same current rating .the number of inductor is $\frac{m-1}{2}$ ($\frac{m-3}{2}-1$).For instance for a seven-level GMCSI this would mean two inductors in parallel closest to the source (on each side, top and bottom) and one inductor at the second inductor position. For a nine-level GMCSI three inductors in parallel would be in the first position followed by two and one inductor.[8]

1.3 Conclusion:

Due to the ability of using more than two voltage levels to synthesize a sinusoidal output voltage, the use of multilevel inverters has been heavily expanded by industry since the introduction of the Neutral- Point Clamped three - level inverter in the eighties. Besides improving the spectrum quality when compared to the conventional two - level topology

multilevel inverters permit to employ power devices with lower voltage rating and lead to reduced switching losses and electromagnetic interference effects .Among the multilevel topologies mentioned, Neutral- Point Clamped And Flying - Capacitors structures are based upon the same concept of using voltage clamping components, diodes and capacitors respectively. However, although these concepts have been extensively used by industry, the practical number of levels is limited by the required number of series connected clamping elements .The necessity to use other design approaches rather than "the clamping - components –based- design" have allowed other structures to emerge. Among of which is the cascaded H- bridge inverters that are able to produce a multilevel output voltage by series connection of single phase H- bridge inverters. Nevertheless, they require a separate dc source for each single –phase cell, which is considered as a limiting factor to the use of such topologies in industrial applications .In terms of the comparison between CSI and VSI topologies, In industrial markets, the VSI design has proven to be more efficient, have higher reliability and faster dynamic response [2], and be capable of running motors without de-rating.

2.1 Introduction

Pulse-width modulation (PWM) is the basis for control in power electronics. The theoretically zero rise and fall time of an ideal PWM waveform represents a preferred y of driving modern semiconductor power devices .The vast majority of power electronic circuits are controlled by PWM signals of various forms. The rapid rising and falling edges ensure that the semiconductor power devices are turned on or turned off as fast as practically possible to minimize the switching transition time and the associated switching losses. Although other considerations, such as parasitic ringing and electromagnetic interference (EMI) emission, may impose an upper limit on the turn-on and turn-off speed impractical situations, the resulting finite rise and fall time can be ignored in the analysis of PWM signals and processes in most cases. The modulation methods used in multilevel inverters can be classified according to switching frequency. Methods that work with high switching frequencies have many commutations for the power semiconductors in one period of the fundamental output voltage. A very popular method in industrial applications is the classic carrier-based sinusoidal PWM (SPWM) that uses the phase-shifting technique to reduce the harmonics in the load voltage. Methods that work with low switching frequencies generally perform one or two commutations of the power semiconductors during one cycle of the output voltages, generating a stair- case waveform selective harmonic elimination is the representative of this family.[10]

2.2 SPWM control methods:

In inverter circuits, the inverter output is expected to be sinusoidal with magnitude and frequency controllable. To reach this goal, the SPWM control method is employed. In this scheme, the PWM signals are generated from the comparison of a fundamental sinusoidal waveform and a high frequency carrier waveform, as shown in figure 2.1. The frequency of the triangular waveform establishes the inverter switching frequency and is generally kept constant along with its amplitude. The amplitude modulation ratio ma, is defined as the ratio of A_0 the amplitude of the modulating signal and Ac the amplitude of the carrier (triangular) signal.

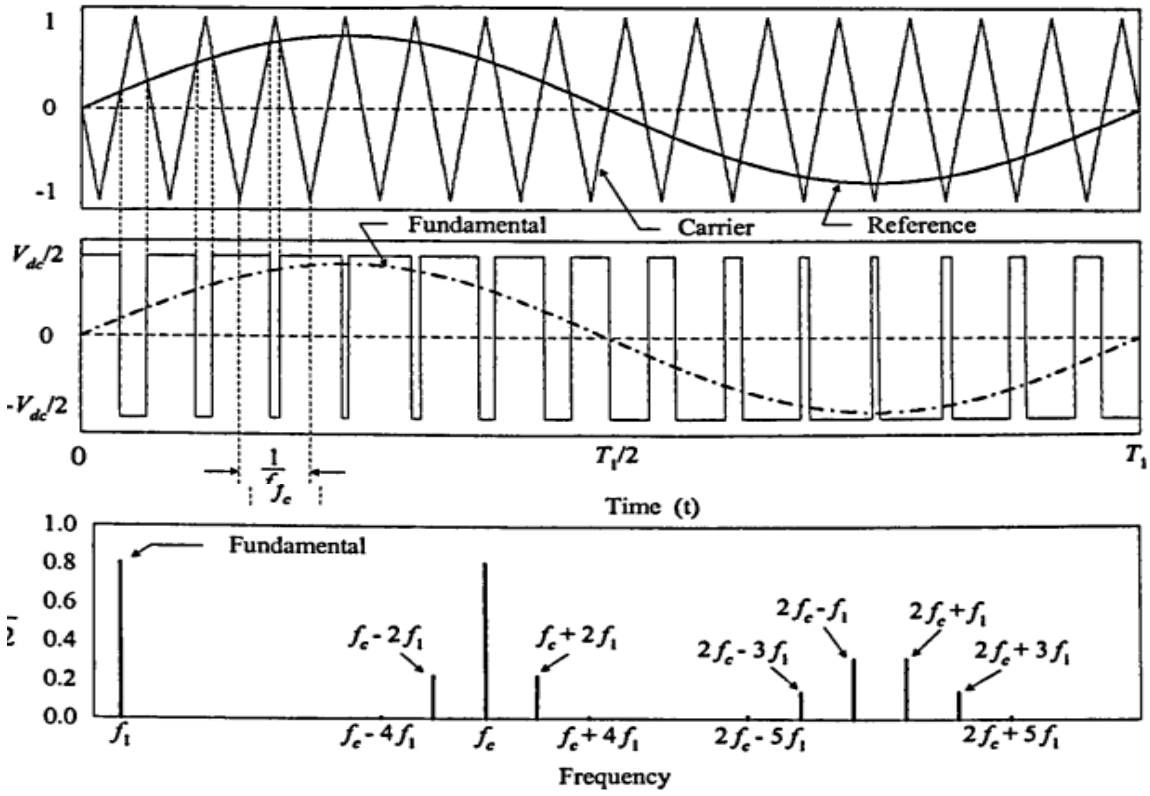


Figure 2-1: Bipolar SPWM applied to the single phase half –bridge inverter: reference sinusoidal and carrier triangular signals for ($fc=15f_1$ and $m_a=0.8$), output voltage waveform, Normalized harmonic amplitude of the voltage waveform V_{Ao} respectively.

-The amplitude modulation ratio ma is defined as the ratio of A_0, the amplitude of the modulating signal and Ac the amplitude of the carrier (triangular) signal

$$m_a = \frac{A_0}{A_c}$$

The SPWM scheme has the following important basic features: (when ma≤l):

The amplitude of the fundamental frequency component is proportional to the amplitude modulation ratio ma. For a single-phase half-bridge inverter, the peak amplitude of the fundamental frequency component V_{AO1}:is expressed by: V_{AO1}=ma $.\frac{Vdc}{2}$ where V_{dc}, is the DC voltage. For a single-phase full-bridge inverter, the line-to-line voltage output peak amplitude of the fundamental frequency component

V_{AB1} is expressed by: $V_{AB1}=ma.V_{dc}$

For a three-phase two-level conventional inverter, the line-to-line voltage output peak amplitude of the fundamental frequency component V_{AB1} is expressed by:

$$V_{AB1}=ma.\frac{\sqrt{3}}{2}.V_{dc}$$

The harmonics in the inverter output voltage waveform appear as sidebands centered around the switching frequency fc and its multiples that is, around harmonics fc, 2fc, 3fc, and so on. Theoretically, the frequencies at which voltage harmonics occur can be indicated as

$$f_h = jfc \pm kf_l$$

where f_1 is the fundamental frequency, j and k are integers. When j is odd, k is even. When j is even, k is odd. For a single-phase half-bridge inverter shown in figure 2-2

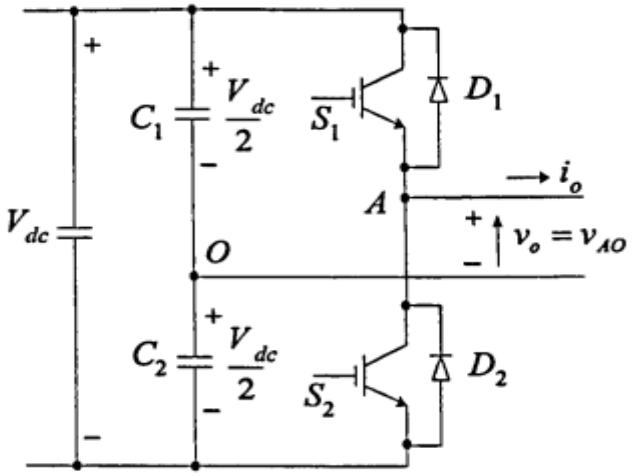


Figure 2-2: A single-phase half-bridge VSI circuit.

A so-called bipolar SPWM scheme can be employed, which is illustrated in figure . 2.1 For a single-phase full-bridge inverter shown in figure. 2.2

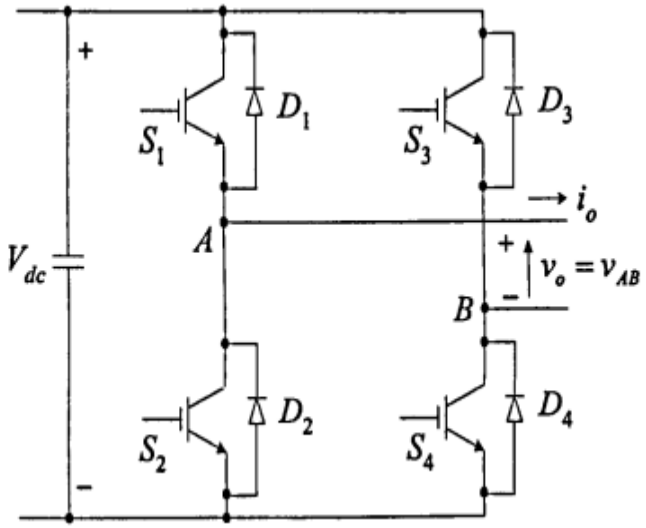


Figure 2-3 : single-phase full-bridge inverter

Two types of SPWM schemes can be chosen. One is SPWM with bipolar voltage switching in which the diagonally opposite switches S_1, and S_4 switch on and off simultaneously (i. e., they are regarded as a switch), S_2 and S_3 are regarded as another complementary switch pair of $S_1$and S_4 switches. The output voltage changes between $+V_{dc}$ and $-V_{dc}$, the waveform is similar to the output voltage in half-bridge inverter, as shown in figure 2-1. Another is SPWM with unipolar voltage switching. With this type of scheme, the switches in the two legs are not switched simultaneously. The legs A and B are controlled separately by comparing one triangular signal with two sinusoidal control signals respectively as shown in the figure below .

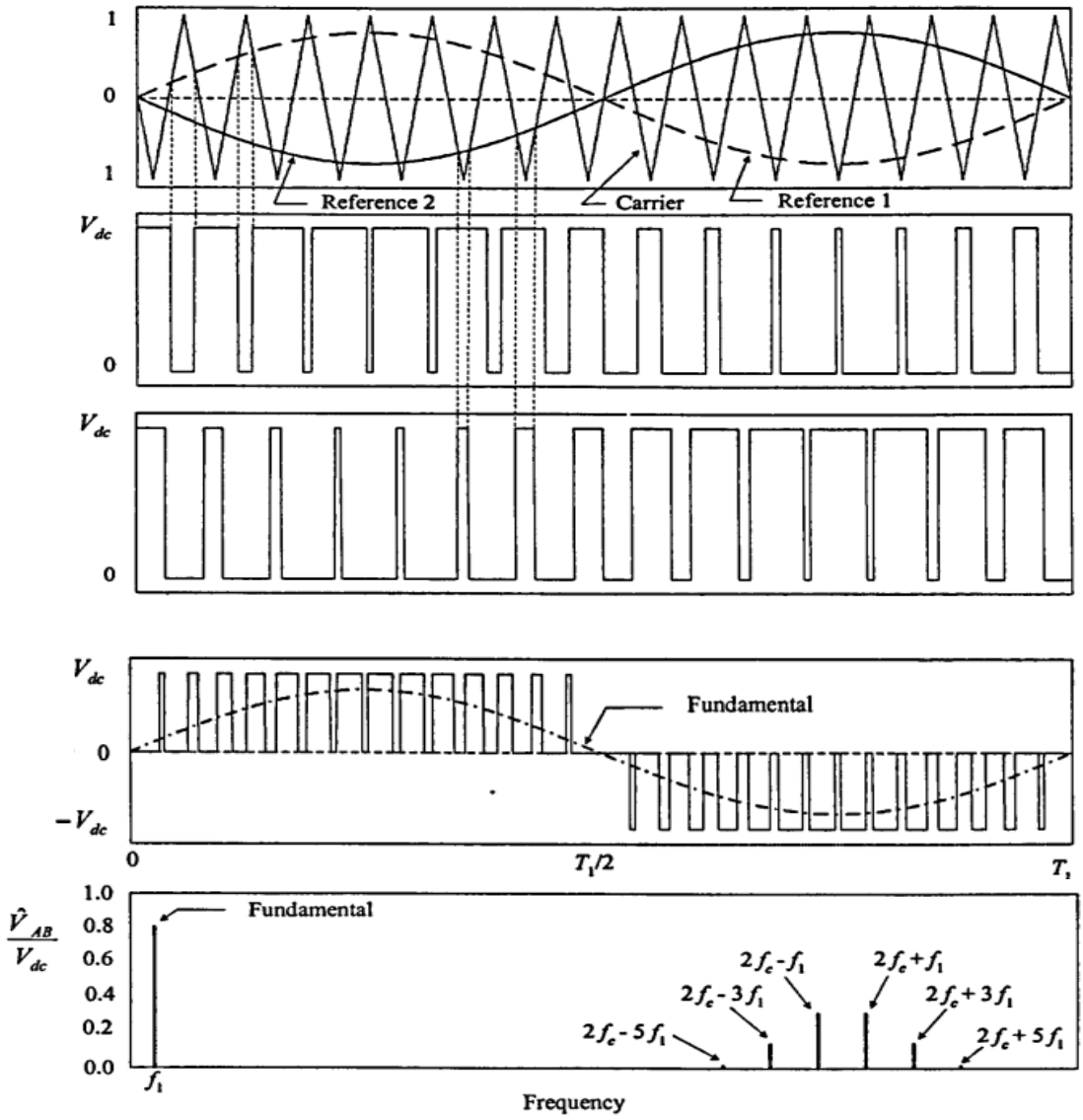


Figure 2-4: Unipolar SPWM for the single-phase full-bridge inverter: Two reference signals (sinusoidal) and one carrier (triangular) signal (fc=15f_1, and ma=0.8),Output voltage waveform v_{AN}. Output voltage waveform v_{BN}, Output voltage waveform V_{AB}, Normalised harmonic amplitude of the voltage waveform V_{AB}.

The output voltage changes between $+V_{dc}$, and zero or zero and $-V_{dc}$,.This scheme has the advantage of effectively doubling the switching frequency as far as the output harmonics are concerned, compared to the bipolar voltage-switching scheme. The harmonics can be written as:

$$f_h = j.(2.fc\ ) \pm k.f_1$$

Where f_1 is the fundamental frequency j and k are integers. When j is odd, k is even. When j is even, k is odd. Also, the voltage jumps in the output voltage at each switching are reduced to Vdc,, as compared to $2V_{dc}$, in bipolar voltage switching scheme.

- For a three-phase inverter shown in figure 2-5,

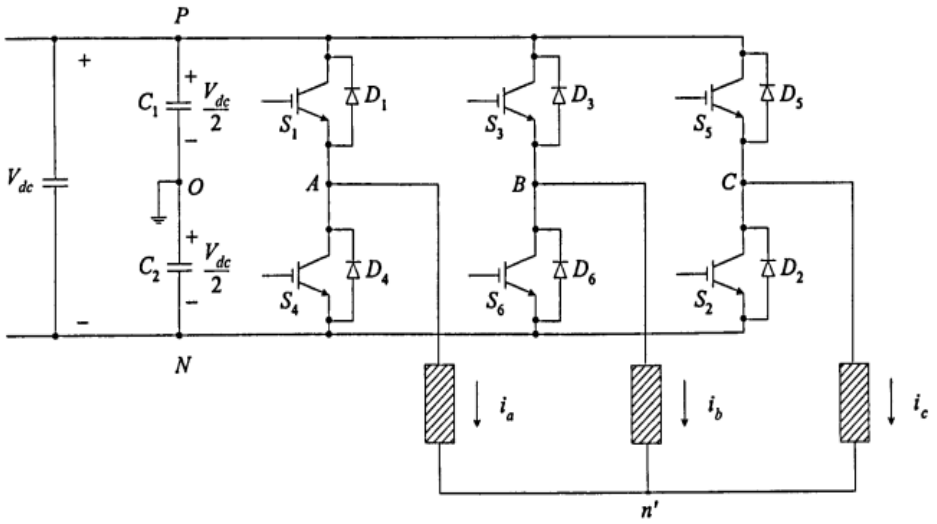


Figure 2-5: A conventional three-phase VSI circuit.

to obtain balanced three-phase output voltages, the same triangular voltage waveform. is compared with three sinusoidal control voltages that are 120° out of phase, as shown below [4]

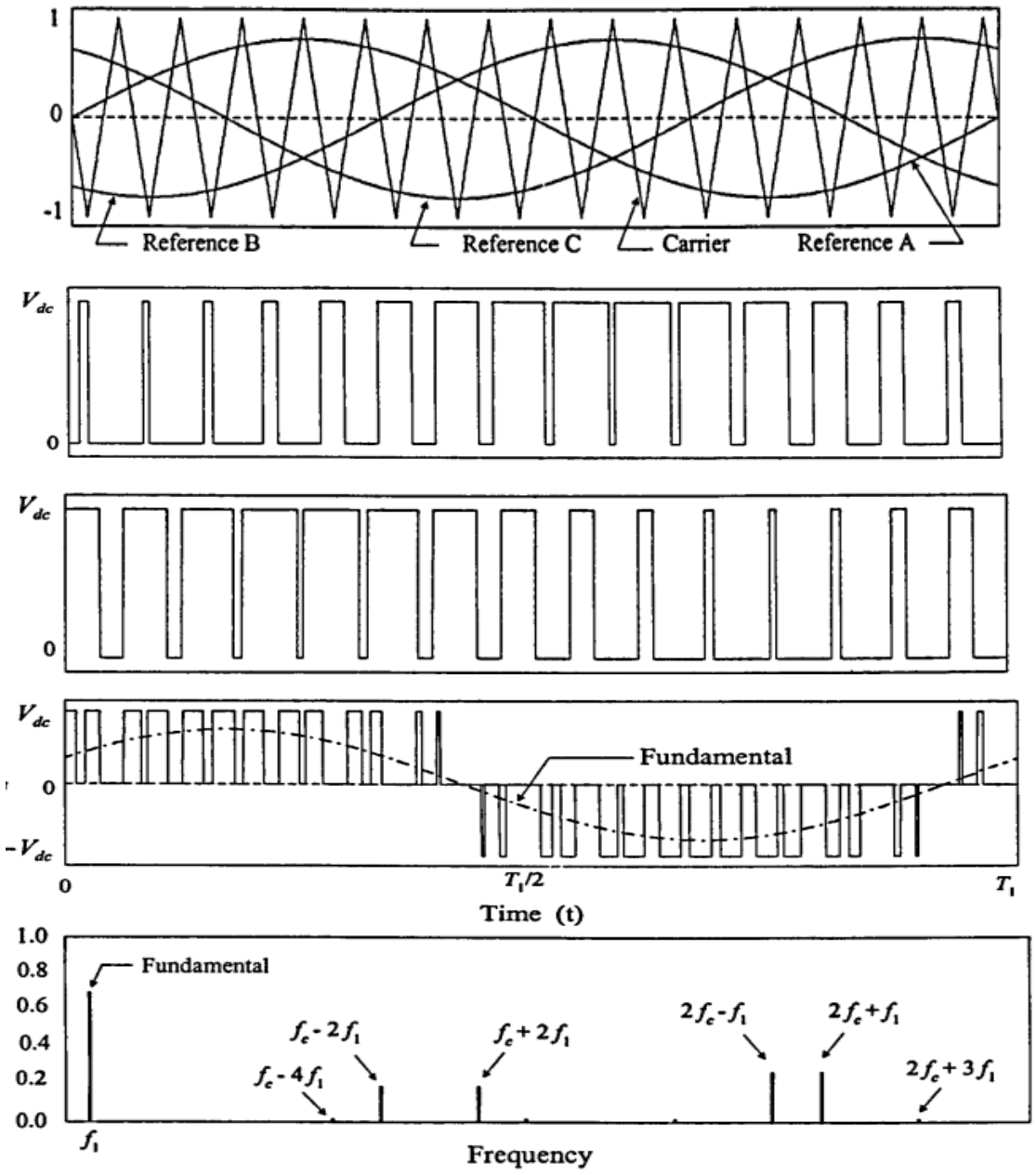


Figure 2-6: Bipolar SPWM for the conventional two-level three-phase inverter:Reference signals (sinusoidal) and carrier (triangular) signal f=15f_1 and ma=0.8),Output voltage wavefomV_{AN} and Output voltage waveform V_{BN} respectively, Output voltage waveform V_{AB}- (d) Normalized harmonic amplitude of the voltage waveform V_{AB}

.

2.3 Multi-carrier SPWM techniques:

Carrier based modulation for more than two level inverter requires more carrier signals. For n level inverter minimum n-1 carrier signals are needed. Each carrier signal is responsible for a pair of switches. One switch is controlled directly by the rectangular signal and second one is controlled by negative sequence. Multiple carrier signals in multilevel inverters create various possibilities of mutual locations of those signals. It has been recognized that different MSPWM methods are suitable for different multilevel topologies. For instance, the PS-MSPWM method is suitable for flying capacitor inverters and cascaded inverters , while CD-MSPWM methods are suitable for the NPC inverter . First, in order to describe and evaluate the different methods, some definitions are given below:

-The frequency modulation ratio m_f,

$$m_f=\frac{f_c}{f_0}$$

where fc, is the frequency of the carrier signal and f_0, is the frequency of the modulating signal.

-The amplitude modulation ratio ma with ma, defined for each modulation technique in Table 2.1, where A_0 is the amplitude of the modulating signal and Ac, is the amplitude of the carrier (triangular) signal, m is the number of the voltage level.

CD-MSPWM	PS-MSPWM
$ma=\frac{A0}{(m-1)Ac}$	$ma=\frac{A0}{Ac}$

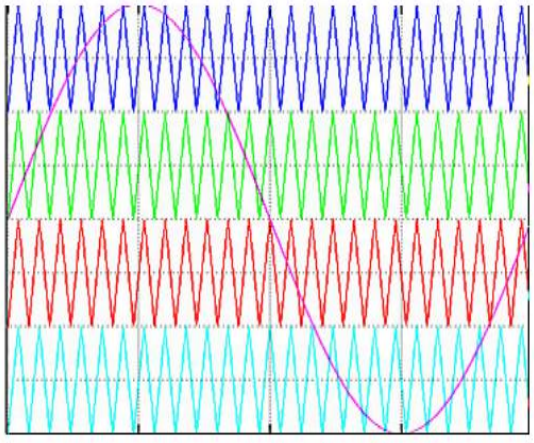
Table 2.1 modulation ratio for each MSPWM

2.3.1 Disposition Multi-carrier SPWM techniques

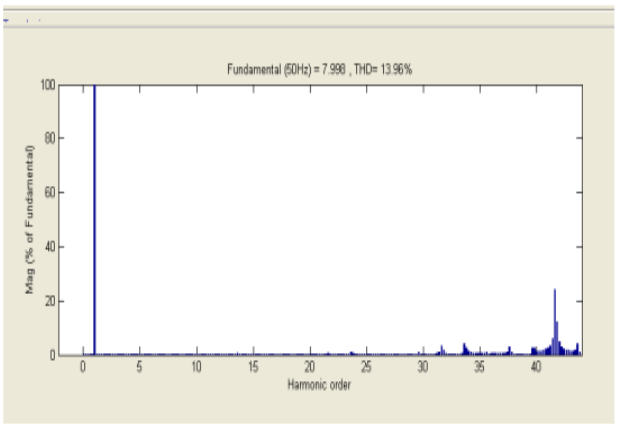
For an m-level inverter, m-1 carriers with the same frequency f, and same amplitude Ac are disposed such that the bands they occupy are contiguous. The reference, or modulation waveform has amplitude A_0 and frequency f_0 and it is centered in the middle of the carrier set. The reference is continuously compared with each of the carrier signals. If the reference is greater than a carrier signal, then the active device corresponding to that carrier is switched on, and if the reference is less than a carrier signal, then the active device corresponding to that carrier is switched off. According to the different dispositions of carrier bands, there are three methods, provided that the number of levels of an inverter is an odd number: in-Phase Disposition (PD), Alternative Phase Opposition Disposition (APOD), and Phase Opposition Disposition (POD). [11]

2.3.1.1 In-Phase Disposition control Method

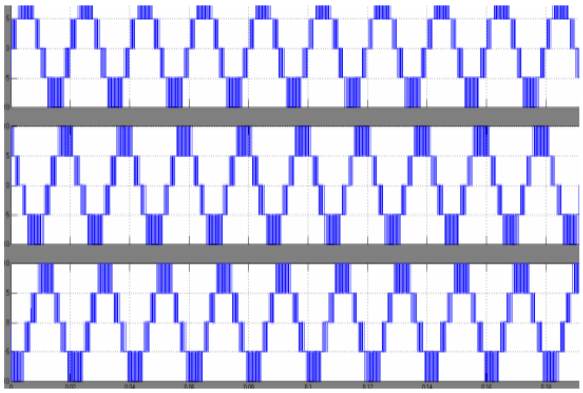
In this method, all the carriers are in phase. For this technique, significant harmonic energy is concentrated at the carrier frequency fc .Figures below illustrate the PD strategy, the output phase voltage waveform and the corresponding spectrum.



a)



b)



(c)

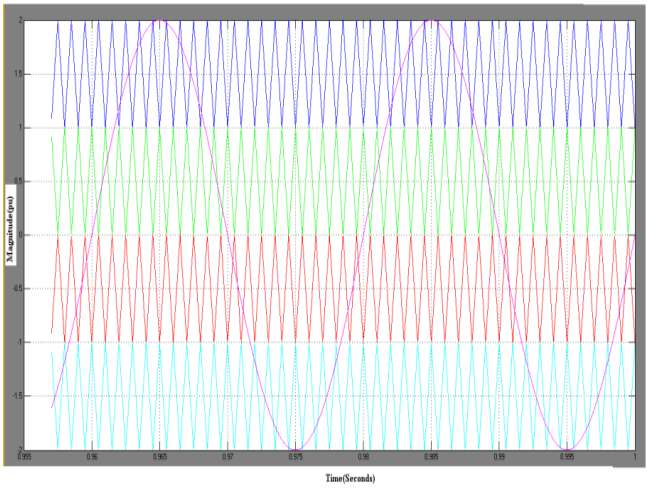
Fig 2-7 a) Carrier arrangement for bipolar mode of PD technique .

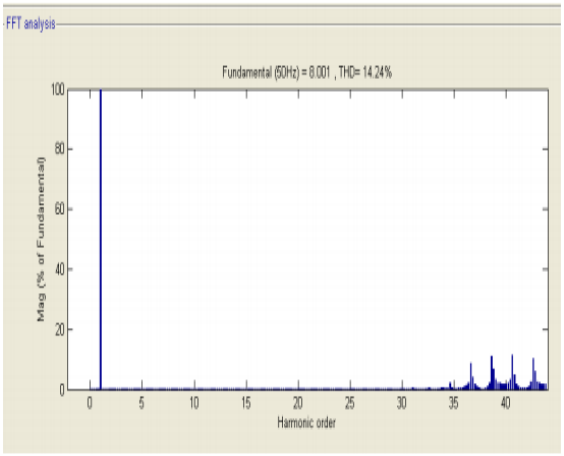
b)Frequency spectrum for PD technique in unipolar mode for ma 0.8.

c) Phase voltage using PD technique in bipolar mode for ma=0.8.

2.3.1.2 Alternative Phase Opposition Disposition Control Method:

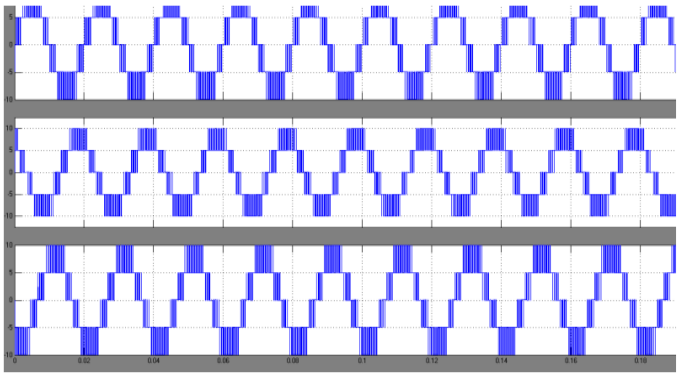
In this method, each carrier band is shifted by 180° from the adjacent bands. With this method, the most significant harmonics are centered in the form of sidebands around the carrier frequency f_C harmonics occur at fc Figures illustrates the APOD strategy, the output voltage phase waveform and its spectrum.





(a) (b)

(b)



c)

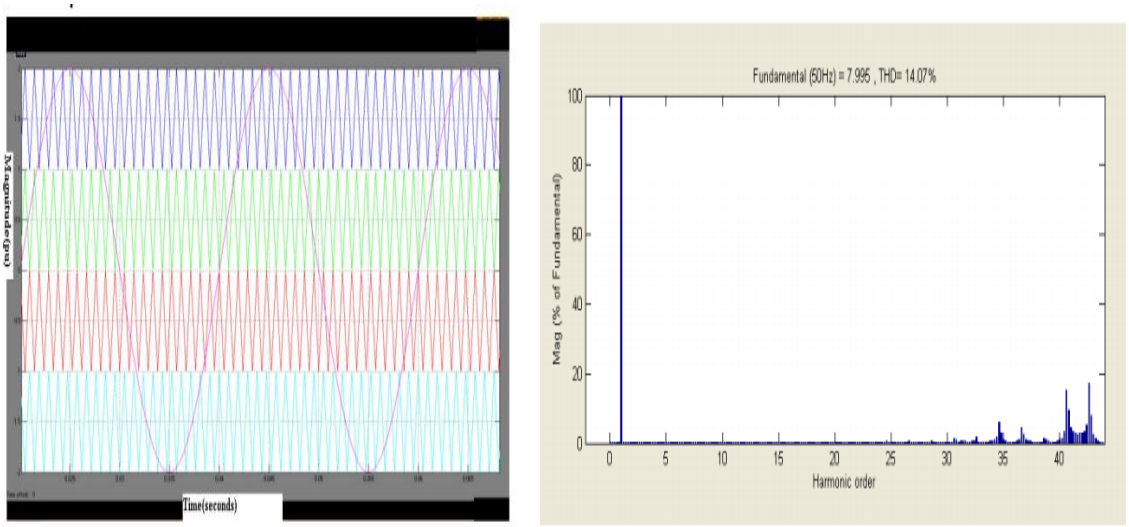
Figure 2-8: a) Carrier arrangement for bipolar mode of APOD technique

b)Frequency spectrum for APOD technique in unipolar mode for ma 0.8

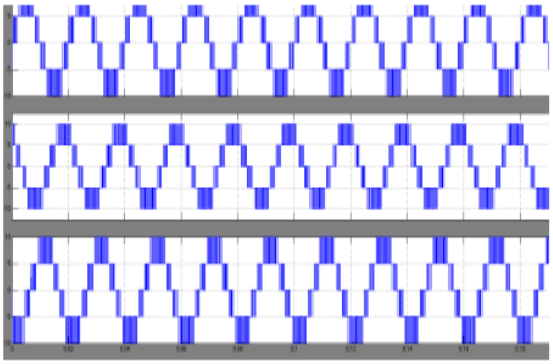
c) Phase voltage using APOD technique in bipolar mode for ma=0.8

2.3.1.3 Phase Opposition Disposition Control Method:

In this method, the carriers above the zero reference are in phase, but shifted by l80° from those carriers below the zero reference. The significant harmonics are located around the fc, for both the phase and line-to-line voltage waveform. Figures illustrate the POD strategy, the output voltage phase waveform and the corresponding spectrum.



a) b)



c)

Figure 2-9: a) Carrier arrangement for bipolar mode of POD technique

b) Frequency spectrum for POD technique in unipolar mode for ma = 0.8

c) Phase voltage using POD technique in bipolar mode for ma=0.8

-For the CD-MSPWM methods, the harmonics in the inverter output voltage waveform appear as sidebands, centered around the switching frequency and its multiples. The frequencies at which voltage harmonies occur can be indicated as:

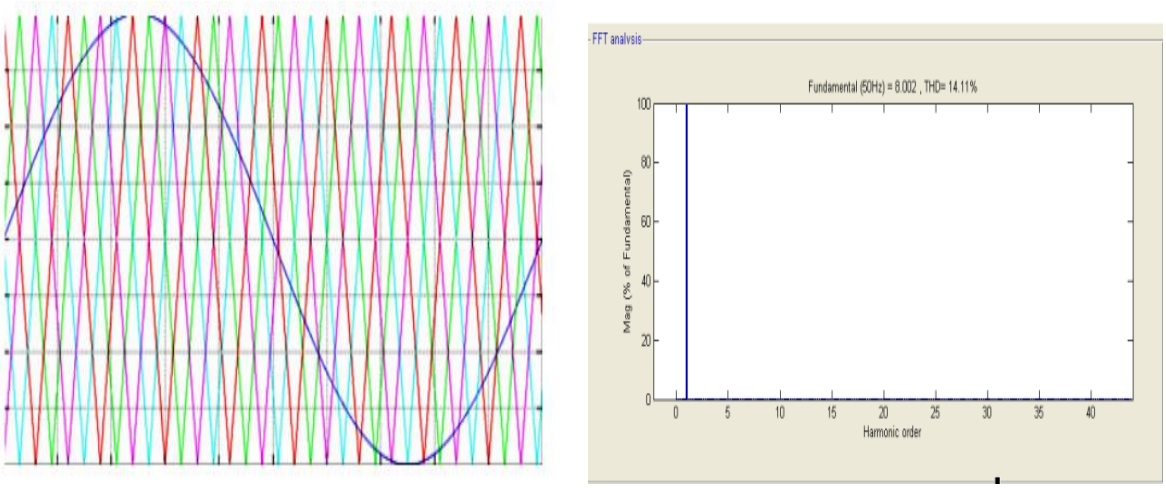
$$f_h = (j.m_f \pm k).f_0$$

where j and k are integers. When j is odd, k is even. When j is even, k is odd

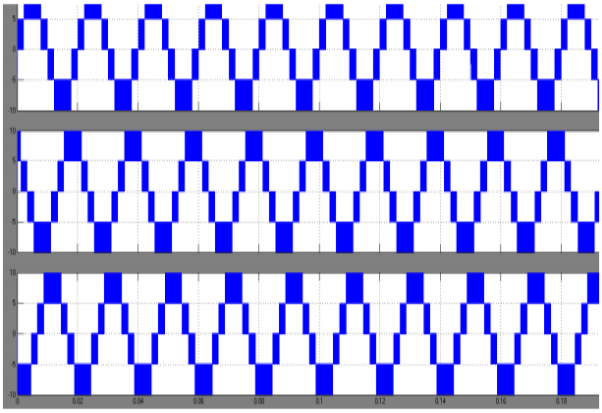
2.3.2 Phase Shifted MSPWM Technique:

For an m-level inverter, m-1 carriers with the same frequency f, and same amplitude A are phase shifted by some degrees $(2\pi/(m-1)$. They are compared with the modulation sinusoidal signal. For example, for a five-level FC converter, the sinusoidal modulation signal is compared with four triangular carrier signals that are phase shifted by 90 degrees (i. e., time shifted by T/4, where T is the period of these carrier signals). The intersections of carrier and modulation signal determine the instants of switching commutations. When the sine value is larger than the carrier value, the switch turns on and otherwise turns off. The resulting four PWM signals are used to control the corresponding switches on the upper leg. The complementary PWM signals then control the switches on the lower leg.[12].

The significant harmonics are located around the (m-1)f, for both the phase and line-to-line voltage waveform. Figures below illustrates the PS-MSPWM strategy, the output phase voltage waveform and its Spectrum Fig 2-15 Phase voltage using PS technique for ma= 0.8 Carrier arrangement for bipolar mode of PS technique. Frequency spectrum for PS technique ma= 0.8



a) b)



c)

Figure 2-10: a) Frequency spectrum for PS technique in unipolar mode for ma = 0.8

b) Carrier arrangement for bipolar mode of PS technique

c): Phase voltage using PS technique in bipolar mode for ma=0.8

2.4 Selective Harmonic Elimination:

In the megawatt range, switching losses caused during the commutation of a power device "especially when the inverter contains freewheeling diodes responsible for large reverse recovery currents during the commutation" can lead to high energy losses in long-term operation. In addition ,it requires larger and more sophisticated heat dissipation systems usually air and water cooled therefore high-switching frequency modulation methods like those based on PWM are not suitable. Unfortunately lowering the carrier frequency in PWM imposes a trade-off between efficiency improvement and power quality reduction .Since linearity is lost in the modulation (carrier gets slow compared to the reference) and low-order sideband harmonics appear which cannot be filtered by the load This results in higher load current THD . As a solution to the aforementioned problem selective harmonic elimination (SHE) has been developed mainly targeted for high-power applications. Basically SHE is a PWM strategy where the commutation angles are predefined and pre calculated in order to eliminate low-order harmonics and keep fundamental component tracking To achieve this the Fourier series of the predefined waveform is used to equal each non-desired low-order harmonic to zero [hence the name] (moreover in three phase systems , all triplen-harmonics in line-to-line voltage will be eliminated by 120 electrical degree phase shift characteristic)nd in additionally match the fundamental component with the desired modulation Index given by the reference . By applying Fourier series analysis, the amplitude of any odd n^{th} harmonic of the stepped waveform can be expressed as below whereas the amplitudes of all even harmonics are zero [13].

Figure 2-16 shows a generalized quarter-wave symmetric stepped-voltage waveform synthesized by (2m+1) a -level inverter, where m is the number of switching angles

$$h_n=\frac{4}{n\pi}\sum_{k=1}^{m}[Vkcos(n\alpha_k)]$$

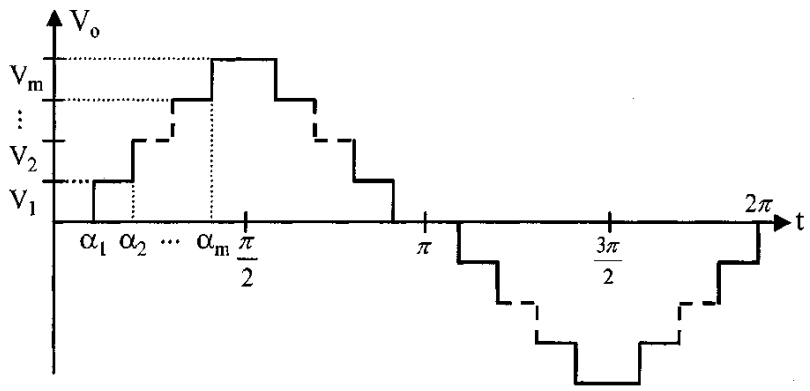


Figure 2-11. Generalized stepped voltage waveform.

Where Vk is the Kth level of dc voltage, n is an odd harmonic order, m is the number of switching angles, and $\alpha_k$is the the switching angle. According to Fig-2 .18 α1 must satisfy α1≤ α 2≤...≤ αm ≤π/2. To minimize harmonic distortion and to achieve adjustable amplitude of the fundamental component, up to harmonic m-1contents can be removed from the voltage waveform. In general, the most significant low-frequency harmonics are chosen for elimination by properly selecting angles among different level inverters, and high-frequency harmonic components can be readily removed by using additional filter circuits. While to keep the number of eliminated harmonics at a constant level. all switching angles ought to be less then $\frac{\pi}{2}$. However if the switching angles do not satisfy the condition, this scheme no longer exists [14]. As a result, this modulation strategy basically provides a narrow range of modulation index, which is its main disadvantage. For example, in a seven-level equally stepped waveform, its modulation index is only available from 0.5 to 1.05. At modulation indexes lower than 0.5, if this scheme is still applied, the allowable harmonic components to be eliminated will reduce from 2 to 1.The total harmonic distortion (THD) increases correspondingly. It is worth mentioning that the set of equations cannot be solved analytically, being one of the disadvantage of SHE .Hence, all the switching patterns have to be pre-calculated offline and stored in lookup tables.

Many types of algorithms are used to solve these equations, mainly based on iterative numerical techniques.

2.5 Conclusion

Multi-carrier based PWM techniques have been investigated to find out a suitable control method that could minimize not only the harmonic content but also the switching losses., the PD method is superior to the other two CDMSPWM methods since it provides the lowest harmonic distortion for the line-to-line voltage and has almost equal number of total switching transitions as others. This is due to the fact that the PD method places significant harmonic energy into a carrier component for each phase leg.. This explains the improved performance of the PD strategy compared to the APOD strategy .Moreover The POD strategy is in turn better than the APOD.[15]

In terms of the elective harmonic elimination its main drawback is the fact it is computed off-line and stored in lookup tables, which are inherently discontinuous in nature and low-order harmonics do appear .These harmonics are fed back in closed-loop operation, affecting the system performance. Hence, SHE is not recommended for high-performance variable speed motor drives.

3.1 Introduction:

In this chapter we are going to give a general description about the practical side of the thesis laying down the broad line of our implementation and the different steps that were carried out in order to end up with the implementation of the voltage source three levels NPC inverter. The laboratory work was mainly divided in between the programing side and the hardware implementation starting by the electronic hub through the implementation of the PWM signals using the Altera DE2 board which will be the main subject of this chapter

3.2 Generation of the PWM pulses :

Through the use of an FPGA kit we were able to generate the electronic signals responsible for the switching process these electronic signals generated by the board were nothing but VHDL code that was loaded into the FPGA through Quartus software ,VHDL code enabled us to generate these signal ;the process of writing the VHDL program was in a way or another the attempt to generate the block of PWM by the means of the MODELSIM environment the main component of the VHDL program are described below Starting in a consecutive way following the order of how the VHDL program was written

3.2.1 Generation of the frequency divider:

In the DE2 FPGA development board, three clocks are provided, in our project we have used that of 50 MHz. But, the operation speed or clock for each module in the design is varying. Therefore, a clock divider is used to generate the clock for sine wave generator, triangular wave generator. In here we describe a frequency divider with VHDL along with the process to calculate the scaling factor .The frequency divider is a simple component which objective is to reduce the input frequency. The component is implemented through the use of the scaling factor and a counter. The scaling factor is the relation between the input frequency and the desired output frequency:

$$S = \frac{f_{in}}{f_{out}}$$

In our case we are asked to generate tow clock dividers one for the reference sinewaves and the other to be for the triangular carrier. The scaling factors of each are determined as follows:

$S = \frac{f_{in}}{f_{out}} = \frac{50\ Mhz}{128.50Hz}$and $S = \frac{f_{in}}{f_{out}} = \frac{50}{128.5KHz}$ respectively taking that the sampling of the sinewave took placethrough the use of 128 samples and the triangular carrier were meant to be of a high frequency near 5KHzThe following figures show the tow obtained clocks after the process of dividing the original clock of the FPGA to the corresponding clockref and clockcar.

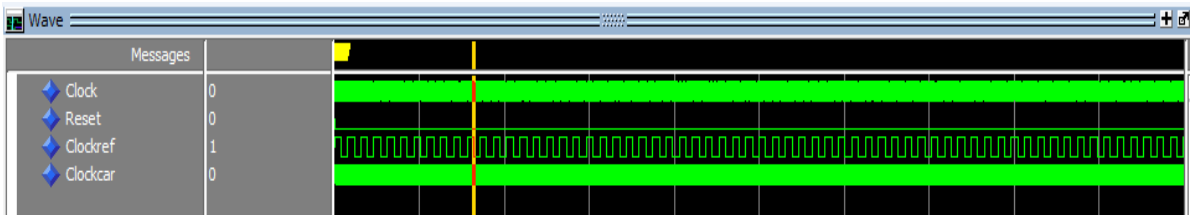


Figure 3-1:generation of the clock dividers

3.2.2 Generation of the triangular wave (the carrier):

Here the concept was simply to use a counter with a flag that controls the direction of the counting. This flag switches when the counting reaches the integer 100,the following figure shows the simulation results of the generation of a triangular waveform with the corresponding clock in MODELSIM environment using the analog format that the MODELSIM provides

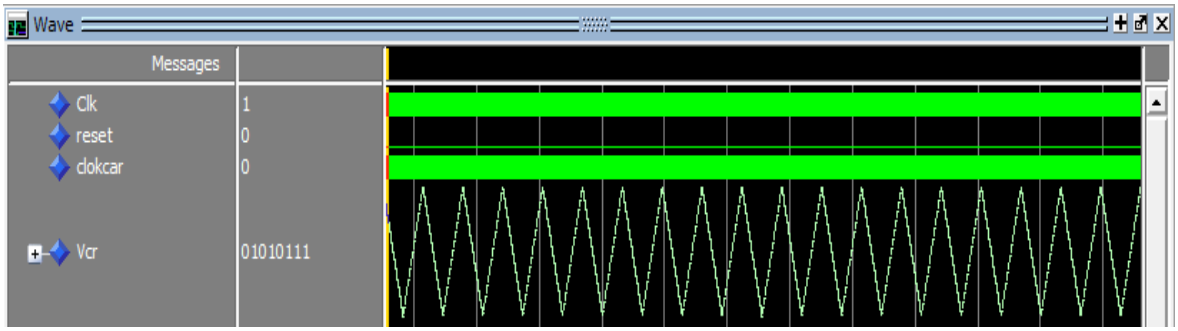


Figure 3-2: generation of the carrier wave

3.2.3 Generation of the sinewave

Here the sinewaves are generated using the concept of a ROM. In other words, a ROM is created that stores the value of sine values from 0 to 2π. Then the ROM is connected to a binary counter and a clkof its ownbesides the read signal and chip select signal inputs. At each rising edge of the clock pulse the binary count is incremented by 1. This causes the sine value stored at the addresses of the ROM to appear at the output. Thus we get a Sine wave signal from the ROM.figure below illustrates this concept.

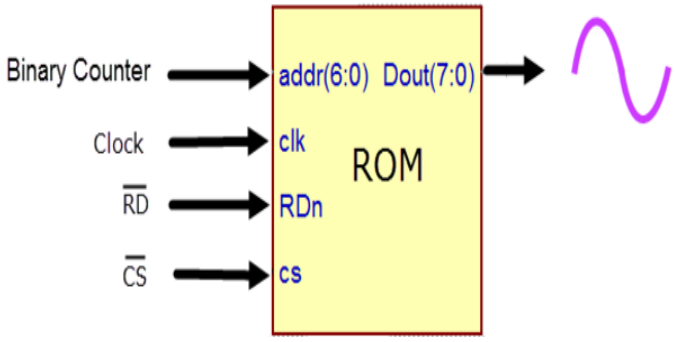


Figure 3-3: Principal of generation of the sinewave

The ROM is implemented as 1D-1D array of both integer types. The address range is from 0 to 127. Each address stores the sine wave magnitude which has range between-100 to 100.In the process, the clk. If the read data and chip select signals are low then we activate the counting, access each of the sine magnitude and thus generate the sine wave. We created the input and output as a standard input and output. That is we used the std_logic_vector for the inputs and outputs. That is why they were converted to integers to access the ROM array. Since we require for this the functions to_integer and to_signed we have declared the numeric_std library. After the count reaches it's end address which is 127 we want the roll back to start fetching from address 0 again. The data at the address is outputted as a std_logic_vector. The cnt+1 is for incrementing the count value.

The values of the sinewave stored in the ROM where generated using Matlab.As the whole system design require us to generate not only one sine wave but three of them being shifted by 120 degrees each ,the same concept is used for each one of them but the idea was to start

reading the data of the same ROM (used to generated the original sinwave) from a different address ,an address that was determined by the relative relationship between the binary number representing the whole 2π(or 360 degree) which is 127 and the desired shift angles which is in our case 120 and 240 So the three were generated just by making the counter starts at different addresses in the ROM,with 127 maintained as the upper limit for counting .the obtained output is an 8 bits vector with the MSB bit representing the sign of the number. The below figures show the simulation trace of the above mentioned waveforms when the code was simulated with Modelism

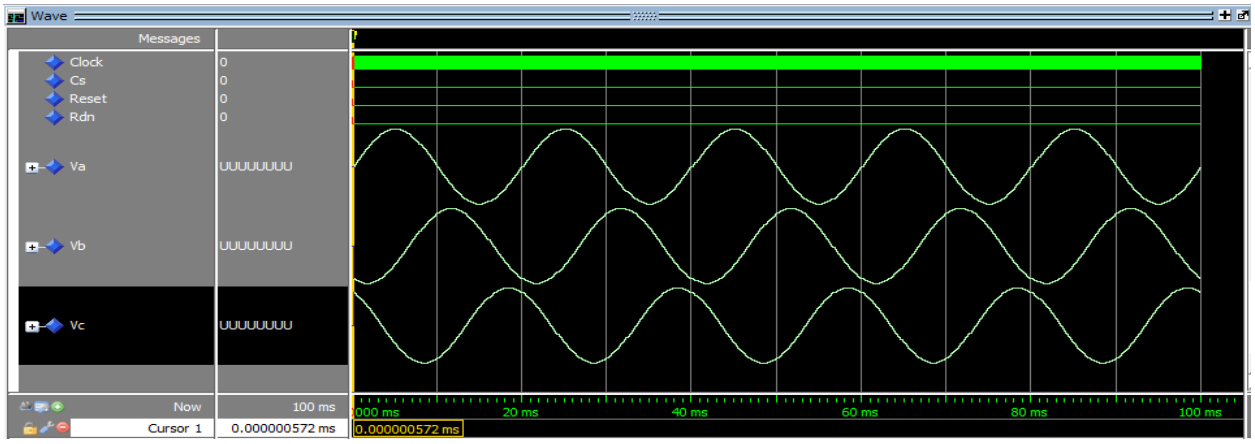


Figure 3-4: generation of the three reference sinewaves

and because we are here in the process of implementing a three level three phase NPC inverter we are required even to break down those 3 sinwaves to 6 ones to be able to carry out the PWM generation process by comparing the obtained sinereferences with the triangular carrier these six waveform were obtained through the breakdown of each sinwave to tow component :the positive half wave and negative half cycle making sure that the negative" half wave forms are inverted to positive one as the below figure shows

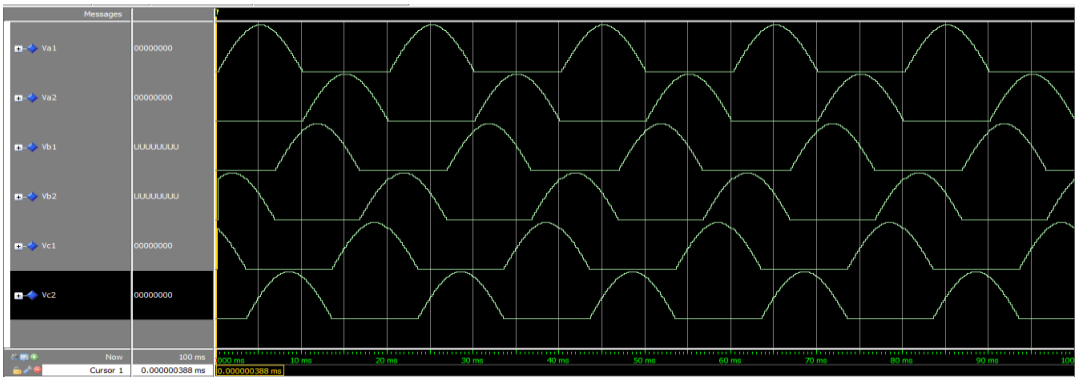


Figure 3-5: generation of six sine half-wave

3.2.4 PWM signal pulses

The different half sine waves are compared with the triangular carrier to obtain six signals these are shown below where the logic was as follows: if the reference signal is greater than that of the triangular the signal outputted is 1 while if the triangular is greater that would result in 0

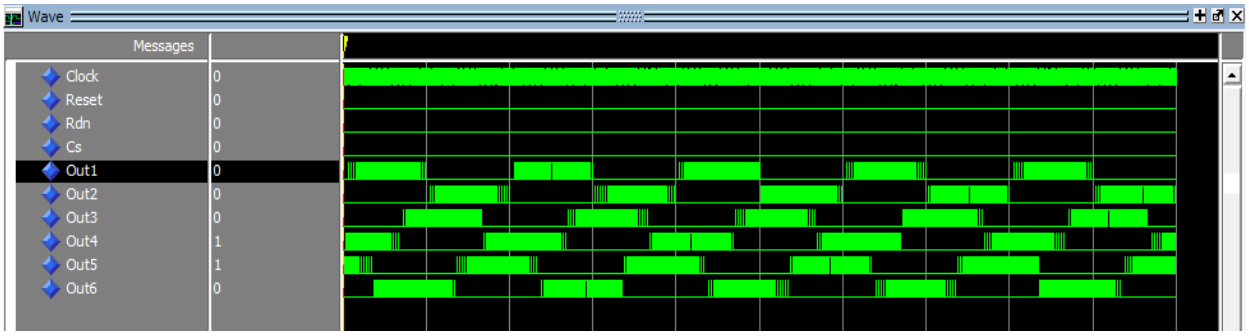


Figure 3-6 generation of the PWM pulses

These 6 signals were under a logical operation of inverting each and every one of them using a not operator to obtain the final twelve signals that each of these signal theoretically will be responsible for switching each MOSFET within the configuration ,these signals are shown in the figure below:

Figure 3-7: generation of the PWM pulses

Practically its not possible to use the direct obtained signals to directly switch the different power valves without introducing a dead time it's extremely important because it will be responsible for preventing each leg from being short circuited by the improper switching of the semiconductor switches.

3.2.5 The dead time

The phase legs of the inverter have to be protected from short circuit. Therefore, a programmable delay-time is introduced in the designed SPWM architecture,and therefore, an appropriate delay time must be inserted between these gating signals the following figure shows the dead time between a tow complementary signals in the first leg

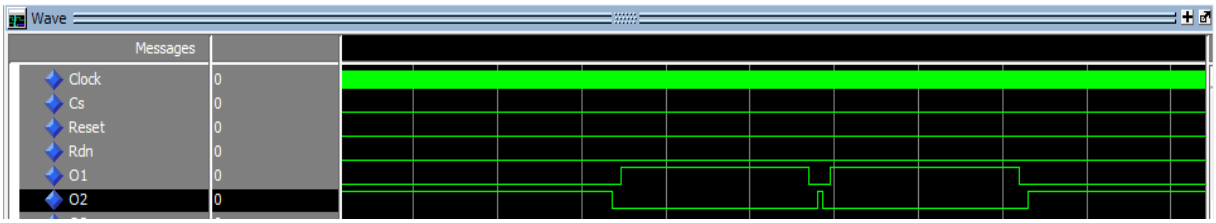


Figure 3-8: dead time effect

This dead time effect can be modeled in the VHDL language by introducing a delay time some microseconds usually 1 to 4 µs to each of the aforementioned signal after introducing the dead time effect the signal will have the following shape (they will not be distinguished from the above signals since the delay time is extremely short compared to the pulses themselves :

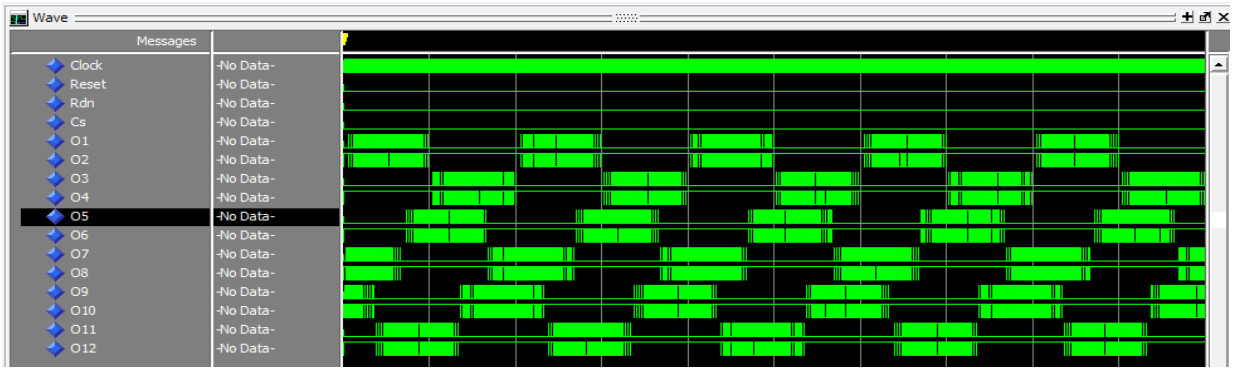


Figure 3-9: generation of the PWM pulses

3.3 Downloading the program to an FPGA

Before being able to download the VHDL program simulated in MODELSIM the Quartus software must be used in order to be able to download the last to the FPGA where the program must be compiled in the Quartus environment .

3.3.1 Quartus:

Programmable logic device design software produced by Altera. Quartus enables analysis and synthesis of HDL designs, which enables the developer to compile their designs, perform timing analysis, , simulate a design's reaction, and configure the target device with the programmer. Quartus includes an implementation of VHDL and Verilog for hardware description, visual editing of logic circuits, and vector waveform simulation[17]. in here the soul purpose we needed quartus software is to load our VHDL code to the FPGA board.

3.3.2 FPGA:

Field programmable Gate Array (FPGA) devices are aimed in the implementation of high performance, large size circuits, thanks to the speed advantage of direct hardware execution on the FPGA, low volume applications, An even more, another important issue in using FPGAs is their re-configurability and reusable hardware architectures for rapid prototyping of the digital system [18].the DE2 FPGA board was utilized in the project ,Our task is to load to the kit our VHDL program , after loading the program on the kit and carrying out the assignment of the output pulses to the GPIO of the board we have connected the GPIO port(JP1) of the FPGA board an oscilloscope to be able to examine experimentally those signals.

3.4 Experimental results

The experimental setup that allows us to get the following results is shown below

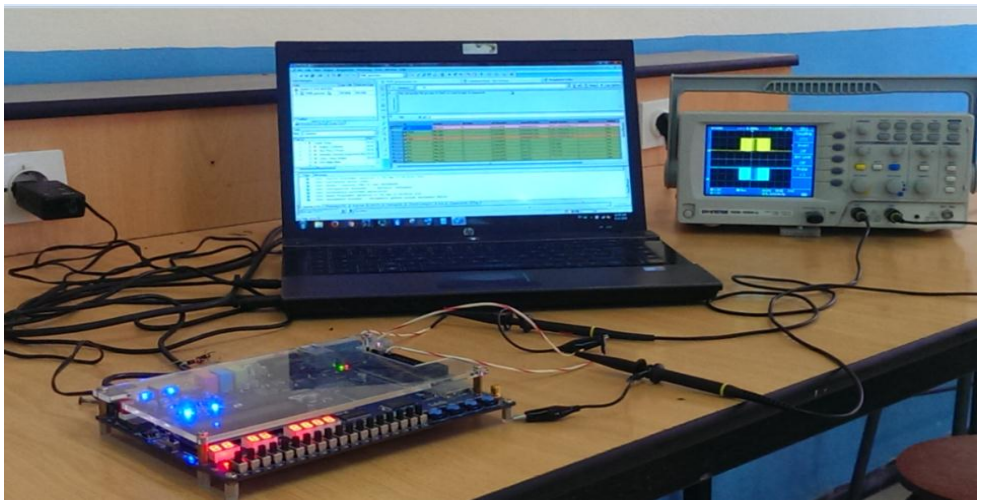
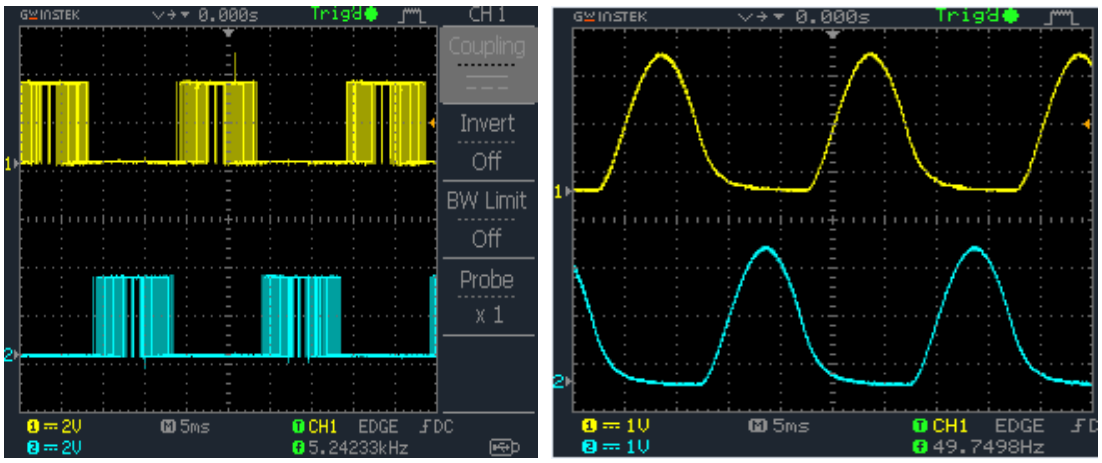


Figure 3-10: experimental setup of the PWM signals generation

The experiment has been carried out in the laboratory and the following results were gotten :

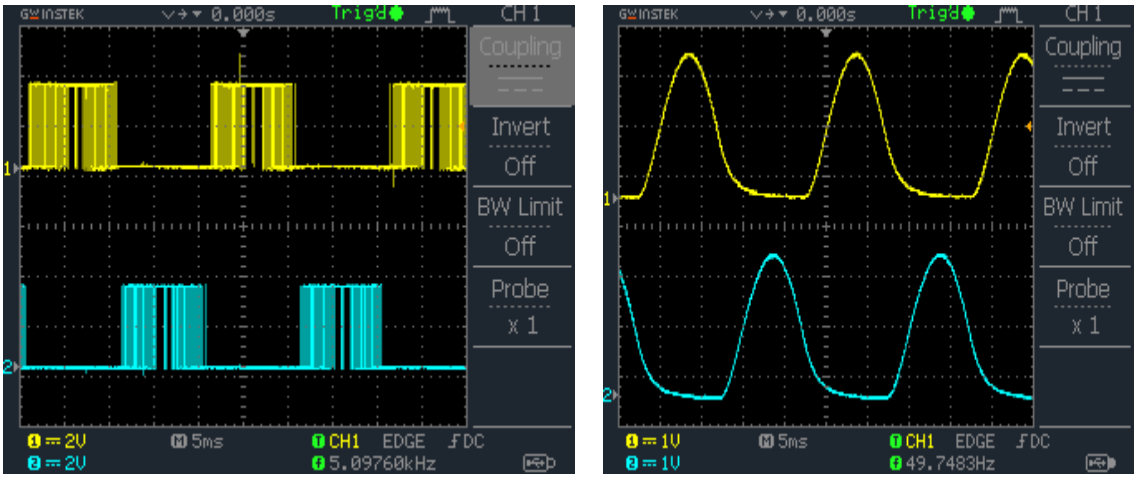
For **phase A:**



a) b)

Figure 3-11: the switching signals (PWM pulses) .a) Switching pulses that corresponds to the first and the second MOSFET's. b) The fundamental component of the previous signals

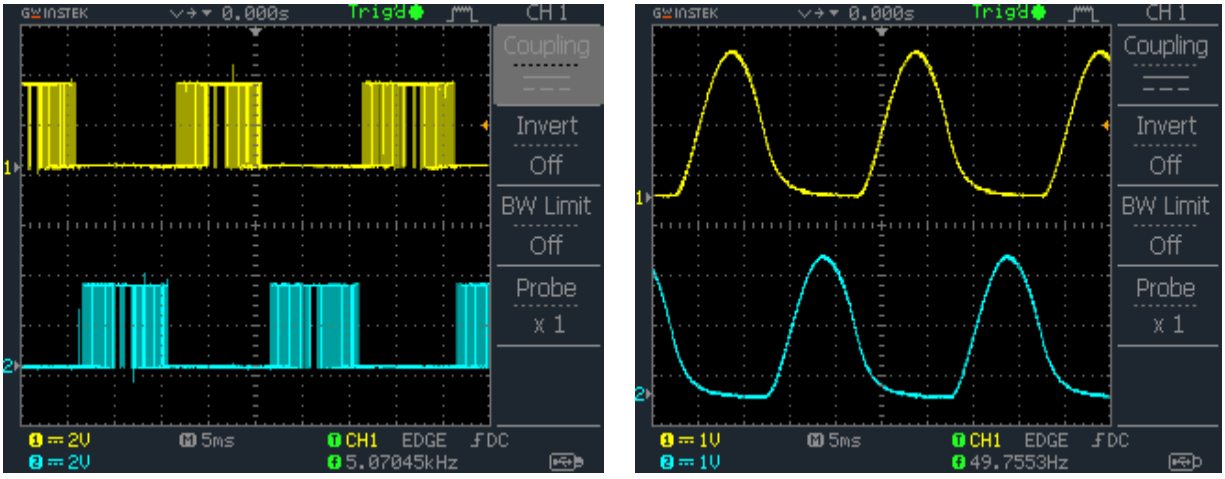
Phase B:



a) b)

Figure 3-12: the switching signals (PWM pulses). a)Switching pulses that corresponds to the first and the second MOSFET's in the topology. b)The fundamental component of the previous signals.

Phase C :



a) b)

Figure 3-13: the switching signals (PWM pulses). a)Switching pulses that corresponds to the first and the second MOSFET's in the topology. b)The fundamental component of the previous signals

-Dead time

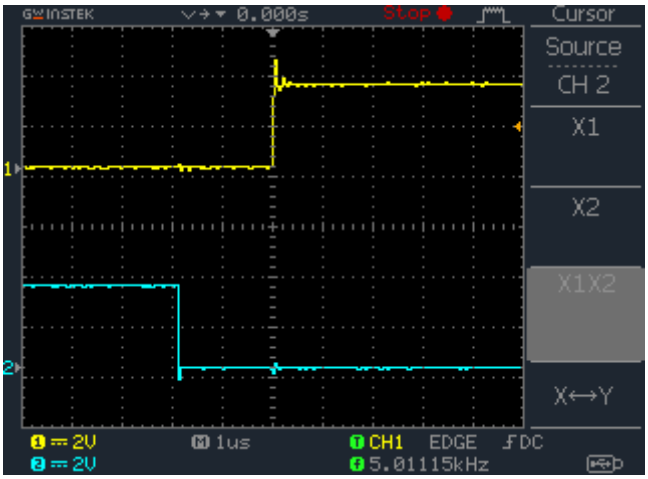


Figure 3-14: dead time effect

3.5 Discussion

In the experimental results shown above the pulses responsible for the first and the second MODFET in each leg are shown while the pulses responsible for the remaining MODFETS are just the complementary of each of the two , taking into consideration the dead time effect that must be forced to avoid the short circuit condition of the leg as a protective measure in our case it was taken to be 2 us .

A low pass filter "implemented through the use of a resistor 10 KΩ in series with 100 nF capacitor the use of the low pass filter enabled us to extract the fundamental component from the switching PWM signals ,this fundamental component has approximately 50 Hz frequency which was the exact frequency used to generate the switching pulses ,as the simulation indicated before and because of the phase shift between the different references used to generate the pulses in each leg we notice also that there is a phase shift between the PWM pulses responsible for switching the different power valves in different legs. This is experimentally demonstrated using a Saleae logic analyzer with Multiple channels as the figure below shows:

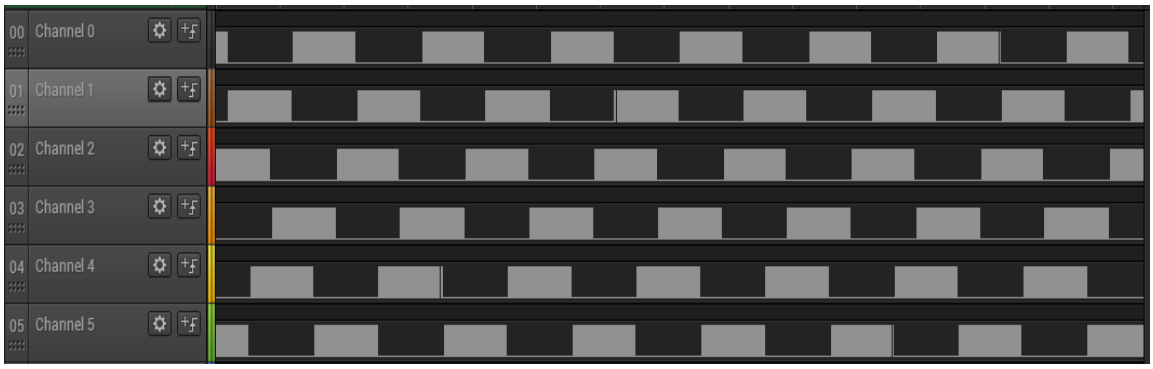


Figure 3-15: shows the phase shifts between different leg's switching pulses

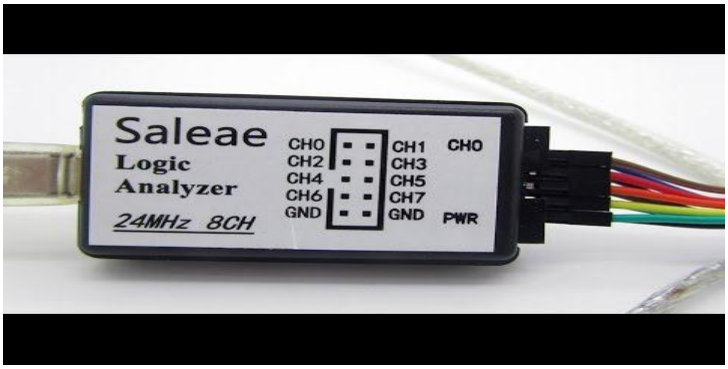
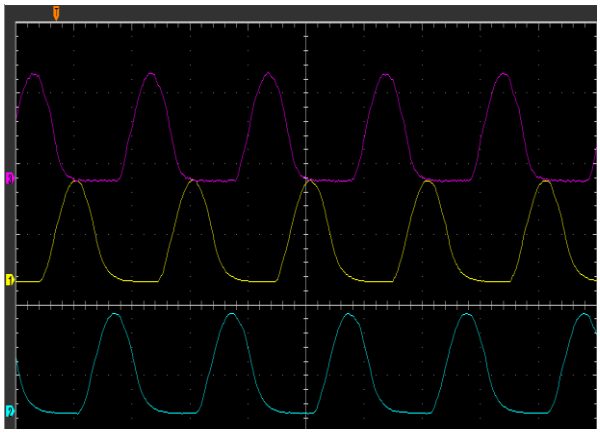


Figure 3-16 Saleae logic analyzer

the same thing is experienced with the fundamental component of these were gotten using a multi-channel oscilloscope.



a) b)

Figure 3-16: a) fundamental components of the different pulses in phases A and B and C,

b) Multichannel oscilloscope

3.6 Conclusion

In this chapter a general guideline was given to the general steps that shaped the process of the implementation of the PWM signals of the voltage source three level NPC inverter, focusing on both the programing side of the implementation and different software that were used in order to obtain these electronic signals.

4.1 Introduction:

In this section of our thesis we are going to give a general description of the different stages that enabled us to implement the three levels NPC inverter starting from the inverter circuit, its main components (general topology) along a brief discussion of the gotten results.

4.2 General procedure of the Implementation:

Generally, the implementation of the whole circuit takes place, in three main stages where the first is programing the FPGA kit by writing the VHDL code that is able to generate the desired pulses,then designing and implementing the gates driving circuitry that represents the electronic part of the whole circuit along with the FPGA ,then ending up by the power circuitry that will be responsible for generating the power signals this logic is depicted in the explanatory figure below :

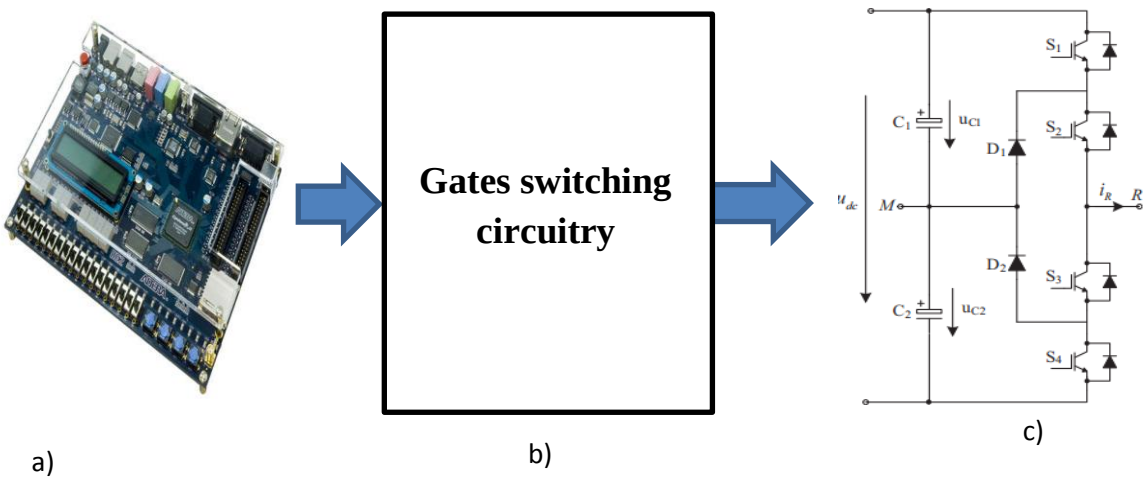


Figure 4-1: a scheme that represents the general procedure followed to implement the inverter

a) DE2 FPGA board
b) Gates driving circuit
c) Power circuit

In here one phase leg is analyzed, The other legs have the same topology of the one leg ;besides all the legs share the same balancing capacitor and the dc source so describing one phase leg will be sufficient for our purpose to seek a general description of the circuit, taking into consideration the phase shift properties that the other legs has over the first leg .the other legs are implemented with the same topology having the same gating circuits .

The difference is made by the switching signals received from the FPGA which themselves differ with just certain amount of phase shift to allow the proper switching of MOSFET's to take place .this is mainly a power electronics circuit means it is made of the combination of an electronic circuit along with a power circuit that are isolated with protective measures .

4.2 Main component of the circuits:

4.2.1 Electronic component:

The following figure depicts the general topology the switching circuit the different components comprising the circuit are described below :

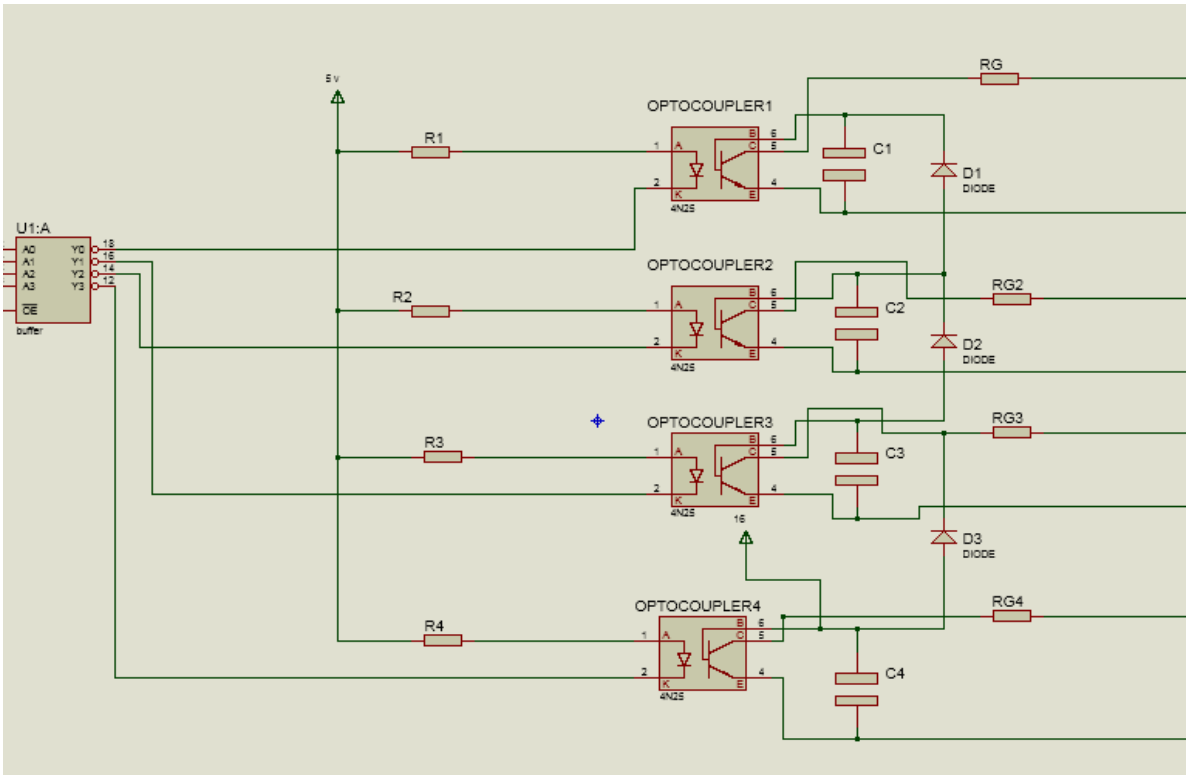


Figure 4-2: gate driving circuitry

-Buffers:

A buffer with the reference (4LS540 MOTOROLA) is used its main role is protect the FPGA from high current .The buffer amplifier (sometimes simply called a buffer) is one that provides electrical impedance transformation from one circuit to another this buffer receives the signals from the FPGA board, providing the optocouplers with the switching signals

-Optocoupler:

Four identical optocouplers with the following reference (HCNW3120:AVAGO technologies) are used as optoisolator, photocoupler, is a component that transfers electrical signals between two isolated circuits by using light. Optoisolators prevent high voltages from affecting the system receiving the signal . The HCNW3120 optocouplers are ideally suited for driving power IGBTs and MOSFETs used in motor control inverter applications. The high operating voltage range of the output stage provides the drive voltages required by gate controlled devices. The voltage and current supplied by these optocouplers make them ideally suited for directly driving IGBTswith ratings up to 1200 V/100 A.Moreover The HCNW3120 has the a very high insulation voltage .

-Diodes:

Three identical diodes are used in the implementation of the floating power supply with reference (1N4001). these diodes are used to implement the floating power supply that will addressed in a later section

-Resistors :

Different resistors with variety of values are used.

-DC sources:

Two power supplies are used in order to feed the electronic components within the circuit, one 5 V was used to feed the buffer IC the other was an implemented power supply used for the optocouplers arrangement this power supply was implemented using 4 ordinary diodes connected in a bridge configuration and a capacitor (12 V), to use of a voltage regulator was not much needed since the optocouplers allow for voltage variation within a range and still keeping a good performance .

The topology used supports the goal of using the minimum number of components to be used this is manifests in the use of one single power supply to activate the four optocouplers, this implemented DC power source is of a special importance since it is a floating supply.

the method we used for implementing this floating supply is called **Bootstrap Supply method** which is a common technique employed to generate a floating supply, the bootstrap supply is a simple circuit using only one diode and a supply storage capacitor. This technique is commonly used for low cost solutions .A simplified schematic of a bootstrap circuit is shown in figure . When the low-side switch M2 is on, the bootstrap diode, D conducts and charges the storage capacitor, the capacitor will charge to approximately the low voltage supply potential, when the high-side switch M1 is on low side switch M2 is off, D is reverse-biased and the high-side circuitry is powered from C, In this condition, the voltage on C droops as it discharges when supplying the high-side circuitry.

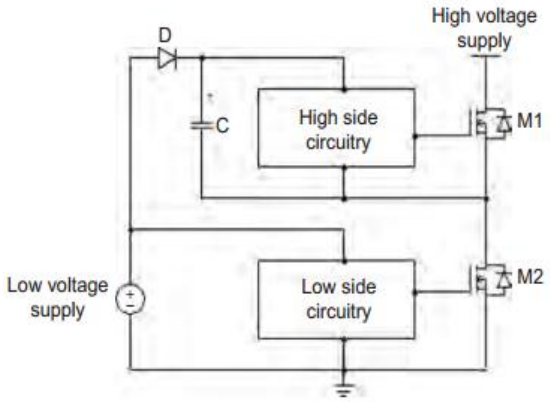


Figure 4-3 : bootstrap technique employed for creating a floating supply.

In our configuration four capacitors were used ,one power supply used in lowermost optocoupler where the voltage is pumped to the other optocouplers through the charging of the other capacitors based on the technique described above ,this way enabling this IC's to deliver the switching signals to the different gates of the power valves through a small resistor

4.2.1 Power components:

These components are labeled as power component as being able to support higher voltages and currents than ordinary components they are designed and fabricated to serve high power applications, they are characterized by having high voltage high current ratings. The used components are described in the following.

Power diodes:

Two of them are used referenced (BY329 Philips Semiconductors-)these are clamping diodes responsible for clamping and blocking the voltage between the capacitors and switching devices these 2 diodes are connected to the neutral point of the the inverter these diodes have the ability to handle much higher voltage compared to the ordinary ones .

-Power MOSFET:

A MOSET is a type of transistor used for amplifying or switching electronic signals. Four MOSFET with the reference of (BUK555/100A -Philips Semiconductors-) are used in our circuit the MOSFET was used solely for the switching purpose in which the turning on/off of this transistors allow us to generate voltage levels though the proper switching of them within the leg .The main advantage of a MOSFET over a regular transistor is that it requires very little current to turn on (less than 1mA), while delivering a much higher current to a load (10 to 50A or more).

-Polarized capacitors:

two of them are used these tow capacitors provide the neutral point for the whole configuration as being able to split the DC voltage one connected to the positive pole of the inverter as the other to the negative this tow capacitors ought to have equal charges. .

-Power supplies:

Tow laboratory power supplies are used since this is an implementing and testing experiment the laboratory component limitations doesn't allow us to force much higher voltages into the circuit though much higher stresses can be supported by the power circuits .

4.3 Experimental results:

The experimental setup that allows us to get the following results is shown below:

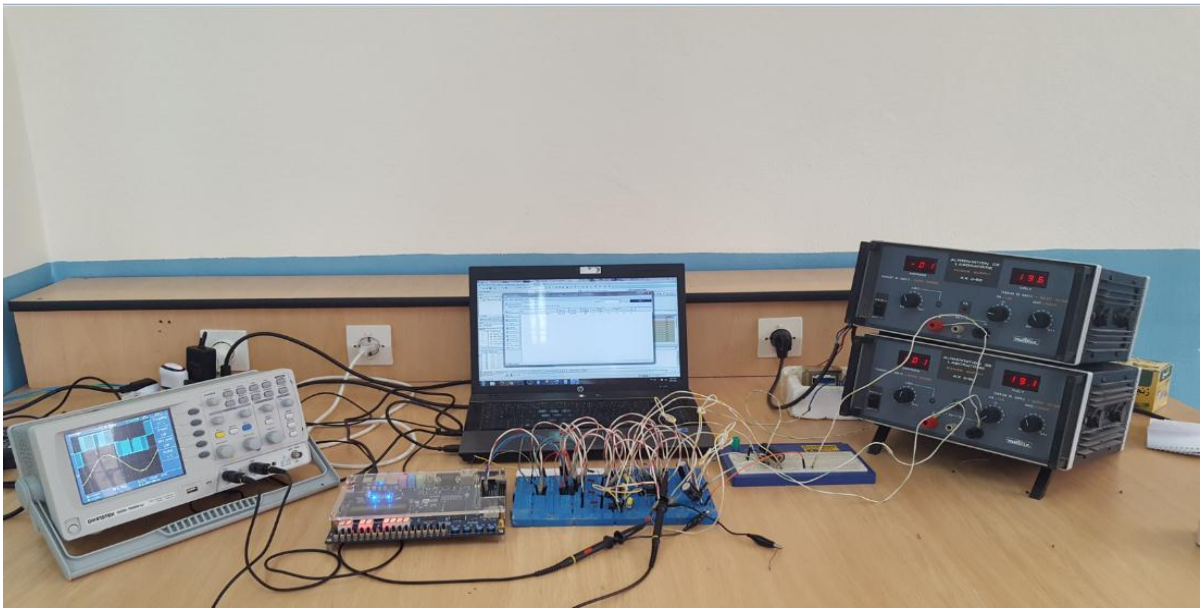
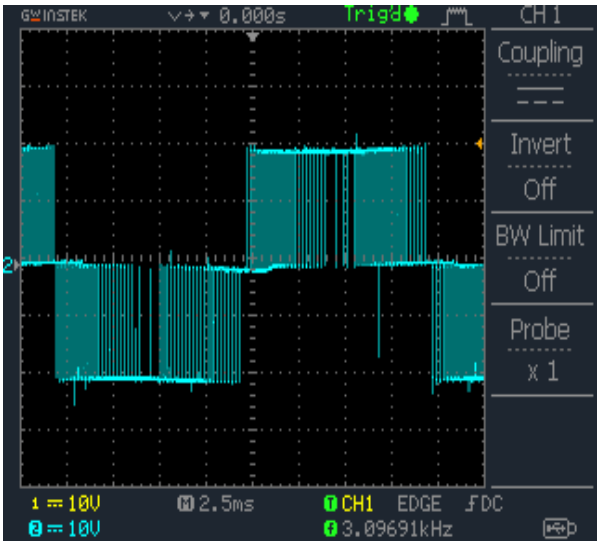
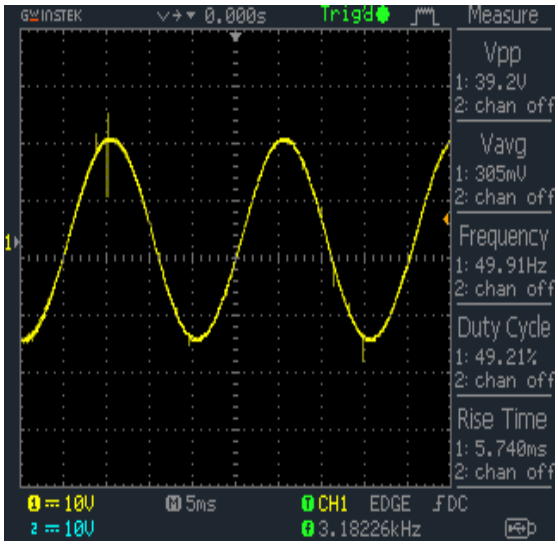


Figure 4-2 : Experimental setup of the three levels NPC inverter

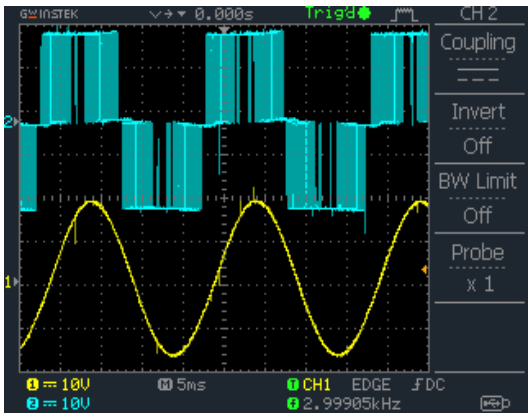
The results gotten are depicted in the following figures:



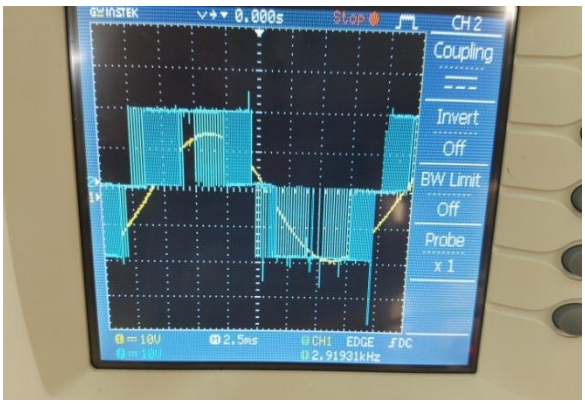
a)



b)



c)



d)

Figure 4-3 :

a) Output phase voltage .

b) Fundamental frequency component of the output phase voltage.

c) And d) output voltage along with its fundamental component

4.4 Discussion :

The results gotten reflexes the three level nature of this inverter this voltage having three levels one positive having V_{dc} value where the negative has - V_{dc} .as a balancing system doesn't exist we see the slight different between these different level beside the null level of voltage figure 4-33 a) ,Due to the use of the low pass filter a capacitance of resistor enables us to see the fundamental component of the signal it was as expected, approximately 50 Hz in one of the figures above figure 4-33 d) we see that there is a slight shift between the different voltage levels and its fundamental component ,that's because of the low pass filter that has shiting properties upon signals filtered .

-This inverter was implanted with the following parameters:

- ma=1 taking that the reference wave has an amplitude of 100 which is the same amplitude of the carrier signal
- mf= 100 since the frequency of the carrier was 5kHz while that of the reference sine wave has 50 as a its frequency

4.5 Conclusion:

This work has described the general procedure of the FPGA based implementation and control of the three level NPC inverter ,this experiment has been carried successfully in the laboratory leading to the desired results this serves the concept of power electronic circuit in a way that employ electronic topologies to serve high power application

Conclusion:

In power electronics, power inverters are becoming increasingly unavoidable. They are present in the most varied fields of application, the most known is probably that of the variation in speed of AC machines. Their strong evolution was based, firstly, on developing fully controllable semiconductor components, powerful, robust and fast, and secondly on the almost universal use of techniques known as pulse width modulation. There are various modulation control strategies. Soon after the introduction of the NPC inverters, the original topology was extended to a higher number of levels using the same principle of diode-clamped intermediate voltage levels. The back-to-back connection of two converters of this type enables bidirectional power flow, facilitates balancing of the intermediate capacitor levels. The main disadvantage of this topology is that the required blocking voltage of the clamping diodes is proportional to the level for which they are used to employ clamping action. Consequently, series connection of the diodes may be required. In addition, because of the high switching speed of today's switching devices, mainly IGBTs ,the clamping diodes can be subject to severe reverse-recovery stress, which challenges this technology. This work comes in order to investigate the neutral point clamped topology along with the powerful features that the FPGA technology provides in terms of generating the switching signals beside the gating circuitry techniques used to switch the power valves this gives a general overview and a guideline for the main structure of the real implementation of such inverters in real life industry.

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