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Title:

Implementation of a PC-Based Phasor Measurement Unit using LabVIEW

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Abstract

In the Wide area Monitoring System (WAMS), it has been possible to continuously monitor the health of power system networks using synchrophasor technology. A Wide Area Monitoring System (WAMS) consists of geographically dispersed Phasor Measurement Units (PMUs) which have the ability to monitor and control power system networks, furthermore advanced network protection in real time. PMUs are able to provide time stamped measurements of voltage and current phasors using Global Positioning System (GPS) satellites, in microseconds.

In this report, we will explain the different steps to construct a Phasor Measurements Unit. These steps include, building an anti-aliasing filter using Sallen-Key topology, demonstrating the synchronization process using GPS and PLL circuit and implementing the phasor estimation based on Discrete Fourier Transform DFT algorithm and LabVIEW. The overall system has been successfully tested by connecting it to real signals and three-phase voltages amplitudes and phases are extracted then plotted on the computer screen either in time domain or as phasor-vectors

Key-words: phasor measurement unit, phasor estimation algorithm, DFT algorithm, anti-aliasing filter, Phased Locked Loop.

Dedication

To our parents, brothers and sisters for their constant support and help throughout our undergraduate studies

To all our friends and colleagues for sharing all the hardest and best moments

To our teachers for providing us with all the required knowledge

We dedicate this modest work

Acknowledgements

My first thanks goes to ALLAH. Secondly, I would like to express my heart felt gratitude to prof Zitouni, for his immense contribution and guidance throughout this research. It has been privileged to work under you as a Master's student.

I would like also to acknowledge the contribution of Dr. Ouadi, who offered suggestions as well as technical support when needed.

Lastly, I would like to thank my family for their continuous of encouragements.

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List of Abbreviations

ADC	Analog to Digital Converter
CMOS	Complementary metal oxide semi-conductor
CP	Charge Pump
CT	Current Transformer
DAQ	Data Acquisition
DFF	Delay flip-flops
DFT	Discrete Fourier Transform
DIO	Digital Input Output
EMS	Energy Management System
GPS	Global Position System
IEEE	Institute of Electrical and Electronics Engineer
IRIG-B	Inter Range Instrumentation Group Format-B
LabVIEW	Laboratory Virtual Instrument Engineering Workbench
LPF	Low Pass Filter
NI	National Instrumentation
PCB	printed circuit boards
PCI	Peripheral Component Interconnect
PDC	Phasor Data Concentrator
PFD	Phase Frequency Detector
PLL	Phased Locked Loop
PMU	Phasor Measurement Unit
PPS	pulse-per-second
PT	Potential Transformer
RIO	Rapid Input Output
ROCOF	rate of change of frequency
SCDR	Symmetrical Component Distance Relay

SE	State Estimation
UTC	Universal Time Coordinated
VCO	Voltage Controlled Oscillator
VCVS	Voltage Controlled Voltage Source
VCXO	Voltage Controlled Crystal Oscillator
VI	virtual instrument
VILS	Voltage Instability Load Shedding
VSA	Voltage Stability Assessment
VT	Voltage Transformer
WAMS	wide area monitoring systems

Chapter1 : Introduction

1.1 Introduction

The August 14, 2003 blackout in the interconnection of North America exposed the urgent need for wide-area information acquisition for better power grid operations. Such catastrophic events are mainly caused by the low stability operating system or small faults that are declared lately after the occurrence of the problem, and imply dramatic consequences on the societies and governments security and development; for they rely heavily on the quality of the power supplied. In order to minimize the future blackouts caused by the cascade tripping, there is a growing interest in the microprocessor-based relays and disturbance recorders to provide an additional protection, control and disturbance analysis of industrial and residential areas, due to this; power utilities have been working on the wide area monitoring systems (WAMS), providing a smart grid, safer, and feasible in practice.

The WAMS is based on the phasor technology, which implies a phasor measurement unit (PMU). In connection with a phasor data concentrator (PDC), and an intelligent communication between the two electronic devices. This communication network is a subject to be investigated and updated aiming an optimization of the protection, and the achievement of a healthier power system.[1]

1.2 Historical Developments

Modern phasor measurement systems can trace their origin to the development of the Symmetrical Component Distance Relay (SCDR) in the early 1970s. [2] Computers available in those days were neither fast enough nor inexpensive enough to handle the requirements of a distance relay algorithm. This led to the invention of the symmetrical component distance relay (SCDR) which used symmetrical components of voltages and currents in order to convert the 6 fault equations of a three-phase transmission line into a single equation using symmetrical components. Over time it became clear that microcomputers had become sufficiently capable so that this innovation was no longer required for line relaying. However, the fact that the SCDR utilized efficient methods of measuring symmetrical components of voltages and currents proved to be very interesting for other applications. In fact, positive sequence voltages and currents of a network are the backbone of most power system analysis programs: load flow, stability, short circuit, optimum power flow, state estimation contingency analysis, etc.

In early 1980s, GPS satellites were being deployed in significant numbers, and it became clear that by using GPS time signals as inputs to the sampling clocks in the measurement system of digital relays one would have a very powerful measurement tool, which would be able to provide instantaneous picture of the state of the power system, and in fact would have many outstanding features which would make these measurements become effective immediately even if complete observability of the network could not be achieved with the new measuring devices.

The start of the modern EMS systems based upon state estimators can be said to have begun with the aftermath of the 1965 catastrophic failure of the North- Eastern power grid in North America. There was a great deal of research conducted in techniques for determining the state of the power system in real time based upon real time measurements. Of course, there was not the possibility of achieving synchronized measurements in those days, and instead a technique was devised whereby measurements could be obtained by sequential scan and from them the state of the power system estimated by a non-linear state estimator. Of course, the state obtained consisted of positive sequence voltages at all the network buses, and it was recognized that the state obtained in this manner at best described a quasi-steady state approximation to the actual state of the network.

Phasor Measurement Units (PMU) using the GPS transmissions to synchronize the sampling clocks, so that the estimated phasors would have a common reference were first developed in the Power System Research Laboratory of Virginia Tech are shown in Figure 1.1.

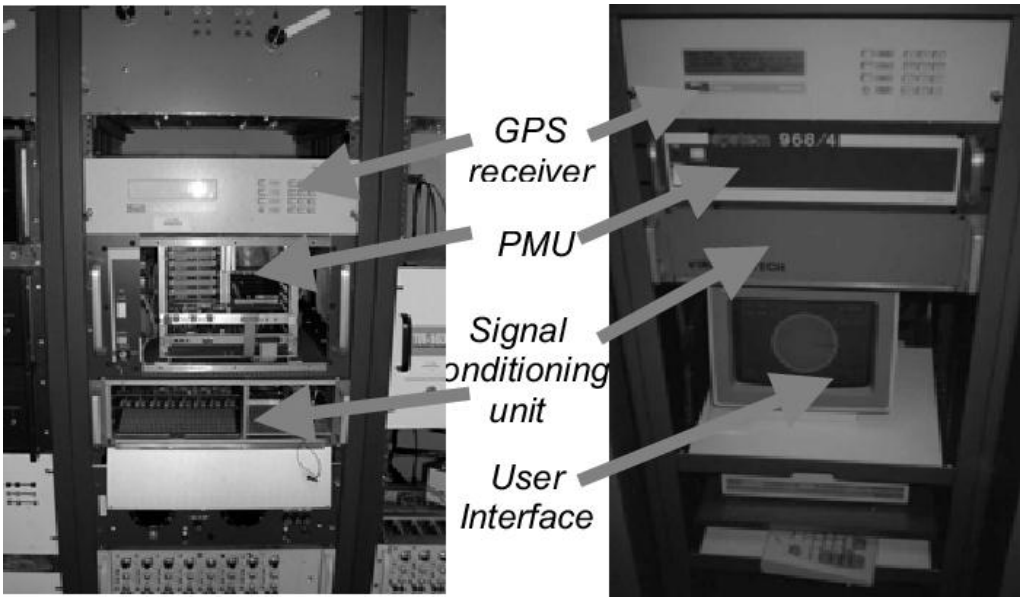

Figure 1.1The first experimental PMUs developed at Virginia Tech in 1980s

At the top of the installation is the stand-alone GPS clock, followed by the PMU processor, analog input system, and the phasor display screen.

Because of incomplete deployment of the satellite system early GPS receivers were expensive because they needed very precise internal crystal clocks to keep time accurately until the next GPS satellite came into view. Today, with the satellite system complete and fully deployed, a chip set of the GPS receivers could be obtained for just a few hundred dollars![3].

1.3 **SynchroPhasor Technology:**

Phasor is a quantity with magnitude and phase (with respect to a reference) that is used to represent a sinusoidal signal. Here the phase or phase angle is the distance between the signal's sinusoidal peak and a specified reference and is expressed using an angular measure. Here, the reference is a fixed point in time (such as time = 0). The phasor magnitude is related to the amplitude of the sinusoidal signal.[4]

A sinusoidal signal of a known frequency is fully described by its magnitude and angular position with respect to an arbitrary time reference

$$x(t) = X_m \cos(2\pi f t + \phi) \tag{1.1}$$

With: X_m : the amplitude of the input signal,

f: the nominal frequency,

ϕ: the initial phase angle of the input signal

The phasor representation of the sinusoid of (1.1) is given by:

$$X = \frac{Xm}{\sqrt{2}} e^{j\phi} = \frac{Xm}{\sqrt{2}} (cos\phi + jsin\phi) \tag{1.2}$$

X is the complex representation of the sinusoid.

Note that the signal frequency is not explicitly stated in the phasor representation. The magnitude of the phasor is the rms value of the sinusoid, and its phase angle is, the phase angle of the signal in (1.1) The sinusoidal signal and its phasor representation given by (1.1) and (1.2) are illustrated.

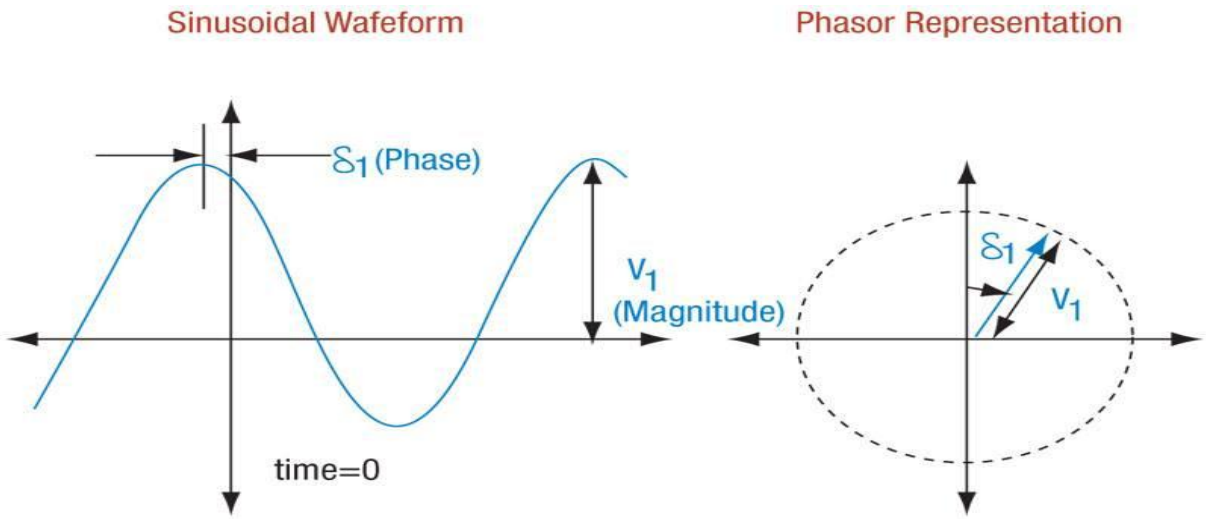

Figure 1.2Phasor representation of a sinusoidal waveform

The phasor of a signal can be derived using Discrete Fourier Transform (DFT) utilizing the data samples of the signal within a selected time window. The magnitude remains constant, while the phase angle depends on the starting point of samples. If the samples obtained by the measurement devices are not synchronized to a common timing reference, the angles of the phasors computed at different locations will not be comparable. To remove this barrier, phasors measured across the power grid should have a common timing reference such that direct comparison is feasible.[5].

The resulting synchronized phasors is known as a synchrophasor. According to The IEEE standard, C37.118, [6] a synchrophasor is "A phasor calculated from data samples using a standard time signal as the reference for the measurement".

1.4 The PMU Device

The PMU is defined as a "device that produces synchronized phasor, frequency, and rate of change of frequency (ROCOF) estimates from voltage and/ or current signals and a time synchronizing signal" [7]

In the real context, PMU's are devices equipped with the functionality to estimate phasor values from electrical waveforms. One of the many applications of PMU is to capture phasor measurements from different locations and report these measurements on the same phasor diagram. The measurements collected from all locations are synchronized to a common time base with the aid of a GPS satellite navigation system. [8]

The measurements done by PMUs from different locations are transmitted to a Phasor Data Concentrator (PDC) which is defined as "a device that combines data from several measurement devices" [7]. It should be known that data is processed by the PDC and displayed

on a user interface for users and can also be stored in a database for future use. Figure 1.3 shows the block diagram of a PMU.

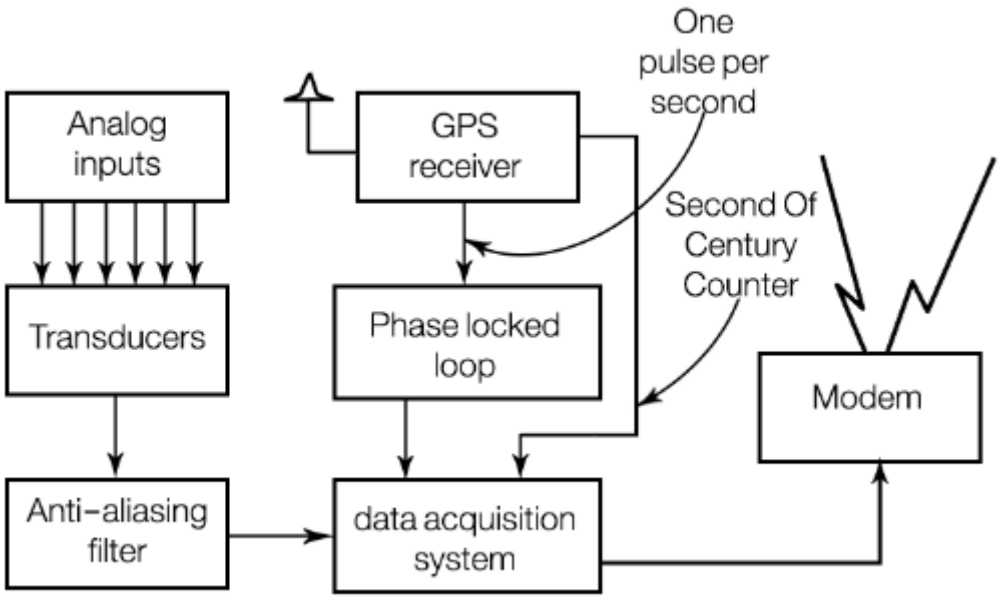

Figure 1.3PMU block diagram

1.5 Application of PMU in Power Systems

PMU has made it possible for a number of functions and roles to be possible today in the power system field. Explained below are some of the major applications of the PMU.

1.5.1 State Estimation

PMUs have become particularly useful and vital in power system state estimation (SE). Real power, reactive power injections and flows are utilized in conventional state estimation algorithms for estimation of system states (voltage amplitude and phase angle)[9]. State estimation is very important in real-time monitoring and control of the power system because it processes redundant measurements and provides steady-state operating state for advance Energy Management System (EMS) application programs[10]. It is known that traditional state estimation uses measured voltage, current, real power and reactive power to determine the operating condition of the electric network. Traditional state estimation has some limitations associated with it and these limitations are: (i) It is technically challenging and computationally more to estimate the likely state of the power system based on measured parameters such as voltages, current, real power and reactive power. (ii) Traditional state estimation is usually solved in one-minute interval, and this means that the result provided by the approach may be old. To overcome these technical and challenging difficulties, improved computational ability

together with synchronized phasor measurement units (PMUs) are deployed to provide globally time synchronized phasor measurements with accuracy of one microsecond for bus voltages and line currents[10].

PMUs have the ability to improve SE accuracy by measuring voltage angles directly, which are the state variables to be estimated. The addition of voltage phase angle measurements to a traditional SE is capable of greatly increasing the accuracy of SE.

1.5.2 Oscillation Detection and Control

The increase in the amount of electric power that is transmitted through lines is capable of causing transmission bottlenecks and oscillations of power transmission systems [10]. Basically, system oscillations originate from interconnected generators in power system. The deviation of one generator from the synchronous speed will prompt other generators in the system to provide power in order to reduce the speed deviation. However, the effect of inertia of the generators could creep in causing the entire system or part of the system to swing. In most cases, this disturbance might not be significant and would decay slowly. However, in other times, it might be very significant and does not decay which causes the system to lose synchronism and a final collapse of the system. PMUs could be used as the eye of the power system to detect oscillations early enough before they lead to critical consequences.[11]

1.5.3 Voltage Stability Monitoring and Control

Severe changes in system conditions is enough to change the operating system of a power system dynamically [12]. Such changes affect the voltage phasor, current phasor and system frequency. Voltage stability has been known to be related to the load ability of a transmission network [10]. Different research has shown that voltage magnitude and phase angles are the best indicators of voltage stability margin.

The use of synchronized phasor measurements units (PMUs) to improve voltage stability monitoring and control has become very efficient. This is possible through the following applications:

* Voltage Instability Load Shedding (VILS).
* Wide Area Voltage Stability Monitoring and Control.

Under the VILS approach, PMUs are used to monitor the electric network to track how close the transmission system is to its load ability limit. If the system is very close to that limit, and every other approach has been exhausted to avoid voltage collapse without significant improvement, the VILS scheme is then deployed as the last safety option to prevent voltage

collapse in the system. The shedding of load is done in pre-defined blocks that are usually triggered in stages due to scheduled maintenance, and unexpected disturbances[10][12].

PMUs provide measurement-based on-line voltage stability monitoring and control which has the ability to improve the power transfer limits and increase security of the system operation[10].

Under the Wide Area Voltage Stability Monitoring and Control scheme, computer simulation tools are used to help operators monitor and control system voltage stability.

One good tool used is a Voltage Stability Assessment (VSA) program which relies on state estimators to provide steady-state solution[10].

1.5.4 Protection of Power Systems

A number of severe protection problems have been resolved by PMUs[8]. Examples of protection problems include: protection of series compensated lines, protection of multi-terminal lines, and the inability to satisfactorily set out-of-step relays. The reliable measurement of voltage or current is possible to offer substantial improvement in protection functions. Furthermore, the communication of such measurements from one end of a protected line to another is necessary to improve protection functions.

These measurements offered by PMUs are effective in improving protection functions which have relatively slow response time [9]. The latency of remote measurements for such protection functions, is not really a significant issue. The differential protection of buses, transformers and generators is a well-established protection principle that emphasizes the importance of synchronized phasor measurements.

True differential protection was not possible before the introduction of synchronized phasor measurements.

Differential protection is important for serie compensated lines and tapped lines. Differential protection involves communication wires or communication band channels. The easy availability of synchronized measurements using GPS technology and the improvement in communication technology makes it possible to consider true differential protection of transmission lines and cables.

Chapter 2: Hardware description part

2.1 Introduction

The design and implementation of the PMU for this project is basically based on the block diagram shown in the previous chapter (Figure1.3). The PMU device includes sensor module, Attenuators or instrument amplifiers, analog filters, phased locked oscillator, GPS receiver, and data acquisition card followed by the LabVIEW software where the phasor measurements were estimated.

This chapter will include the detailed explications and the steps of implementation of the above sub-devices.

2.2 Instrument Transformers:

Sensor module are simply the electrical instrument transformers (Potential Transformer PTs and Current Transformers CTs). Electrical instrument transformers transform high currents and voltages to standardized low and easily measurable values that are isolated from the high voltage. When used for metering purposes, instrument transformers provide voltage or current signals that are very accurate representations of the transmission line values in both magnitude and phase.

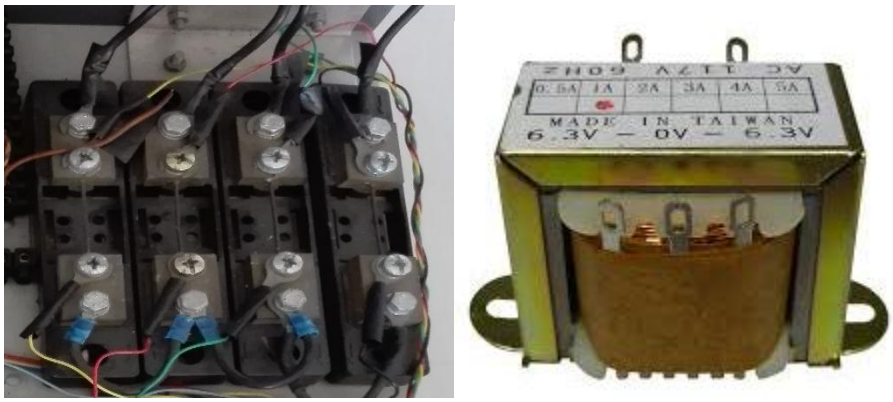

Figure 2.1Instrument Voltage and Current Transformers

it is preferable to add potentiometers as an attenuator for the voltage inputs to protect the analog circuit from high voltages and the instrument amplifier for suitable reading of the currents. For more security, resistance can be added at the output of each phase.

2.3 **The Anti-aliasing filter:**

The most common technique for determining the phasor representation of an input signal is to use data samples taken from the waveform, and apply the discrete Fourier transform (DFT) to compute the phasor. Since sampled data are used to represent the input signal it is essential that antialiasing filters be applied to the signal before data samples are taken. The antialiasing filters are analog devices which limit the bandwidth of the pass band to less than half the data sampling frequency (Nyquist criterion). A fourth-order Butterworth low pass filter with Sallen-Key architecture is used in this project.

2.3.1 Low pass Butterworth Filter:

The Butterworth low-pass filter provides maximum passband flatness. Therefore, a Butterworth low-pass is often used as anti-aliasing filter in data converter applications where precise signal levels are required across the entire passband[13]. Those kinds of filters are defined by the property that the magnitude response is maximally flat in the passband. For an Nth-order lowpass filter, this means that the first (2N-1) derivatives of the magnitude-squared function are zero at Ω= O. Another property is that the magnitude response is monotonic in the passband and the stopband. The magnitude-squared function for a continuous-time Butterworth lowpass filter is of the form

$$|\mathrm{Hc}(\mathrm{j}\Omega)|^2 = \frac{1}{1 + (\frac{\mathrm{j}\Omega}{\mathrm{j}\Omega c})^{2\mathrm{N}}} \qquad (2.1)$$

With: N: the order of the filter.

Ωc: the cut-off frequency.

Ω : the operating frequency

The function is plotted in Figure2.2

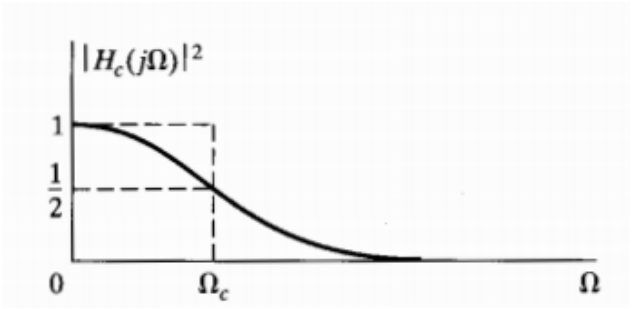

Figure 2.2Magnitude squared function for continuous-time Butterworth Filter

As the parameter N in Eq (2.1) increases, the filter characteristics become sharper: that is, they remain close to unity over more of the passband and become close to zero more rapidly

in the stopband, although the magnitude-squared function at the cutoff frequency Ωc will always be equal to one-half because of the nature of Eq. (2.1), The dependence of the Butterworth filter characteristic on the parameter N is indicated in Figure 2.3. [14]

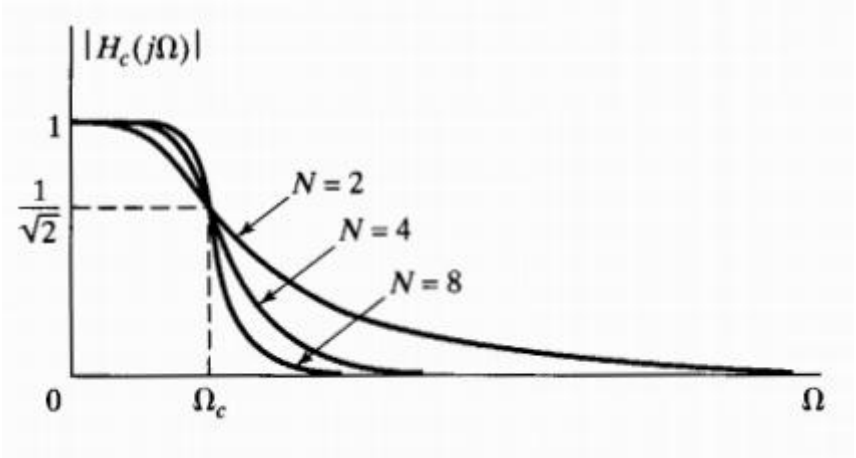

Figure 2.3Dependence of Butterworth magnitude characteristics on the order N

2.3.2 The Sallen- Key topology

The Sallen- Key configuration, also known as a voltage control voltage source (VCVS), is a filter topology used to implement second order active filters that is particularly valued for its simplicity. It was first introduced in 1955 by R.P Sallen and E.L.Key of MIT's Lincoln Labs, it's a degenerate form of a voltage –controlled voltage-source (VCVS) filter topology. A VCVS filter uses a voltage amplifier with practically infinite input impedance and zero output impedance to implement a 2- pole low pass, high pass, band pass, band stop pass, or all pass response. A VCVS filter allows high Q factor and passband gain without the use of inductors. VCVS filters can be cascaded without the stages affecting each other tuning .A Sallen and Key filter is a variation on a VCVS filter that uses a unity voltage gain amplifier (i.e. a pure buffer amplifier).The generic unity gain Sallen and Key filter topology implemented with a unity gain operational amplifier is shown in the Figure 2.4, assuming that the operational amplifier is ideal .because the operational amplifier is in a negative feedback configuration ,it's V+ and V- input must match (i.e. ,V+=V-).However ,the inverting input V- is connecting directly to the output V_{out} ,and so .

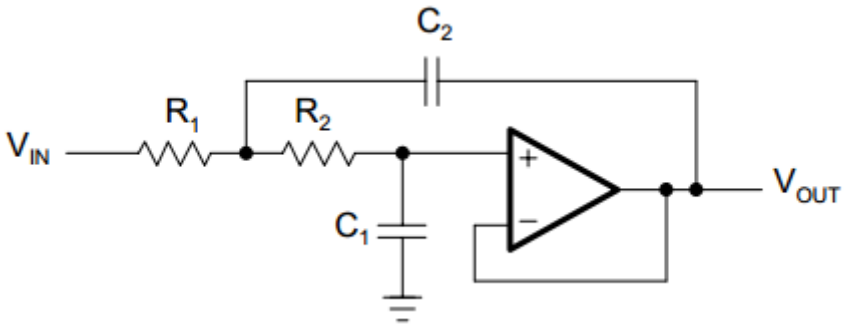

Figure 2.4Unity-Gain Sallen-Key Low-Pass Filter

The Sallen and Key filter has the advantage that quality factor (Q) can achieve via the inner gain (G), without modifying the frequency ,multi-feedback .Furthermore this filter is sharpness we can pick a different cutoff frequency for a law pass filter ,also easy to convert it to high pass filter by just swap resistors location by capacitors location .The Sallen and Key has very low "active sensitivity" figures (sensitivity against op-amp non- idealities) and rather high " passive sensitivity " figures (sensitivity against passive tolerances).However there is a big disadvantage of this filter which is the damping characteristics are not good as it should be ,means that the magnitude shows a rising characteristics for larger frequencies .We can improve this by scaling the parts values : smaller capacitors and larger resistor values .[15]

For the unity-gain circuit in Figure 2.4, the transfer function is obtained as: [16]

$$A(s) = \frac{1}{1 + \omega_c C_1(R_1 + R_2)s + \omega_c{}^2 R_1 R_2 C_1 C_2 s^2} \qquad (2.2)$$

ω_c: the angular frequency.

The general transfer function of a second order low-pass filter is:

$$A(s) = \frac{A_0}{1 + a_1 s + b_1 s^2} \qquad (2.2)$$

The coefficient comparison between this transfer function (2.3) and Equation (2.2) yields:

$A_0 = 1$

$a_1 = \omega_c C_1(R_1 + R_2)$

$b_1 = \omega_c{}^2 R_1 R_2 C_1 C_2$

Given C1 and C2, the resistor values for R1 and R2 are calculated through:

$$R_{1,2} = \frac{a_1 C_2 \mp \sqrt{a_1^2 c_2^2 - 4 b_1 C_1 C_2}}{4\pi f_c C_1 C_2} \quad (2.4)$$

In order to obtain real values under the square root, C2 must satisfy the following condition:

$$C_2 \geq C_1 \frac{4b_1}{a_1^2} \quad (2.5)$$

Notice that the coefficient a1 and b1 are obtained from the table 1 in the appendix.

2.3.3 The implementation of the filter:

According to the calculations described in the previous section, we set C_1=25 nf and C_2= 330nf and f_c=300Hz. We found R_1=6kΩ and R2= 4kΩ.

The implementation of the of the anti-aliasing filter circuit was done by PROTEUS software as shown in Figure 2.5

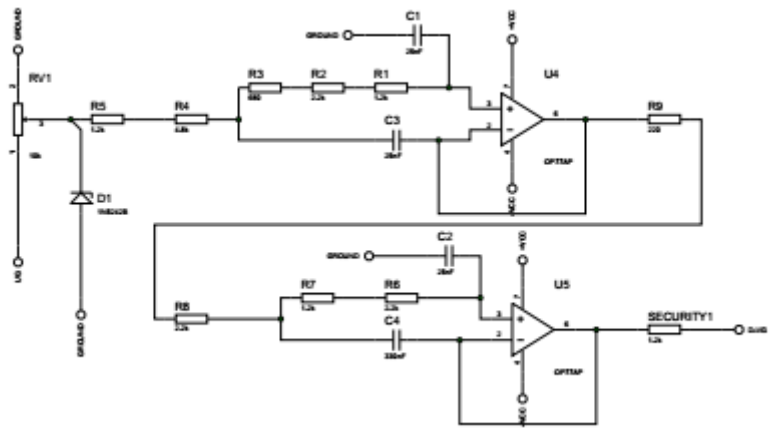

Figure 2.5A 4th order Low pass Butterworth Filter for voltage phase

For the other phases (3 phases for voltage and 3 phases for current) is just a duplication of the circuit in Figure 2.5 except for the phases of current which the attenuators are replaced by amplifiers to rise up the coming amplitude from the transducers. Figure 2.6 shows the circuit diagram of the amplifier followed by its filter.

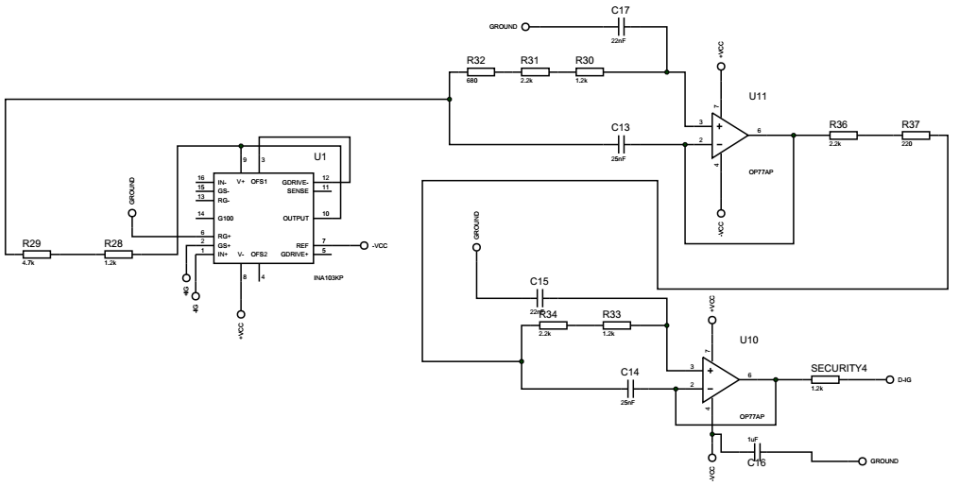

Figure 2.6the circuit diagram of the amplifier followed by its filter.

One of the important reasons for using PROTEUS is that it has the ability to convert schematics directly to their equivalent printed circuit boards (PCB) layout with ease. PCBs comprise of a sandwich of one or more insulating layers and one or more copper layers which will normally bear the signal traces.

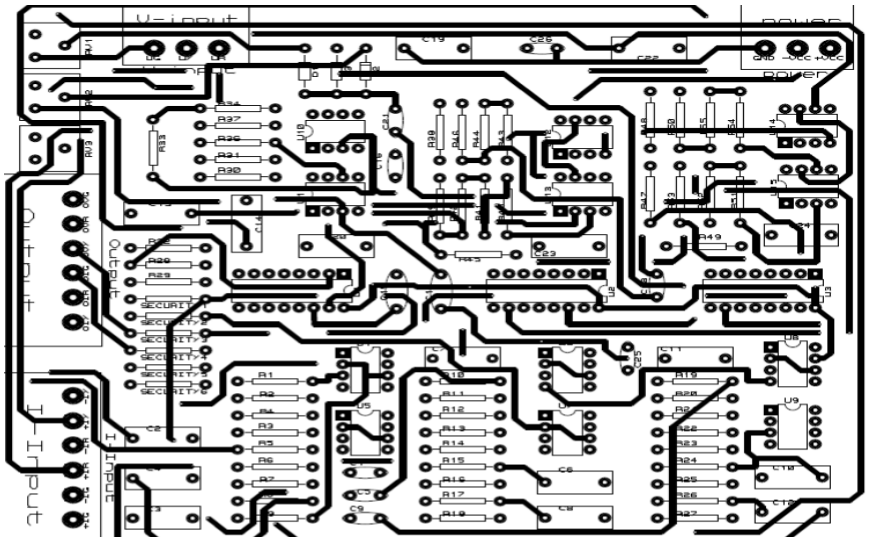

Figure 2.7 PCB Configuration of the schematic

After the circuit schematic has undergone, the routing process and converted to the PCB design as shown in Figure 2.7, it is checked for errors. After this check is done, and all errors corrected, the PCB files (Gerber files) were obtained and sent for the manufacturing process. The Gerber file is the file standard format used by virtually all PCB industry software to describe the information contained in the PCB design. Such information includes drill holes, copper layers, legend etc. Figure 2.8 show the designed PCB layout of the filters.

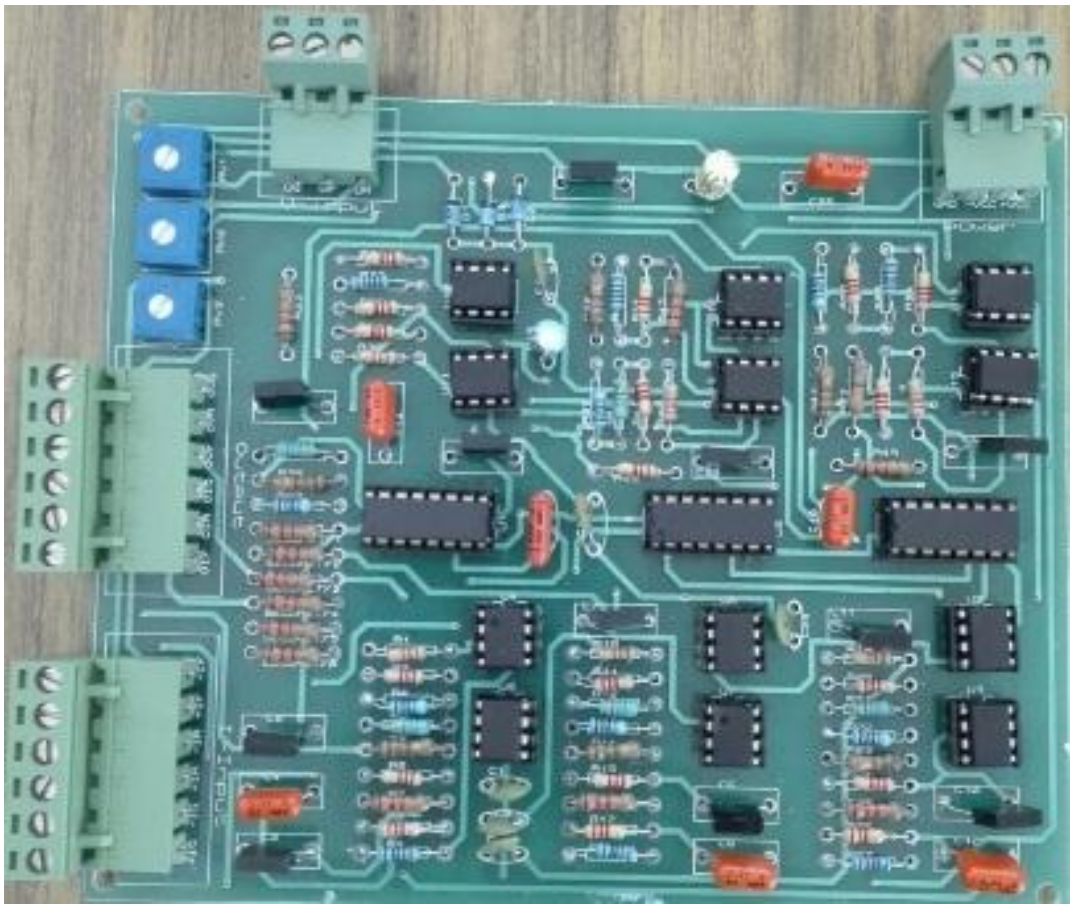

Figure 2.8A top view of the implemented circui

Figure 2.9 The generated signal (yellow) and the output signal (blue).

A quick test on this PCB circuit is by generating a signal to an input (voltage or current) phase and increasing the frequency until the amplitude will be zero. The results of this test are shown in the Figures bellow:

After rising up the frequency to 500 Hz, the amplitude of the output signal start to decrease and it goes to zero at 1.8 KHz.(Figure 2.10 and Figure 2.11).

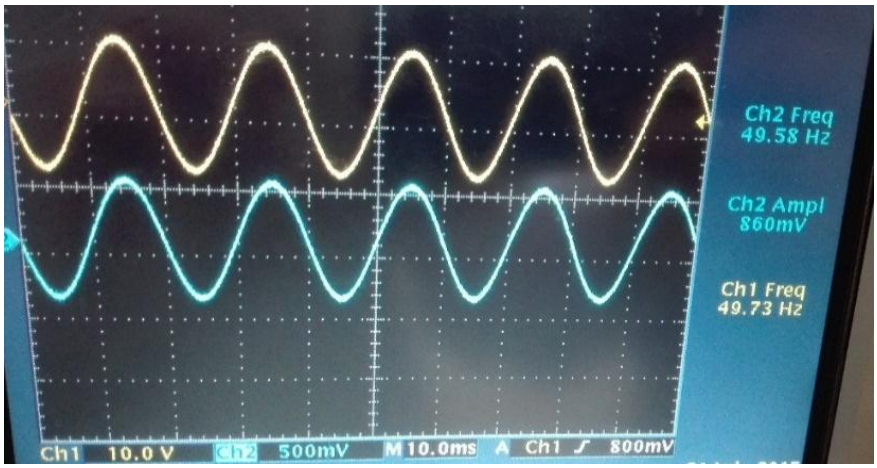

Figure 2.10The cutoff frequency ≈ 500 Hz

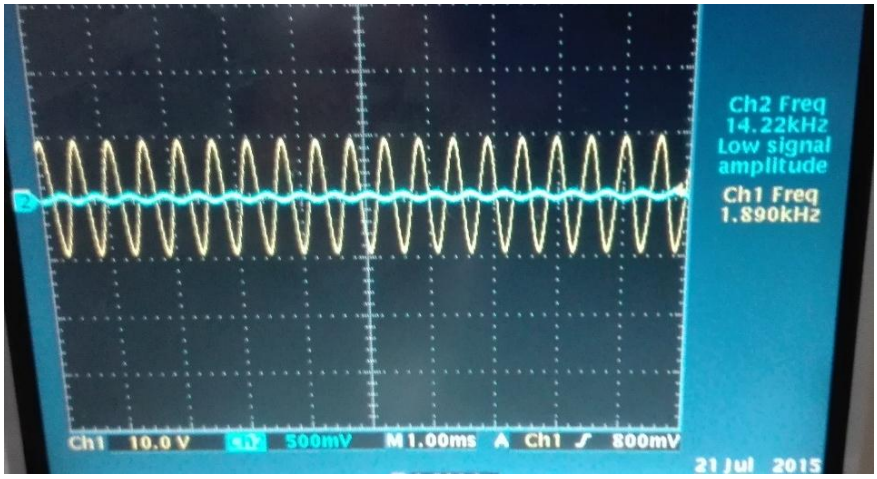

Figure 2.11The output signal goes to zero at ≈ 1.8KHz

2.4 **Phased Locked Loop PLL:**

A PLL is a feedback system that compares the output frequency/phase with the input frequency/phase. Phase-locked loops can be utilized for frequency synthesizing, carrier synchronization, carrier recovery, frequency division, frequency multiplication and frequency demodulation.[17]

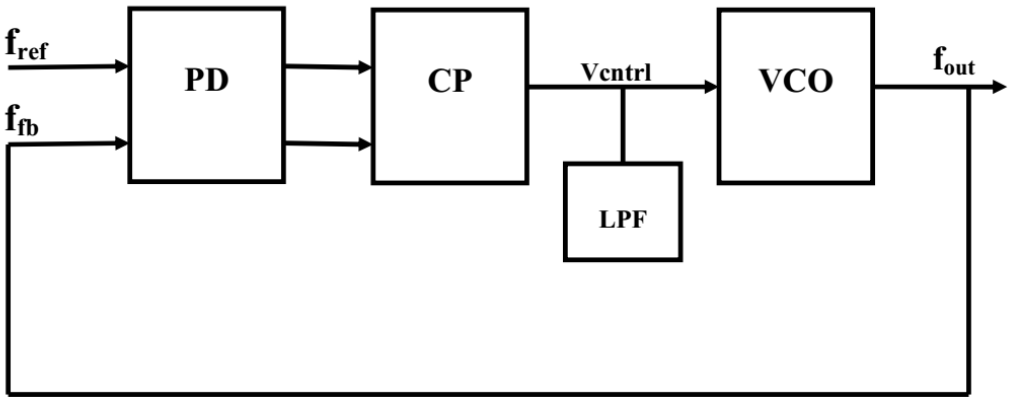

Figure 2.12Basic Phase Locked Loop block diagram

The basic components of a PLL are:

1. Phase Detector or Phase Frequency Detector (PD or PFD)
2. Charge Pump (CP)
3. Low Pass Filter (LPF)
4. Voltage Controlled Oscillator (VCO)

The phase frequency detector, PFD, measures the difference in phase between the reference and feedback signals. If there is a phase difference between the two signals, it generates "up" or "down" synchronized signals to the charge pump/ low pass filter. If the error signal from the PFD is an "up" signal, then the charge pump pumps charge onto the LPF capacitor which increases the control voltage, Vcntrl. On the contrary, if the error signal from the PFD is a "down" signal, the charge pump removes charge from the LPF capacitor, which decreases Vcntrl. Vcntrl is the input to the VCO. Thus, the LPF is necessary to only allow DC signals into the VCO and is also necessary to store the charge from the CP. The purpose of the VCO is to either speed up or slow down the feedback signal according to the error generated by the PFD. If the PFD generates an "up" signal, the VCO speeds up. On the contrary, if a "down" signal is generated, the VCO slows down. The output of the VCO is then fed back to the PFD in order to recalculate the phase difference, thus creating a closed loop frequency control system.[18]

It is possible to have a phase offset between input and output, but when locked, the frequencies must exactly track.

$$\phi_{out}(t) = \phi_{in}(t) + \text{const} \quad (2.6)$$

$$\omega_{out}(t) = \omega_{in}(t) \quad (2.7)$$

$\phi_{out}(t)$: the output phase.

$\phi_{in}(t)$: the input phase.

$\omega_{out}(t)$: the output frequency

$\omega_{in}(t)$: the input frequency.

2.4.1 Phase detector (PFD)

A phase frequency detector (PFD), is a device which compares the phase of two input signals and provides a signal $v_e(t)$ in the form of phase error.

$$v_e(t) = K_D[\phi_{out}(t) - \phi_{in}(t)] \quad (2.8)$$

K_D :is the gain of the phase detector.

The conventional Phase Frequency Detector block diagram and behavior is shown in Figure 2.13. As can be seen, the frequency information is coded at the output of a PFD that uses two D flip-flops (DFF).

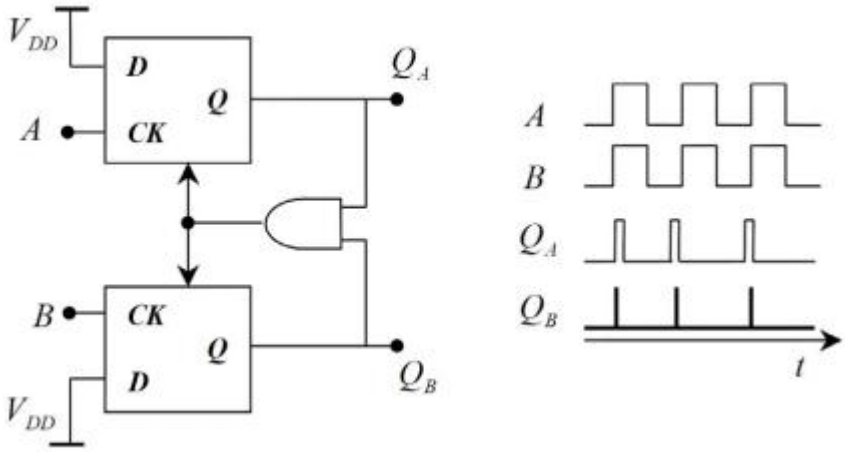

Figure 2.13The conventional Phase frequency Detector block diagram and behavior

The DFF outputs are denoted Q_A (or up) and Q_B (or down). Assuming both outputs are initially low, a rising edge on the A input (reference) causes the UP signal to go high. This indicates that the VCO frequency needs to be increased in order to match the input. Similarly, when the VCO input (B) transitions high, the Q_B output rises. This state corresponds to the need to decrease the VCO frequency in order to match the input. When both outputs switch high, the AND gate propagates a reset signal returning the PD to the zero state. Thus, the $Q_A = Q_B$ = high state is suppressed by the feedback, and the PD is essentially a three-state device. This behavior of the output signals is also demonstrated in Figure 2.13, where the minimum pulse width is determined by the reset path delay.[19]

2.4.2 Charge Pump / Low Pass Filter

The function of a charge pump and loop filter is to take the digital UP and DOWN pulses from the PFD and convert them into an analog control voltage, V_{cntrl}. Figure 2.14 shows A CMOS CP/LPF circuit.

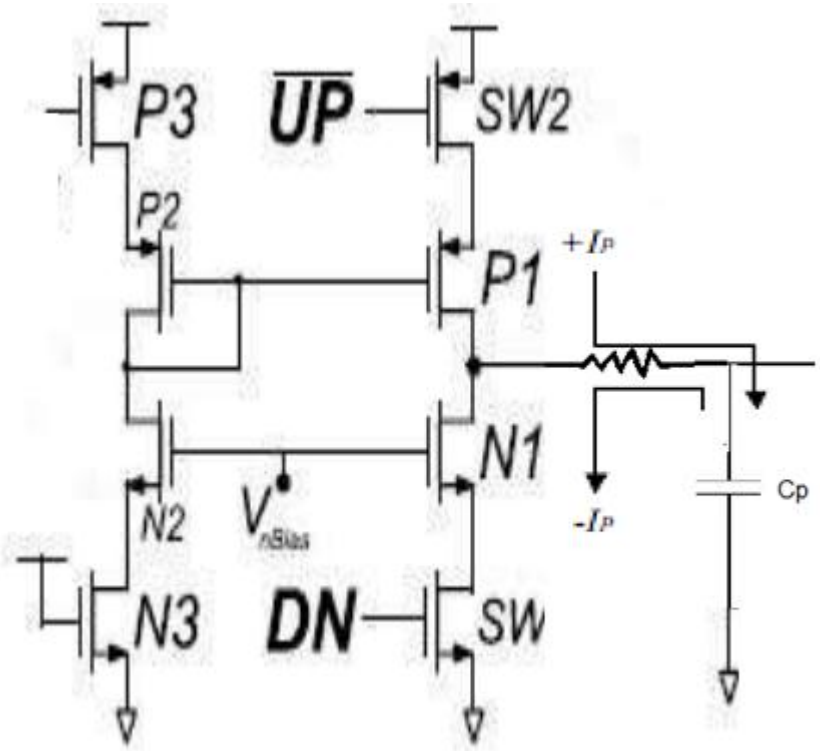

Figure 2.14CMOS charge pump with LPF[20]

When a circuit contains both NMOS and PMOS transistors we say it is implemented in CMOS (Complementary MOS). The conventional CP has 4 PMOS and 4 NMOS transistor Two MOS transistor work as switching device as ON-OFF and the others two equalize the charging, and discharging current.

2.4.3 Voltage controlled oscillator

In this part, a voltage controlled crystal oscillator is used in the PLL design.A voltage controlled crystal oscillator (VCXO) is is an oscillator whose frequency is determined by a crystal, but can be adjusted by a small amount by changing a control voltage.The circuit shown in Figure 2.15 includes varactors, crystal (10MHz) and two stage common collector amplifier.

As the capacitance of the varactors D1 and D2 changes, the crystal's model is affected and the oscillation frequency changes. The shunt capacitors are used to adjust the tuning range and offset the center frequency.

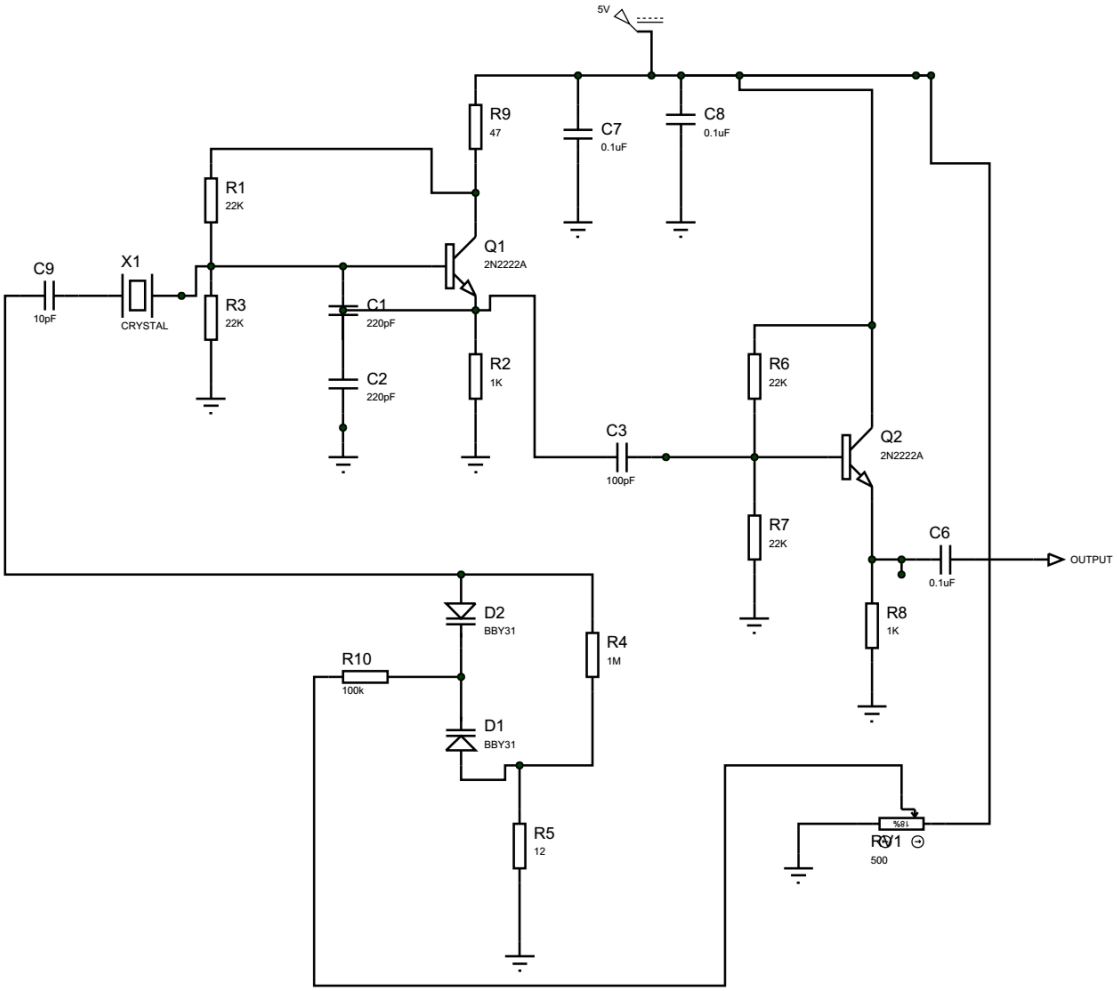

Figure 2.15VCXO circuit

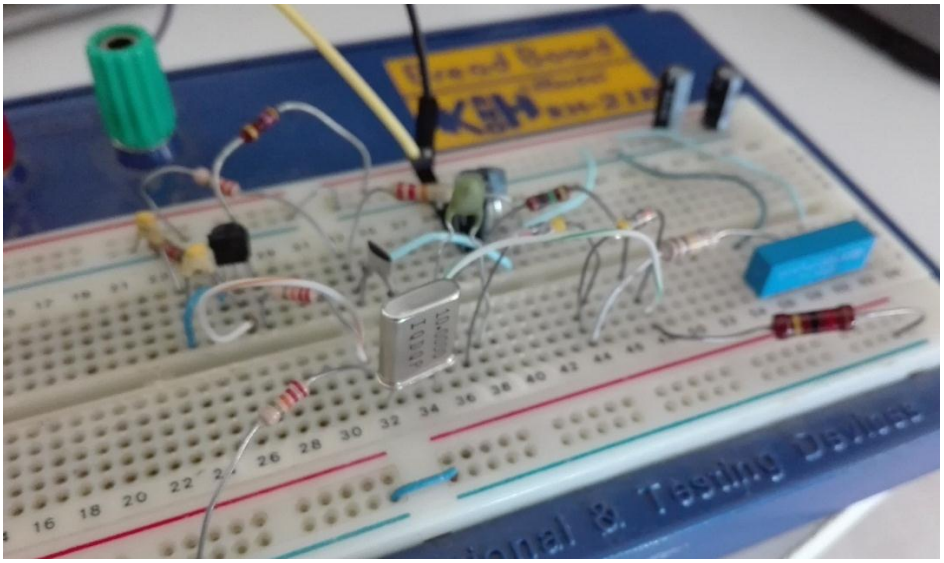

Figure 2.16 The implementation of the VCXO circuit

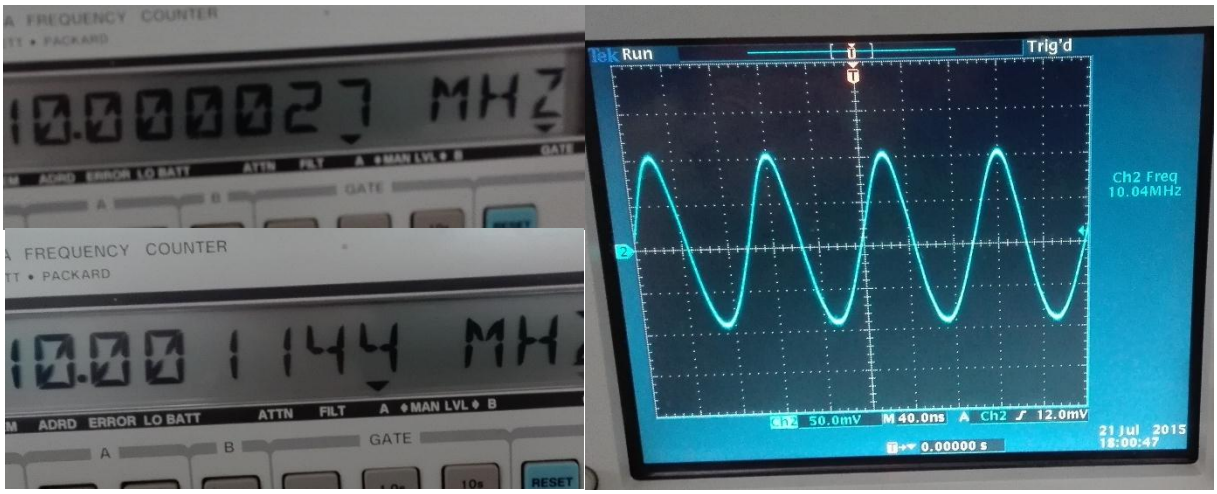

Figure 2.17 The results obtained from the 10 MHz VCXO

As can be seen in Figure 2.17, The Frequency change in range of 1.1 kHz as the voltage varies from 0V to 5V and the amplitude of the Obtained signal is almost 200 mV.

2.5 The Time Synchronization

The time synchronization module is the basis of the synchrophasor measurement architecture and is the element that distinguishes a PMU from a traditional digital measurement device. In fact, it allows the retrieval of an accurate source of time used to disseminate the time all over the system and discipline the synchronization of the other internal clocks and of the produced measurements.

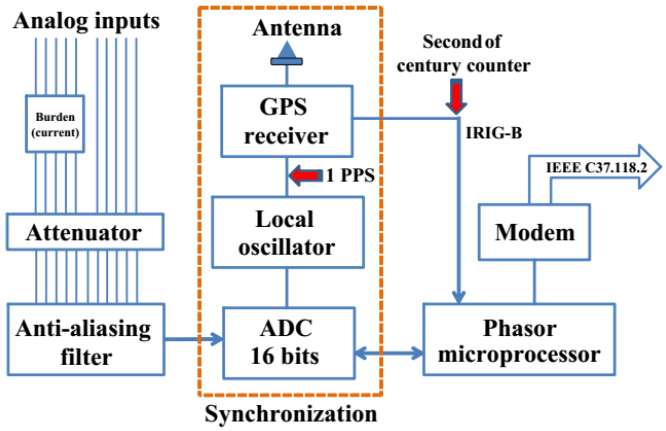

Figure 2.18 time synchronization module

The time synchronization required for synchrophasor estimation can be provided using a GPS receiver. The specification of the required GPS receiver which is typical for most GPS is the ability to generate two signal types (Figure 2.18). One of them is a 1PPS which provides the pulse-per-second that is, the accurate information about the start of the UTC second. No other time information is codified in the simple PPS signal and, for this reason, the

synchronization source should also be able to provide other absolute time information necessary to determine the UTC time label. [21]

The sampled signal is synchronized with the 1PPS reference signal using a digital phase local loop (Figure 2.19). This consists of the VCXO output signal, the reference clock (1PPS), a phase difference detector and a low pass filter. This digital phase locked loop technique is used to quickly lock the locally generated sampling frequency with the 1PPS synchronizing accurate reference clock. The generated clock provides the timing signals to the data acquisition module for sampling the voltage and current signals. The accurate time information used for stamping the measured phasors is acquired from the transmitted time format according to the IRIG-B standard.[22]

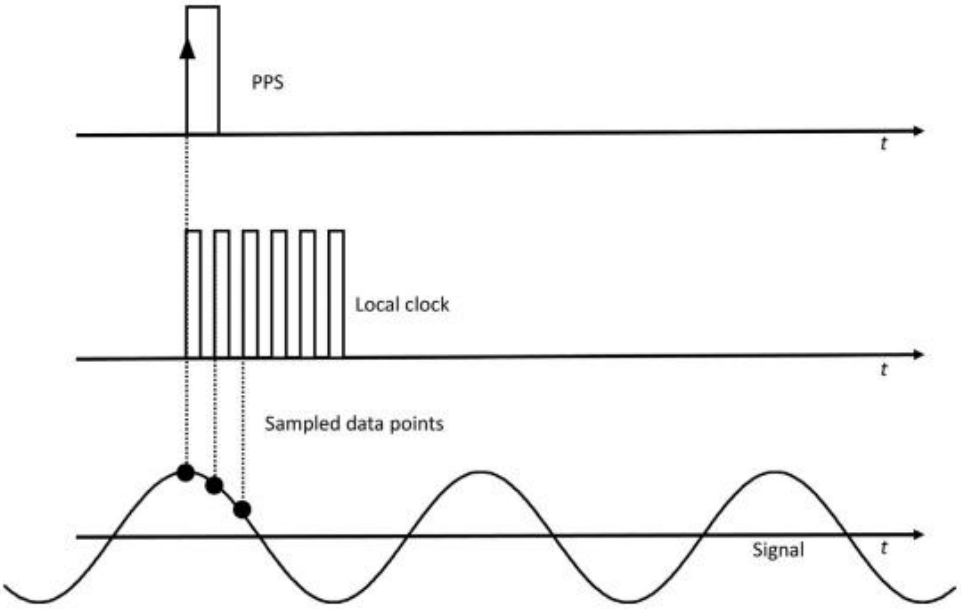

Figure 2.19Disciplined data acquisition

An example of time synchronization module is the Garmin GPS, it is used extensively in PMU research. Figure 2.20 shows a snapshot of the Garmin GPS receiver.

Figure 2.20 Garmin GPS receiver

2.6 **Data Acquisition System**

The DAQ is the front-end of the PMU. It includes the analog signal conditioning and the ADC. As aforementioned, the signal conditioning is the first stage of PMU elaboration that follows the transduction process performed, for example, by the Voltage Transformers (VTs) or Current Transformers (CTs) installed on the network. The voltage levels, the anti-aliasing filter cut-off frequency and the characteristics of the filter itself must match the ADC settings (the frequency) and the needs of the synchrophasor computation module.

The DAQ card selected here is the National Instruments NI DAQ. The reason for selecting the NI DAQ is because a lot of research work has been done on PMU using the NI software. NI-DAQ is a robust, time-proven driver for NI data acquisition and signal conditioning hardware. This software helps you quickly install your device and begin taking measurement data. NI-DAQ includes hundreds of application examples like:

- Jump-start your application development. NI-DAQ delivers the same ease of use and performance across many development environments.

-operating systems, and computer buses.

-Measurement & Automation Explorer simplifies the configuration of your measurement hardware.

-Quickly detect and configure all hardware.

-Use test panels to verify the operation of your hardware.

- Make simple, interactive measurements.

-Name and scale your I/O channels to physical or engineering units.

-Powerful Programming.

-Synchronization of measurements across multiple devices.

In this project we are going to use NI PCI 6221 as shown in the Figure 2.21. The NI PCI 6221 uses M series technology to deliver high performance, reliable data acquisition capabilities to meet a wide range of application requirements. Here are some characteristics of The NI PCI 6221:

-Easy to use powerful, graphical development with LabVIEW.

-16-bit,250KS/s,16 analog Inputs; two 16-bit analog outputs

-24 digital I/O lines,32-bit counters; digital triggering.

-correlated DIO (8 clocked lines, 1MHZ).

-NI-DAQ DAQmx measurements services to simplify configuration and measurements.

-Includes a cable and connector block.[23]

Figure 2.21 NI PCI 6221 DAQ card

We connect the DAQ to the computer and install all the necessary programs, of course, making sure that it is running well with LabVIEW. Using the NI 189588c-02 SHC68-68-RMIO Cable shown in the Figure 2.23, which connects to the terminal block of multifunction reconfigurable I/O (RIO) device known as NI CB- 68LP for displaying data in LabVIEW .These data is gotten through the PCB board so we use the RC68-68 Ribbon Cable shown in the Figure 2.22 which connects the PCB board to the NI CB-68LP.

Figure 2.23 NI 189588c-02 SHC68-68-RMIO Cable

Figure 2.22RC68-68 Ribbon Cable

The NI CB-68LP Figure 2.24 is a low-cost termination accessory with 68 screw terminals for easy connection of field I/O signals to 68-pin DAQ devices. It includes one 68-pin male connector for direct connection to 68-pin cables. The connector blocks include standoffs for use on a desktop or for mounting in a custom panel. The NI CB series digital and trigger I/O terminal block come in a variety of configuration and form factors, allowing the user to choose which I/O connector would best serve their needs.

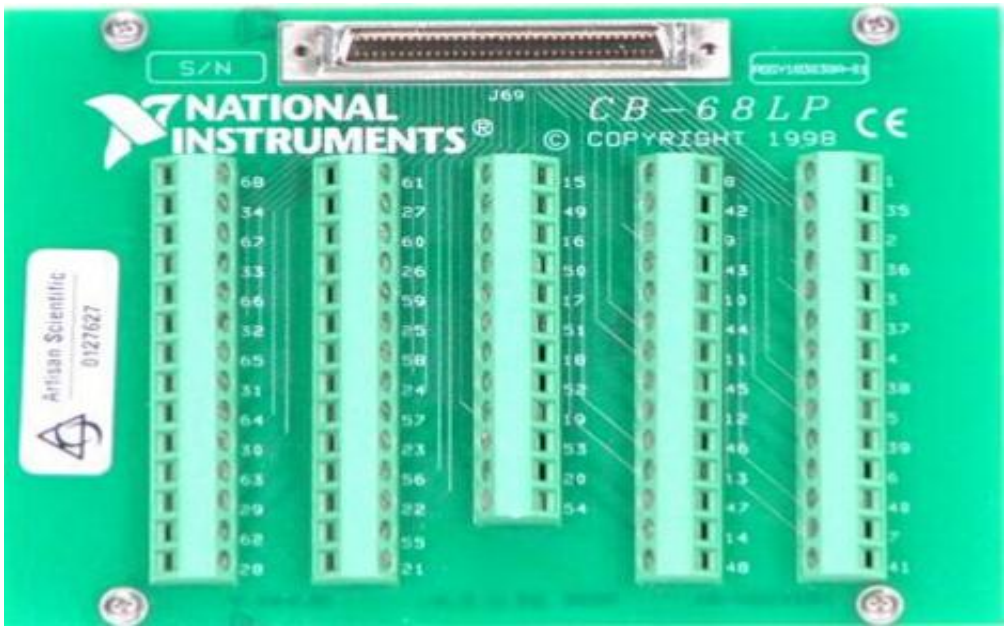

Figure 2.24NI CB-68LP board

2.7 **Conclusion**

This chapter takes a part of this report as generalities about the PMU device. From the design view side, a typical hardware and software architecture structure performing different functions have been discussed and described. So, we have been familiar with all PMU components and how to use in a perfect manner.so now we can install our PMU device and do all the necessary analysis based on the LabVIEW in the next chapter.

Chapter 3: Software Description and System Testing

3.1 Introduction

Chapter 2 covered basically the design as well as the implementation of the hardware blocks of the PMU. In this chapter we will demonstrate the algorithm that generate the phasor estimator and the software that perform these calculations, the next stage was testing the PMU device which involved evaluating the performance of the PMU through some experiments as well as obtaining results and drawing conclusions based on the results.

3.2 Phasor Estimation Techniques

Phasors are the most important quantities in power system operation. Phasor can constitute the state of the power system. It is therefore essential to find the best algorithm for estimating the phasor and implements it. The most popular algorithms of PMU measurements are assumed to be:

- Zero Crossing [24]
- Discrete Fourier Transformation (DFT)][25]
- Least Error Squares[26]
- Wavelet approach [27]
- Level Tracking [26]

3.2.1 Discrete Fourier Transform (DFT):

Discrete Fourier Transform (DFT) is widely used as phasor estimation algorithm of fundamental frequency. Due to their good harmonic rejection property conventional DFT algorithm achieve excellent performance when the signal contains only fundamental frequency and integer harmonic frequency components. DFT technique has been used in this research for modelling of PMU with the help of NI LabVIEW software.

Consider a sinusoidal input signal of frequency f_o given by:

$$x(t) = X_m \cos(2\pi f_o + \varphi_i) \quad (3.1)$$

Where

X_m : maximum value of the input signal,

f_0: the nominal frequency,

φ_i : the initial phase angle of the input signal

the signal is conventionally represented by a phasor $\overline{X}$

$$\overline{X} = \frac{X_m}{\sqrt{2}} e^{j\phi} = Xe^{j\phi} \tag{3.2}$$

Assuming that the signal x(t) is sampled N times per fundamental period (50Hz or 60Hz) waveform to generate the sample set:

$$x_k = X_m \cos\left(\frac{2\pi}{Nf_o} k + \varphi_i\right) \tag{3.3}$$

The phasor $\overline{X}$ is given by:

$$\overline{X} = \frac{\sqrt{2}}{N}\left(\sum_{k=1}^{N} x_k \left\{\cos\left(\frac{2\pi}{N}k\right) - j\sin\left(\frac{2\pi}{N}k\right)\right\}\right) \tag{3.4}$$

Equation (3.4) represents a phasor measurement performed by the DFT algorithm for a period data window that is a set of N samples for a fixed data window. This DFT procedure provides the phasor computation for a fixed-length data window, but Eq. (3.4) represents non recursive estimations. This means that Eq. (3.4) calculations are repeated for each data window as shown in Figure 3.1 as time progresses. This procedure requires 2N multiplications and (N-l) additions to produce the phasor X. It should however be noted that in progressing from one data window to the next, only one sample (X) is discarded and only one sample (X_N) is added to the data set. It is therefore advantageous to develop a technique which retains 2(N-1) multiplications and 2(N-1) sums corresponding to that portion of the data which is common to the old and new data windows.[5]

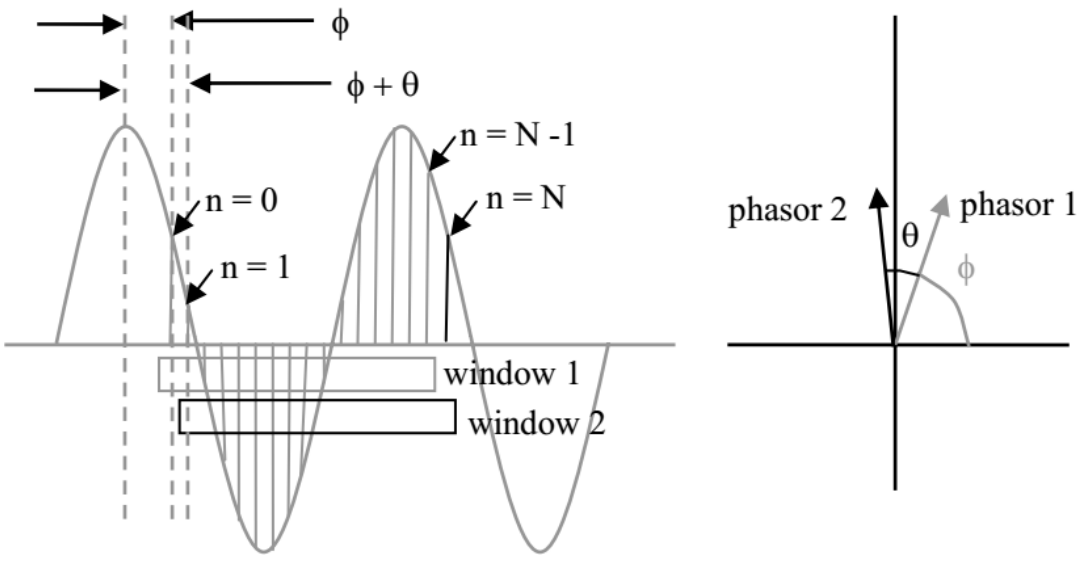

Figure 3.1 Non-recursive phasor estimation for two windows

A modified algorithm which saves computation taking into account data from previous window is called as recursive algorithm [10-14] which can be given by the equation below:

$$\hat{x}_N = \hat{x}_{N-1} + \frac{\sqrt{2}}{N}(x_N - x_0)\, e^{-j(0)\frac{2\pi}{N}} \tag{3.5}$$

X_N: the last sample.

X_0: the first sample.

Last sample in the window being (N + r) the phasor is given as:

$$\hat{x}_{N+r} = \hat{x}_{N+r-1} + \frac{\sqrt{2}}{N}(x_{N+r} - x_r)\, e^{-j\frac{2\pi}{N}r} \tag{3.6}$$

The recursive phasor estimation differs from the non-recursive estimate by an angular retardation of θ ($\frac{2\pi}{N}$). The advantage of using this alternative definition for the phasor from the new data window is that (N – 1) multiplications by the Fourier coefficients in the new window are the same as those used in the first window. Only a recursive update on the old phasor needs to be made to determine the value of the new phasor.[25]

It is interesting to note that when the input signal is a pure sine wave of fundamental frequency $\hat{x}_{N+r} = \hat{x}_r$ for all r as shown in Figure3.2

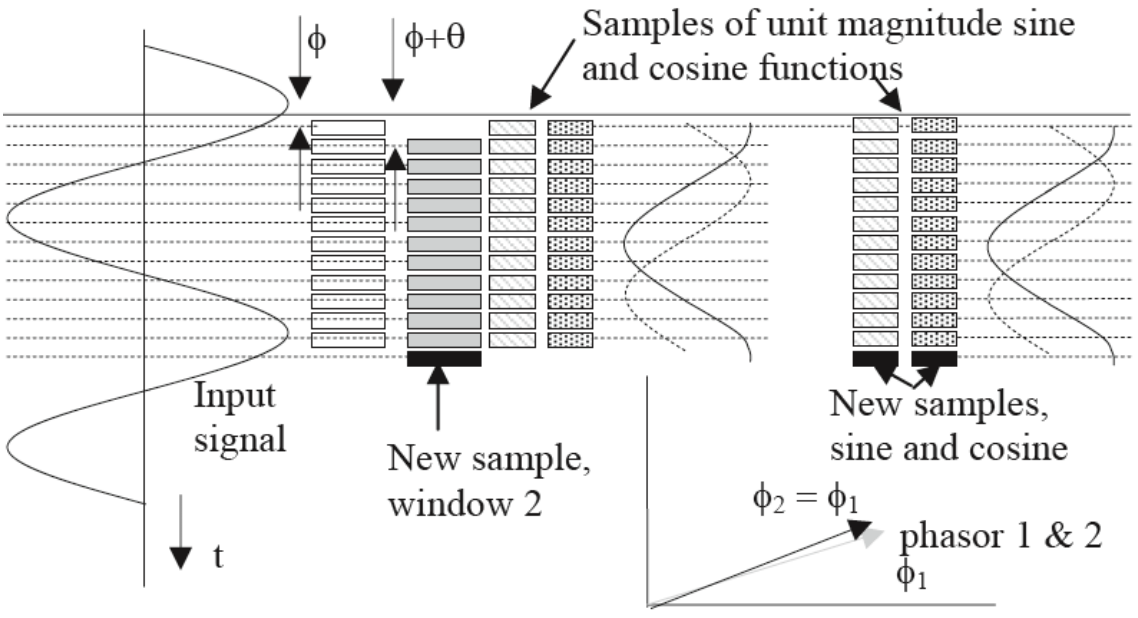

Figure 3.2 recursive phasor estimation for 2 windows

3.3 What is LabVIEW?

Laboratory Virtual Instrument Engineering Workbench (LabVIEW) is systems engineering software for applications that require test, measurement, and control with rapid access to hardware and data insights. An application created in LabVIEW is called a virtual instrument (VI). For the developer, a VI consists of two different panels (Figure3.3): a graphical programming panel (or the block diagram), and a visual front panel. The front panel contains buttons and other control components. The actual calculations are performed in the graphical programming panel, with the front panel control actions as inputs. The outputs from the calculations are sent to the front panel indicators for visualization. The front panel is the only visible panel to the user, which makes the applications developed in LabVIEW more user friendly than most. If a project demands large amounts of code, or some part of code is reusable in other places, LabView conveniently allows the developer to extract it into a different secondary virtual instrument (subVI). A subVI is basically an ordinary VI, with the exception that it is intended to be dependent on input, and to result in outputs provided and required from elsewhere. This subVI can be placed and connected where desired in the other VI, in order to perform the part of code it contains. This makes the graphical programming more manageable, as well as allowing easier reassembly of VIs, that only require parts of the original VI. An illustrative comparison is to think of the subVIs as Lego bricks, that constitute the assembled Lego object, which then corresponds to the main VI.

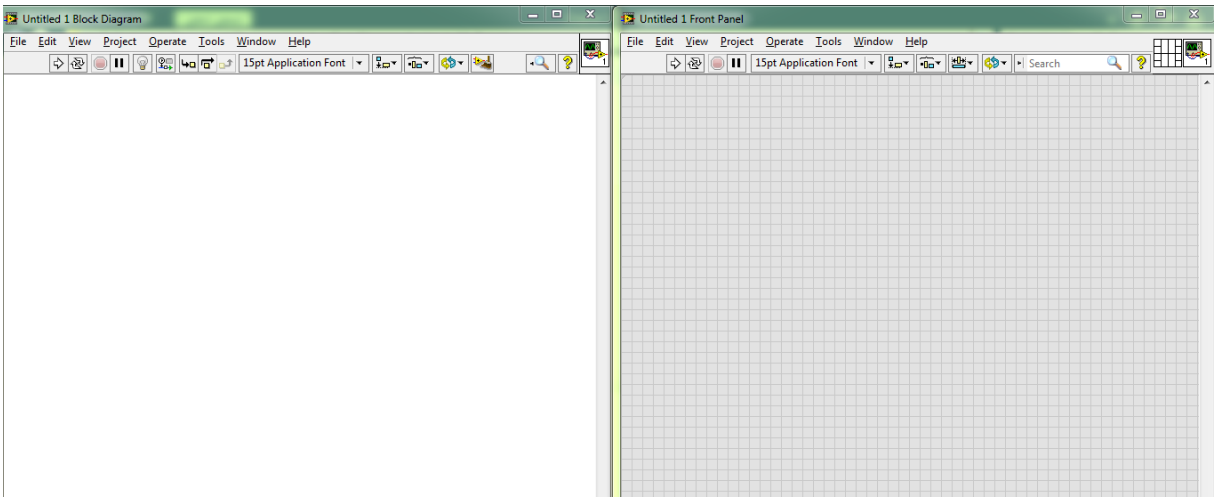

Figure 3.3 Block Diagram and Front Panel for VI

In the past, LabVIEW was just a graphical programming language that was developed to make it easier to collect data from laboratory instruments using data acquisition systems.

LabVIEW was always easy to use once you got used to wiring connectors to write your computer programs, and it definitely makes data acquisition an easier task than without LabVIEW, but LabVIEW is not just for data acquisition any more.

LabVIEW can be used to perform the following:

• acquire data from instruments

• process data (e.g., filtering, transforms)

• analyze data

• control instruments and equipment

For engineers, LabVIEW makes it possible to bring information from the outside world into a computer, make decisions based on the acquired data, and send computed results back into the world to control the way a piece of equipment operates.[28]

3.4 Simulation of the phasor estimator:

In the non-recursive algorithm, the input signal can be generated from library VI i.e. Simulate Signal VI. This analog input signal is then converted to discrete signal and stored in an array. Here data window is considered for 12samples. A user defined VI has to be prepared for calculating the Fourier coefficient of the data samples. Appropriate arithmetic operations are performed to estimate phasor for first data window. The complex term obtained after phasor estimation is converted into polar form and displayed as output. This algorithm is repeated for subsequent data samples. As newer estimate of phasor is performed, the phasor rotates anticlockwise by an angle Θ due to delay of each sample by one sampling angle. The non-recursive block diagram and its LabVIEW model are given in Figure 3.4 and Figure 3.5

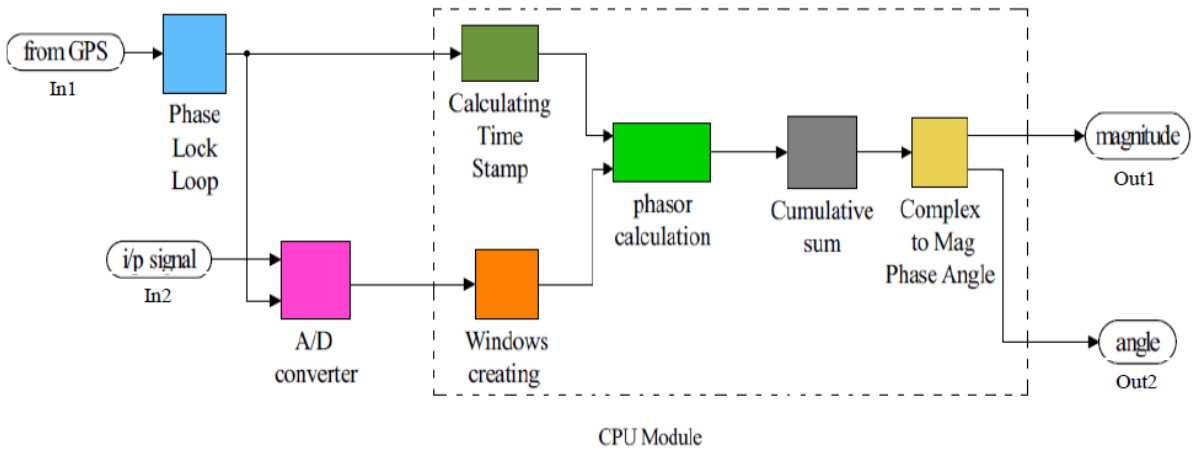

Figure 3.4 block diagram for Non-recursive algorithm

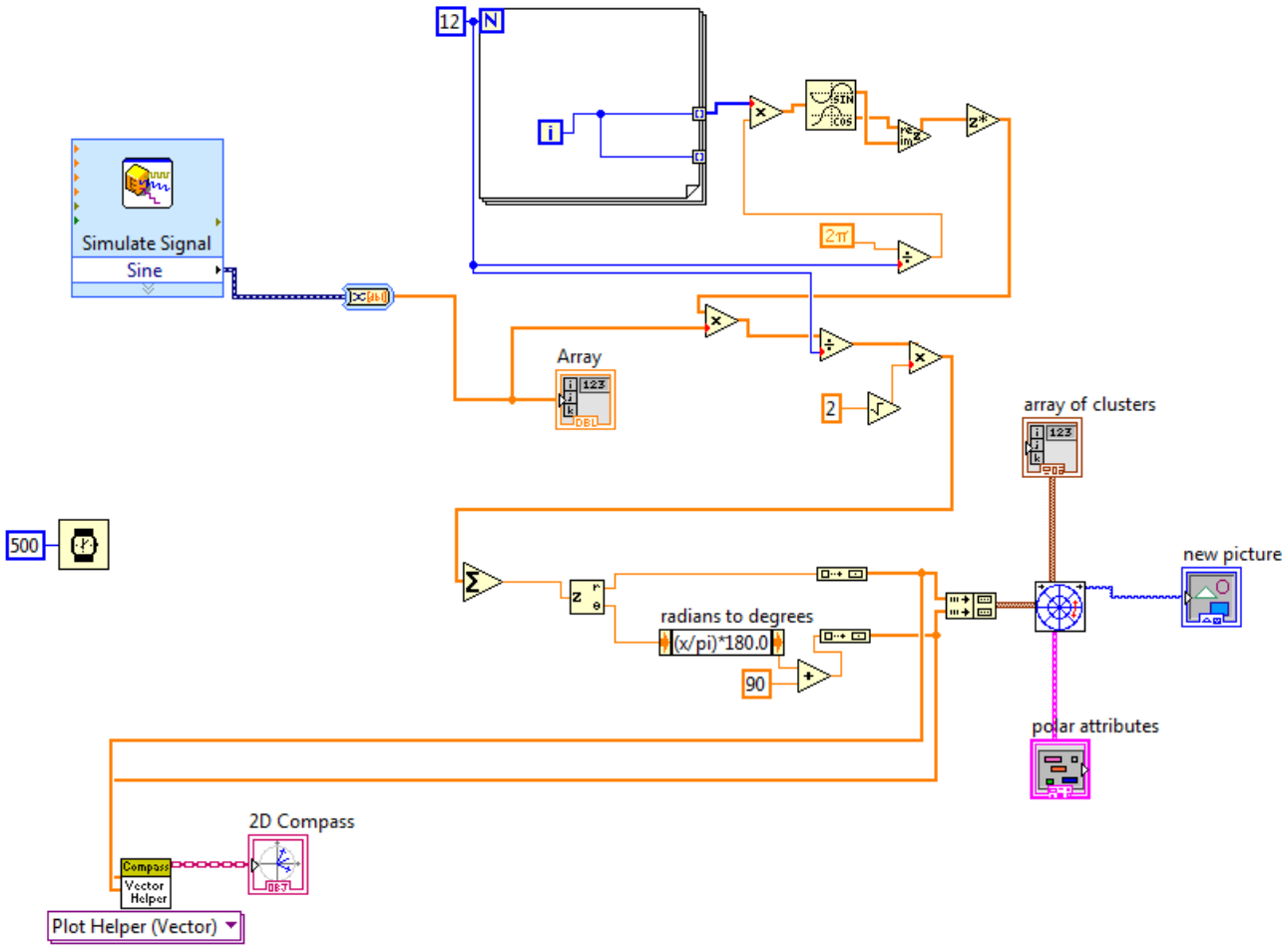

Figure 3.5 LabVIEW Model for Single Phase Non-recursive algorithm

For recursive algorithm we need to have a phasor estimate obtained over a data window preferably by non-recursive algorithm. The above-mentioned algorithm is used to generate the first estimate of phasor in the case studies here. Once the phasor has been obtained for one data window, recursive algorithm is used. When phasor estimate is obtained for $(N+r-1)^{th}$ sample, $(N+r)^{th}$ sample is compared with r^{th} sample using suitable mathematical operands provided in the standard library. The difference in the sample value dictates in the updation of new estimates of phasor utilizing Equation (3.6).

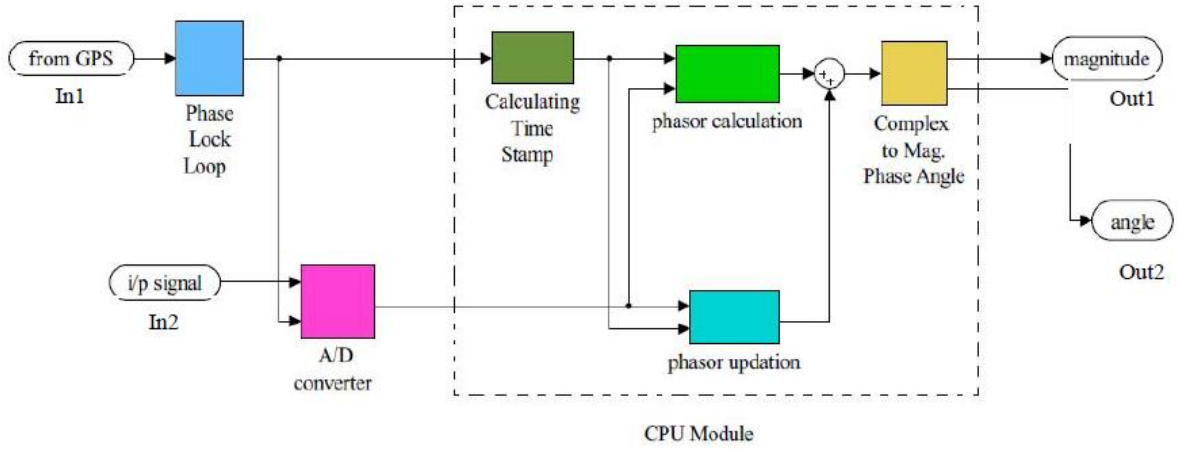

Figure 3.6 Block diagram for Recursive algorithm

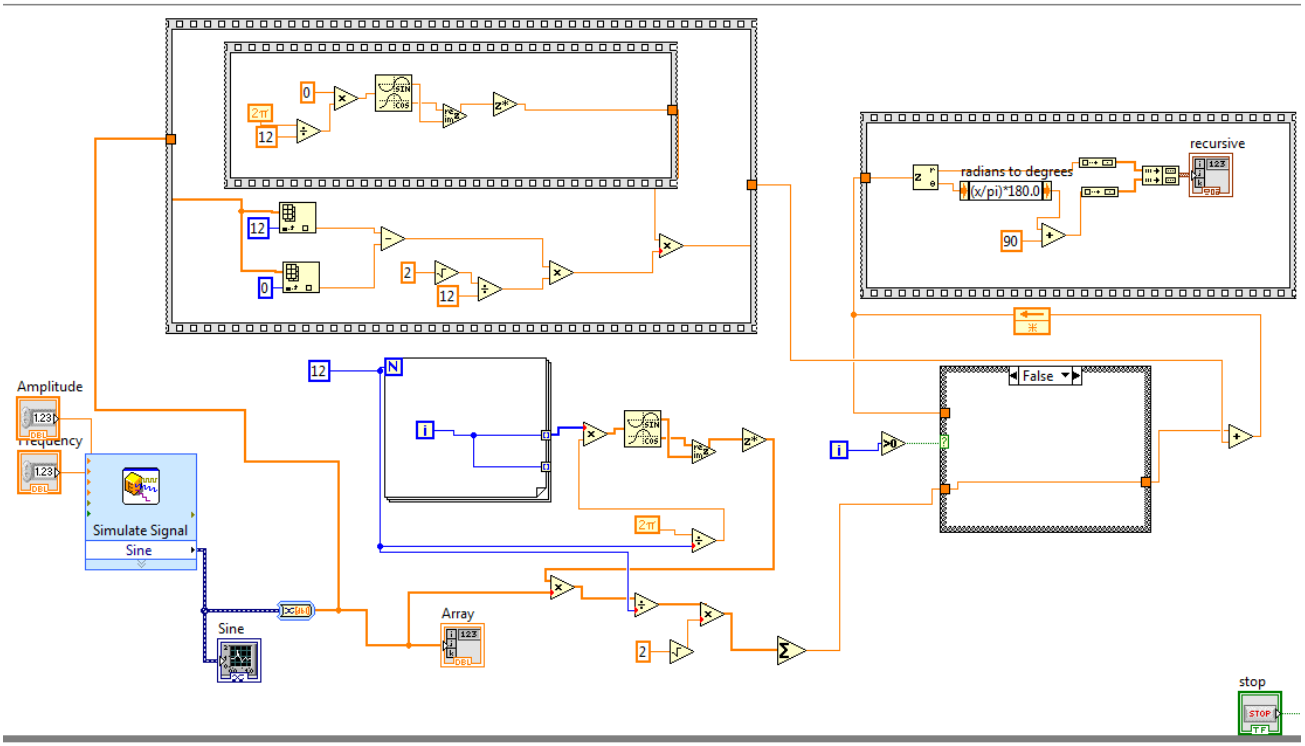

Figure 3.7 LabVIEW Model for Single Phase recursive algorithm (False case)

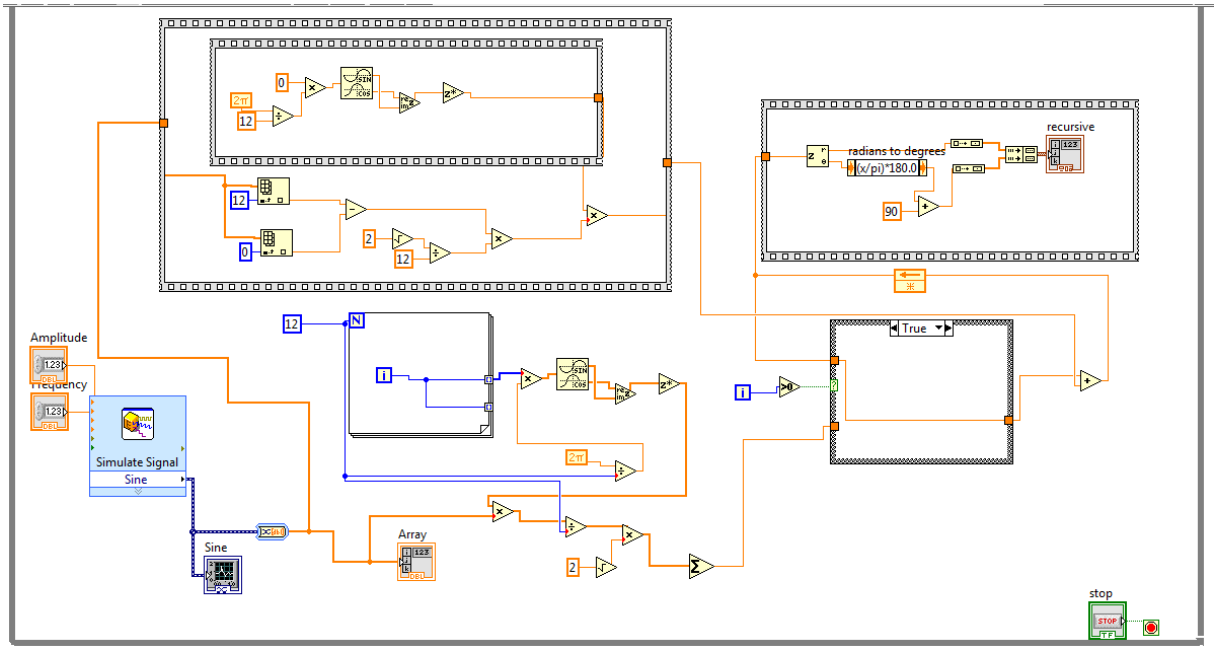

Figure 3.8 LabVIEW Model for Single Phase recursive algorithm (True case)

3.4.1 Results of simulation:

Figures3.9 and 3.10 show phasor estimates for non-recursive updates and Figures3.11 and 3.12 show phasor estimates for recursive updates. Itis evident from Figure 3.10 that the new phasor has been progressed by 30^{o} from the phasor shown in Figure 3.9. This doesn't happen with recursive phasor estimation and both the Figure 3.11 and 3.12 are identical in spite of the fact that they have been computed over different data windows. Since recursive algorithm performs less computations to estimate phasor, it is way faster than the non-recursive estimate.

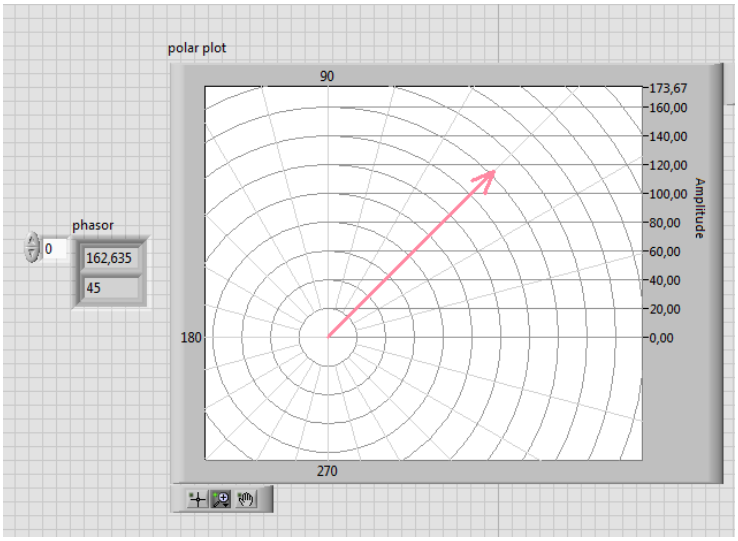

Figure 3.9 Phasor estimation using Non-recursive algorithm for first data window

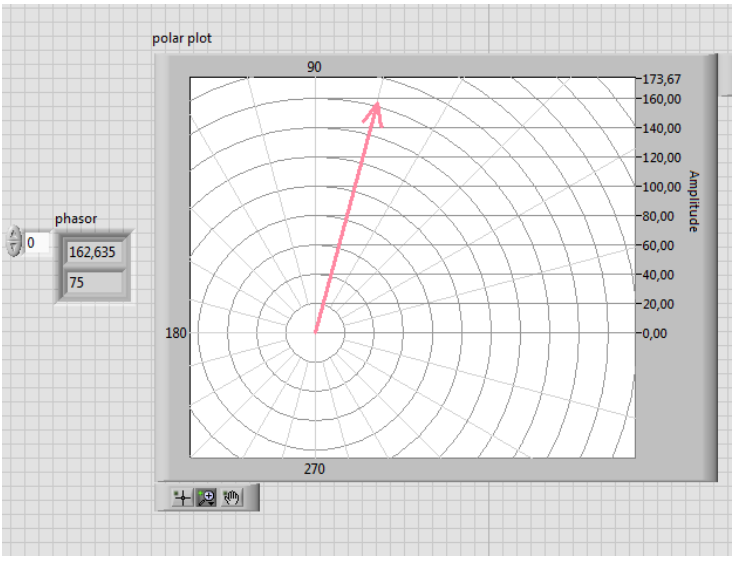

Figure 3.10 Phasor estimation using Non-recursive algorithm for second data window

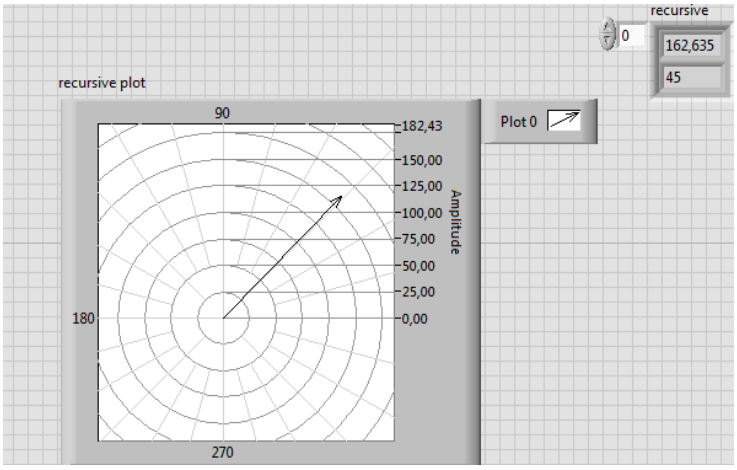

Figure 3.11 Phasor estimation using recursive algorithm for first data window

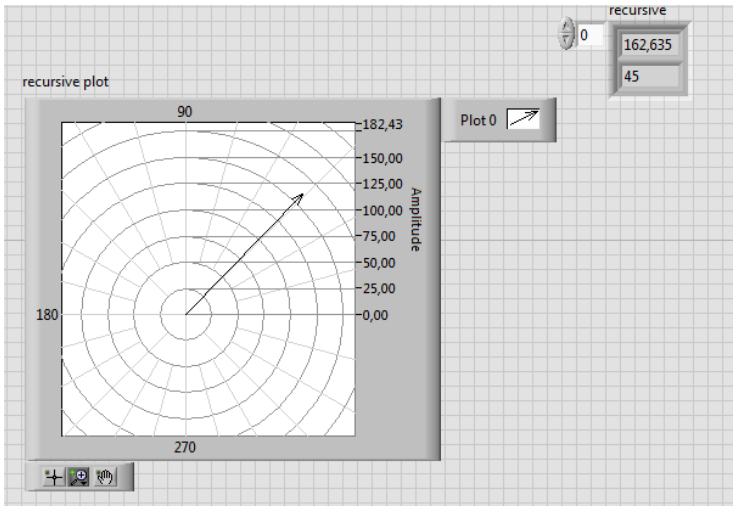

Figure 3.12 Phasor estimation using recursive algorithm for second data window.

Since phasor estimation is performed over a cycle, the first phasor is obtained after obtaining 12 samples i.e. after one complete cycle of the sinusoid. That is why the first 11 columns of Table 2.1 are empty of the recursive and non-recursive phasor updates. After the first 12 samples are acquired phasor is computed by both the algorithm and is presented below. As stated before, phasor estimates obtained from non-recursive phasor update will have a constant magnitude but will rotate anti-clockwise with each estimate.

Table 3-1 Phasor estimation for recursive and non-recursive algorithm

Sample no.	Sample Xn	Non-recursive phasor estimate	Recursive Phasor estimate
0	162.635	_____	_____
1	59.5284	_____	_____
2	-59.5284	_____	_____
3	-162.635	_____	_____
4	222.163	_____	_____
5	-222.163	_____	_____
6	-162.635	_____	_____
7	-59.5284	_____	_____
8	59.5284	_____	_____
9	162.635	_____	_____
10	222.163	_____	_____
11	222.163	$162.635\angle 45^o$	$162.635\angle 45^o$
12	162.635	$162.635\angle 75^o$	$162.635\angle 45^o$
13	59.5284	$162.635\angle 105^o$	$162.635\angle 45^o$
14	-59.5284	$162.635\angle 135^o$	$162.635\angle 45^o$
15	-162.635	$162.635\angle 165^o$	$162.635\angle 45^o$
16	222.163	$162.635\angle -165^o$	$162.635\angle 45^o$
17	-222.163	$162.635\angle -135^o$	$162.635\angle 45^o$
18	-162.635	$162.635\angle -105^o$	$162.635\angle 45^o$
19	-59.5284	$162.635\angle -75^o$	$162.635\angle 45^o$

3.5 **Implementation of the phasor estimator:**

The only thing to do is to change the simulated signal block by the DAQ assistant block. The implementation of the 3phase estimator is nothing but a replica of single-phase system with each phased is placed by 120°. the Figures below Show implemented program and the results obtained.

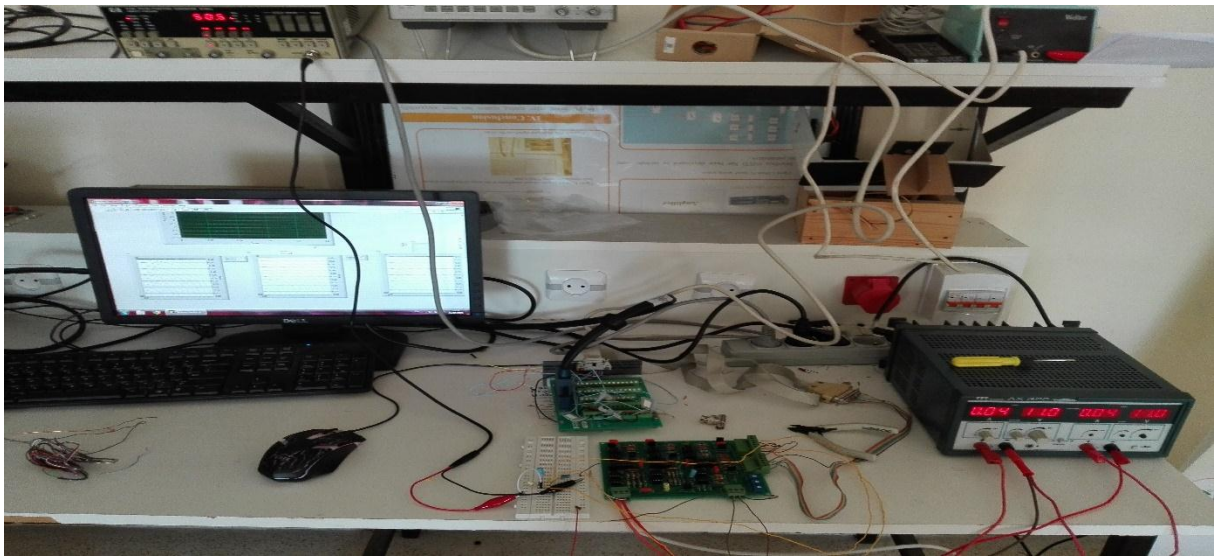

Figure 3.13PMU device setup

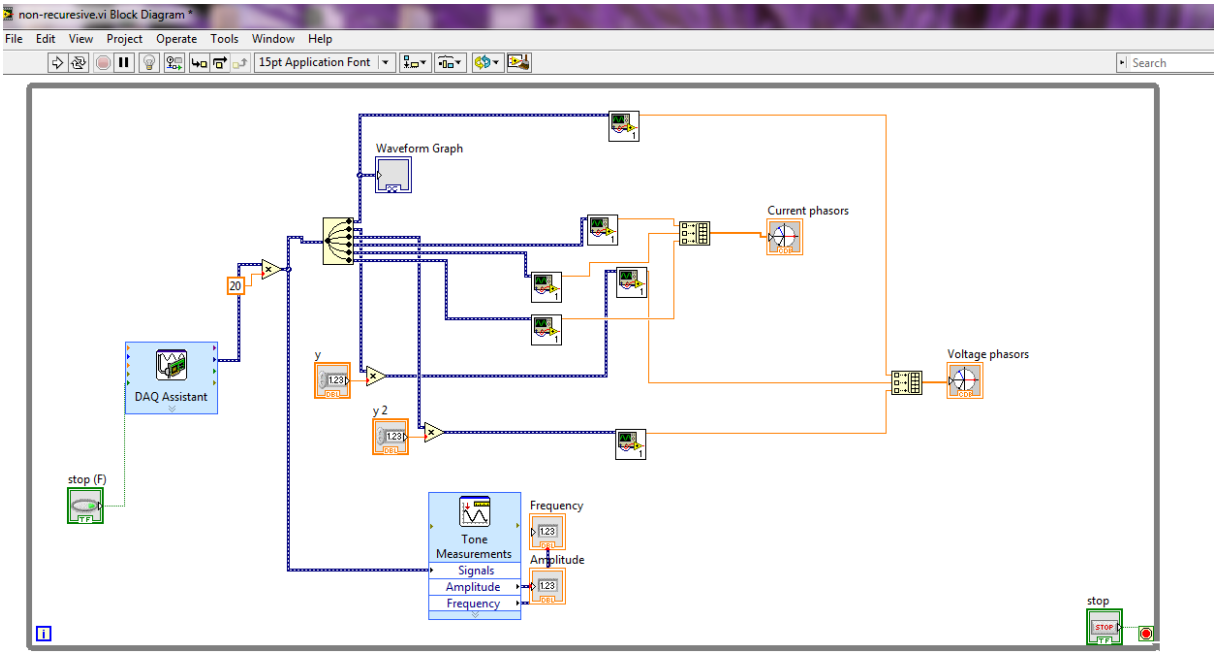

Figure 3.14 The complete program for the phasor estimator (3 phase)

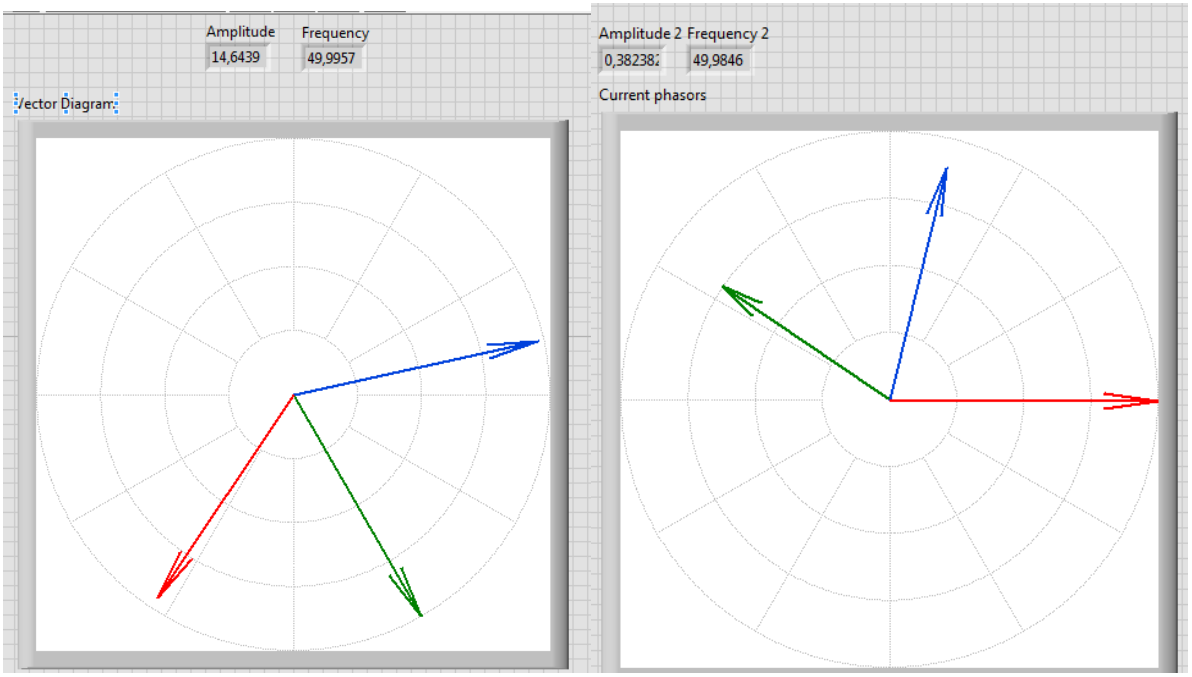

Figure 3.15 Estimated phasor for 3 phase (Voltages and Currents)

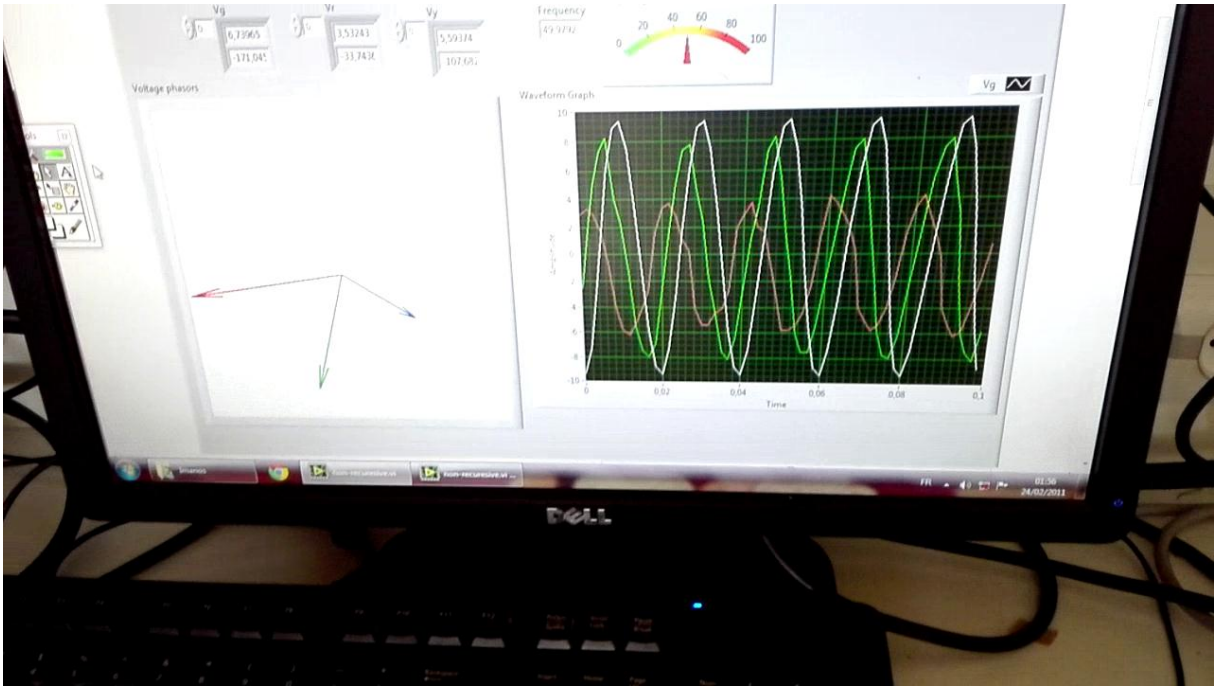

Figure 3.16 The results obtained from the implemented program

3.5.1 Results discussion

For protection purposes, emulation of the power lines is implemented using a combination of resistors and capacitors in series (Figure 3.17) to generate phase shift between each phase voltage. Since a power system is never in steady state, the phase angles rotate clock wise or anti clock wise when the frequency is smaller or greater than the nominal frequency respectively.

A proposed solution to this issue is to implement a new algorithm known as frequency tracking which can estimate the real frequency and correct the amplitude and the phase angle according to that measured frequency.

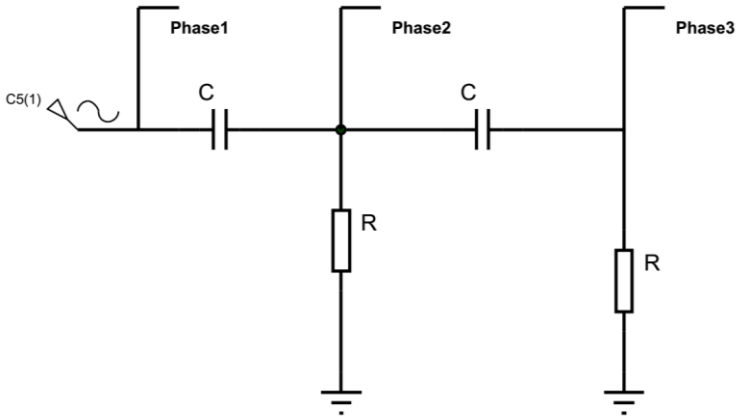

Figure 3.17 The RC circuit that gives phase shift between phase voltages.

Conclusion

At the end of this project, we can say that a 70% percent of the constructed PMU was done successfully.

The anti-aliasing filters was designed, implemented as a PCB board and tested in successful way. The only remarkable thing is that the transition band of these filters is little wide. As a solution to this problem is to increase the order of the filter

The implementation of synchronization module is incomplete, we demonstrated the function of the phase locked oscillator and explained its components by analyzing the circuit of each part. The only part that is implemented of this feedback system is the voltage-controlled crystal oscillator. We tested it and we found that the range of the frequency that the VCXO can control it is 1 KHz. This value must be increased by changing the amount of the capacitors.

After completing the hardware implementation, we moved to the software one, where we used the Discrete Fourier Transform DFT algorithm to estimate the phasors from voltage and current signals. Both of Non-recursive and recursive methods are used in this project. We found that the non-recursive is more complex in computations but it is more accurate than the recursive algorithm.

Further work

The constructed PMU has been able to achieve the fundamental purpose of estimating phasors. However, the performances of estimated phasors are unsatisfactory. So, and as a future work, an improvement of the performance of phasor estimation algorithms is needed. Also, the synchronization of the acquired data must be implemented by following the demonstration given in chapter2.

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Appendix

Table A-1Butterworth Coefficients

n	i	a_i	b_i	$k_i = f_{Ci} / f_C$	Q_i
1	1	1.0000	0.0000	1.0000	____
2	1	1.4142	1.0000	1.0000	0.71
3	1	1.0000	0.0000	1.0000	____
	2	1.0000	1.0000	1.272	1.00
4	1	1.8478	1.0000	0.719	0.54
	2	0.7654	1.0000	1.390	1.31
5	1	1.0000	0.0000	1.0000	____
	2	1.6180	1.0000	0.859	0.62
	3	1.6180	1.0000	1.448	1.62
6	1	1.9319	1.0000	0.676	0.52
	2	1.4142	1.0000	1.0000	0.71
	3	0.5176	1.0000	1.479	1.93
7	1	1.0000	0.0000	1.0000	____
	2	1.8019	1.0000	0.745	0.55
	3	1.2470	1.0000	1.117	0.80
	4	0.4450	1.0000	1.499	2.25
8	1	1.9616	1.0000	0.661	0.51
	2	1.6629	1.0000	0.829	0.60
	3	1.1111	1.0000	1.206	0.90
	4	0.3902	1.0000	1.512	2.56
9	1	1.0000	0.0000	1.0000	___
	2	1.8794	1.0000	0.703	0.53
	3	1.5321	1.0000	0.917	0.65
	4	1.0000	1.0000	1.272	1.00
	5	0.3473	1.0000	1.521	2.88
10	1	1 1.9754	1.0000	0.655	0.51
	2	1.7820	1.0000	0.756	0.56
	3	1.4142	1.0000	1.0000	0.71
	4	0.9080	1.0000	1.322	1.10
	5	0.3129	1.0000	1.527	3.20