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Department of Power and Control

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MASTER

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Title:

PC Based Relay Tester

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Dedication

I lovingly dedicate this work to my family, all languages known to man cannot translate the sentiments my heart harbors for them into words, and all the knowledge of the world cannot quantify the amount of love and appreciation I have for them, to my parents, brothers and sister.

To all the friends I knew and hopefully will know for years to come, friends whose companionship pushed me through the hard times and their very presence and friendship made the sweet sweeter.

I dedicate this work to those whose lives crossed paths with mine, whose words and actions shaped who I am today, to anyone who has ever offered me a word of encouragement or guidance, a pat on the back or a smile.

MAZOUZ Alaa Eddine

Dedication

I dedicate this work to the dearest people to my heart, my parents whose love blessed me and care sheltered me from the moment I opened my eyes to this world, to all my family, my brothers and sisters I dedicate this work with my heart filled with the hope that it would brighten your day and put a smile in your face.

To my friends for their unwavering support, for offering me a shoulder to lean on whenever I needed one, for simply being there with me and bearing the burdens of my journey, I would not be standing where I am if not for you.

For all the people who believed in me and had my best interest in their hearts, I dedicate this humble work and share this tremendous joy with each and every one of you.

MESSAOUDI Mohammed

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This humble work would never have come into fruition if not for the continuous support of our supervisor Pr. Hamid Bentarzi whose guidance and directions paved the path for our success from the first lecture we attended to the last correction session.

No words can express our gratitude to all the teachers of the institute who spared no effort in providing us with all the knowledge we needed up to this point and will need in our future endeavors.

We also would like to extend our thanks to the administration of the institute for the logistic support that was provided and all the equipment that was unhesitatingly put at our disposal.

A special thanks to our dear friend REFAFA Abderrahman for his invaluable help and selfless contributions.

To anyone who contributed to the final work, no matter how small the contribution, even with a few words of encouragement, this work could not have been made possible if not for you.

Abstract

Power quality disturbances are an issue that is gaining so much attention within the research community because of its detrimental consequences on the power grid, instruments and customers alike. Relays are the first line of defense in the face of these disturbances rendering their existence the most important in the protection scheme; relay testing is therefore just as important.

This project deals with the design and implementation of a Relay Tester, which is based on the simulation of power quality disturbances and fault signals using LabVIEW environment and the generation of these signals using data acquisition card. These fault signals are amplified to the standard relay values using a Class-D amplifier. The amplified signals are injected into the relay to test its functionality.

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Introduction

Relays are protective devices used to protect all elements of power systems, their main purpose is to detect and isolate faults quickly and reliably in order to maintain the availability of the system and ensure its safety.

Therefore, the availability of the power grid is highly dependent on the functionality of these devices. With usage relays get deteriorated and malfunction therefore it's the interest of both the end user as well as the manufacturer to check their behavior regularly from their initial development through production and commissioning to periodical maintenance during operation, and that is where relay testing comes into the picture.

There are three types of testing methods performed on relays, steady state, dynamic state and transient. All of these methods rely on injecting different kinds of signals into the relay and monitoring its behavior and statues and drawing conclusions based on that behavior. It is essential for any relay testing device to be capable of outputting a wide range of variable signals that simulate all possible fault signals and power disturbances that a protective relay may be subjected to in its working environment within the power grid.

These disturbances can be one of many; the most frequently encountered are voltage sag, voltage swell, harmonic disturbance, DC offset [1].

The use of innovative testing solutions offers a high degree of efficiency and effectiveness for testing the complete range of different protection equipment, and contributes to the future reliability of the protection system.

The aim of this project is to design and implement a protective relay testing system that is PC based, capable of simulating and generating fault signals to be used for testing the functionality of the relay, the simulation is made in LabVIEW environment, the generation is done through a NI's PCIe card and an amplifier.

Chapter I: Protective Relays

The IEEE defines protective relays as: "relays whose function is to detect defective lines or apparatus or other power system conditions of an abnormal or dangerous nature and to initiate appropriate control circuit action" [2]

Relays detect and locate faults by measuring electrical quantities in the power system, which are different during normal and intolerable conditions.

The most important role of protective relays is to prevent the power system from cascading failures thereby providing necessary equipment protection and minimizing damages resulting from faults, these faults can occur as a result from insulation deterioration or unforeseen events and are usually referred to as power quality disturbances or faults.

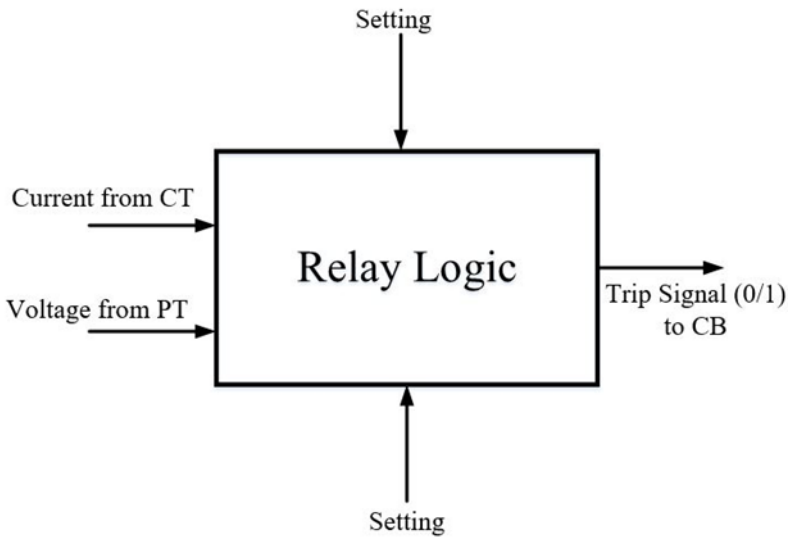


Figure 1. 12:Conceptual Diagram of Protective Relay

1.1 Relay Requirements

Dependability

A relay is said to be dependable if it trips only when it is expected to trip. This happens either when the fault is in its primary jurisdiction or when it is called upon to provide the back-up protection. However, false tripping of relays or tripping for faults that is either not within its jurisdiction, or within its purview, compromises system operation.

Security

On the other hand, security is a property used to characterize false tripping on the relays. A relay is said to be secure if it does not trip when it is not expected to trip. It is the degree of certainty that the relay will not operate incorrectly. False trips do not just create nuisance. They can even compromise system security. For example, tripping of a tie line in a two-area system can result in load-generation imbalance in each area, which can be dangerous.

Selectivity

Like sensitivity, selectivity also implies an ability to discriminate. A relay should not confuse some peculiarities of an apparatus with a fault. For example, transformer when energized can draw up to 20 times rated current (inrush current) which can confuse, both overcurrent and transformer differential protection. Typically, inrush currents are characterized by large second harmonic content.

Reliability

A relaying system has to be reliable. Reliability can be achieved by redundancy i.e. duplicating the relaying system. Obviously, redundancy can be a costly proposition. Another way to improve reliability is to ask an existing relay say, protecting an apparatus A to backup protection of apparatus B. Both the approaches are used (simultaneously) in practice.

Sensitivity

For simplicity, consider the case of overcurrent protection. The protective system must have ability to detect the smallest possible fault current. The smaller the fault it can detect, the more sensitive it is.

1.2 Power Quality Disturbances

Interest in Power Quality

Figure 1.2 gives the number of papers in the INSPEC database [3] that use the term power quality in the title, the abstract, or the list of keywords, the chart perfectly outlines an increasing academic interest in the concept of power quality, this can be due to the fact that modern equipment has become less tolerant of voltage quality disturbances, production processes have become less tolerant of incorrect operation of equipment, and consumers have become less tolerant of production stoppages.

The Institute of Electrical and Electronics Engineers (IEEE) dictionary states "Power quality is the concept of powering and grounding sensitive equipment in a matter that is suitable to the operation of that equipment." [4]

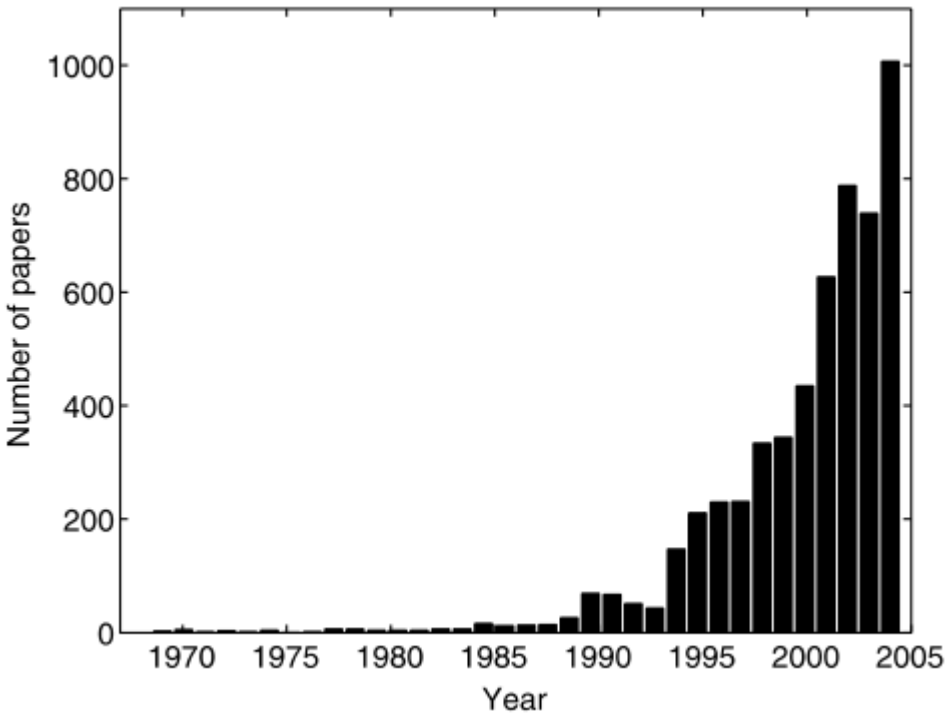


Figure 1. 2: The number of papers in the INSPEC database

The definition used in this thesis is the same as in [5]: Power quality is the combination of voltage quality and current quality. Voltage quality is concerned with deviations of the actual voltage from the ideal voltage. Current quality is the equivalent definition but for the current, the ideal voltage/current is a sinusoidal voltage waveform with constant amplitude and constant frequency. [3]

1.3 Types of disturbances

Any deviation of voltage or current from the ideal is a power quality disturbance; the quality of the voltage must fulfill requirements stipulated in national and international standards.

In these standards, some of the most encountered voltage disturbances are [6]:

Interruptions

An interruption as shown in figure 1.3 is defined as the complete loss of supply voltage or load current. Depending on its duration, an interruption is categorized as instantaneous, momentary, temporary, or sustained.

Figure 1. 3: : Interruption waveform

Voltage Sag

A voltage sag as shown in figure 1.4 is a reduction of AC voltage at a given frequency for the duration of 0.5 cycles to 1 minute's time. Common causes of sags include system faults, starting large loads and remote fault clearing performed by utility equipment.

Figure 1. 4: Voltage Sag

Voltage Swell

A voltage swell as shown in figure 1.5 is the reverse form of a sag, having an increase in AC voltage for a short duration. For swells, high-impedance neutral connections, sudden load reductions, and a single-phase fault on a three-phase system are common sources. The result can be data errors, flickering of lights, degradation of electrical contacts, semiconductor damage in electronics, and insulation degradation

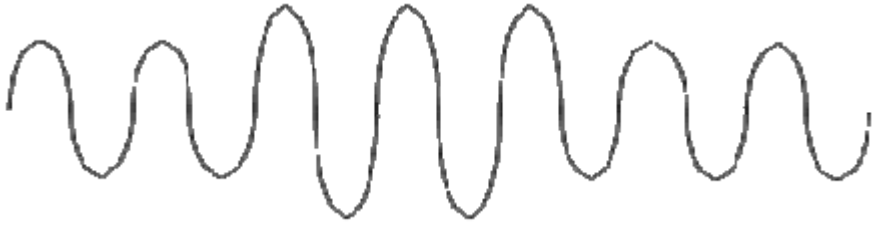


Figure 1. 5: Voltage swell

Frequency Variations

Frequency variation as shown in figure 1.6 is extremely rare in stable utility power systems, especially systems interconnected via a power grid and it is a momentary deviation in the signal's frequency from the ideal one.

Figure 1. 6: Frequency Variations

Harmonics

Harmonic distortion as shown in figure 1.7 is the corruption of the fundamental sine wave at frequencies that are multiples of the fundamental, the most common ones are third, fifth and seventh degree harmonics.

Figure 1. 7: Harmonics

Noise

Noise as shown in figure 1.8 is unwanted voltage or current superimposed on the power system voltage or current waveform. Power electronic devices, control circuits, arc welders, switching power supplies and radio transmitters, can generate noise.

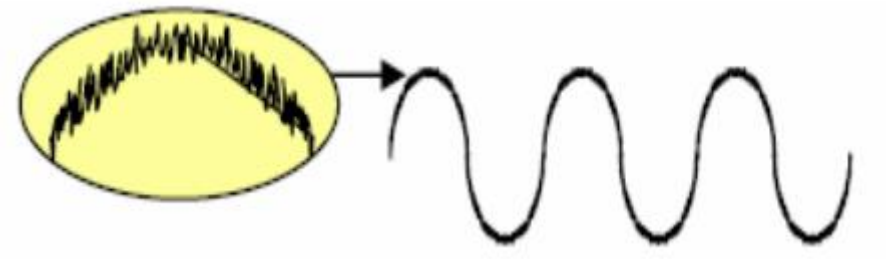


Figure 1. 8: Noise

DC offset

Direct current (dc) can be induced into an AC distribution system, often due to failure of rectifiers within the many ac to dc conversion technologies that have become prominent in modern equipment. A dc offset is shown in figure 1.9.

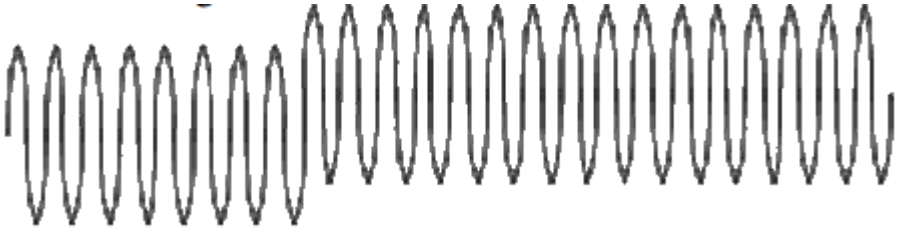


Figure 1. 9: DC Offset

1.4 Relay Testing

Relays are frequently found device in high voltage or medium voltage power systems. Their main duty is to isolate a faulty section within few cycles but by ensuring minimum interruption to healthy sections. Therefore, an ideal relay is a unit, which would act by minimizing damage to faulty sections without interfering with the healthy ones.

With usage relays get deteriorated. Therefore, it is the interest of both the end-user as well the manufacturer to check its behavior regularly.

1.4.1 Types of Tests

Acceptance Testing

This is a bench test performed by either the manufacturer or end-user to check the acceptability of the unit for sale or purchase.

Commissioning

A field-test to determine the relay functions accurately in the environment in which it is installed, this starts at the point of procurement. The specs will be matched with the submitted drawings from the suppliers. Finally, after installing it checks

- Accuracy of assembling the components in relay
- Ratings.
- Calibration.
- Conformity with entire system.

Periodic Maintenance Testing

After a relay is commissioned, it is important to carry out regular maintenance tests. Some of the advantages of such testing can be stated as, it will pin point a defective relay before it fails to act during a fault, relay coordination, its adaptability to latest power system as many loads might have gotten added over the years after the relay was installed.

Troubleshooting

This kind of test comes into effect after a power system disturbance had occurred and relay acted in an unanticipated way.

1.4.2 Methods of Testing

The method used by a tester will depend mainly on the used equipment. The methods, which are frequently used, are:

Steady State

Usually steady state testing is for checking the relay pick up. Injected current, voltage or frequency is held at predetermined value for duration longer than the planned time for relay. Then varied gradually at a rate much smaller than resolution of relay, either manually turning a knob or by an automated system. The figure 1.10 indicates how relay picks when the current is raised and then fluctuated around pick up. This test is mostly found at the point of commissioning. Due to lack of relation to actual power system faults, this test is used less frequently.

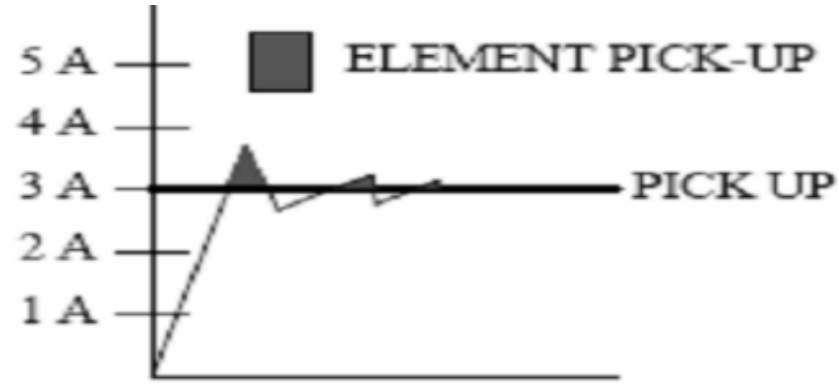


Figure 1. 10: Steady state pick up test

Dynamic state

Dynamic-state test is defined as simultaneously applying fundamental frequency components of voltage & current, which represents power system states of pre-fault, fault and post fault. Time for relay operation is measured and used at commissioning and troubleshooting.

Transient Test

By definition transient testing is, simultaneously applying fundamental and non-fundamental frequency components of voltage & current that represent power system conditions obtained from digital fault recorders (DFR), electromagnetic transient programs (EMTP) or a simulation to a relay. Both Dynamic state and Transient test can be stated as far better than steady state test. [7]

1.4.3 Testing Principles

There are two main principles as primary injection and secondary injection.

• Primary injection- High current is injected to primary side of the CT. Tests carried out Cover CT, conductors, relay and sometimes circuit breaker as well. The relay unit has to be isolated from the power system. Usually this principle is used at commissioning and if the secondary of the CTs not accessible.

• Secondary injection- Relay is disconnected from the CT and the stepped down current is directly injected to relay. Therefore, no need for the primary side of the CT to be disconnected from the rest of the system.

1.5 Computer Aided Relay Testing

Testability

The testing of protection equipment schemes presents a number of problems, this is because the main function of protection equipment like protective relays is solely concerned with operation under system fault conditions, and cannot readily be tested under normal system operating conditions.

This situation is aggravated by the increasing complexity of protection schemes.

Since the principle function of the protection relay is to operate correctly under abnormal power conditions, it is essential that the performance be assessed under such conditions; a recreation of these conditions from simulating the most common disturbances to generating the fault signal and amplifying it to the standard amplitude is therefore needed; making relay testers indispensable devices for modern day power systems. [8]

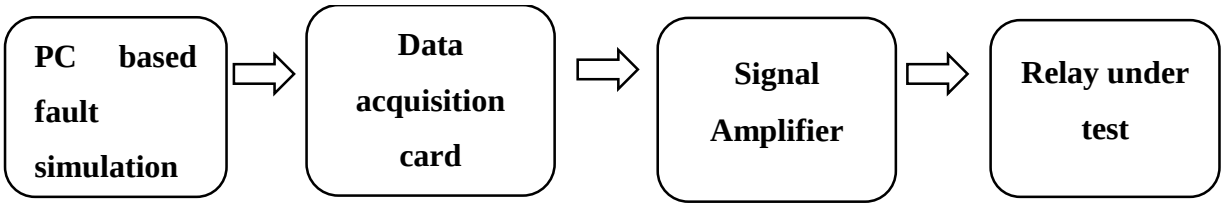


Figure 1. 11: General Block Diagram

Chapter II: PC Based Simulation

2.1 Introduction

Software application for simulating and generating typical power disturbances discussed in the previous chapter is presented in this chapter. Generation system is functionally based on the virtual instrumentation concept using LabVIEW and NI USB data acquisition card or FPGA card NI PCIe-7851 installed in standard PC environment, besides standard undisturbed voltage signal waveforms, different categories of the PQ disturbances characteristic can be simulated: voltage swells, sags, interruptions, high-order voltage harmonics, noise and DC offset. Each of the simulated PQ disturbances can be predefined and easily changed according to user requirements, using a simple user interface in the front panel. Data acquisition card NI-7851 provides real-time generation of the disturbances using analog output channels.

2.2 Description of the implementation

Proposed system consists of two parts. First part performs the basic PQ disturbances simulation done in LabVIEW environment and the latter is concerned with generating said signals using the NI -PCIe-7851.

2.2.1 Software

Although the project takes advantage of NI PCIe-7851 board, which is compatible with LabVIEW's FPGA module, In the interest of making the simulation compatible with both Data Acquisition devices provided by National Instruments, two VIs that perform the same function but operate on different platforms were created, (basic USB DAQ working in standard LabVIEW and FPGA Boards working in LabVIEW FPGA module) the focus of this thesis will be on the FPGA module code but a quick illustration of the real time module code will be given.

2.2.1.1 Standard Module

The LabVIEW project consists of two windows working side by side, The Block Diagram and the Front Panel, the block diagram window has the main graphical source code that controls the program, the block diagram contains functions and structures from built-in LabVIEW VI libraries.

The proposed VI relies on LabVIEW's "*Simulate Signal*" block controlled using a number of variables specified by the user, conditional loops and signal-merging nodes working side by side to generate the desired output, the block diagram for simulating PQ disturbances in the standard module is presented in figure 2.1.

The developed VI gives possibilities for variations and adjustments of the basic disturbance parameters. These adjustments are provided using a number of control buttons and knobs implemented in the front panel, which is the user interface of the VI.

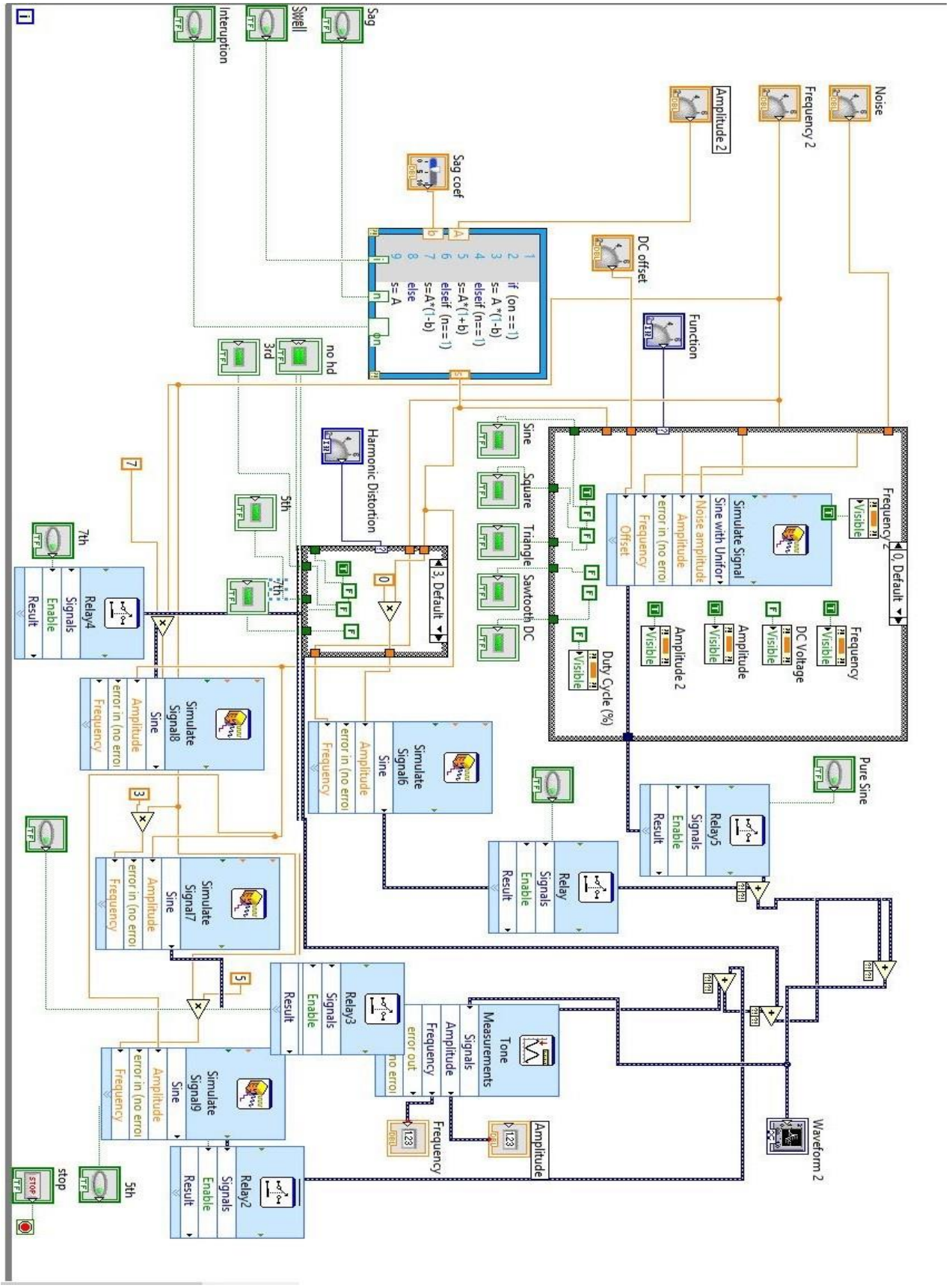


Figure 2. 13:PQ Simulation Block Diagram

The front panel is built with controls and indicators, which are the interactive input and output terminals of the VI, Controls simulate input devices and supply data to the block diagram. Indicators simulate instrument output devices and display data; the front panel for the standard module power disturbance simulator is presented in figure 2.2.

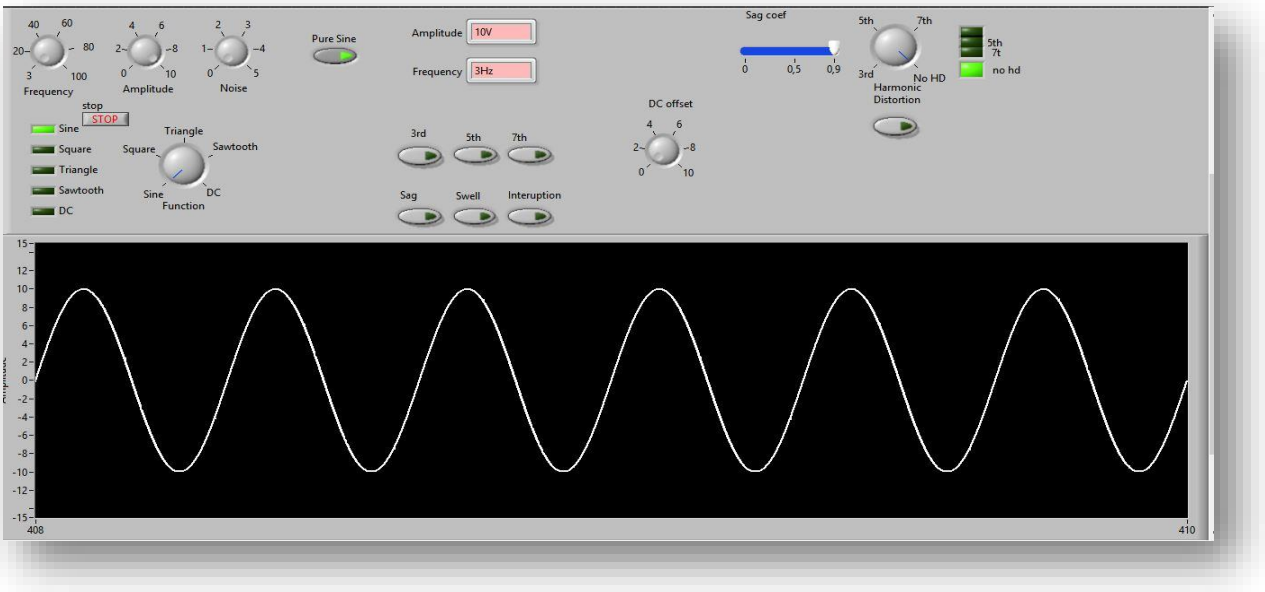


Figure 2.2: VI Front Panel

The front panel contains control buttons for regulation of the signal's frequency and amplitude, push buttons to trigger sag, swell, interruption faults and harmonics of a chosen degree, the front panel allows the user to easily control the Sag and Swell coefficient, add DC offset and noise.

The illustrated front panel also performs graphical presentation of the voltage waveforms. Figure 2.3 shows some simulated waveforms done using the proposed VI. These signals can be generated using any NI USB Data acquisition card that supports continuous generation.

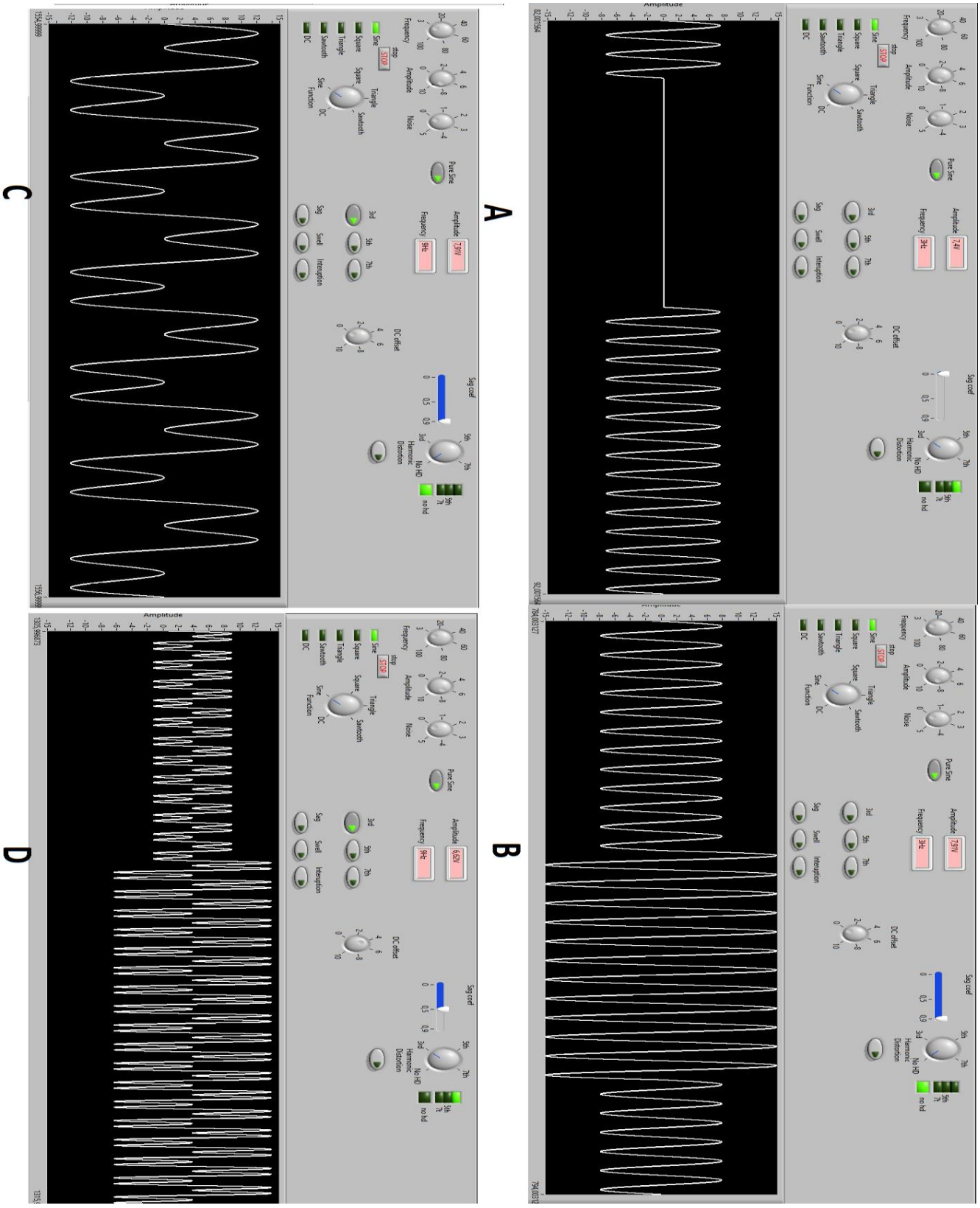


Figure 2. 3: Some simulation waveforms, (A)Signal interruption, (B) Signal Swell, (C) Sine wave with 3rd harmonic, (D) Sag with harmonics

2.2.1.2 FPGA Module

The NI LabVIEW FPGA Module allows the user to graphically implement digital circuits within an FPGA chip using LabVIEW to create VIs and functions that control the I/O, timing, and logic of the device, PCIe-7851 in our case, to generate the desired output [9].

Interactive Front Panel Communication can be used to communicate directly with the FPGA using an FPGA VI, but the communication is limited in the number of functions and operations that can be performed and lacks real times updating, so we use a separate HOST VI running simultaneously that references the FPGA VI, to interact with it in real time and provide the user with more control over the inputs of the FPGA, Host Vis are used to send information between the host computer and the FPGA target for the following reasons:

- Doing more data processing than you can fit on the FPGA.
- Performing operations not available on the FPGA target.
- Controlling the timing and sequencing of data transfer.

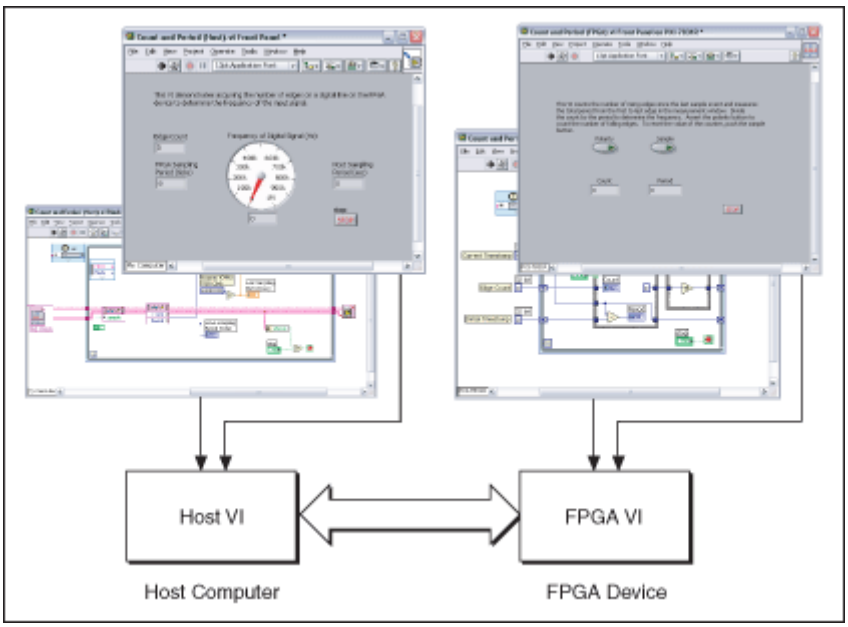


Figure 2. 4: Using a Host VI to Communicate with the FPGA Target

Host VI

The Host VI takes advantage of a limited number of LabVIEW's inbuilt functions and relies on the FPGA interface functions like *Open FPGA VI Reference, Close FPGA VI Reference* to establish a connection between the FPGA VI and the Host VI and close it when needed, *Read/Write Control* to read a value from or write a value to a control or indicator in the FPGA VI., Figure 2.5 and Figure 2.6 show the Front Panel and the Block Diagram Host VI for power disturbance generation.

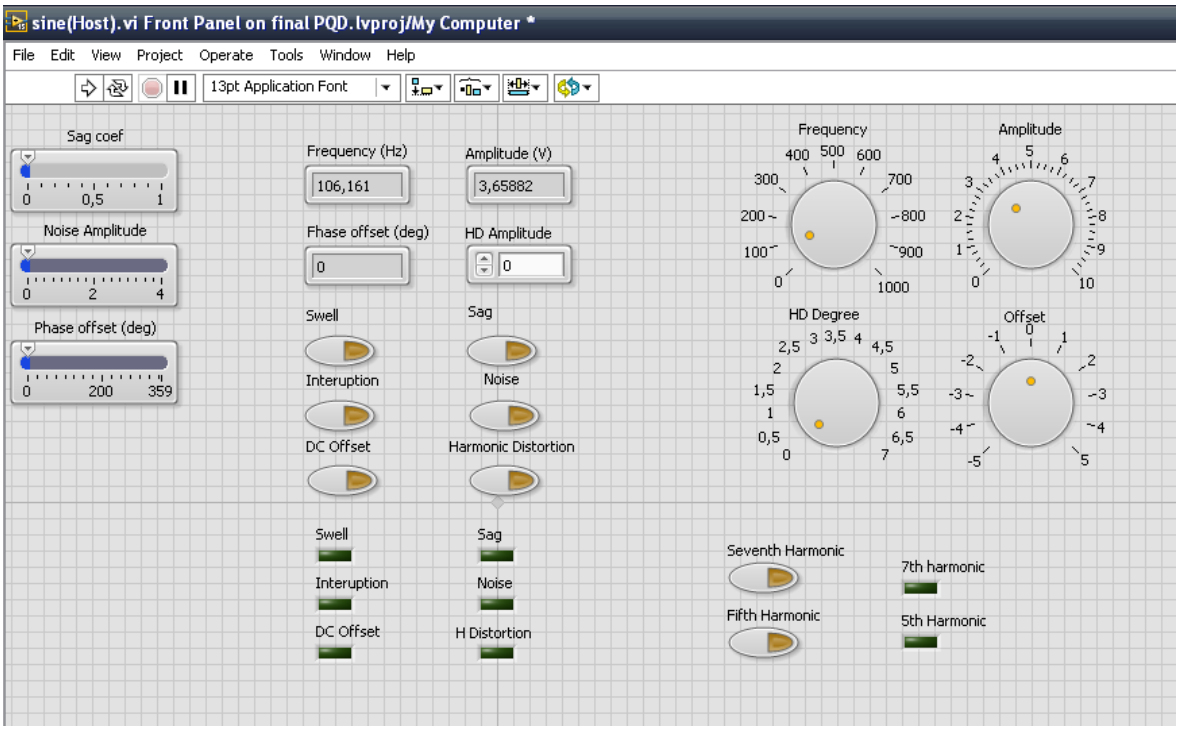


Figure 2. 5: Host VI Front Panel

The proposed Host VI allows the user to input the parameters for the desired signal and then converts these values to an appropriate binary representation before writing them to the FPGA VI.

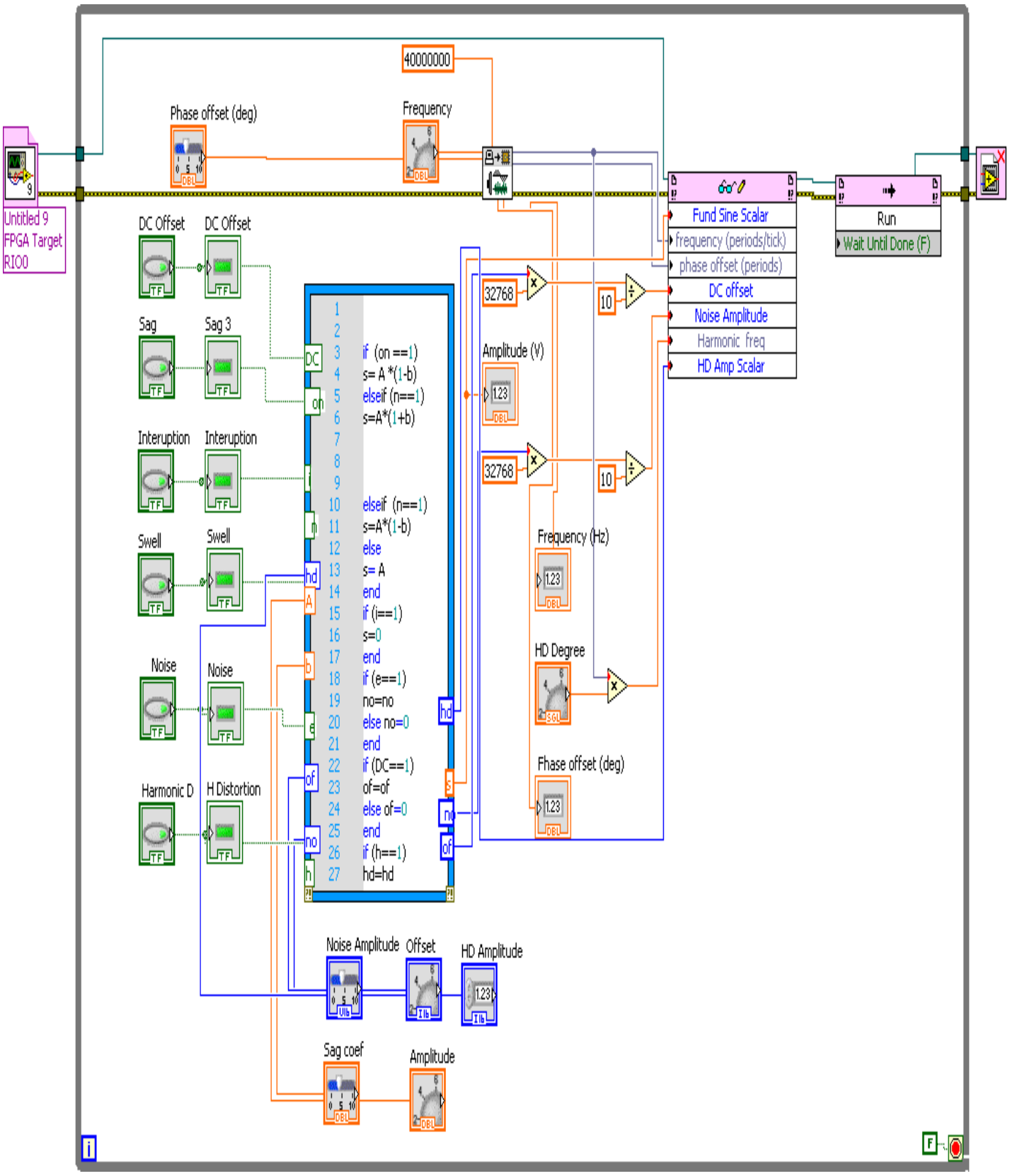


Figure 2. 6: Host VI Block Diagram

FPGA VI

The FPGA VI reads and updates values from the Host VI in real time, and employs them into its graphical code, which is pre-compiled and sent to the board, Figure 2.7 shows the Host VI for our Power Disturbance generator, which outputs signals in analog outputs 0 and 1.

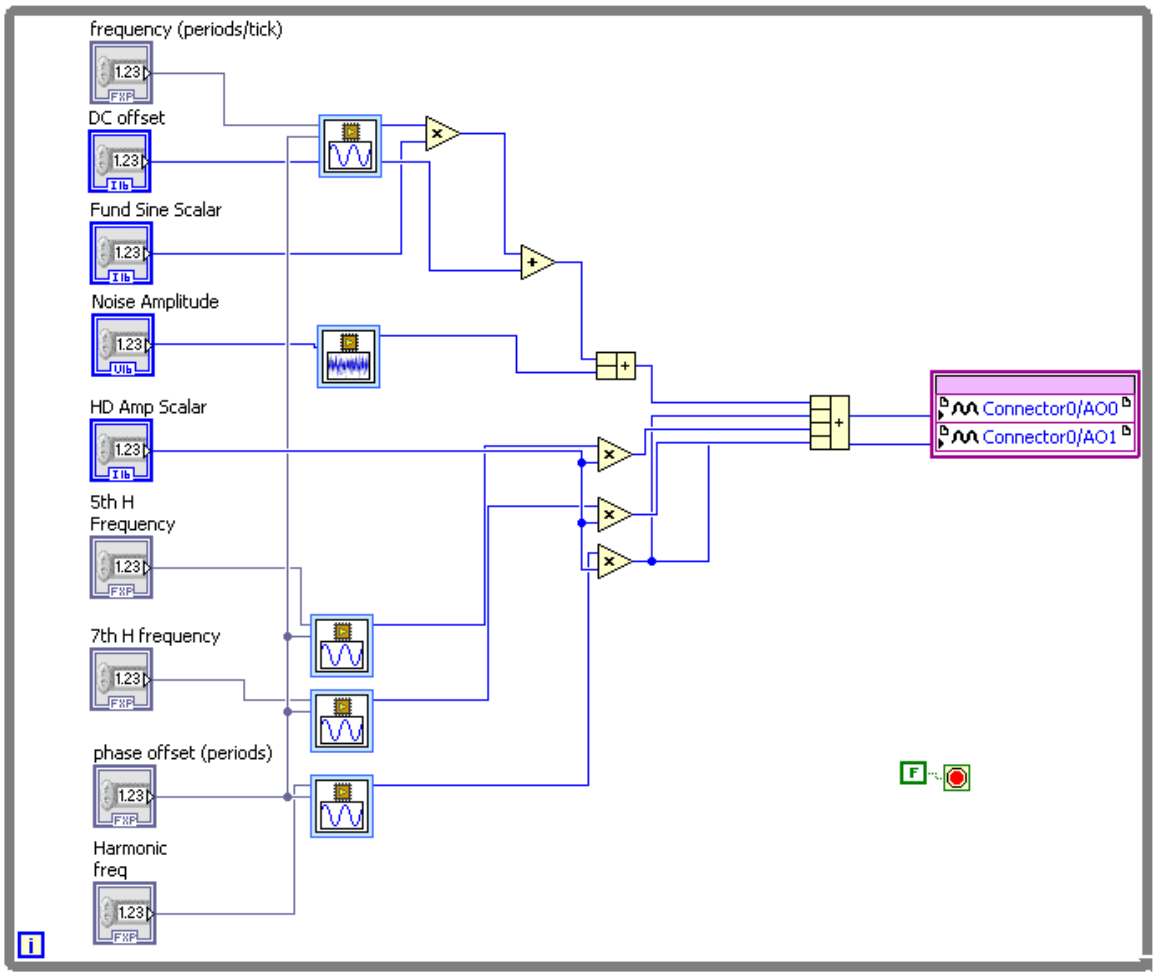


Figure 2. 7: FPGA VI Block Diagram

The FPGA VI receives different signal parameters from the HOST VI in real time and generates the desired signals accordingly.

2.2.2 Hardware

NI PCIE 7851

Generation of the PQ disturbance signal waveforms, previously defined, and simulated is based on 8-channel data acquisition PCI express card NI -7851 (figure 2.8), developed with 16-bit resolution and maximum amplitude output voltages of *20Vp-p*. This acquisition card designed with possibility for digital to analog data conversion, from manufacturer National Instruments Corporation, for this specific application purpose uses eight analog output channels, which provide waveforms generation, based on the previously determined values of the samples per period, memorized into acquisition card data buffer. [10]

Figure 2. 8: NI PCIe 7851

The FPGA I/O Node is used to write an analog output, the FPGA I/O Node writes the binary representation of the voltage to the digital-to-analog converter (DAC), which sets the analog output voltage. Voltage information can be generated from two sources—the host VI or the FPGA VI. Typically, the host VI converts the voltage to an appropriate binary representation before writing the value to the FPGA VI. If the FPGA VI determines the voltage, typically the FPGA VI performs the calculations using the appropriate binary representations. In both cases, the DAC produces a voltage that corresponds to the binary representation. [11]

The card's different specification are listed in table 2.1

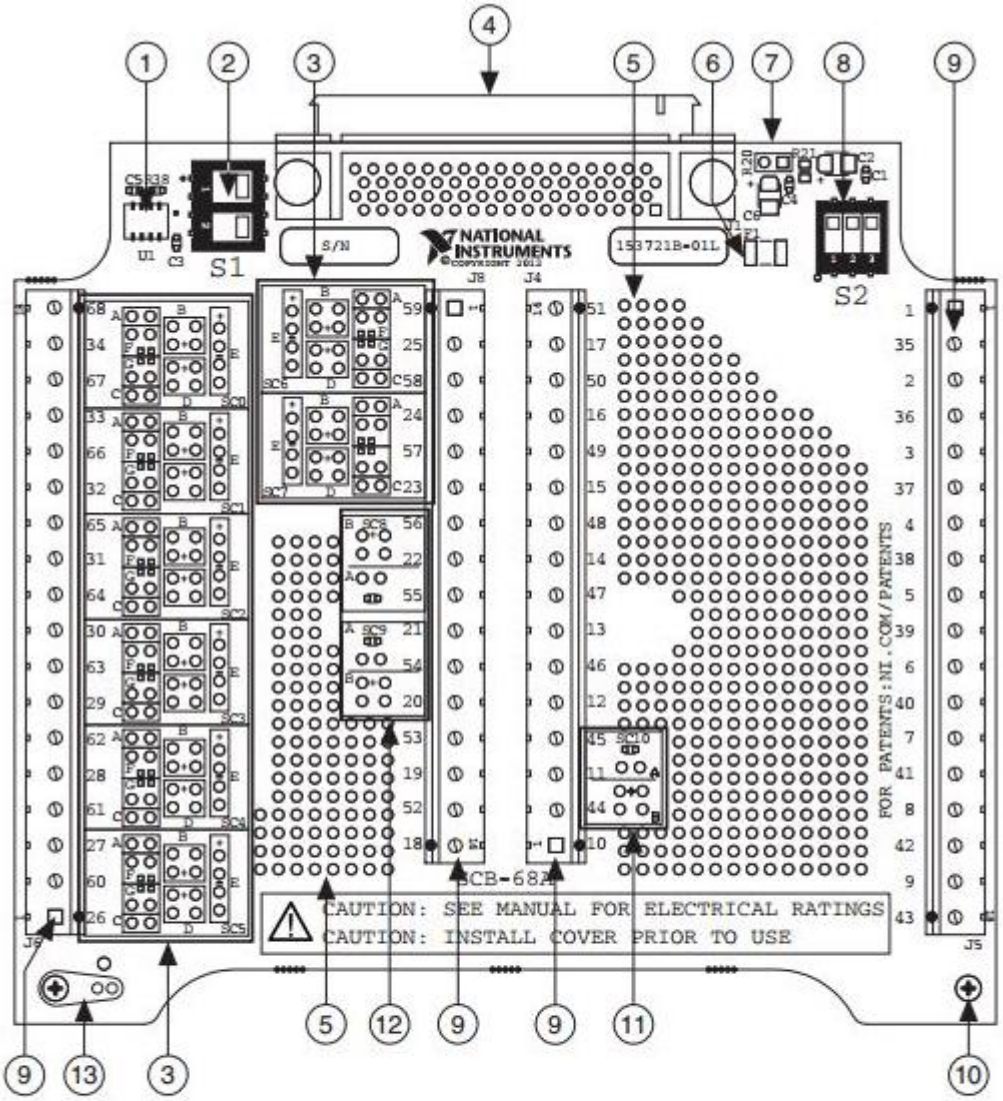
Output Type	Single ended, voltage output
Number of channels	8
Resolution	16 bits
Update time	1.0µs
Maximum update rate	1MS/s
Type of DAC	Enhanced R-2R
Nominal Range (V)	$20V_{p-p}$
Offset	2366µV
Absolute Accuracy at Full Scare	5.88±mV

Table 2. 1: NI PCIe 7851 specifications

SCB 68A

The SCB-68A, shown in Figures 2.9 and 2.10, is a shielded I/O Analog and Digital connector block with 68 screw terminals for easy signal connection to National Instruments FPGA DAQ device.

Figure 2. 9: SCB 68A Connecter



1	Temperature Sensor	8	Switches S2.1, S2.2, and S2.3
2	Switches S1.1 and S1.2	9	Screw Terminals
3	Analog Input Pads	10	Printed Circuit Board Mount Screw
4	68-Pin I/O Connector	11	PFI 0 Pads
5	Breadboard Area	12	Analog Output Pads
6	1 A Self-Resetting Fuse	13	Printed Circuit Board Mount Screw and Chassis Ground Lug
7	+5 V Power Pads, R20 and R21		

Figure 2. 10: SCB-68A Printed Circuit Board Diagram

2.3 Results

Simulation of all the power disturbances discussed in chapter I was successful, the simulation was done using the LabVIEW FPGA Module and PCIe-7851 setup as seen in figure 2.11.

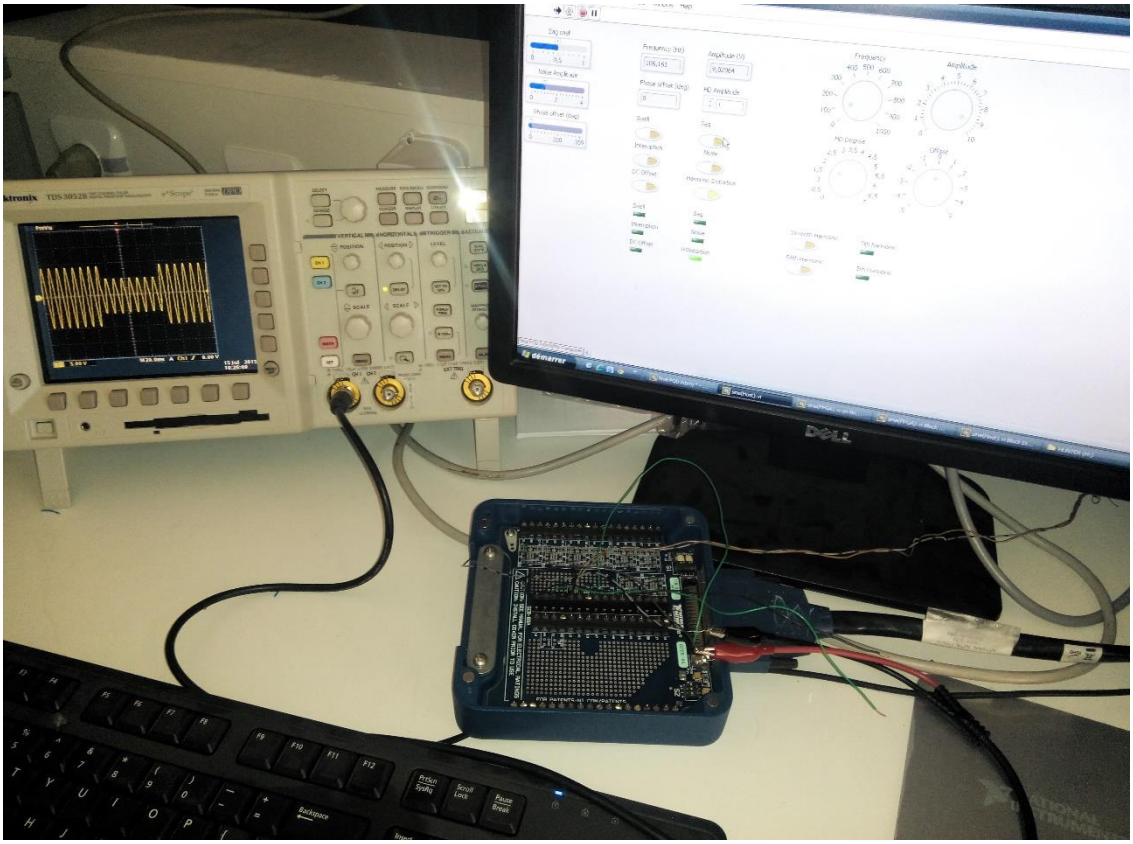
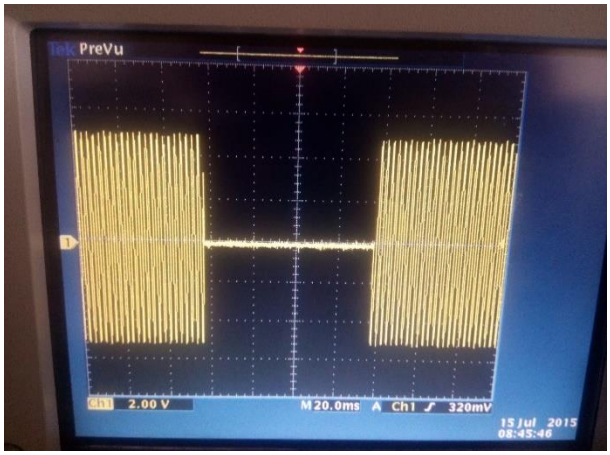


Figure 2. 11 Fault simulation setup

The setup allows for the generation of multiple separate fault signals simultaneously

Some of the generated signals are seen in Figure 2.12, the figure shows a voltage sag, swell, interruption, 3rd, 5th and 7th harmonic injections, DC offset and noise signals were simulated as well.



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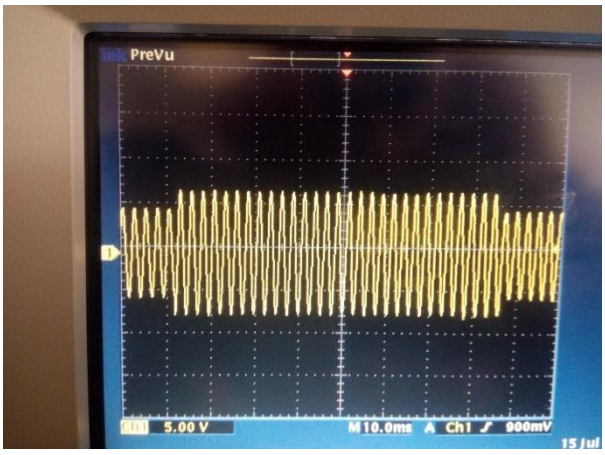

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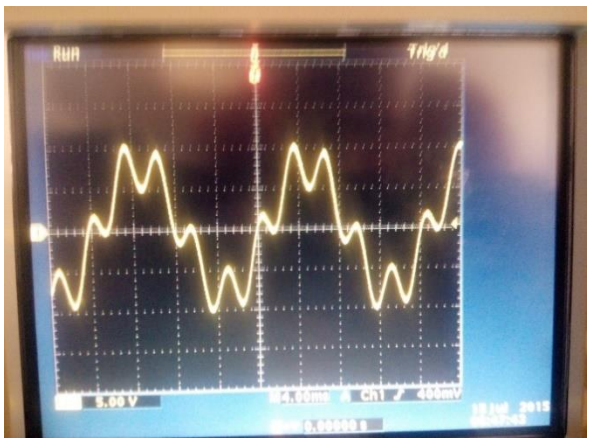

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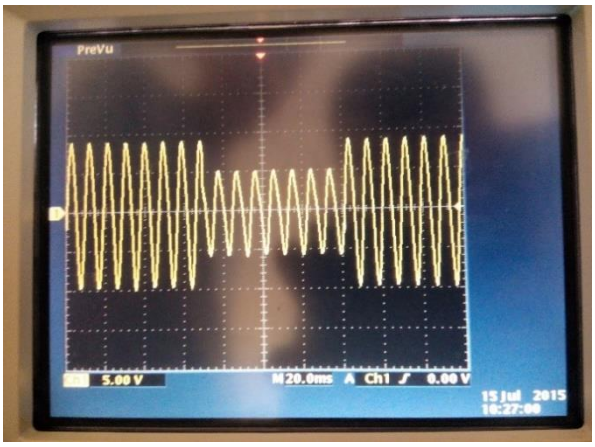

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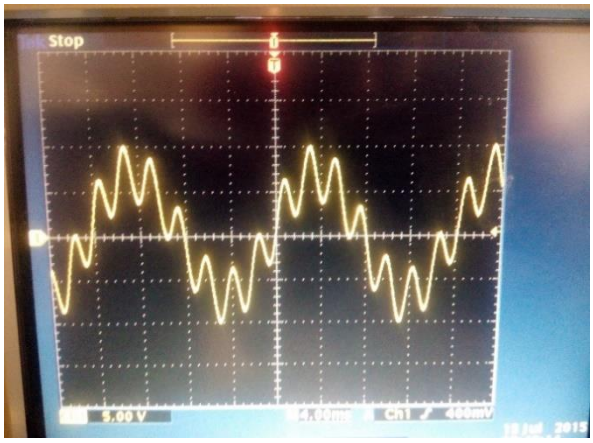

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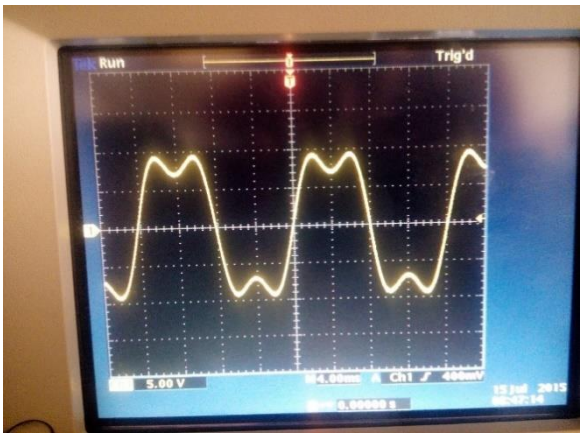

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Figure 2. 12: Generated Fault signals : a) Interruption , b) Swell, c) 5th degree Harmonic, d) Sag, e) 7th degree Harmonic, f) 3rd degree Harmonic

Chapter III: Class D amplifier Design

3.1 Introduction

In today's industries, power amplifiers are used in many devices for a wide variety of applications. In general, an amplifier takes a low power input and regenerates the signal at several watts higher. Ideally, the input will be reproduced without any changes with an efficiency of 100% but that cannot be achieved in practice. Various types of power amplifiers exist and they are classified by their efficiency and topology. [12]

This chapter presents the design and implementation of a Class-D amplifier for a single phase voltage source, the design is comprised of three major stages working simultaneously to generate the amplified signal, sinusoidal pulse width modulation (SPWM) generation, H-Bridge and lastly the Low Pass Filter, This type of amplifier has demonstrated to have a very good performance yielding power efficiencies up to 90%, THD under 0.01%, whereas class AB amplifiers can only achieve 78.5%.

3.2 State of the art

The history of the Class-D amplifier goes back, as is so often the case with technology**,** the principle is generally regarded as having surfaced in the 1950s, but the combination of high switching frequencies and valve output transformers probably did not appear enticing. The first public appearance of Class-D in the UK was the Sinclair X10, which claimed an output of 10W this was followed by the X20, alleging a more ambitious 20W. The biggest problem of the technology at that time was that bipolar transistors of suitable power-handling capacities were too slow for the switching frequencies required; this caused serious losses that undermined the whole point of Class-D amplifier, and produced unappealingly high levels of distortion. It was not until power FETs, with their very fast switching times, appeared that Class-D began to become a practical proposition. [13]

3.3 Class-D amplifier design

Class-D amplifiers consist mainly of three stages: the input switching or modulation stage, the power amplification stage, and the output filter stage.

Figure 3. 1: Block Diagram of a Class D Amplifier

3.3.1 Sinusoidal Pulse Width Modulation SPWM

For Class-D amplifiers to operate in switching mode, pulse-width modulation (PWM) can be used. This technique takes an input signal and converts it into a high frequency switching Waveform. To achieve this, the signal is compared to a high frequency triangular waveform using a comparator as shown in Figure. 3.2.

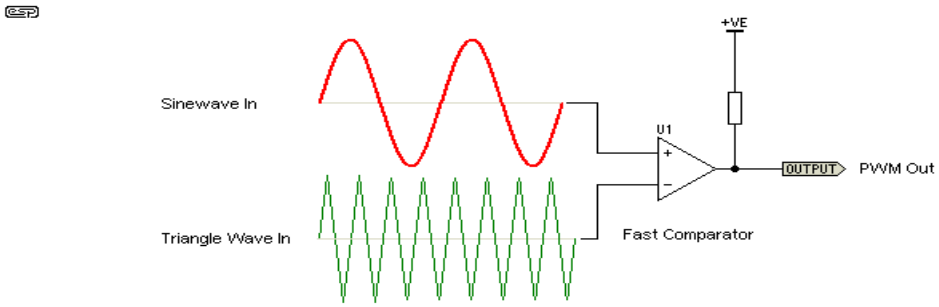

Figure 3. 2: Comparator to Create SPWM Waveform

When the voltage at the inverting input is bigger than the one at the non-inverting input, the output voltage is low. When the voltage at the inverting input is smaller than the one at the non-inverting input, the output voltage is high; the output SPWM is shown in Figure. 3.3

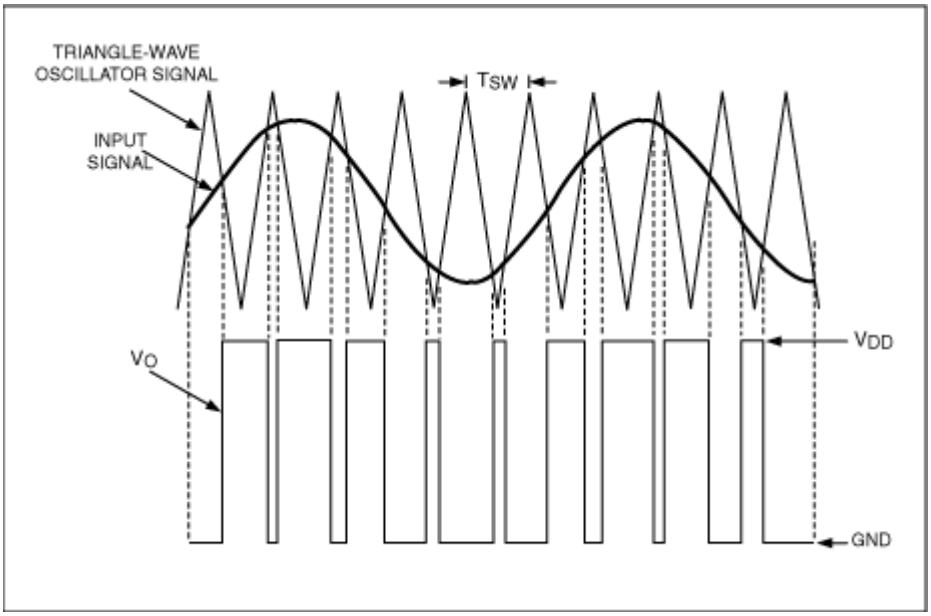

Figure 3. 3: Derivation of PWM From Input and Reference

When the modulating signal is a sinusoid of amplitude A_m, and the amplitude of the triangular carrier is A_c, the ratio m=Am/Ac is known as the modulation index. Controlling the modulation index therefore controls the amplitude of the output voltage of the amplifier. With a sufficiently high carrier frequency the high frequency components do not propagate significantly to the load due to the presence of the inductive elements. However, a higher carrier frequency results in a larger number of switchings per cycle and hence in an increased power loss. Typically, switching frequencies in the 2-15 kHz range are considered adequate for power systems applications, the design chosen uses a carrier signal with switching frequency of *5 KHz* and an amplitude of *10V* [14].

The output PWM signal will be fed to the H-Bridge for amplification stage but before doing so this signal need to be level shifted with zero volt reference; this is done by using an inverter by inverting this signal twice then feeding it to the first gate driver. The second gate driver input is fed with a PWM signal, which is inverted only once .

3.3.2 H-Bridge

Topologies

Half Bridge vs. Full Bridge

Many Class D amplifiers are also implemented using a full-bridge output stage. A full bridge uses two half-bridge stages to drive the load differentially. This type of load connection is

often referred to as a bridge-tied load (BTL); the full-bridge configuration operates by alternating the conduction path through the load as seen in Figure 3.4. This allows bidirectional current to flow through the load without the need of a negative supply or a DC-blocking capacitor.

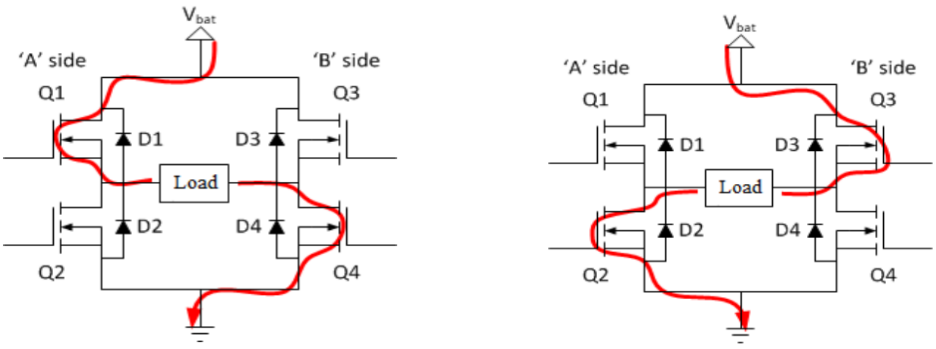

Figure 3. 4: Negative and Positive Voltage states

A full-bridge Class D amplifier shares the same advantages of a Class AB BTL amplifier, but adds high power efficiency. The first advantage of BTL amplifiers is that they do not require DC-blocking capacitors on the outputs when operating from a single supply. The same is not true for a half-bridge amplifier as its output swings between V_{DD} and ground and idles at 50% duty cycle. This means that its output has a DC offset equal to $V_{DD}/2$. With a full-bridge amplifier, this offset appears on each side of the load, which means that zero DC current flows at the output. The second advantage they share is that they can achieve twice the output signal swing when compared to a half-bridge amplifier with the same supply voltage because the load is driven differentially as seen in figure 3.5.

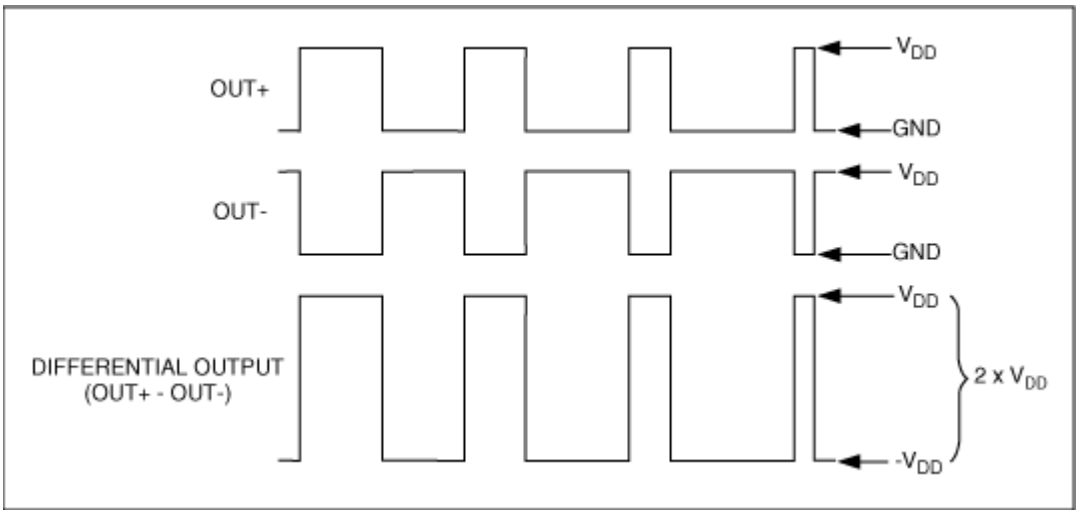

Figure 3. 5: Full-bridge Class D output waveforms complement each other, thus creating a differential PWM signal

MOSFETs

In class D amplifiers, the output of the comparator is connected to the power amplification stage. Metal-oxide-silicon field effect transistors (MOSFETs) are used at this stage instead of bipolar junction transistors (BJTs) because MOSFETs have a faster response time, ideal for high frequency operation. Class-D amplifiers require two or four MOSFETs depending on the topology used. Every two MOSFETs are either fully turned on or turned off for a very short period. When a MOSFET is fully turned on, the voltage drop across the transistor is small. When a MOSFET is turned off, the current across it is zero. The rapid switching of MOSFETs between these two stages makes it very efficient. Less power is dissipated as heat, thus a Class-D amplifier does not require a heat sink.

Gate Driver

In an H-Bridge MOSFETs Q1 and Q2, Q3 and Q4 must never be turned on at the same time, if this happens the power supply is short circuited, at minimum this will result in wasted power, but in some cases it will results in the destruction of the output stage causing damage to the circuit, this condition is called a 'Shoot through', this problem can be negated by introducing a short period of time between the operation of the two switches called Dead Time as seen in figure 3.6 , one way to achieve this is through the use a Gate Driver.

In addition to introducing Dead Time, a Gate Driver is used to convert the low voltage, level from the modulator to the higher voltage required to turn on the MOSFETs.

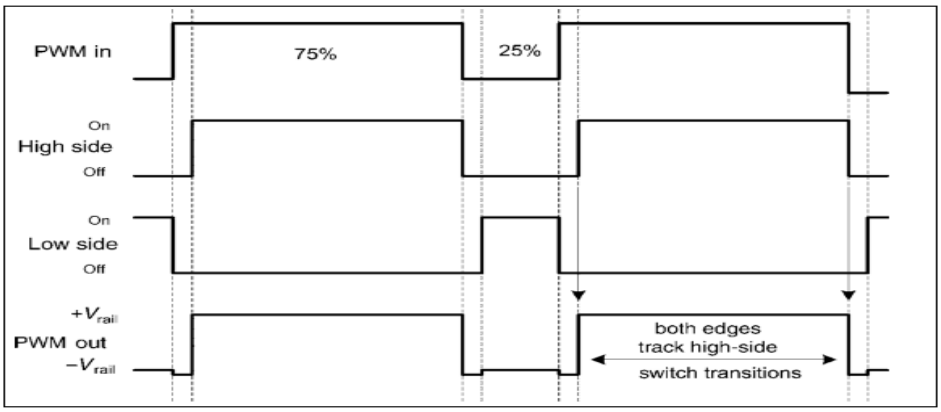

Figure 3. 6: High and Low PWM signals with dead time

3.3.3 Low Pass Filter

Class D amplifiers generally use a low-pass filter to attenuate the switching noise in the output waveform while passing the signal to the load; the heart of a Class-D amplifier filter is an L-C low-pass filter. The corner frequency of the filter is chosen so that the filter will have minimal effect on the desired output frequency range while attenuating the switching noise as much as possible. The LC filter's cutoff frequency (f_c), determined by equation (3.1), should be set above the input signal's bandwidth. Furthermore, since the filter is used to convert the PWM signal back to its original form, f_c has to be determined with respect to the switching frequency of the amplifier, which is equal to the frequency of the triangular wave (f_T). Therefore, f_c and f_T are related and both of these values will affect the amount of harmonics present at the output. [15]

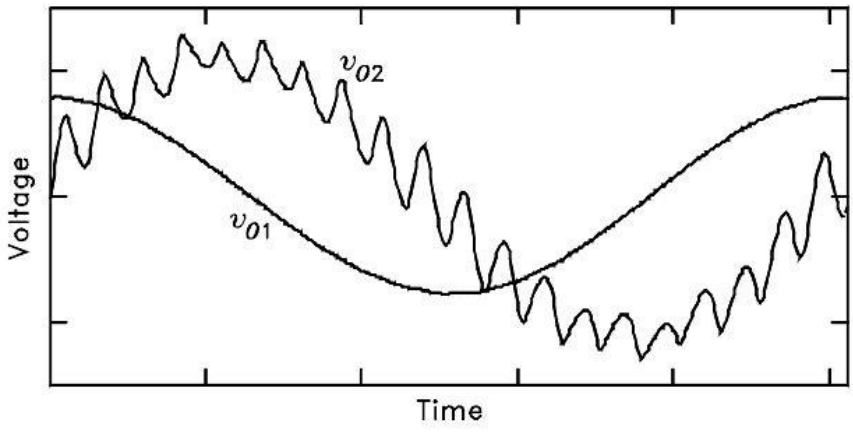

Figure 3. 7: Output voltage waveforms for two different LC filter cutoff frequencies

The optimum value for the filter inductor is

$$L = \frac{R_L}{2\pi fc} \qquad \text{R}_\text{L} \text{ is the load resistance} \qquad (3.\ 1)$$

Rather than calculating the inductor and capacitor values independently and then adjusting their values, it is better to calculate the inductor value, select the closest standard inductance value, and then calculate the required capacitance using the selected inductor.

$$C = \frac{1}{((2\pi fc)^2 \times L)} \qquad (3.\ 2)$$

Not only is it important to choose the correct L-C filter values, it is also important to choose the correct types of components for the class-D amplifier in order to avoid losses and minimize harmonic distortion.

Chapter IV: Results and Discussion

This chapter will focus on the implementation of the proposed design then discuss the obtained results.

4.1 Class-D Amplifier Implementation & Results

The design discussed in chapter III was successfully constructed, the circuit schematic and the final circuit implementation are seen in figures 4.1 and 4.2 ; this section will give a presentation of the components chosen for the implementation and display the results of every stage of the design up until the final output.

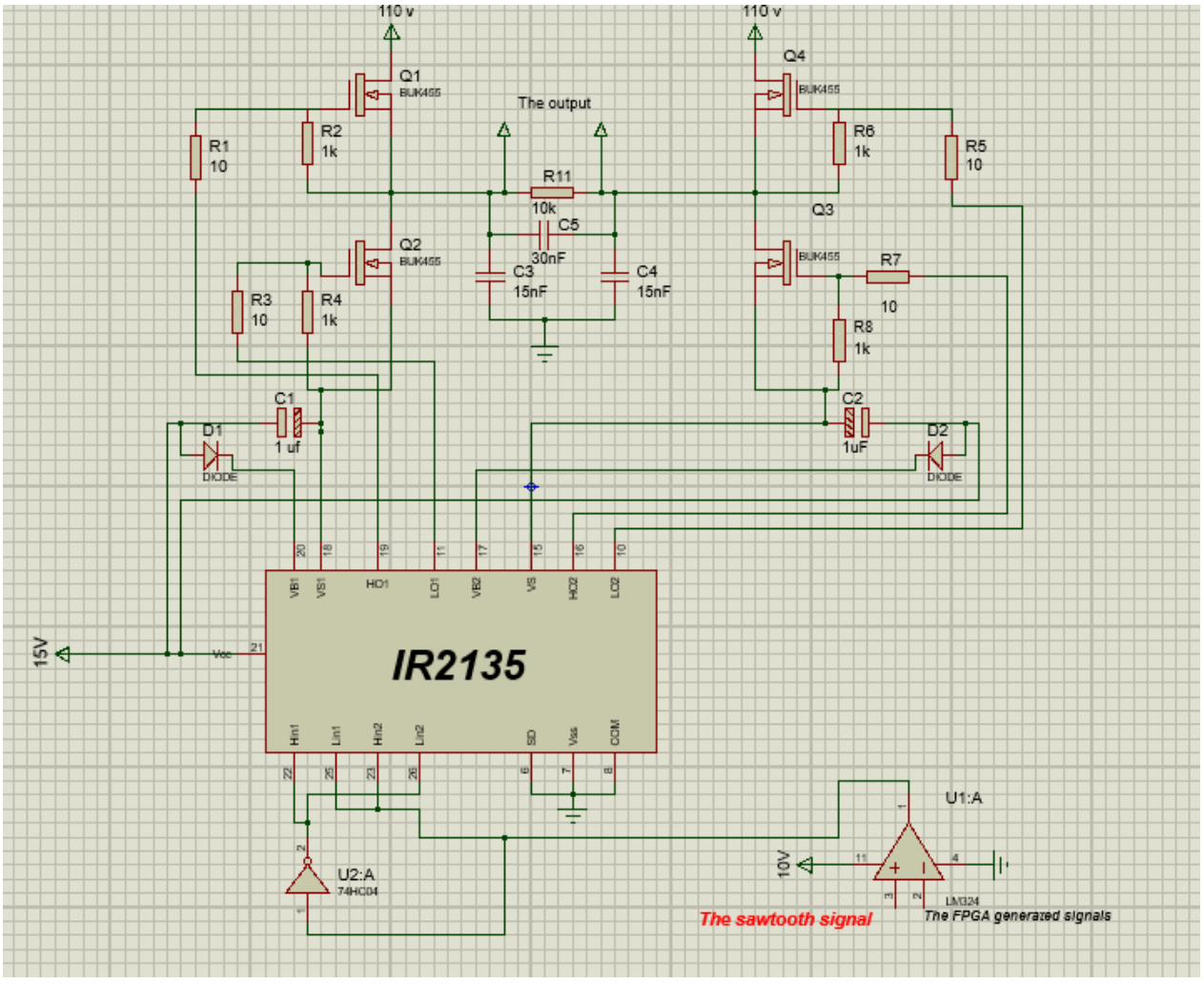

Figure 4. 1: Schematic Diagram for the final circuit

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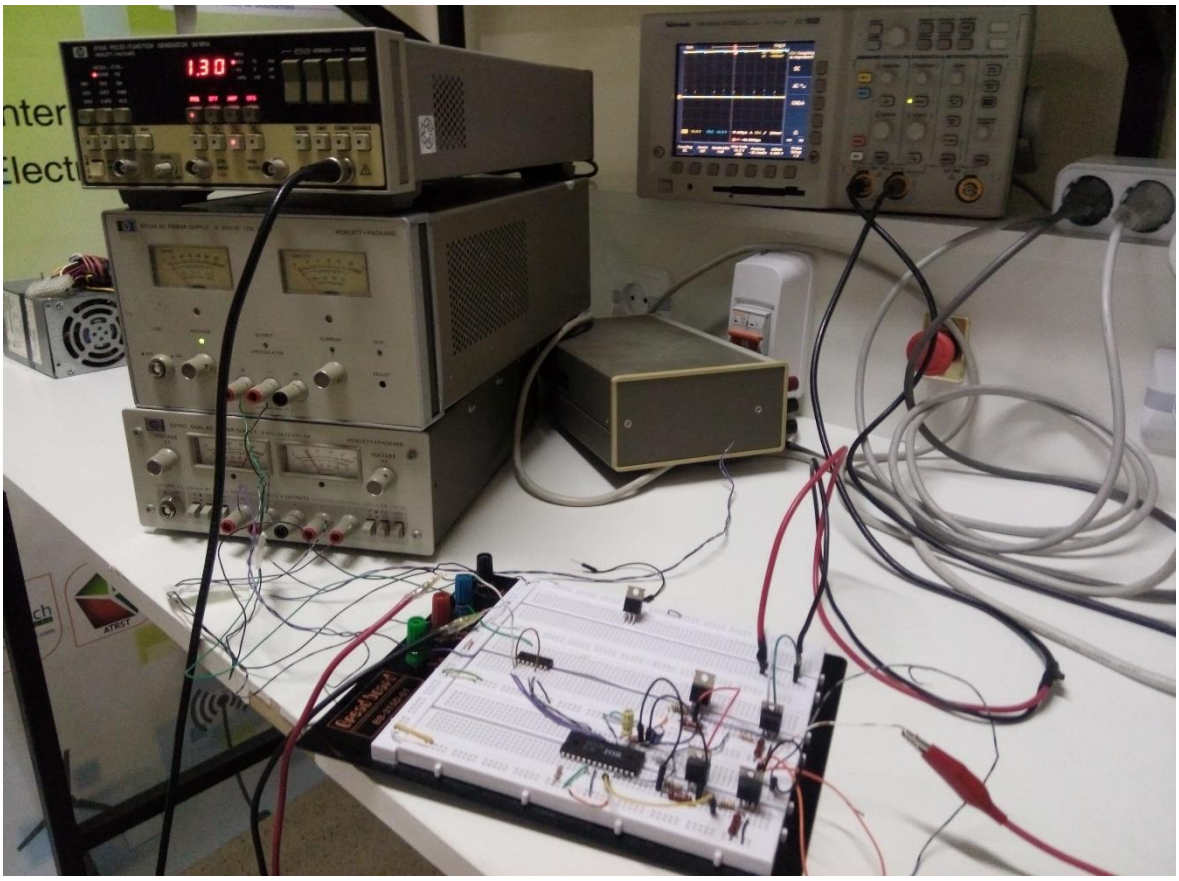

Figure 4. 2: Class D amplifier final experimental Setup

4.1.1 Modulation Stage

Comparator: For the comparator stage, the LM324 quad-operational amplifier has been chosen, the LM124-N series consists of four independent High-gain, internally frequency compensated operational amplifiers designed to operate from a single power supply over a wide range of voltages. [16]

Inverter: The 74HC04 has been used to invert the output signal of the comparator to provide the Gate Driver with two inverted signals.

The input and output of the Modulation Stage are illustrated in Figures 4.3 and 4.4

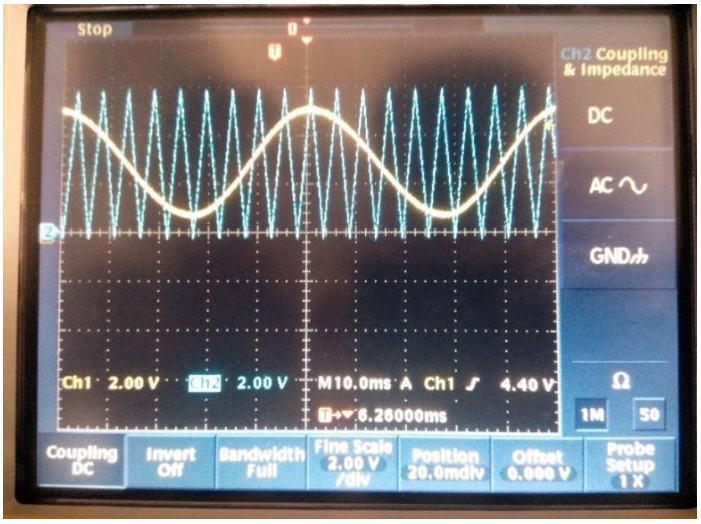

Figure 4. 3: The Input Signals of the comparator

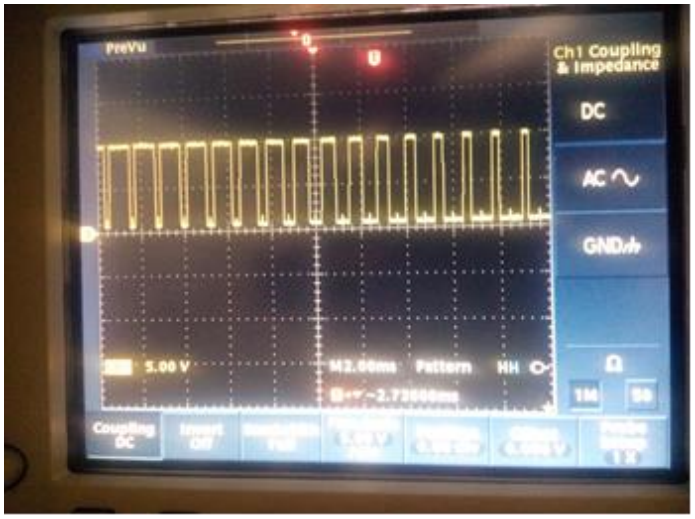

Figure 4. 4: The Output Signal of the comparator (SPWM)

4.1.2 Amplification Stage

Gate Driver

For driving the MOSFETs the IR2135 was used, The IR2135 is a high voltage, high-speed power MOSFET and IGBT driver with three independent high side and low side referenced output channels, the IR2135 has the advantage of allowing for the driving of a full bridge circuit without the need for two drivers, it also has a dead time of 250ns.

MOSFETs

For switching**,** the BUK555 MOSFET was used, the drain can withstand up to 100 volts, which is sufficient for our design, the output of the Half, and Full Bridge are seen in Figures 4.5 and 4.6.

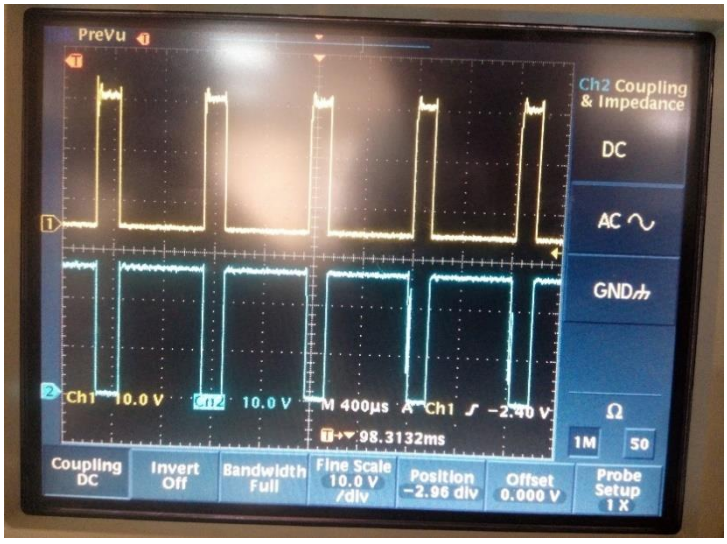

Figure 4. 5: The outputs of both the Half Bridges

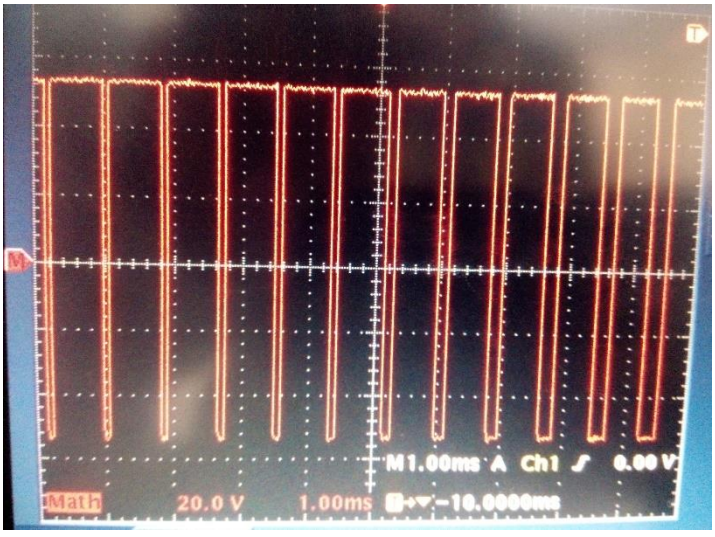

Figure 4. 6: The final output of the H Bridge, 110Vp-p

4.1.3 Filter

Equations (3.1) and (3.2) have been used to determine the suitable values of the LC filter parameters for a cut-off frequency of 500Hz. R_L is chosen to be 5KΩ for each half bridge amounting to 10KΩ for the full bridge, and the capacitor was chosen to be 15nF.
The output signals for the two half bridges and the full bridge are shown in Figures 4.7 and 4.8.

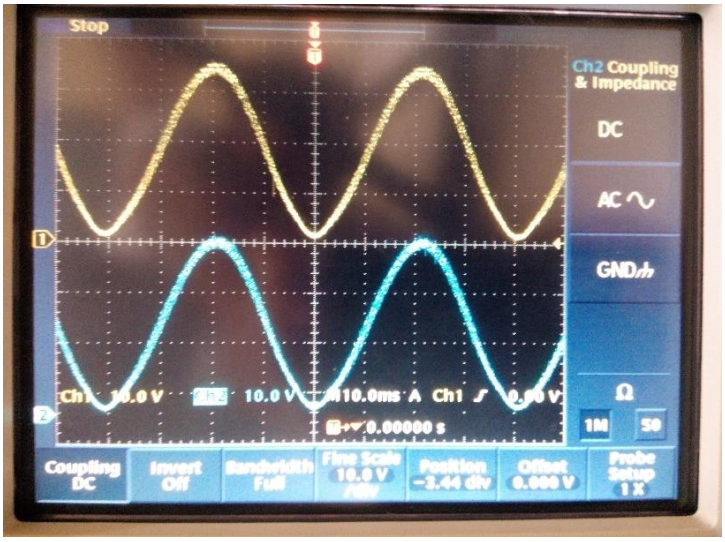

Figure 4. 7: The filtered signals of both the Half Bridges

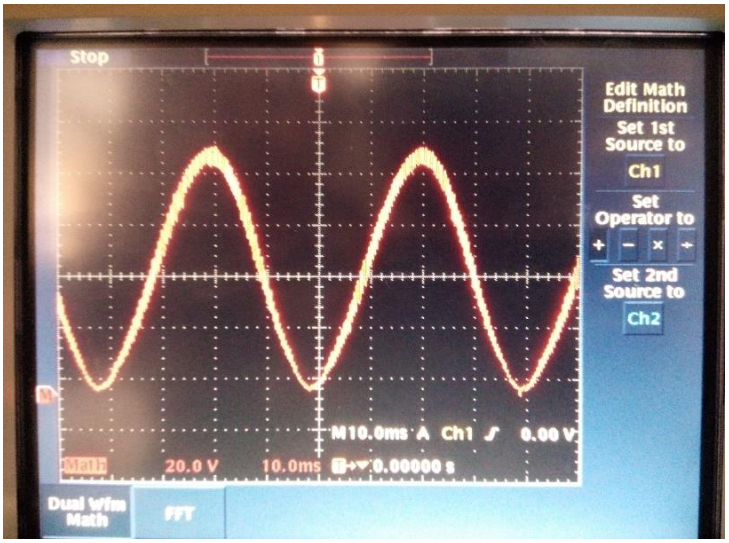

Figure 4. 8: The filtered signal of the Full Bridge

4.2 Discussion

The implementation of a Class-D amplifier was successful, the circuit was able to replicate the input signals with minimum distortion; the output signal can reach up to 110 V_{p-p} using a 10V,60 Hz sinewave input, the amplifier can function correctly within a high range of frequencies reaching the cutoff frequency of 500Hz which is enough to amplify signals up to the 7^{th} harmonic.

- The Class-D Amplifier was implemented and tested using only the function generator to generate the input sine wave, the input signal will be generated by an NI-FPGA card 7851. This is a very sophisticated card that was first setup and used by us; it proved very accurate and effective in generating all the disturbance signals, which were well explained in Chapter II. In the next section, the required signals will be generated using the NI-FPGA card toward the Class-D amplifier and the results will be seen in practice.

4.3 Fault generation using the amplifier and the FPGA card

The signals discussed in Chapter I and generated in Chapter II were fed into the input of the Class-D and successfully amplified, below are some of the amplified fault signals; the amplitude in the figures does not represent the full output range of the amplifier:

Figure 4. 9: Pure sine wave input and amplified output

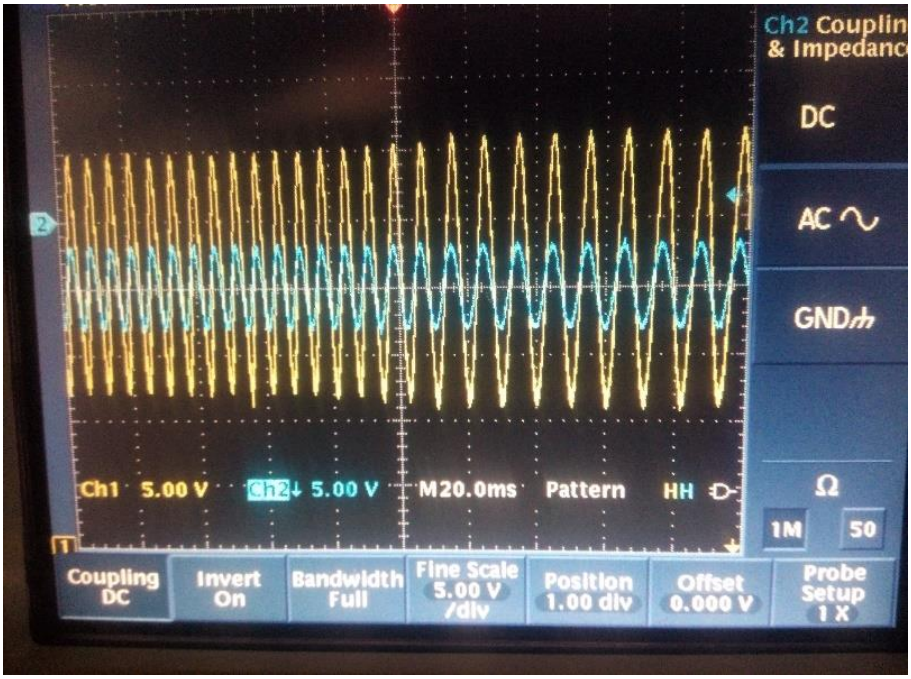

Figure 4. 10: Sine with frequency variation input and amplified output

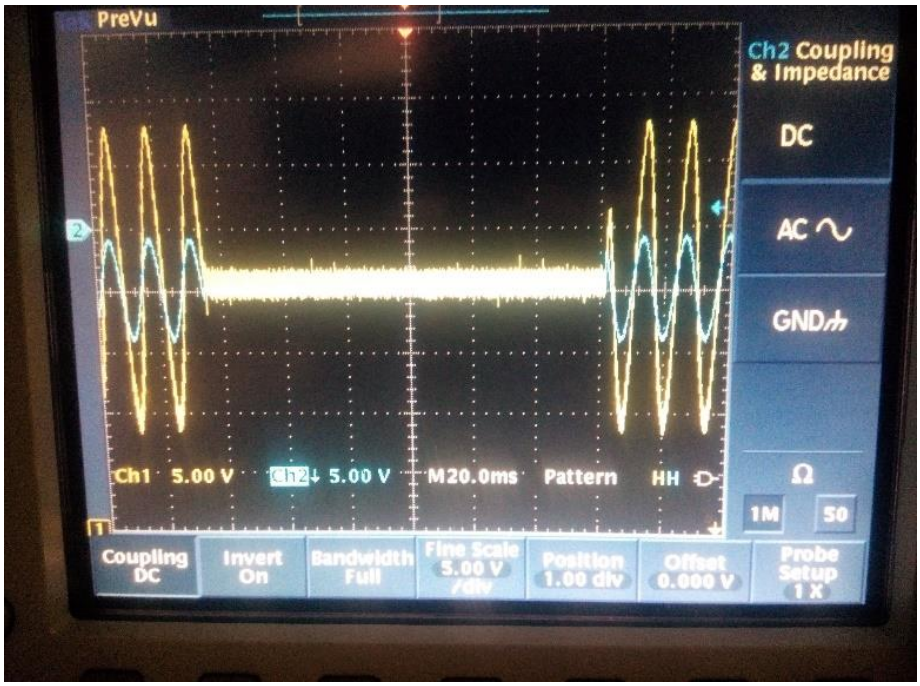

Figure 4. 11: Momentary interruption input and an amplified output.

Figure 4. 12: The amplified 7th degree Harmonic

Figure 4. 13: The amplified 3rd degree Harmonic

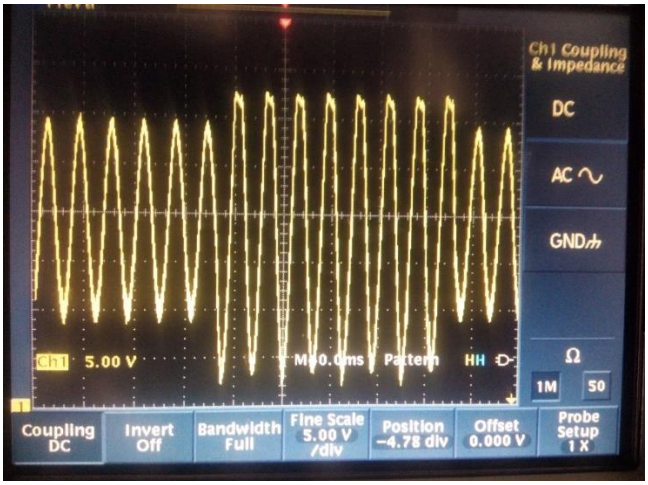

Figure 4. 14: The amplified swell signal

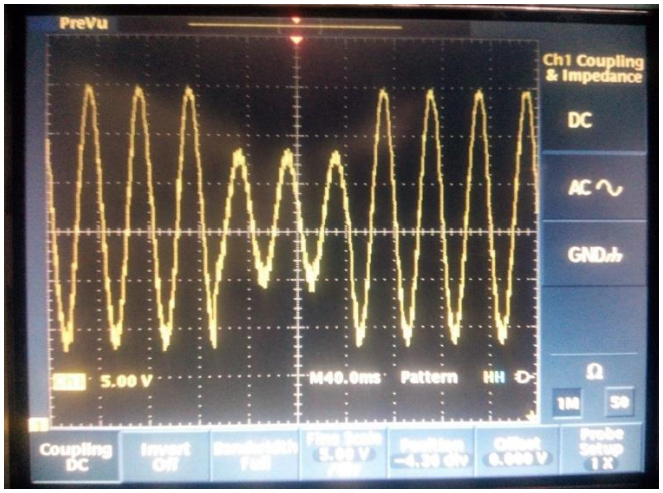

Figure 4. 15: The amplified Sag signal

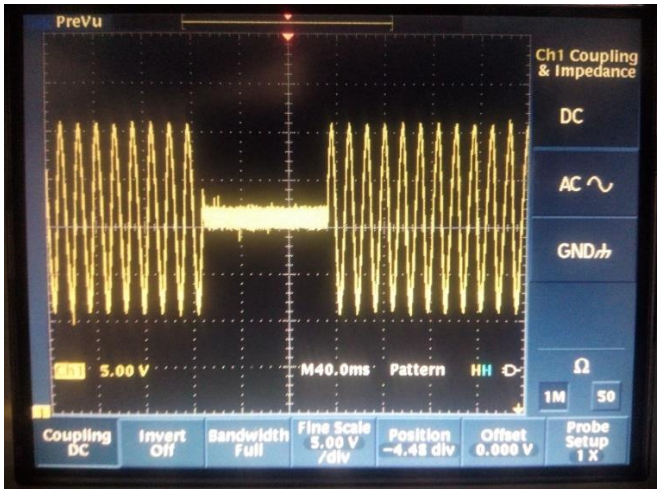

Figure 4. 16: Interruption

4.4 Results discussion

The Class-D amplifier that has been used in our project can amplify all of the simulated signals with a wide range of frequencies up to the 7^{th} harmonic with minimum distortion. A peak-to-peak voltage of 110 can be achieved using the Full Bridge topology, which is the standard input voltage for the relay. The output voltage depends on the DC voltage fed into the bridge. The use of MOSFETs with shorter t_{on} and t_{off} can reduce the switching losses.

Some of the protective relay functionality tests require the injection of both current and voltage signals simultaneously, this can be achieved using the NI PCIe-7851; two separate fault signals can be easily generated in 2 of the 8 different analog outputs of the card and controlled separately using the Block Diagram discussed in chapter II. The full bridge topology that can be used for amplifying each signal separately as seen in figure 4.7 provides two controllable and amplified signals than can be fed into the protective relay. In this approach, the amplification stage has been designed to use a half-bridge for each signal; however, an additional full bridge can be used for amplifying the second signal just by a duplication of the developed and tested circuit.

Conclusion

The goal of this project has been attained by simulating fault signals and amplifying them in order to inject them into a protective relay for testing its functionality. The task in hand put certain conditions on both stages of the work. The simulation of a wide range of fault signals and disturbances has been investigated to include fault signals that can be found in real life and the amplification stage has been added to yield signals large enough to test the real relay's functionality. After an extensive research on the subject in hand, and acquiring sufficient knowledge on Relay Testing principles, the two parts have been performed using LabVIEW virtual instrumentation principle and Class-D amplifier design.

The obtained results show that the performance of the system was very satisfying. Indeed the simulation also show the system has performed its intended functions perfectly and the performance of the amplification stage proved to be very satisfying as well, accomplishing high output range with minimum distortion.

Our contribution in this work includes the simulation of a great number of fault signals by controlling their parameters online. Additionally the final setup allows for the generation of multiple number of separate and fully controllable fault signals at once, which would allow for the injection of both three phase current and three phase voltage signals if needed.

This area is still open for further development and improvement of the overall system, by using the FPGA chip to directly output the desired fault's SPWM signal in order to bypass the hardware modulation stage and eliminate the problems associated with it.

Another improvement can be through the use of a different output device that is more affordable, during our research in the area of signal generation; we discovered that a standard PC sound card could be used to generate defined signals provided that the user has sufficient knowledge on the inner workings of the sound card.

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